S6AE102A / S6AE103A

Energy Harvesting PMIC for Wireless Sensor Node

Data Sheet (Preliminary)

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S6AE102A / S6AE103A

Energy Harvesting PMIC for Wireless Sensor Node

Data Sheet (Preliminary)

1. Description

The S6AE102A/103A is a power management IC (PMIC) for energy harvesting that is built into circuits of solar cells connected in series, dual output power control circuits, output capacitor storage circuits, power switching circuits of primary batteries, a LDO, a comparator and timers. Super-low-power operation is possible using a consumption current of only 280 nA and startup power of only 1.2 µW. As a result, even slight amounts of power generation can be obtained from compact solar cells under low-brightness environments of approximately 100 lx.

This IC stores power generated by solar cells to an output capacitor using built-in switch control, and it turns on the power switching circuit while the capacitor voltage is within a preset maximum and minimum range for supplying energy to a load. The output power control circuit has 2 outputs, and 1 of 2 outputs can control On and OFF of the power gating circuit using interrupt signal. The output capacitor storage circuits have 2 capacitor connection circuit for a storage of system load and a storage of surplus power, and if the power generated from solar cells is enough, the power is stored to the capacitor of surplus power storage. If the power generated from solar cells is not enough, energy can also be supplied in the same way as solar cells from the capacitor of surplus power storage or connected primary batteries for auxiliary power.

This IC has also an independent LDO. The LDO can provide stable voltage that a sensor requires. And also an independent comparator which can make voltage comparison signal output a lot of flexibility is built in. Also, an overvoltage protection (OVP) function is built into the input pins of the solar cells, and the open voltage of solar cells is used by this IC to prevent an overvoltage state.

The S6AE102A/103A is provided as a battery-free wireless sensor node solution that is operable by super-compact solar cells or non-disconnect energy harvesting based wireless sensor node solution with the capacitor of surplus storage or primary batteries for auxiliary power

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2. Features

- Operation input voltage range
  - Solar cell power : 2.0V to 5.5 V
  - Primary battery power : 2.0V to 5.5 V
- Adjustable output voltage range : 1.1V to 5.2V
- Low-consumption current : 280 nA
- Minimum input power at startup : 1.2 µW
- Low-consumption current LDO : 400 nA
- Low-consumption current Timer : 30 nA
- Low-consumption current comparator : 20 nA (S6AE103A only)
- Hybrid control of solar cell and primary battery with power path control
- Solar powered power control without battery
- System power reduction control with power gating
- Power gating control with interrupt signal
- Power gating control with timer (S6AE103A only)
- Hybrid storage system for a storage of system load and a storage of surplus power
- Power supply and switch control signal output for external path switch control
- Input overvoltage protection : 5.4V
- Compact QFN-20/QFN-24 package : 4 mm × 4 mm

3. Applications

- Energy harvesting power system with a very small solar cell
- Bluetooth Smart® sensor
- Wireless HVAC sensor
- Wireless lighting control
- Security system
- Smart home / Building / Industrial wireless sensor

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Tables

4. Product Lineup

Function

Product Name	S6AE102A	S6AE103A
Pin count	20	24
Power supply voltage range	2.0V to 5.5 V	
Output voltage range	1.1V to 5.2V	
Output channel	2ch	
LDO	1ch	
Overvoltage protection (OVP)	VDD pin	
Timer	1unit	3units
Comparator	−	1ch

5. Packages

Package \ Product Name	S6AE102A	S6AE103A
VNF020	○	−
VNF024	−	○

○: Available

Note:

- See "18. Package Dimensions" for detailed information on each package.

6. Pin Assignment

Figure 6-1 Pin Assignment of S6AE102A

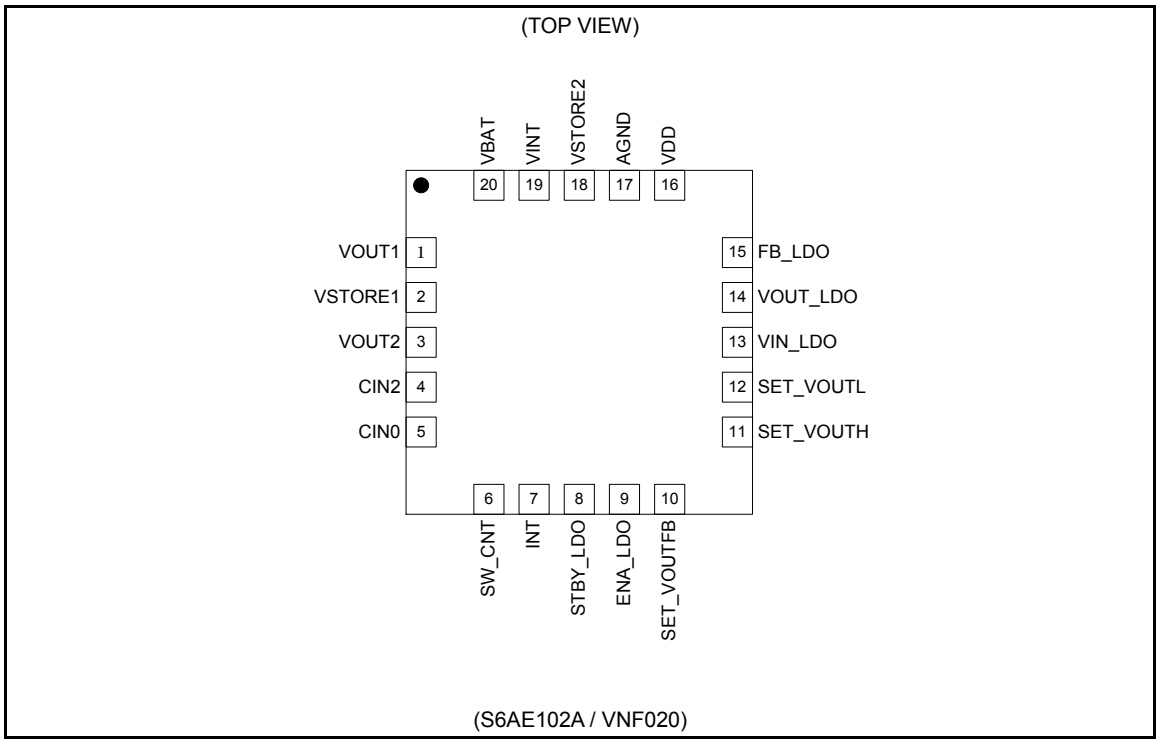
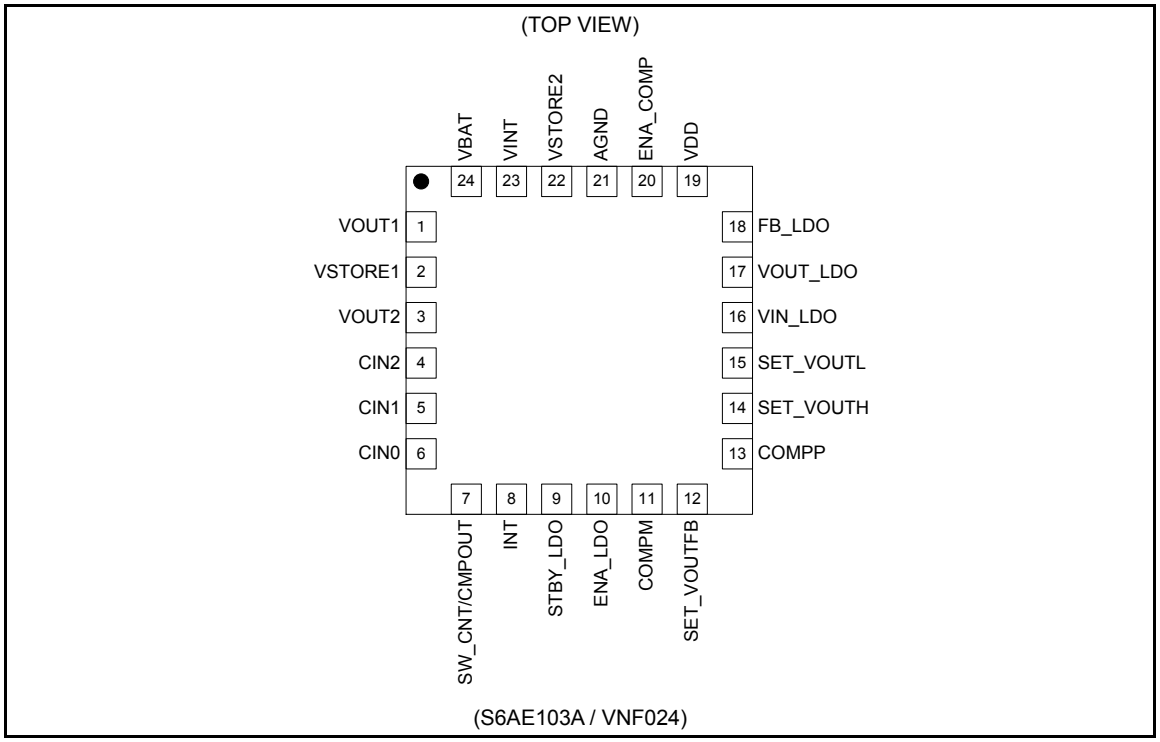


Figure 6-2 Pin Assignment of S6AE103A



7. Pin Descriptions

Table 7-1 Pin Descriptions

Pin No.		Pin Name	I/O	Description
S6AE102A	S6AE103A			
1	1	VOUT1	O	Output voltage pin
2	2	VSTORE1	O	Storage output pin
3	3	VOUT2	O	Output voltage pin
4	4	CIN2	O	Timer time 2 (T2) setting pin(for connecting capacitor) For the pin setting, refer to "Table 12-2 Power Gating Operation Mode"
−	5	CIN1	O	Timer time 1 (T1) setting pin(for connecting capacitor) For the pin setting, refer to "Table 12-2 Power Gating Operation Mode"
5	6	CIN0	O	Timer time 0 (T0) setting pin(for connecting capacitor) For the pin setting, refer to "Table 12-2 Power Gating Operation Mode"
−	7	SW_CNT/COMPOUT	O	VOUT1 switch interlocking output pin / Comparator output pin
6	−	SW_CNT	O	VOUT1 switch interlocking output pin
7	8	INT	I	Event driven mode control pin For the pin setting, refer to "Table 12-2 Power Gating Operation Mode" (when being not used, connect this pin to AGND)
8	9	STBY_LDO	I	LDO operation mode setting pin For the pin setting, refer to "Table 12-4 LDO Operation Mode" (when being not used, connect this pin to AGND)
9	10	ENA_LDO	I	LDO output control pin For the pin setting, refer to "Table 12-4 LDO Operation Mode" (when being not used, connect this pin to AGND)
−	11	COMPM	I	Comparator Input pin (when being not used, leave this pin open)
10	12	SET_VOUTFB	O	Reference voltage output pin (for connecting resistor)
−	13	COMPP	I	Comparator input pin (when being not used, leave this pin open)
11	14	SET_VOUTH	I	VOUT1, VOUT2 output voltage setting pin (for connecting resistor)
12	15	SET_VOUTL	I	VOUT1, VOUT2 output voltage setting pin (for connecting resistor)
13	16	VIN_LDO	I	LDO power input pin (when being not used, connect this pin to AGND)
14	17	VOUT_LDO	O	LDO output pin
15	18	FB_LDO	I	LDO output voltage setting pin (for connecting resistor) (when being not used, leave this pin open)
16	19	VDD	I	Solar cell input pin (when being not used, leave this pin open)
−	20	ENA_COMP	I	Comparator control pin For the pin setting, refer to "12.5 General-Purpose Comparator" (when being not used, connect this pin to AGND)
17	21	AGND	−	Ground pin
18	22	VSTORE2	O	Storage output pin
19	23	VINT	O	Internal circuit storage output pin
20	24	VBAT	I	Primary battery input pin (when being not used, leave this pin open)

8. Block Diagram

Figure 8-1 Block Diagram of S6AE102A

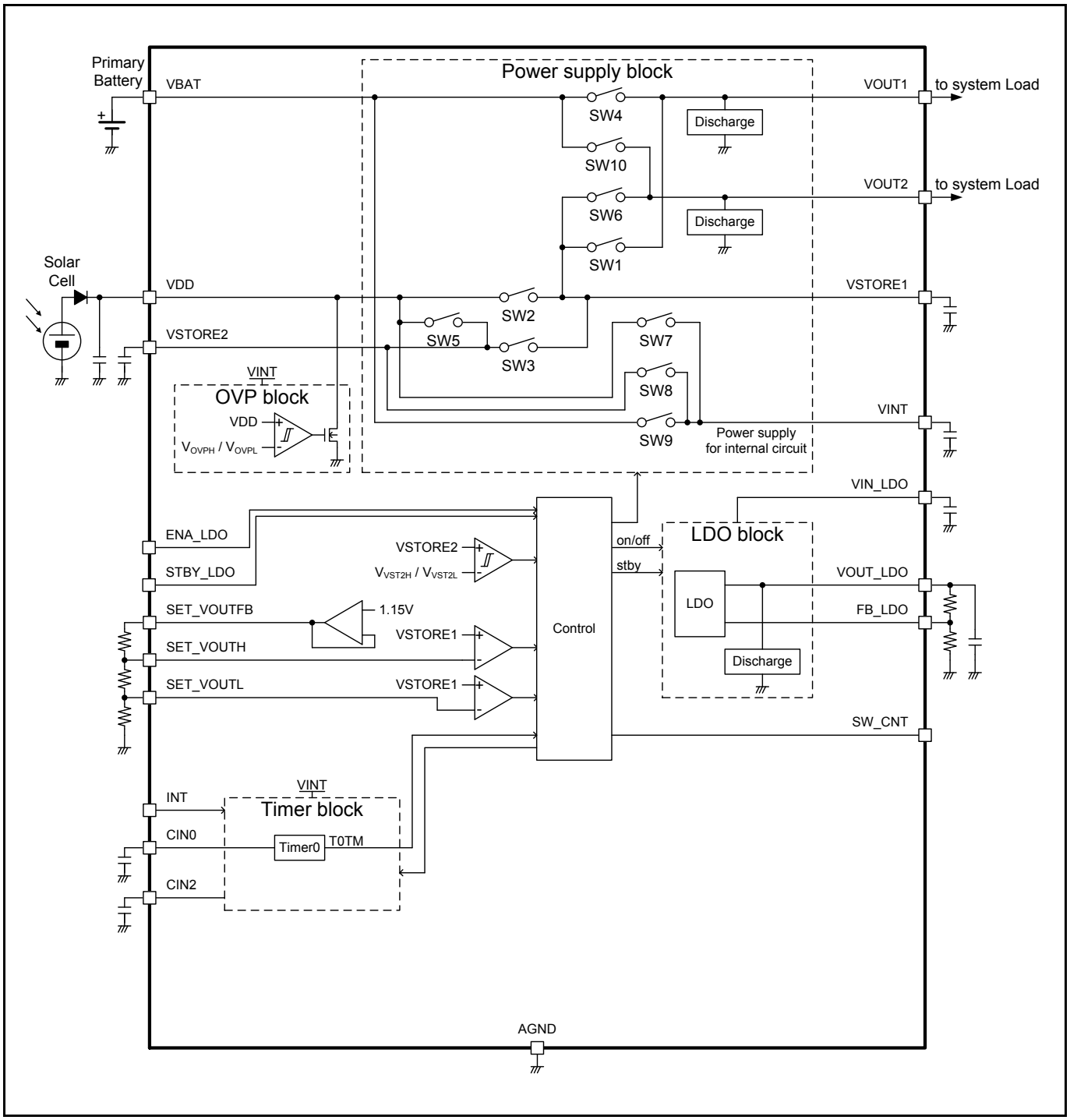
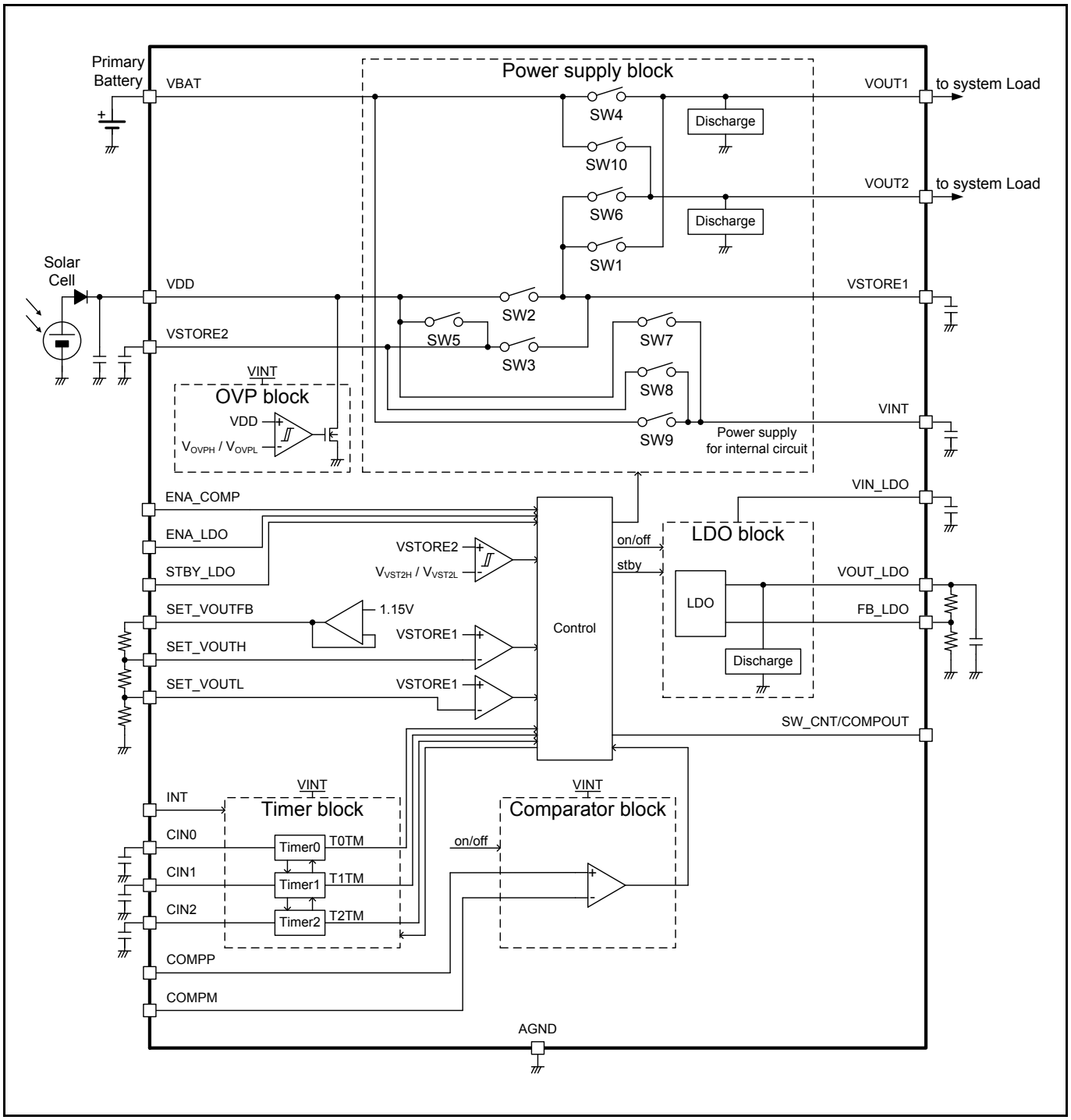


Figure 8-2 Block Diagram of S6AE103A



9. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage (*1)	V_{MAX}	VDD, VBAT, VIN_LDO pin	−0.3	+6.9	V
Signal input voltage (*1)	$V_{INPUTMAX}$	SET_VOUTH, SET_VOUTL, INT, ENA_LDO, STBY_LDO, ENA_COMP, COMPP, COMPM pin	−0.3	+6.9	V
VDD slew rate	V_{SLOPE}	VDD pin	−	0.1	mV/µs
Power dissipation (*1)	P_D	Ta ≤+ 25°C	−	1400 (*2)	mW
Storage temperature	T_{STG}	−	−55	+125	°C

*1: When AGND = 0V

*2: θja (wind speed 0m/s): +50°C/W

Warning:

1. Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

10. Recommended Operating Conditions

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply voltage 1 (*1)	V_{VDD}	VDD pin	2.0	3.3	5.5	V
Power supply voltage 2 (*1)	V_{VBAT}	VBAT pin	2.0	3.0	5.5	V
Power supply voltage 3 (*1)	V_{VINLDO}	VIN_LDO pin	2.0	−	5.3	V
Signal input voltage (*1)	V_{INPUT}	INT, ENA_LDO, STBY_LDO, ENA_COMP, COMPP, COMPM pin	−	−	VINT pin voltage (*2)	V
VOUT1 setting resistance	R_{VOUT}	Sum of R1, R2, R3	10	−	−	MΩ
LDO setting resistance	R_{LDO}	Sum of R4, R5	100	−	−	MΩ
VDD capacitance	C_{VDD}	VDD pin	10	−	−	µF
VINT capacitance	C_{VINT}	VINT pin	1	−	−	µF
VOUT upper limit setting voltage	V_{SYSH}	VSTORE1 pin	1.25	−	5.2	V
VOUT lower limit setting voltage	V_{SYSL}	VSTORE1 pin	1.1	−	V_{SYSH} ×0.9	V
General-purpose comparator input voltage	V_{COMP}	COMPP, COMPM pins	0.2	−	VINT pin voltage −1.5 (*2)	V
LDO output setting voltage	V_{SETLD}	VOUT_LDO pin	1.3	−	5.0	V
Timer time 0	T0	CIN0 pin, Timer 0	0.1	−	3600	s
Timer time 1	T1	CIN1 pin, Timer 1	0.1	−	3600	s
Timer time 2	T2	CIN2 pin, Timer 2	0.1	−	3600	s
Operating ambient temperature	Ta	−	−40	−	+85	°C

*1: When AGND = 0V

*2: Refer to "Table 12-1 VINT Pin Voltage".

Warning:

1. *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.*
2. *Any use of semiconductor devices will be under their recommended operating condition.*
3. *Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.*
4. *No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.*

11. Electrical Characteristics

The following electrical characteristics are the values excluding the effect of external resistors and external capacitors.

Table 11-1 Electrical Characteristics (System Overall)

(Unless specified otherwise, these are the electrical characteristics under the recommended operating environment.)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Minimum Input power in start-up	W_{START}	VDD pin, Ta = +25°C, V_{VOUTH} setting = 3V, By applying 0.4 µA to VDD, when VOUT1 reaches 3V×95% after the point when VDD reaches 3V.	−	−	1.2	µW
Power detection voltage	V_{DETH}	VDD, VBAT ,VINT, VSTORE2 pins	1.30	1.55	2.00	V
Power undetection voltage	V_{DETL}		1.15	1.45	1.90	V
Power detection hysteresis	V_{DETHYS}		−	0.1	−	V
Power detection voltage 2	V_{DETH2}	VDD pin, When connecting a capacitor to VSTORE2 pin	2.0	2.1	2.2	V
Power undetection voltage 2	V_{DETL2}		1.9	2.0	2.1	V
Power detection hysteresis 2	$V_{DETHYS2}$		−	0.1	−	V
VOUT upper limit voltage	V_{VOUTH}	VSTORE1 pin, VOUT1 Load = 0 mA, VOUT2 Load = 0 mA	−	V_{SYSH}	−	V
Input power reconnect voltage	V_{VOUTM}	VSTORE1 pin, VOUT1 Load = 0 mA, VOUT2 Load = 0 mA	−	V_{VOUTH} ×0.95	−	V
VOUT lower limit voltage	V_{VOUTL}	VSTORE1 pin, VOUT1 Load = 0 mA, VOUT2 Load = 0 mA	−	V_{SYSL}	−	V
VSTORET2 upper limit voltage	V_{VST2H}	VSTORE2 pin, V_{VOUTH} setting>2.4V	−	V_{VOUTH}	−	V
		VSTORE2 pin, V_{VOUTH} setting≤2.4V	2.3	2.4	2.5	V
VSTORET2 lower limit voltage	V_{VST2L}	VSTORE2 pin, V_{VOUTH} setting>2.4V	−	V_{VOUTL}	−	V
		VSTORE2 pin, V_{VOUTH} setting≤2.4V	2.2	2.3	2.4	V
OVP detection voltage	V_{OVPH}	VDD pin	5.2	5.4	5.5	V
OVP release voltage	V_{OVPL}		5.1	5.3	5.4	V
OVP detection hysteresis	V_{OVPHYS}		−	0.1	−	V
OVP protection current	I_{OVP}	VDD pin input current	6	−	−	mA
Input voltage	V_{IH}	INT, ENA_LDO, STBY_LDO, ENA_COMP pins	1.1	−	VINT pin voltage (*1)	V
	V_{IL}	INT, ENA_LDO, STBY_LDO, ENA_COMP pins	0	−	0.3	V
Output voltage	V_{OH}	SW_CNT/COMPOUT, SW_CNT pins, Load = 2 µA	0.7×VINT pin voltage (*1)	−	VINT pin voltage (*1)	V
	V_{OL}	SW_CNT/COMPOUT, SW_CNT pins, Load = 2 µA	0	−	0.3×VINT pin voltage (*1)	V

*1: Refer to "Table 12-1 VINT Pin Voltage".

Table 11-2 Electrical Characteristics (Consumption Current)

(Unless specified otherwise, these are the electrical characteristics under the recommended operating environment.)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Consumption current 1	I_{QIN1}	VDD pin input current, Energy driven mode (*2), SW2 = OFF, VDD = 3V, open VBAT pin, open VSTORE2 pin, VIN_LDO = GND, INT = GND, ENA_COMP = GND, ENA_LDO = GND, STBY_LDO = GND, V_{VOUTH} setting = 1.25V, Ta = +25°C, SET_VOUTFB resistance>100 MΩ, VOUT1 Load = 0 mA, VOUT2 Load = 0 mA	−	280	420	nA
Consumption current 2	I_{QIN2}	Sum of I_{QIN1} and I_{INLD2} (LDO operation current) ENA_LDO = VINT (*1)	−	680	1020	nA
Consumption current 3	I_{QIN3}	Sum of I_{QIN1} and comparator operation current, ENA_COMP = VINT (*1)	−	300	450	nA

*1: Refer to "Table 12-1 VINT Pin Voltage".

*2: Refer to "12.2 Power Gating"

Table 11-3 Electrical Characteristics (Switch)

VDD ≥ 3V, VBAT ≥ 3V, VINT ≥ 3V, VSTORE2 ≥ 3V, V_{VOUTL} ≥ 3V, VSTORE1 ≥ V_{VOUTL}

(Unless specified otherwise, these are the electrical characteristics under the recommended operating environment.)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Switch resistance 1	R_{ON1}	SW1, In connection of VSTORE1 pin and VOUT1 pin	−	1.5	2.5	Ω
Switch resistance 2	R_{ON2}	SW2, In connection of VDD pin and VSTORE1 pin	−	50	100	Ω
Switch resistance 3	R_{ON3}	SW3, In connection of VSTORE2 pin and VSTORE1 pin	−	50	100	Ω
Switch resistance 4	R_{ON4}	SW4, In connection of VBAT pin and VOUT1 pin	−	1.5	2.5	Ω
Switch resistance 5	R_{ON5}	SW5, In connection of VDD pin and VSTORE2 pin	−	50	100	Ω
Switch resistance 6	R_{ON6}	SW6, In connection of VSTORE1 pin and VOUT2 pin	−	1.5	2.5	Ω
Switch resistance 10	R_{ON10}	SW10, In connection of VBAT pin and VOUT2 pin	−	1.5	2.5	Ω
Discharge resistance	R_{DIS}	VOUT1, VOUT2 pins	−	1	2	kΩ

Table 11-4 Electrical Characteristics (LDO)

(Unless specified otherwise, these are the electrical characteristics under the recommended operating environment.)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Output voltage	V_{OUTLD}	VOUT_LDO pin, Load = 0.01 mA	V_{SETLD} ×0.95	−	V_{SETLD} ×1.05	V
		VOUT_LDO pin, Ta = +25°C, VIN_LDO = V_{OUTLD}+1V STBY_LDO = VINT (*1) , Load = 0.01 mA	V_{SETLD} ×0.98	−	V_{SETLD} ×1.02	V
Input/output voltage difference (Normal mode)	V_{DELLD1}	Between VIN_LDO and VOUT_LDO pins, STBY_LDO = VINT (*1), Load ≤ 1 mA	0.3	−	−	V
Input/output voltage difference (Standby mode)	V_{DELLD2}	Between VIN_LDO and VOUT_LDO pins, STBY_LDO = AGND, Load ≤ 0.001 mA	0.3	−	−	V
Maximum output current (Normal mode)	I_{OUTLD1}	VOUT_LDO pin, (VIN_LDO−V_{OUTLD}×1.05) > 0.7V STBY_LDO = VINT (*1)	10	−	−	mA
Maximum output current (Standby mode)	I_{OUTLD2}	VOUT_LDO pin, (VIN_LDO−V_{OUTLD}×1.05) > 0.7V, STBY_LDO = AGND	0.1	−	−	mA
Line regulation	L_{INELD}	VOUT_LDO pin, VIN_LDO = (V_{OUTLD}×1.05+0.7V) to 5.3V	−	−	50	mV
Load regulation (Normal mode)	L_{OADLD1}	VOUT_LDO pin, STBY_LDO = VINT (*1) , Load = 1 mA to 10 mA	−	−	50	mV
Load regulation (Standby mode)	L_{OADLD2}	VOUT_LDO pin, STBY_LDO = AGND, Load = 0.001 mA to 0.1 mA	−	−	50	mV
OVP operation current	I_{LIMLD}	VOUT_LDO pin, STBY_LDO = VINT (*1)	−	50	100	mA
LDO consumption current (Normal mode)	I_{INLD1}	Sum of VINT and VIN_LDO input current, Ta = +25°C, STBY_LDO = VINT (*1), Load = 0 mA	−	6	9	µA
LDO consumption current 2 (Standby mode)	I_{INLD2}	Sum of VINT and VIN_LDO input current, Ta = +25°C, STBY_LDO = AGND, Load = 0 mA, VOUT_LDO resistance > 100 MΩ, V_{OUTLD} setting = 1.3V	−	400	600	nA
OFF current	I_{OFFLD}	VIN_LDO pin, Ta = +25°C, ENA_LDO = AGND	−	60	120	nA
Discharge resistance	R_{DISLD}	VOUT_LDO pin, 1.35 ≤ V_{OUTLD} ≤ 5.0V	−	1	2	kΩ

*1: Refer to "Table 12-1 VINT Pin Voltage".

Table 11-5 Electrical Characteristics (Timer)

(Unless specified otherwise, these are the electrical characteristics under the recommended operating environment.)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Accuracy	T_{ATM}	Ta = +25°C	−15	−	+15	%
Each timer consumption current	I_{QTM}	Timer 0, Timer 1, Timer 2, Ta = +25°C	−	30	45	nA

12. Functional Description

12.1 Power Supply Control

This IC can operate by two input power supplies, namely, the solar cell voltage VDD and the primary battery voltage VBAT.

When a capacitor is connected to the VSTORE2 pin, the surplus power of the solar cell accumulates in this capacitor and operates as input power supply.

The input power (from solar cell or VSTORE2 capacitor) is accumulated once in the capacitor connected to the VSTORE1 pin. When the voltage of the VSTORE1 pin reaches the threshold or higher, the power gating switch connects VSTORE1 to VOUT1 and VOUT2.

The input power (from primary battery) is not accumulated in the capacitor connected to the VSTORE1 pin. When the voltage of the VBAT pin reaches the threshold or higher, the switch for power gating connects VBAT to VOUT1 and VOUT2.

The VINT pin voltage is output as shown in the table below.

Table 12-1 VINT Pin Voltage

VDD Voltage (Solar Cell)	VBAT Voltage (Primary Battery)	VSTORE2 Voltage	VSTORE1 Voltage	VINT Voltage (Output)
V_{DETL} or less	V_{DETL} or less	V_{DETL} or less	−	−
		V_{DETH} or higher	−	VSTORE2
	V_{DETH} or higher	V_{DETL} or less	−	VBAT
		V_{DETH} or higher	V_{VOUTL} detection (*1)	VBAT
			V_{VOUTH} detection (*2)	VSTORE2
V_{DETH} or higher	V_{DETL} or less	V_{DETL} or less	−	VDD
		V_{DETH} or higher	−	VDD
	V_{DETH} or higher	V_{DETL} or less	V_{VOUTL} detection (*1)	VBAT
			V_{VOUTH} detection (*2)	VDD
		V_{DETH} or higher	V_{VOUTL} detection (*1)	VBAT
			V_{VOUTH} detection (*2)	VDD

*1: Value from when voltage at VSTORE1 pin reaches V_{VOUTL} voltage until it reaches V_{VOUTH} voltage

*2: Value from when voltage at VSTORE1 pin reaches V_{VOUTH} voltage until it reaches V_{VOUTL} voltage

VDD Input Power Operation

This section describes operation when the VDD pin is set as the input power (Figure 12-1).

When the voltage of the VBAT pin falls to the power undetection voltage (V_{DETL} = 1.45 V) or less, and a capacitor is not connected to the VSTORE2 pin.

[1] When the voltage of the VDD pin reaches the power detection voltage (V_{DETH} = 1.55V) or higher, the switch (SW2) connects VDD and VSTORE1 (path S1). Also, when the voltage of the VDD pin falls to the power undetection voltage (V_{DETL} = 1.45V) or less, SW2 disconnects the path S1.

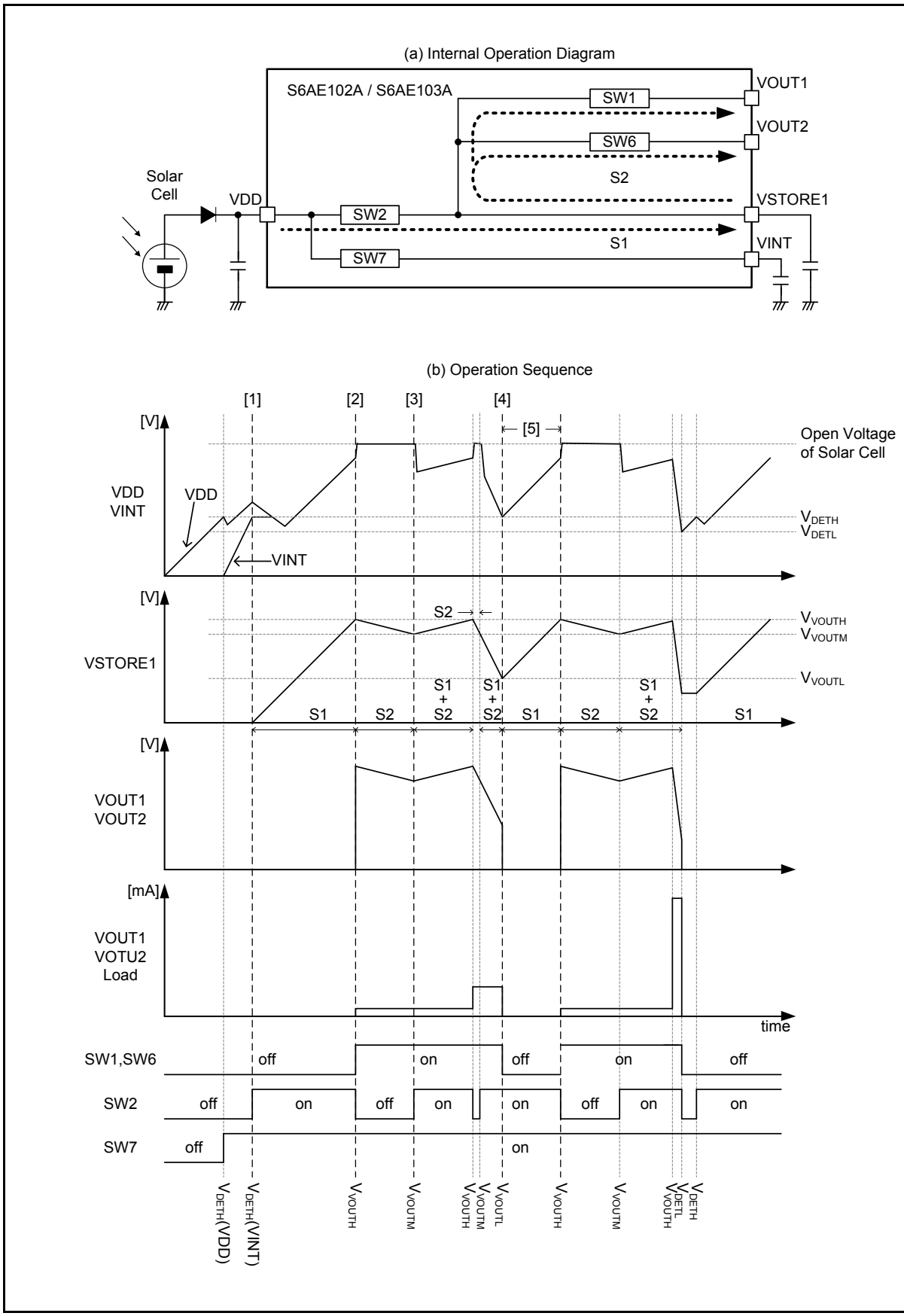
[2] When the voltage of the VSTORE1 pin reaches the threshold value (V_{VOUTH}) or higher that was set by the SET_VOUTH pin, SW2 disconnects the path S1. Also, the VOUT1 switch (SW1) connects VSTORE1 and VOUT1, and the VOUT2 switch (SW6) connects VSTORE1 and VOUT2 (path S2).

[3] When the voltage of the VSTORE1 pin falls to the input power reconnect voltage (V_{VOUTM}) or less, SW2 connects the path S1 (path S1+S2).

[4] In addition, when the voltage falls to the threshold value (V_{VOUTL}) or less that was set by the SET_VOUTL pin, SW1 and SW6 disconnect the path S2.

[5] When SW1 and SW6 disconnects the path S2, the discharge function is activated.

Figure 12-1 VDD Input Power Operation



VBAT Input Power Operation

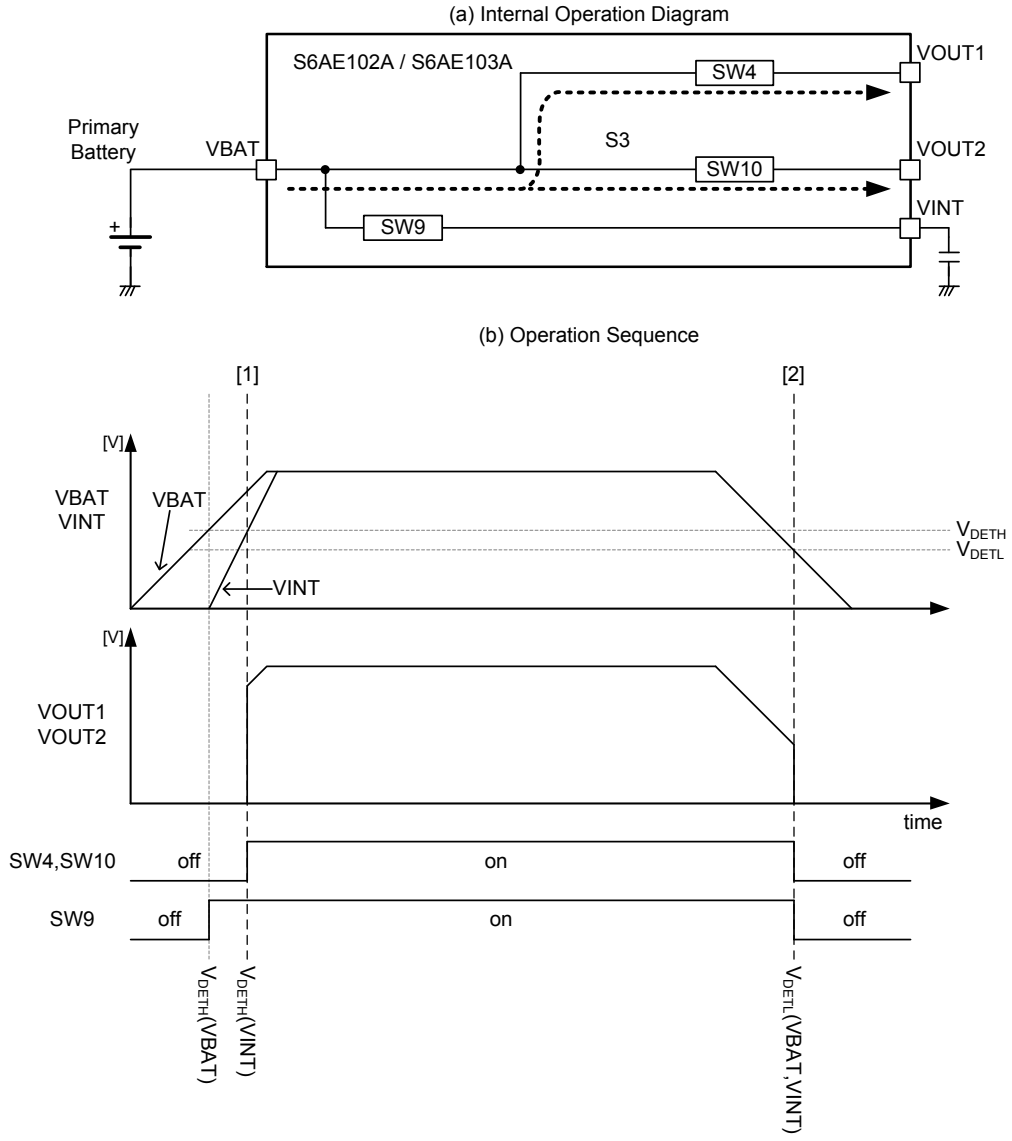
This section describes operation when the VBAT pin is set as the input power (Figure 12-2).

When the voltage of the VDD pin falls to the power undetection voltage (V_{DETL} = 1.45 V) or less, and a capacitor is not connected to the VSTORE2 pin.

[1] When the voltage of the VBAT pin reaches the power detection voltage (V_{DETH} = 1.55V) or higher, the switch (SW4) connects VBAT and VOUT1, and the switch (SW10) connects VBAT and VOUT2 (path S3).

[2] When the voltage of the VBAT pin falls to the power undetection voltage (V_{DETL} = 1.45V) or less, SW4 and SW10 disconnects the path S3.

Figure 12-2 VBAT Input Power Operation



VDD/VBAT Input Power Operation

This section describes operation when the VDD and VBAT pins are set as the input power (Figure 12-3).

A capacitor is not connected to the VSTORE2 pin.

[1] When the voltage of the VDD pin and the VBAT pin reaches the power detection voltage (V_{DETH} = 1.55 V) or higher and the voltage of the VSTORE1 pin is not detected as the VOUT upper limit voltage (V_{VOUTH}), the VOUT1 switch (SW4) connects VBAT and VOUT1 and the VOUT2 switch (SW10) connects VBAT and VOUT2 (path S3). Also, the switch (SW2) connects VDD and VSTORE1 (path S1).

[2] When the voltage of the VSTORE1 pin reaches the VOUT upper limit voltage (V_{VOUTH}) or higher, SW4 and SW10 disconnect path S3.Also, the VOUT1 switch (SW1) connects VSTORE1 and VOUT1 and the VOUT2 switch (SW6) connects VSTORE1 and VOUT2 (path S2).

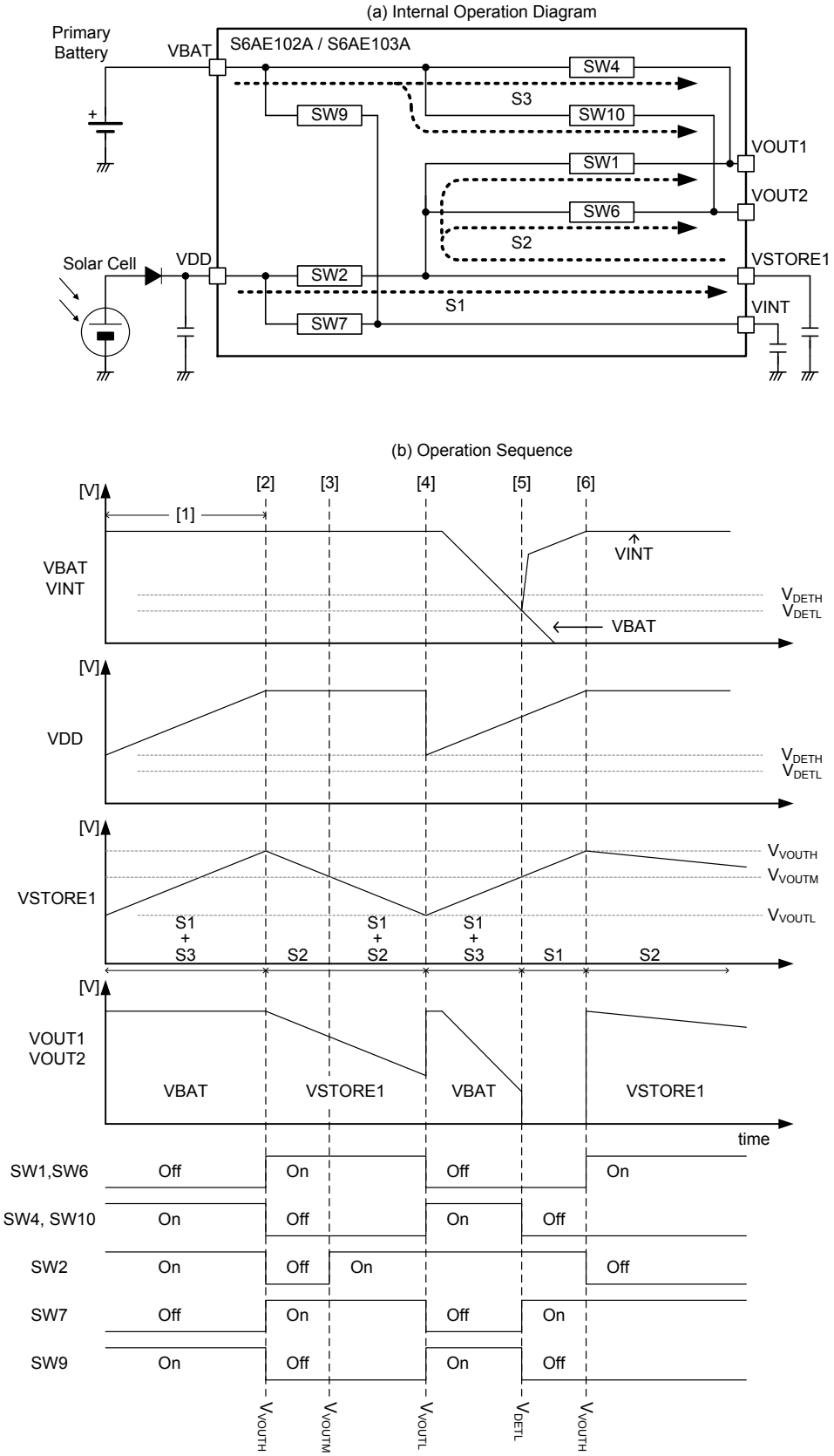
[3] When the voltage of the VSTORE1 pin falls to the input power reconnect voltage (V_{VOUTM}) or less, SW2 connects path S1 (path S1 + S2).

[4] When the voltage of the VSTORE1 pin falls to the VOUT lower limit voltage (V_{VOUTL}) or less, switches SW1 and SW6 disconnect path S2. Also, SW4 and SW10 connect path S3 (path S1 + S3).

[5] When the voltage of the VBAT pin falls to the power undetection voltage (V_{DETL} = 1.45 V) or less, switches SW4 and SW10 disconnect path S3.

[6] When the voltage of the VSTORE1 pin reaches the VOUT upper limit voltage (V_{VOUTH}) or higher, SW1 and SW6 connect path S2 (path S2).

Figure 12-3 VDD/VBAT Input Power Operation



VDD/VSTORE2 Input Power Operation

This section describes operation when the VDD pin is set as the input power (Figure 12-4).

A capacitor is connected to the VSTORE2 pin.

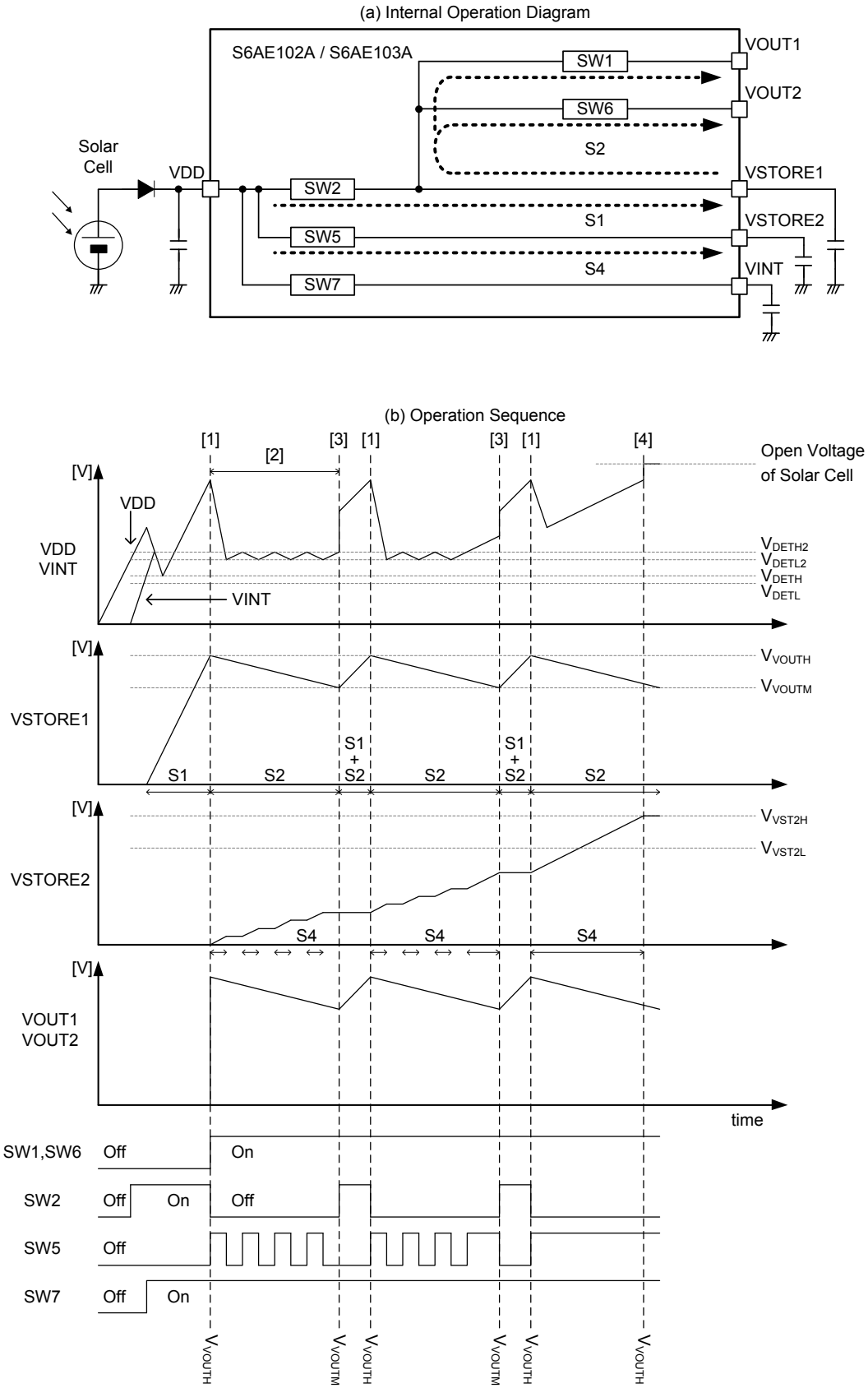
[1] When the voltage of the VSTORE1 pin reaches the threshold value (V_{VOUTH}) or higher that was set by the SET_VOUTH pin, switch (SW5) connects VDD and VSTORE2 (path S4).

[2] When the voltage of the VDD pin falls to the power undetection voltage 2 (V_{DETL2} = 2.0 V) or less, SW5 disconnects path S4. When it reaches the power detection voltage 2 (V_{DETH2} = 2.1 V) or higher, SW5 connects path S4.

[3] When the voltage of the VSTORE1 pin falls to the threshold value (V_{VOUTM}) or less that was set by the SET_VOUTH pin, SW5 disconnects path S4.

[4] When the voltage of the VSTORE2 pin reaches the VSTORE2 upper limit voltage (V_{VST2H}) or higher, SW5 disconnects path S4.

Figure 12-4 VDD/VSTORE2 Input Power Operation



VSTORE2 Input Power Operation

This section describes operation when the VSTORE2 pin is set as the input power (Figure 12-5).

A capacitor is connected to the VSTORE2 pin.

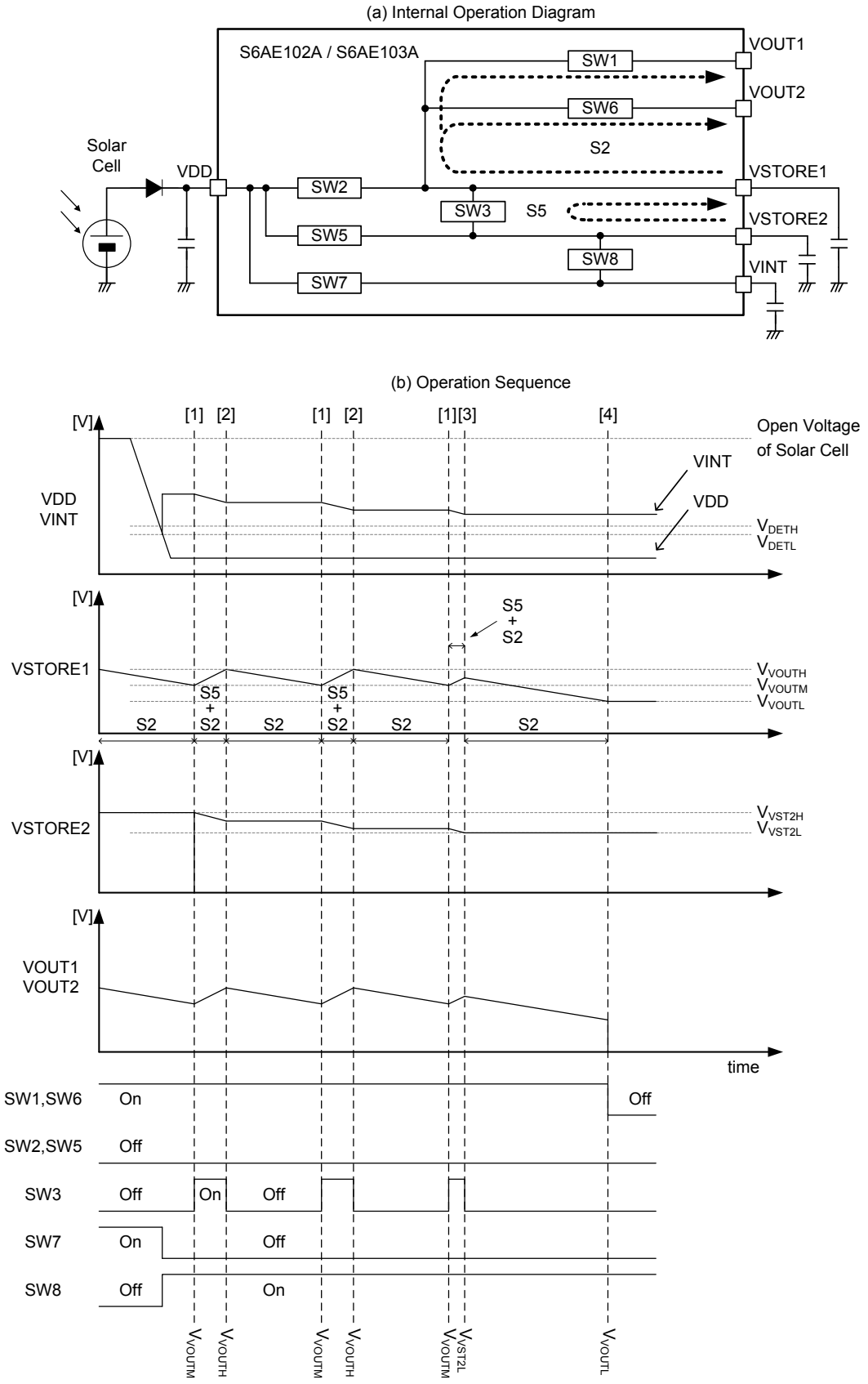
[1] When the voltage of the VDD pin falls to the power undetection voltage (V_{DETL} = 1.45 V) or less, and when the voltage of the VSTORE1 pin falls to the threshold value (V_{VOUTM}) or less set by SET_VOUTH pin, switch (SW3) connects VSTORE2 and VSTORE1 (path S5 + S2).

[2] When the voltage of the VSTORE1 pin reaches the threshold value (V_{VOUTH}) or higher that was set by the SET_VOUTH pin, SW3 disconnects path S5.

[3] When the voltage of the VSTORE2 pin falls to the VSTORE2 lower limit voltage (V_{VST2L}) or less, SW3 disconnects path S5.

[4] When the voltage of the VSTORE1 pin falls to the threshold value (V_{VOUTL}) or less that was set by the SET_VOUTL pin, the VOUT1 switch (SW1) disconnects VSTORE1 and VOUT1 and the VOUT2 switch (SW6) disconnects VSTORE1 and VOUT2.

Figure 12-5 VSTORE2 Input Power Operation



12.2 Power Gating

This IC has a power gating function for external systems.

The power gating function is to control supplying power accumulated in VSTORE1 or power from VBAT to external system loads connected to VOUT1 and VOUT2 by internal switches.

The power gating function has four operating modes.

This IC determines the power gating operation mode through the connection status of pins CIN1 and CIN2 at the power detection (V_{DETH} = 1.55 V) timing of the VINT pin.

Table 12-2 Power Gating Operation Mode

Each Pin Settings		Operation Mode
CIN1(*1)	CIN2	
Open	Open	Energy driven mode
Open	Connect AGND	Event driven mode 1
Connect capacitor (*2)	Open	Event driven mode 2 (*1)
Connect capacitor (*2)	Connect capacitor (*2)	Timer driven mode (*1)

*1: S6AE103A only

*2: For the timer time setting, refer to"14.1 Setting the Operation Conditions".

Energy Driven Mode

1) VDD input power operation

Switches are controlled by monitoring VSTORE1 voltage.

Internal switches (SW1 and SW6) connect VSTORE1 and VOUT1, as well as VSTORE1 and VOUT2 from when VOUT upper limit voltage (V_{VOUTH}) is detected until VOUT lower limit (V_{VOUTL}) is detected.

2) VBAT input power operation

Switches are controlled by monitoring VBAT voltage.

Internal switches (SW4 and SW10) connect VBAT and VOUT1, as well as VBAT and VOUT2 from when power detection voltage (V_{DETH}) is detected until power undetection voltage (V_{DETL}) is detected.

Event Driven Mode 1

Switches are controlled in the same way as the energy driven mode to supply to VOUT1. The INT input controls switching to supply to VOUT2. While the timer 0 is counting, the flag output (T0TM) disables internal switching controls through INT input. The timer time (T0) is set by the capacitor connected to CIN0.

1) VDD input power operation

Internal switch (SW6) connects VSTORE1 to VOUT2 while INT is high level. Detecting upper limit voltage (V_{VOUTH}) is a trigger to start timer 0, after the timer time reaches count (T0), it stops and is reset.

2) VBAT input power operation

Internal switch (SW10) connects VBAT to VOUT2 while INT is high level. Detecting power detection voltage (V_{DETH}) is a trigger to start timer 0, after the timer time reaches count (T0), it stops and is reset.

Event Driven Mode 2

Switches are controlled in the same way as the energy driven mode to supply to VOUT1. The INT input and the flag output (T1TM) control switching to supply to VOUT2.

1) VDD input power operation

Detecting upper limit voltage (V_{VOUTH}) is a trigger to start counter, after the timer time reaches count (T0), timer 0 stops and is reset. When the timer time (T0) is set by the capacitor connected to CIN0.

The highness of INT is a trigger to start counter, after the timer time reaches count (T1), timer 1 stops and is reset. When the timer time (T1) is set by the capacitor connected to CIN1.

For each timer, they are reset by detecting VOUT lower limit voltage (V_{VOUTL}).

Internal switch (SW6) connects VSTORE1 to VOUT2 while timer 1 is counting. Disables internal switching controls through INT input while the timer 0 is counting.

2) VBAT input power operation

Detecting power detection voltage (V_{DETH}) is a trigger to start counter, after the timer time reaches count (T0), timer 0 stops and is reset. When the timer time (T0) is set by the capacitor connected to CIN0.

The highness of INT is a trigger to start counter, after the timer time reaches count (T1), timer 1 stops and is reset. When the timer time (T1) is set by the capacitor connected to CIN1.

Each timer is reset by detecting power undetection voltage (V_{DETL}).

Internal switch (SW10) connects VBAT to VOUT2 while timer 1 is counting. Disables internal switching controls through INT input while the timer 0 is counting.

Timer Driven Mode

The timer 0 flag output (T0TM), timer 1 flag output (T1TM), and timer 2 flag output (T2TM) control switching to supply to VOUT1 and VOUT2

1) VDD input power operation

This section describes the operation of each timer.

Detecting upper limit voltage (V_{VOUTH}) the first time is a trigger to start counter, after the timer time reaches count (T0), timer 0 stops and is reset. From the second time onward, the completion of timer 2 is a trigger to start the count, after the timer time reaches count (T0), the timer stops and is reset. When the timer time (T0) is set by the capacitor connected to CIN0.

Detecting upper limit voltage (V_{VOUTH}) the first time is a trigger to start counter, after the timer time reaches count (T1), timer 1 stops and is reset. From the second time onward, the completion of timer 2 is a trigger to start the count, after the timer time reaches count (T1), the timer stops and is reset. When the timer time (T1) is set by the capacitor connected to CIN1.

The completion of timer 1 is a trigger to start counter, after the timer time reaches count (T2), timer 2 stops and is reset. When the timer time (T2) is set by the capacitor connected to CIN2.

Timer 0 and 1 are reset by detecting VOUT lower limit voltage (V_{VOUTL}). Timer 2 is reset by power undetection voltage (V_{DETL}) of VINT.

This section describes the operation of VOUT1.

Internal switch (SW1) connects VSTORE1 to VOUT1 while timer 1 is counting. Internal switch (SW1) disconnects VSTORE1 and VOUT1 while timer 2 is counting.

This section describes the operation of VOUT2.

Internal switch (SW6) connects VSTORE1 to VOUT2 while timer 1 is counting after timer 0 ends. Internal switch (SW6) disconnects VSTORE1 and VOUT2 while timer 2 is counting.

2) VBAT input power operation

This section describes the operation of each timer.

Detecting power detection voltage (V_{DETH}) the first time is a trigger to start counter, after the timer time reaches count (T0), timer 0 stops and is reset. From the second time onward, the completion of timer 2 is a trigger to start the count, after the timer time reaches count (T0), the timer stops and is reset. When the timer time (T0) is set by the capacitor connected to CIN0.

Detecting power detection voltage (V_{DETH}) the first time is a trigger to start counter, after the timer time reaches count (T1), timer 1 stops and is reset. From the second time onward, the completion of timer 2 is a trigger to start the count, after the timer time reaches count (T1), the timer stops and is reset. When the timer time (T1) is set by the capacitor connected to CIN1.

The completion of timer 1 is a trigger to start counter, after the timer time reaches count (T2), timer 2 stops and is reset. When the timer time (T2) is set by the capacitor connected to CIN2.

Each timer is reset by detecting power undetection voltage (V_{DETL}).

This section describes the operation of VOUT1.

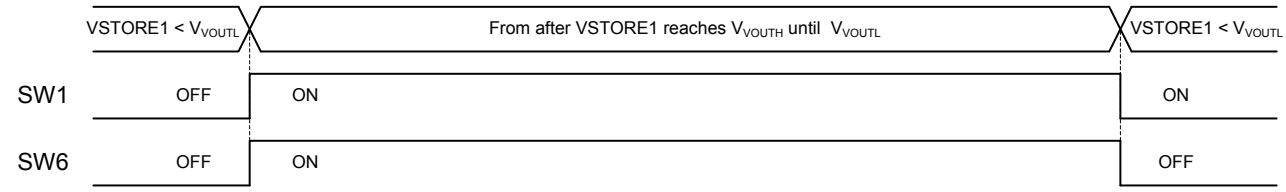
Internal switch (SW4) connects VBAT to VOUT1 while timer 1 is counting. Internal switch (SW4) disconnects VBAT and VOUT1 while timer 2 is counting.

This section describes the operation of VOUT2.

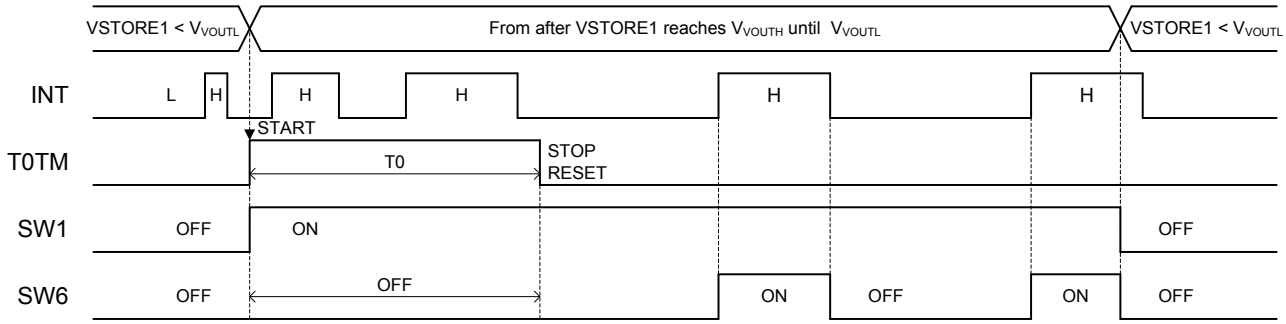
Internal switch (SW10) connects VBAT to VOUT2 while timer 1 is counting after timer 0 ends. Internal switch (SW10) disconnects VBAT and VOUT2 while timer 2 is counting.

Figure 12-6 Power Gating Operation (VDD Input Power)

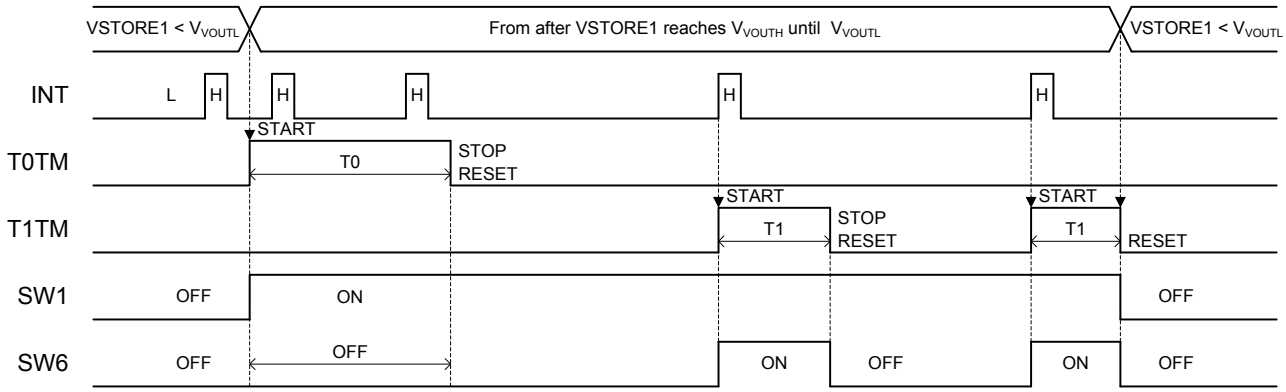
Energy driven mode (S6AE102A / S6AE103A)



Event driven mode 1 (S6AE102A / S6AE103A)



Event driven mode 2 (S6AE103A)



Timer driven mode (S6AE103A)

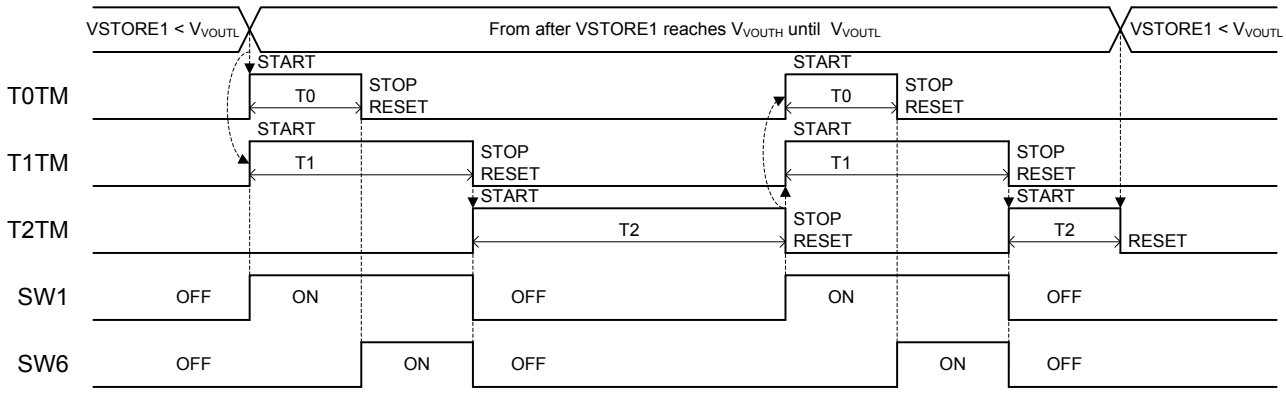
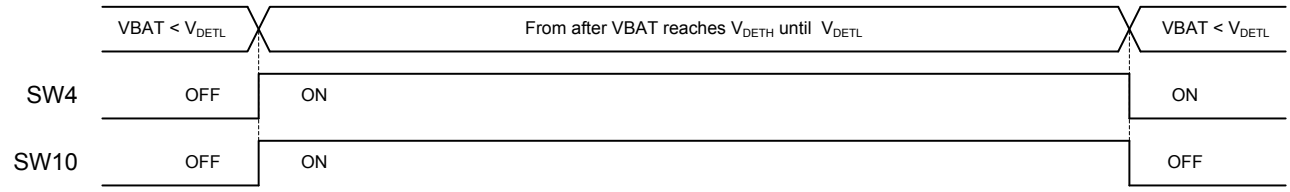
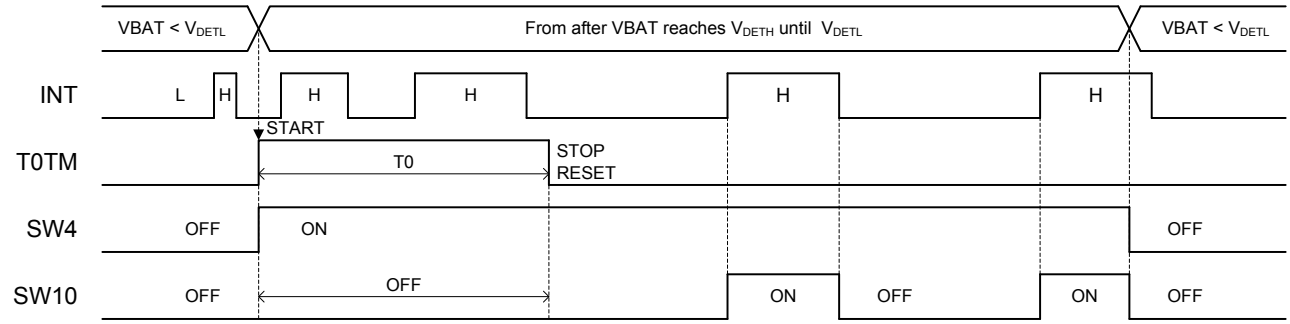


Figure 12-7 Power Gating Operation (VBAT Input Power)

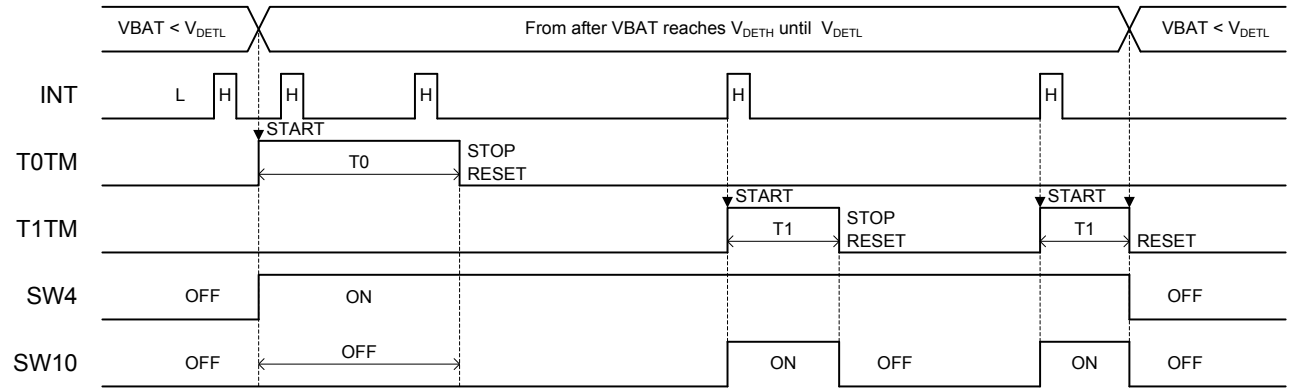
Energy driven mode (S6AE102A / S6AE103A)



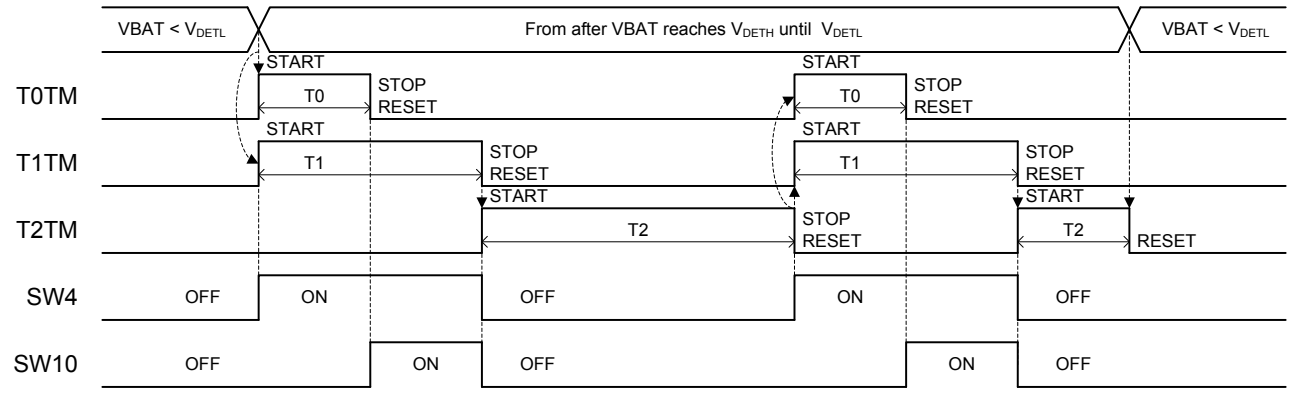
Event driven mode 1 (S6AE102A / S6AE103A)



Event driven mode 2 (S6AE103A)



Timer driven mode (S6AE103A)



12.3 Discharge

This IC has VOUT1 pin, VOUT2 pin, and VOUT_LDO pin discharge functions.

While SW1 and SW4 are OFF, the discharge circuit function between the VOUT1 pin and GND works. The VOUT1 pin's power is discharged to GND level.

While SW6 and SW10 are OFF, the discharge circuit function between the VOUT2 pin and GND works. The VOUT2 pin's power is discharged to GND level.

While LDO is OFF, the discharge circuit function between the VOUT_LDO pin and GND works. The VOUT_LDO pin's power is discharged to GND level.

12.4 SW_CNT Control

This IC has a control signal output function for external switching.

S6AE102A

The signal, which is interlocked with the switch for VOUT1, is output at the SW_CNT pin. While the VBAT input power is operating, it is interlocked to the ON/OFF control of the switch (SW4) between VBAT and VOUT1. While the VDD and VSTORE2 input power is operating, it is interlocked to the ON/OFF control of the switch (SW1) between VSTORE1 and VOUT1. Output to the SW_CNT pin is High while SW1 or SW4 is ON.

S6AE103A

While ENA_COMP pin is Low, the signal, which is interlocked with the switch for VOUT1, is output at the SW_CNT/COMPOUT pin. While the VBAT input power is operating, it is interlocked to the ON/OFF control of the switch (SW4) between VBAT and VOUT1. While the VDD and VSTORE2 input power is operating, it is interlocked to the ON/OFF control of the switch (SW1) between VSTORE1 and VOUT1. Output to the SW_CNT/COMPOUT pin is High while SW1 or SW4 is ON.

12.5 General-Purpose Comparator

S6AE103A

This IC has one general-purpose comparator.

It compares the voltage at the COMPP pin and the COMPM pin while ENA_COMP pin is High, and outputs the results to the SW_CNT/COMPOUT pin.

Table 12-3 General-Purpose Comparator Operation

Each Pin Settings		SW_CNT/COMPOUT (Output)
ENA_COMP	COMPP, COMPM	
L	−	Operation described in "12.4 SW_CNT Control"
H	COMPP < COMPM	L
	COMPP > COMPM	H
	"COMPP = COMPM" is prohibited	L or H

12.6 LDO

This IC has one LDO with VIN_LDO pin as a power supply.

The output voltage is set by the resistance value at VOUT_LDO pin and FB_LDO pin connection. The discharge function operates while output is stopped.

Also, there are two operating modes, standby mode for operating at low power consumption, and normal mode in which the maximum output current is 10 mA, which are set at the STBY_LDO pin.

Refer to the following table for the LDO operating modes.

Table 12-4 LDO Operation Mode

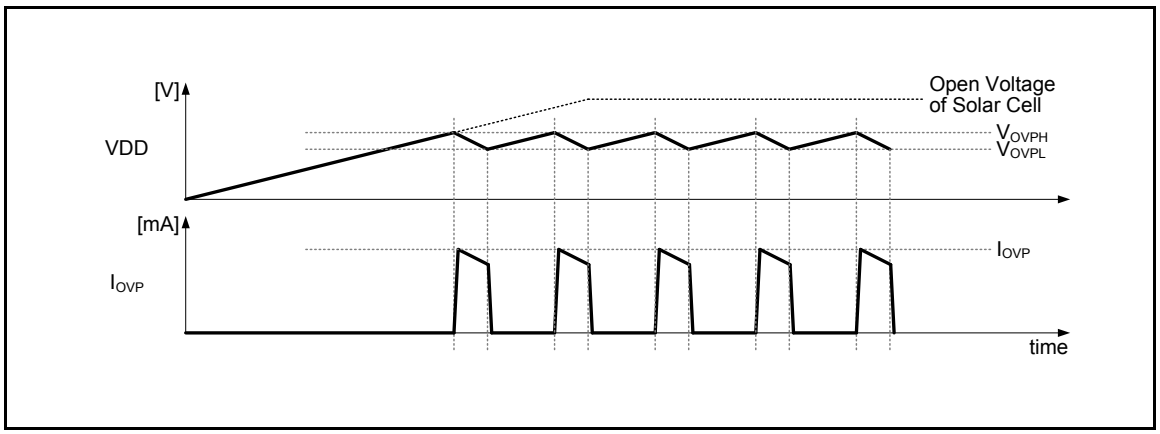
Each Pin Settings		LDO Output State
ENA_LDO	STBY_LDO	
L	L	Output is stopped
	H	
H	L	Standby mode
	H	Normal mode

12.7 Over Voltage Protection (OVP Block)

This IC has an input overvoltage protection (OVP) function for the VDD pin voltage.

When the VDD pin voltage reaches the OVP detection voltage (V_{OVPH} = 5.4V) or higher, the OVP current (IOVP) from the VDD pin is drawn in for limiting the increase in the VDD pin voltage for preventing damage to the IC. Also, when the OVP release voltage (V_{OVPL} = 5.3V) or less is reached, drawing-in of the OVP current is stopped.

Figure 12-8 OVP Operation



13. Application Circuit Example and Parts list

Figure 13-1 Application Circuit Example of S6AE102A

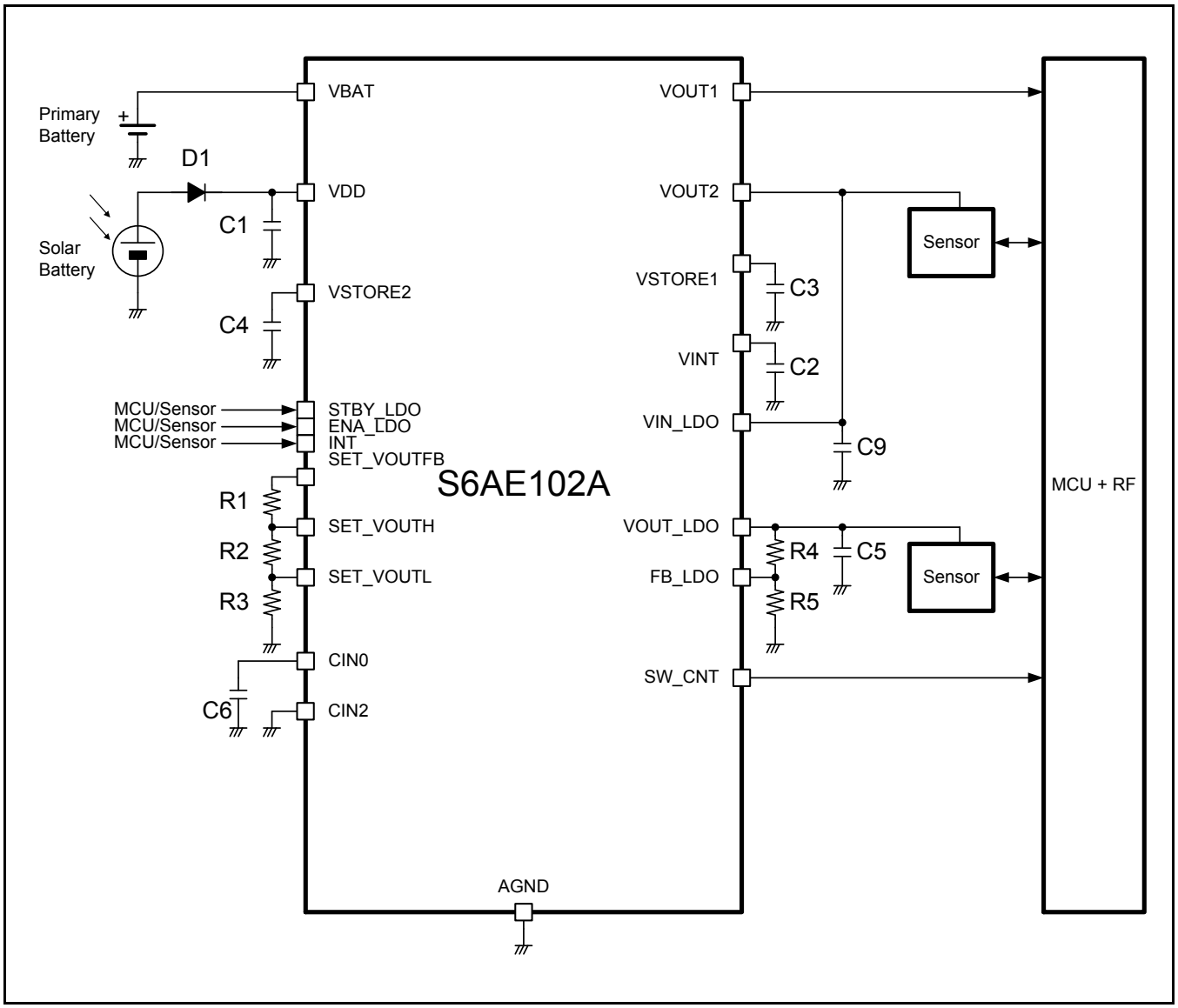


Figure 13-2 Application Circuit Example of S6AE103A

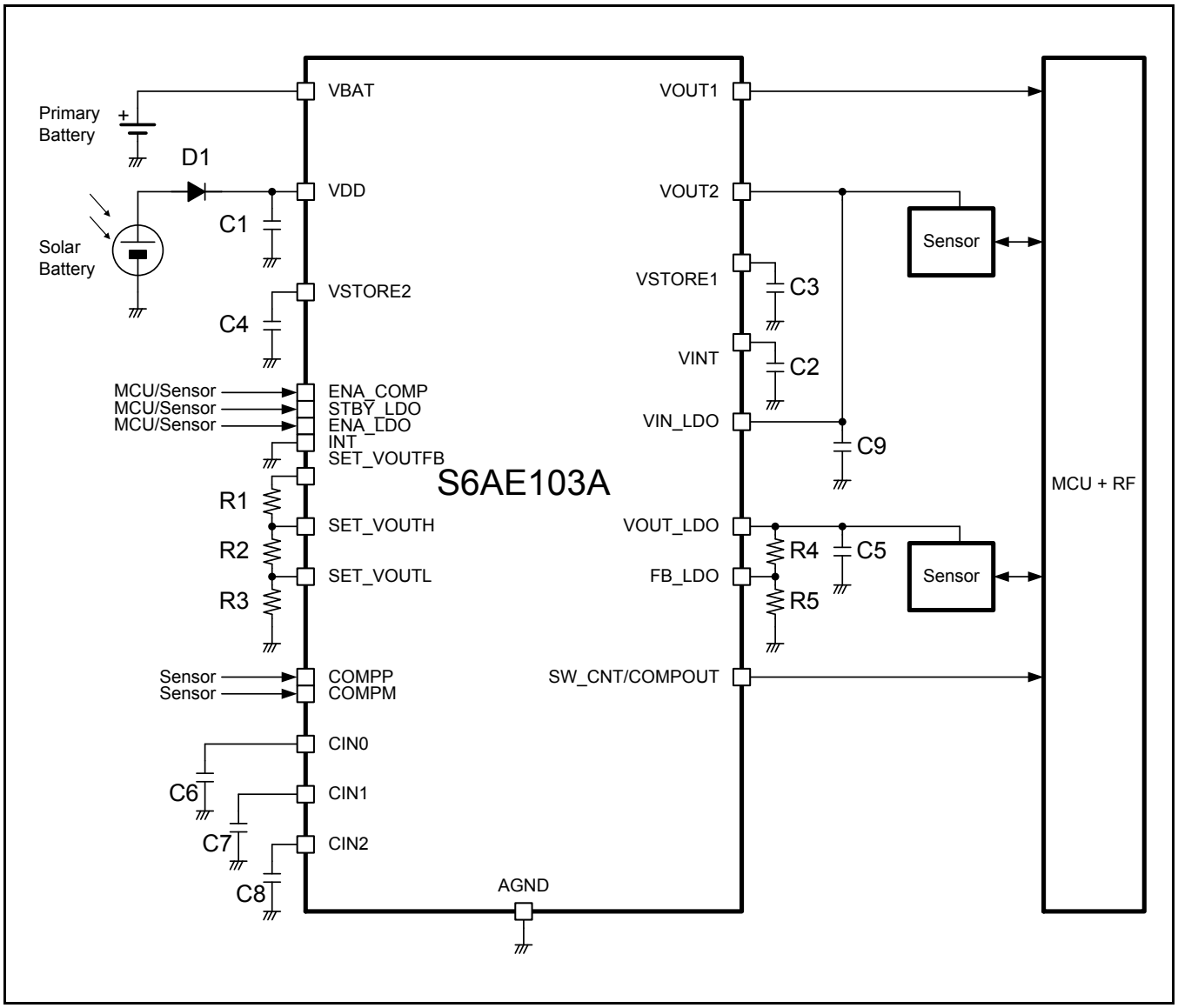


Table 13-1 Parts List

Part Number	Item	Specification	Remarks
C1	Ceramic capacitor	10 µF	−
C2	Ceramic capacitor	1 µF	−
C3	Ceramic capacitor	100 µF	−
C4	Ceramic capacitor	0.5F	−
C5	Ceramic capacitor	22 µF	−
C6	Ceramic capacitor	150 pF (*1)	−
C7	Ceramic capacitor	330 pF (*1)	−
C8	Ceramic capacitor	330 pF (*1)	−
C9	Ceramic capacitor	1 µF	−
R1	Resistor	33 MΩ (*2)	−
R2	Resistor	12 MΩ (*2)	−
R3	Resistor	47 MΩ (*2)	−
R4	Resistor	39 MΩ (*3)	−
R5	Resistor	68 MΩ (*3)	−
D1	Diode	−	−

*1: Timer time 0 (T0) ≈ 0.26s by the use of C6, Timer time 1 and 2 (T1, T2) ≈ 0.57s by the use of C7 or C8.

*2: VOUT upper limit voltage (V_{VOUTH}) ≈ 3.32V, VOUT lower limit voltage (V_{VOUTL}) ≈ 2.65V.

*3: LDO output voltage (V_{OUTLD}) ≈ 1.81V

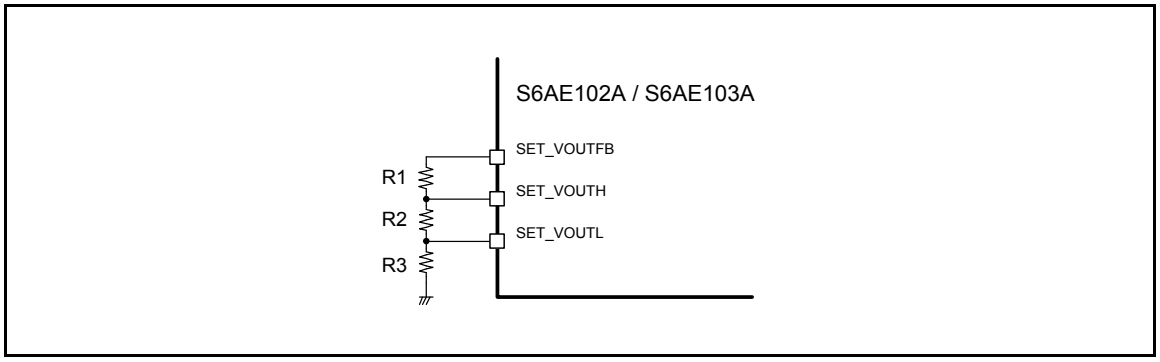
14. Application Note

14.1 Setting the Operation Conditions

Setting of Output Voltage (VOUT1, VOUT2)

The VOUT1 and VOUT2 output voltage of this IC can be set by changing the resistors connecting the SET_VOUTH pin and SET_VOUTL pin. This is because the VOUT upper limit voltage (V_{VOUTH}) and VOUT lower limit voltage (V_{VOUTL}) are set based on the connected resistors. The SET_VOUTFB pin outputs a reference voltage for setting the VOUT upper limit voltage and VOUT lower limit voltage. The voltages applied to the SET_VOUTH and SET_VOUTL pins are produced by dividing this reference voltage outside the IC.

Figure 14-1 Setting of Output Voltage (VOUT1, VOUT2)



The VOUT upper limit voltage (V_{VOUTH}) and VOUT lower limit voltage (V_{VOUTL}) can be calculated using the formulas below.

VOUT upper limit voltage

$$V_{VOUTH}\ [V] = \frac{57.5 \times (R2 + R3)}{11.1 \times (R1 + R2 + R3)}$$

VOUT lower limit voltage

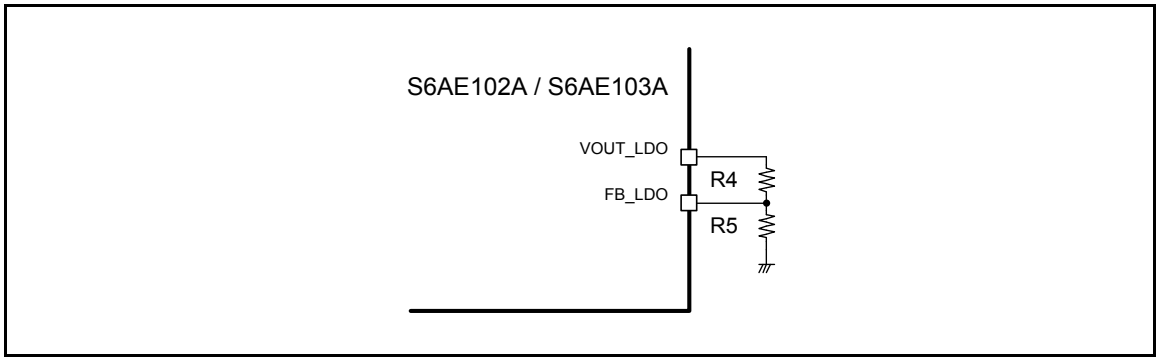
$$V_{VOUTL}\ [V] = \frac{57.5 \times R3}{11.1 \times (R1 + R2 + R3)}$$

The characteristics when the total for R1, R2, and R3 is 10 MΩ or more (consumption current 1 is 100 MΩ or more) are shown in "11. Electrical Characteristics".

Setting of LDO Output Voltage (VOUT_LDO)

The VOUT_LDO output voltage of this IC can be set by changing the resistors connecting the VOUT_LDO pin and FB_LDO pin.

Figure 14-2 Setting of LDO Output Voltage (VOUT_LDO)



The LDO output voltage (V_{OUTLD}) can be calculated using the formula below.

$$V_{OUTLD}\ [V] = \frac{1.15 \times (R4 + R5)}{R5}$$

Setting of Timer Time (T0, T1, T2)

The timer times 0, 1, and 2 (T0, T1, and T2) are set according to the capacitance value at the connections between the CIN0, CIN1, and CIN2 pins and the AGND pin.

The timer time 0 (T0), timer time 1 (T1) and timer time 2 (T2) can be calculated using the formula below.

$$T\ [s] = 1.734 \times 10^{9} \times C\ [F]$$

15. Usage Precaution

Printed circuit board ground lines should be set up with consideration for common impedance.

Take appropriate measures against static electricity.

- Containers for semiconductor materials should have anti−static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ in serial body and ground.

Do not apply negative voltages.

The use of negative voltages below −0.3V may make the parasitic transistor activated to the LSI, and can cause malfunctions.

16. RoHS Compliance Information

This product has observed the standard of lead, cadmium, mercury, Hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE).

17. Ordering Information

Part Number	Package
S6AE102A0DGN1B000 (*1)	Plastic QFN-20 (0.5 mm pitch), 20-pin (VNF020)
S6AE102A0DEN1B000 (*2)	
S6AE103A0DGN1B000 (*1)	Plastic QFN-24 (0.5 mm pitch), 24-pin (VNF024)
S6AE103A0DEN1B000 (*2)	

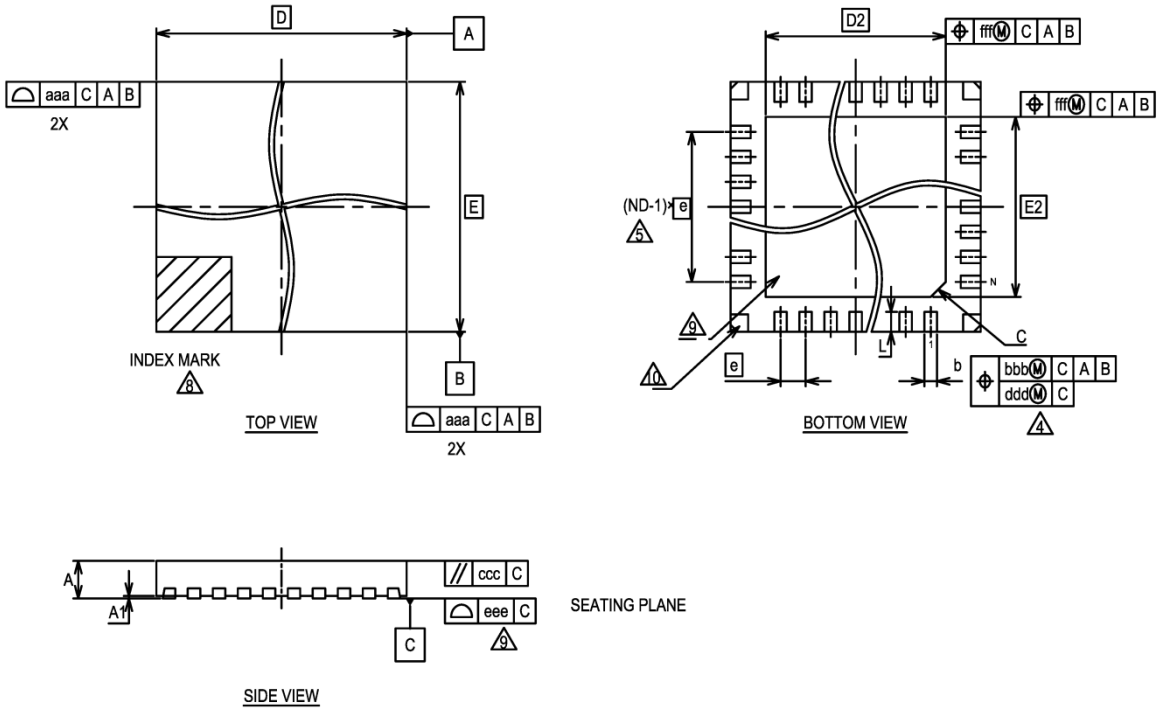
*1: Commercial Sample (CS)

*2: Engineering Sample (ES)

18. Package Dimensions

Figure 18-1 Package Dimensions of S6AE102A (VNF020)

VNF020 VERY THIN PLASTIC QUAD FLAT NO LEAD PACKAGES



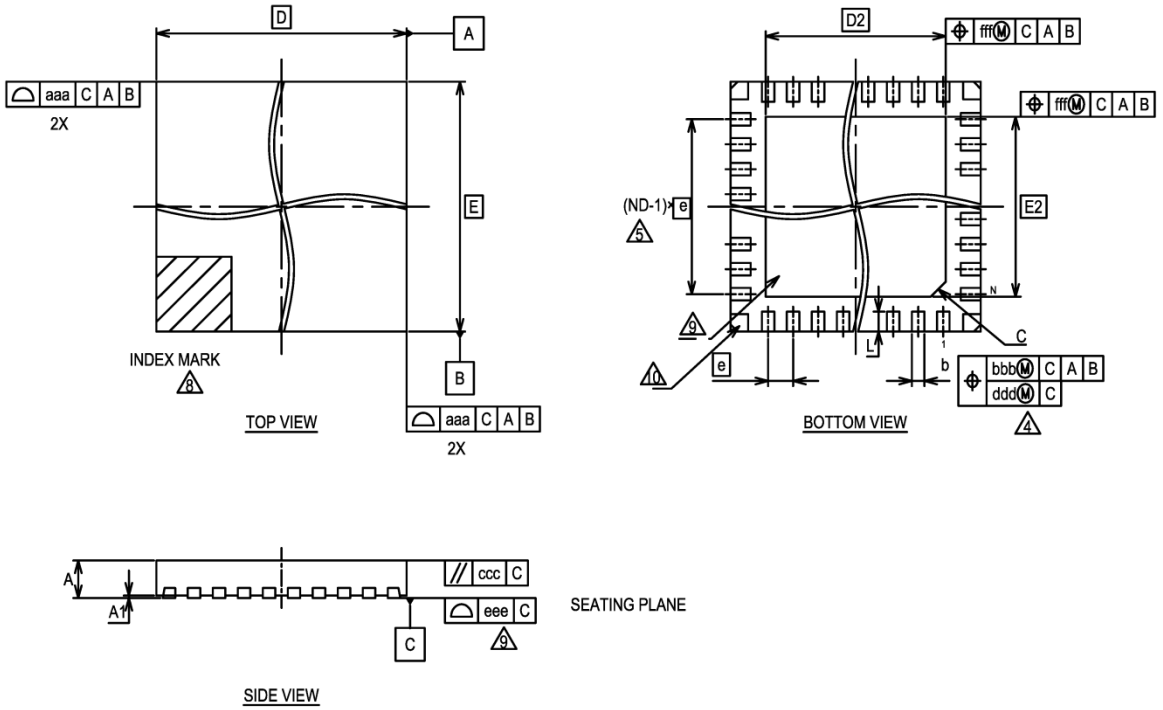
SYMBOL	MILLIMETER			NOTE
	MIN.	NOM.	MAX.	
A	—	—	0.90	PROFILE
A_1	0.00	—	0.05	TERMINAL HEIGHT
D		4.00 BSC.		BODY SIZE
E		4.00 BSC.		BODY SIZE
b	0.20	0.25	0.30	TERMINAL WIDTH
D_2		2.60 BSC.		EXPOSED PAD SIZE
E_2		2.60 BSC.		EXPOSED PAD SIZE
e		0.50 BSC.		TERMINAL PITCH
N		20		TERMINAL COUNT
L	0.30	0.40	0.50	TERMINAL LENGTH
C		C0.50		EXPOSED PAD CHAMFER
aaa	—	—	0.2	
bbb	—	—	0.05	
ccc	—	—	0.2	
ddd	—	—	—	
eee	—	—	0.05	
fff	—	—	—	

1. DIMENSIONING AND TOLERANCINC CONFORMS TO ASME Y14.5-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL. THE DIMENSION "b"SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFER TO THE NUMBER OF TERMINALS ON D OR E SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN INDICATED ZONE.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. Reinforcement Land size:0.35mm SQ.

Rev. A

Figure 18-2 Package Dimensions of S6AE103A (VNF024)

VNF024 VERY THIN PLASTIC QUAD FLAT NO LEAD PACKAGES



SYMBOL	MILLIMETER			NOTE
	MIN.	NOM.	MAX.	
A	—	—	0.90	PROFILE
A_1	0.00	—	0.05	TERMINAL HEIGHT
D		4.00 BSC.		BODY SIZE
E		4.00 BSC.		BODY SIZE
b	0.20	0.25	0.30	TERMINAL WIDTH
D_2		2.60 BSC.		EXPOSED PAD SIZE
E_2		2.60 BSC.		EXPOSED PAD SIZE
e		0.50 BSC.		TERMINAL PITCH
N		24		TERMINAL COUNT
L	0.30	0.40	0.50	TERMINAL LENGTH
C		C0.50		EXPOSED PAD CHAMFER
aaa	—	—	0.2	
bbb	—	—	0.05	
ccc	—	—	0.2	
ddd	—	—	—	
eee	—	—	0.05	
fff	—	—	—	

1. DIMENSIONING AND TOLERANCINC CONFORMS TO ASME Y14.5-1994.
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Rev. A

19. Major Changes

Page	Section	Change Results
Preliminary 0.1		
-	-	Initial release
Preliminary 0.2		
-	-	Typo error correction

Colophon

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