1.2W MONAURAL SPEAKER AMPLIFIER WITH ELECTRONIC VOLUME

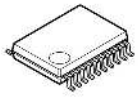
■GENERAL DESCRIPTION

The **NJU72065** is a 1.2W output speaker amplifier with electronic volume. It is suitable for various equipment with voice guidance and beep sound.

The **NJU72065** has a standby function providing low current consumption at no input signals (mute). It also reduces pop noise at turning active and standby mode. All functions are controlled by I^2C BUS interface.

■PACKAGE OUTLINE

NJU72065RB2

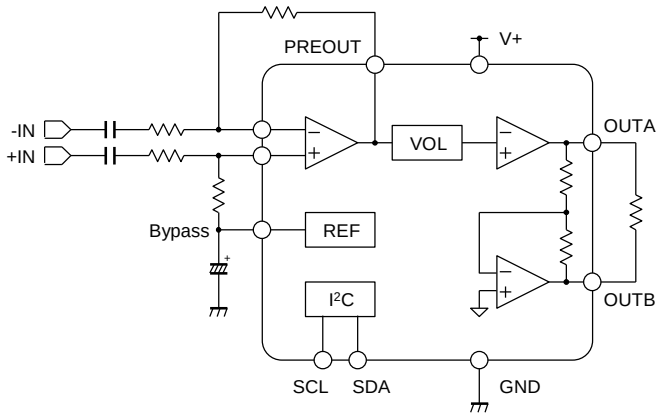


NJU72065VC3

■FEATURES

- Operating Voltage: +2.7 to +5.5V
- Output Power: 1.2W typ. (V^+=5V, R_L=8Ω, THD=1%)
  500mW typ. (V^+=3.3V, R_L=8Ω, THD=1%)
- Volume: 0 to -42dB/3dBstep, Mute
- I^2C BUS Control
- Standby function
- Single-end Input / Differential Input
- Thermal Shutdown Circuit
- Pop Noise Suppression Circuit
- Current Limit
- CMOS Technology
- Package: MSOP10(TVSP10), SSOP20-C3

■BLOCK DIAGRAM



■ PIN CONFIGURATION

No.		Symbol	Function
MSOP 10	SSOP 20-C3		
1	4	SDA	I^2C Data Input / Acknowledge Output
2	5	SCL	I^2C Clock Input
3	6	Bypass	Reference Voltage
4	7	+IN	Non-inverted Input
5	8	-IN	Inverted Input
6	13	PREOUT	Pre Output
7	14	OUTA	Output A
8	15	V+	Supply Voltage
9	16	GND	Ground
10	17	OUTB	Output B

■ABSOLUTE MAXIMUM RATING (Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V^+	+7	V
Power Dissipation	P_D	505 *1) / 700 *2) (MSOP10) 945 *1) / 1350 *2) (SSP20-C3)	mW
Output Current	I_O	600	mA
Input Voltage Range	V_{IN}	-0.3 to V^++0.3 *3)	V
Operating Temperature Range	Topr	-40 to +105	°C
Storage Temperature Range	Tstg	-40 to +150	°C

*1) EIA/JEDEC STANDARD Test board (76.2x114.3x1.6mm, 2layer, FR-4) mounting
*2) EIA/JEDEC STANDARD Test board (76.2x114.3x1.6mm, 4layer, FR-4) mounting
*3) +IN, -IN, PREOUT, OUTA, OUTB terminals

■RECOMMENDED OPERATING VOLTAGE RANGE (Ta=25°C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage Range	V^+	-	+2.7	+5.0	+5.5	V

■ELECTRICAL CHARACTERISTICS

(Ta=25°C, V^+=+5V, R_L=8Ω, Ri=20kΩ, Rf=20kΩ, f=1kHz, Volume Setting=0dB unless otherwise specified)

♦DC CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current 1	I_{DD1}	No signal, R_L=∞	-	2.7	3.7	mA
Supply Current 2	I_{DD2}	No signal, R_L=∞, V^+=+3.3V	-	2.3	2.8	mA
Supply Current (Standby)	I_{SD}	No signal, R_L=∞, Standby V_{Pullup}=5V *4)	-	-	2	μA
Output Offset Voltage	V_{OD}	No signal	-	-	50	mV

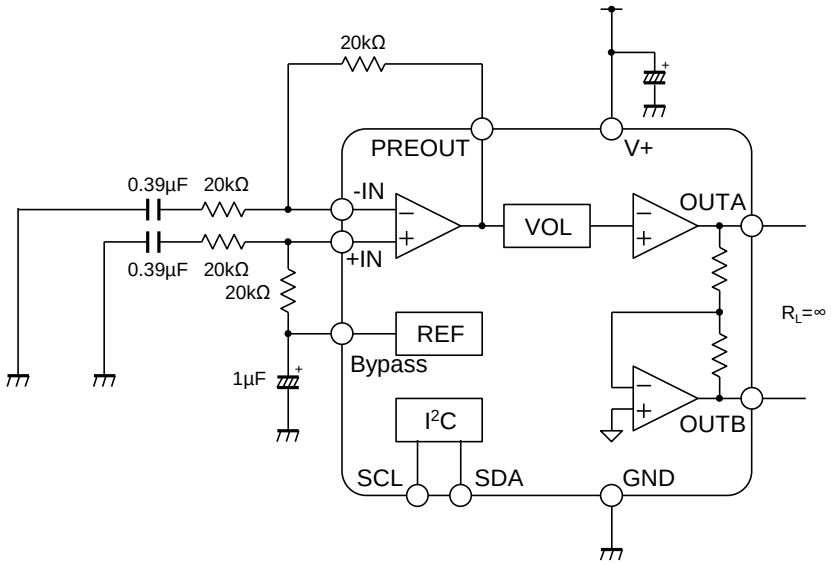
♦AC CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Voltage Gain 1	Gv_1	Vin=1Vrms	+5	+6	+7	dB
Voltage Gain 2	Gv_2	Vin=1Vrms, Volume Setting=-21dB	-16	-15	-14	dB
Maximum Attenuation	A_{TT}	Vin=1Vrms, Standby	-	-110	-	dB
Output Power 1	P_{O1}	THD≤1%	0.9	1.2	-	W
Output Power 2	P_{O2}	THD≤1%, V^+=+3.3V	375	500	-	mW
Total Harmonic Distortion	THD+N	P_O=1W	-	0.1	-	%
Supply Voltage Rejection Ratio	PSRR	Vripple=100mVrms	-	55	-	dB

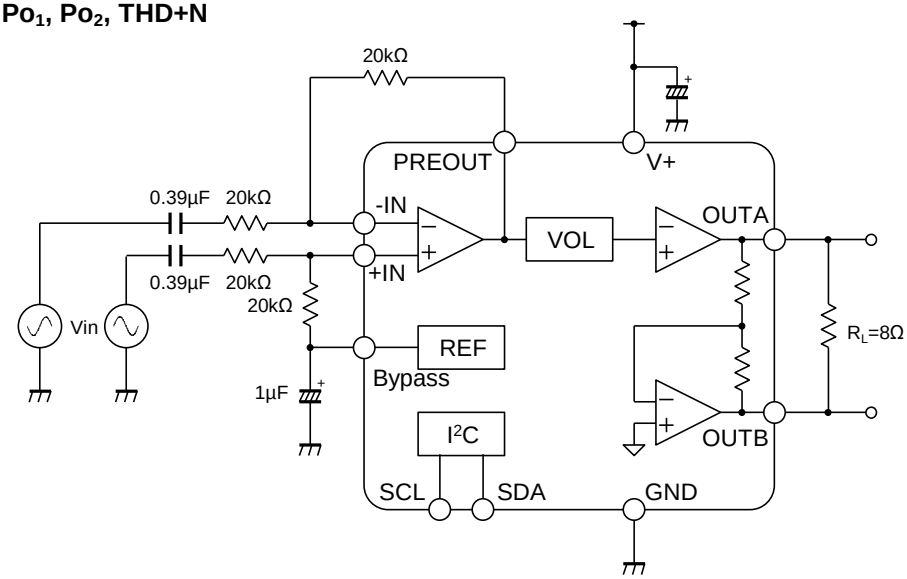
*4) V_{Pullup} is I^2C BUS's pull up voltage.

■ TEST CIRCUIT

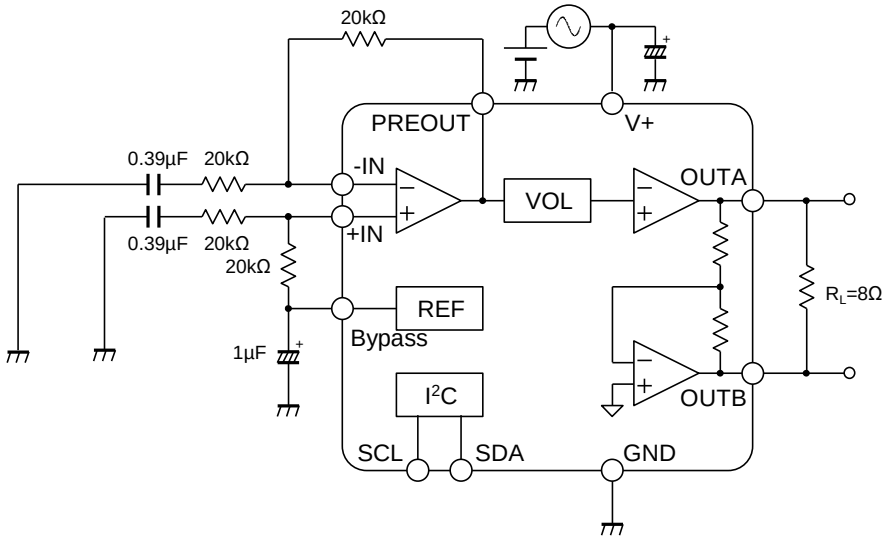
♦ I_{DD1}, I_{DD2}, I_{ST}, V_{OD}



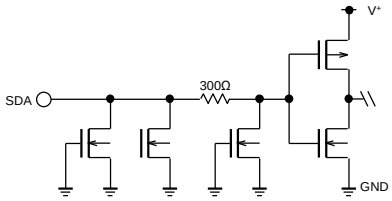
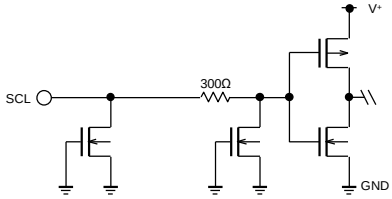
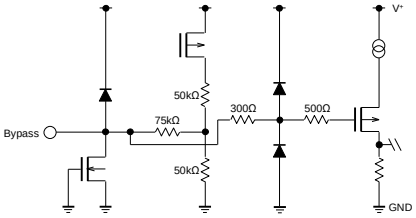
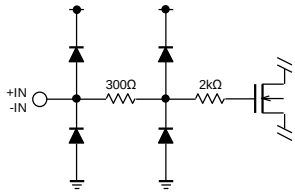
♦ Gv_1, Gv_2, ATT, Po_1, Po_2, THD+N

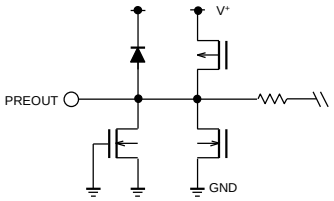
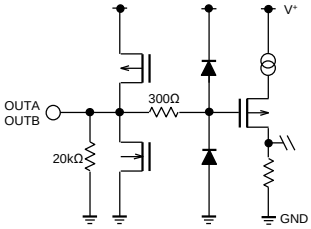


♦ PSRR



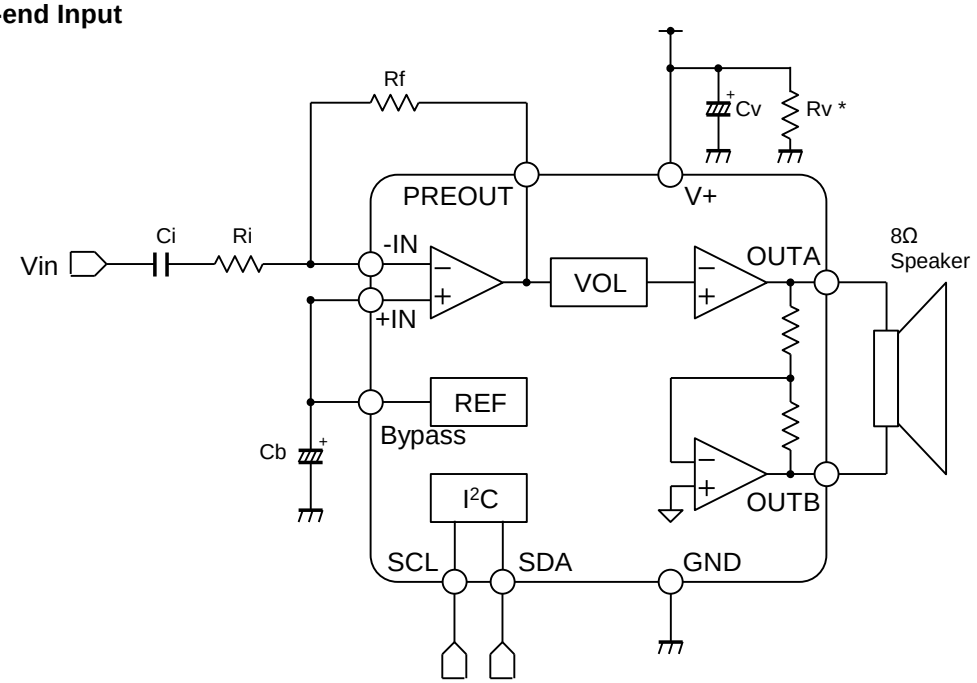
■ TERMINAL DESCRIPTION

TERMINAL		SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLTAGE
MSOP 10	SSOP 20-C3				
1	4	SDA	I^2C Data Input / Acknowledge Output		-
2	5	SCL	I^2C Clock Input		-
3	6	Bypass	Reference Voltage		$V^+/2$
4 5	7 8	+IN -IN	Non-Inverted Input Inverted Input		$V^+/2$

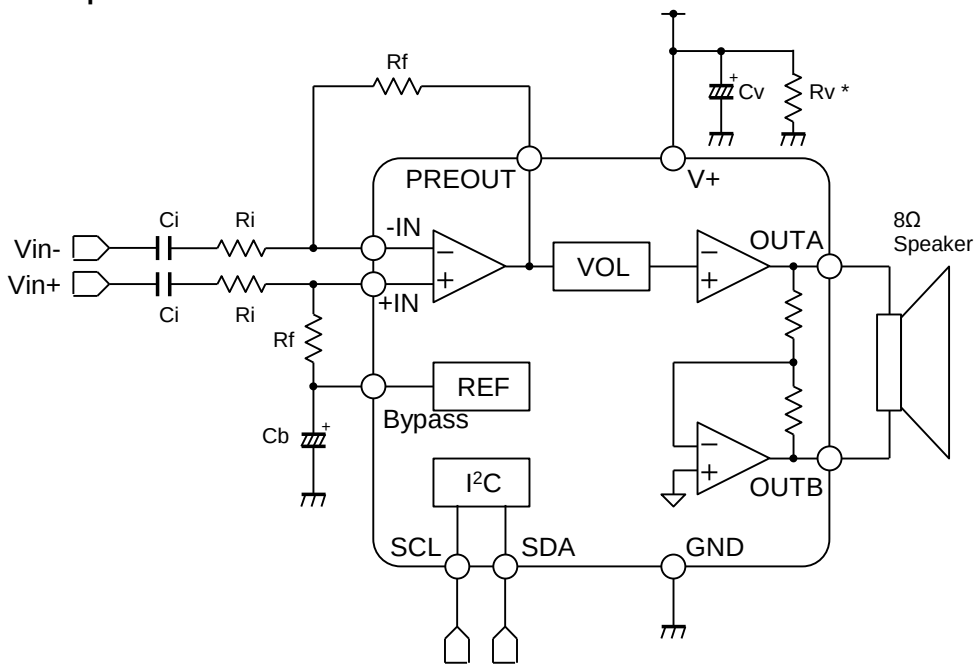
TERMINAL		SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLTAGE
MSOP 10	SSOP 20-C3				
6	13	PREOUT	Pre Output		$V^+/2$
7 10	14 17	OUTA OUTB	Output A Output B		$V^+/2$

■ APPLICATION CIRCUIT

♦ **Single-end Input**

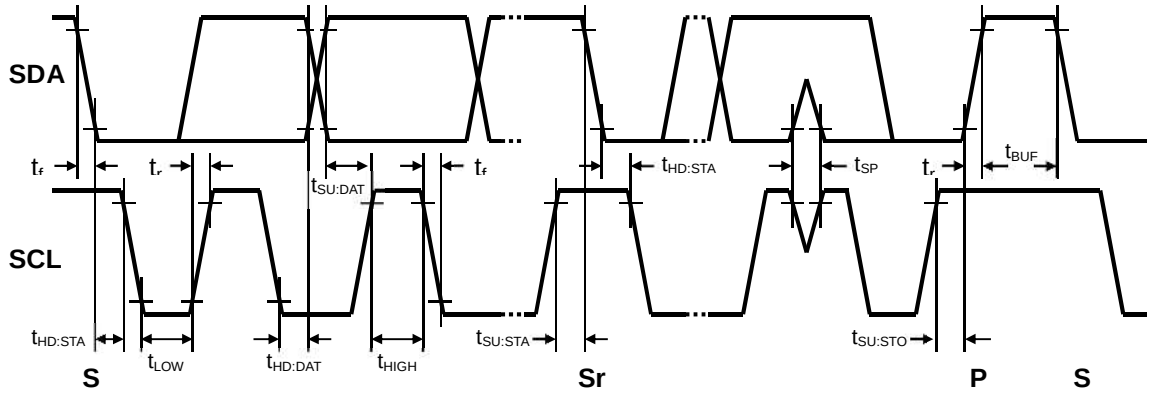


♦ **Differential Input**



* It is a discharge resistor assuming that the Supply Voltage terminal voltage does not drop to 0V after turning off power supply. For details, see application notes 2.5 on page 12.

■TIMING ON THE I²C BUS (SDA, SCL)



■CHARACTERISTICS OF I/O STAGES FOR I²C BUS (SDA, SCL)

I²C BUS Load Conditions

Standard mode : Pull up resistance 4kΩ (Connected to +5V), Load capacitance 200pF (Connected to GND)

Fast mode : Pull up resistance 4kΩ (Connected to +5V), Load capacitance 50pF (Connected to GND)

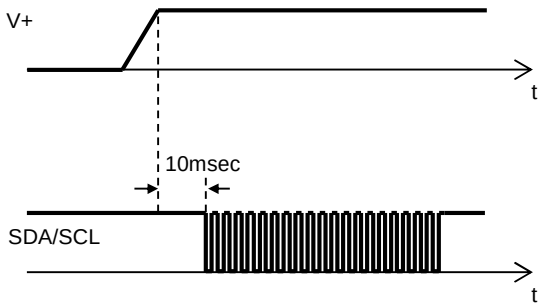
PARAMETER	SYMBOL	Standard mode			Fast mode			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Low Level Input Voltage	V_{IL}	0.0	-	$0.2*V^+$	0.0	-	$0.2*V^+$	V
High Level Input Voltage	V_{IH}	$0.5*V^+$	-	V^+	$0.5*V^+$	-	V^+	V
Low Level output voltage (3mA at SDA pin)	V_{OL}	0	-	0.4	0	-	0.4	V
Input current each I/O pin with an input voltage between $0.1V_{DD}$ and $0.9V_{DDmax}$	I_i	-10	-	10	-10	-	10	μA

■CHARACTERISTICS OF BUS LINES (SDA, SCL) FOR I²C BUS DEVICES

PARAMETER	SYMBOL	Standard mode			Fast mode			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
SCL clock frequency	f_{SCL}	-	-	100	-	-	400	kHz
Hold time (repeated) START condition	$t_{HD:STA}$	4.0	-	-	0.6	-	-	μs
Low period of the SCL clock	t_{LOW}	4.7	-	-	1.3	-	-	μs
High period of the SCL clock	t_{HIGH}	4.0	-	-	0.6	-	-	μs
Set-up time for a repeated START condition	$t_{SU:STA}$	4.7	-	-	0.6	-	-	μs
Data hold time	$t_{HD:DAT}$	0	-	-	0	-	-	μs
Data set-up time	$t_{SU:DAT}$	250	-	-	100	-	-	ns
Rise time of both SDA and SCL signals	t_r	-	-	1000	-	-	300	ns
Fall time of both SDA and SCL signals	t_f	-	-	300	-	-	300	ns
Set-up time for STOP condition	$t_{SU:STO}$	4.0	-	-	0.6	-	-	μs
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	-	1.3	-	-	μs
Capacitive load for each bus line	C_b	-	-	400	-	-	400	pF
Noise margin at the Low Level	V_{nL}	0.5	-	-	0.5	-	-	V
Noise margin at the High Level	V_{nH}	1	-	-	1	-	-	V

C_b ; total capacitance of one bus line in pF.

■ RECOMMENDED POWER-UP SEQUENCE



■ CONTROL DATA

Note) Please don't send except specified data for avoiding an incorrect operation.

♦I²C BUS FORMAT

	MSB	LSB		MSB	LSB		
S	Slave Address		A	Data		A	P
1bit	8bit		1bit	8bit		1bit	1bit

S: Starting Term
A: Acknowledge Bit
P: Ending Term

♦SLAVE ADDRESS

Slave Address								Hex
MSB							LSB	-
1	0	0	0	1	0	0	0	88(h)

♦CONTROL REGISTER TABLE

<Write Mode>

Data							
D7	D6	D5	D4	D3	D2	D1	D0
*	*	*	STANDBY	VOLUME			

*: Don't Care

♦CONTROL REGISTER DEFAULT VALUE

Control register default value is all "0".

Data							
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

Note.) This product starts up by Standby mode when power supply is turned on. Select each setting and use it after turning on power supply.
When power supply is turned off, it may cause initial condition abnormality in the case that turn on power supply again before the Supply Voltage terminal voltage drop to 0V or any audio signal is applied the input signal terminal before turning on power supply. In such cases, it is necessary to set the Standby data of STANDBY register table in order to prevent the abnormal initial condition.

■ DEFINITION OF REGISTER

♦STANDBY: Select “Standby” or “Active”

	Data
	D4
Standby *	0
Active	1

*: Default Value

♦VOLUME: Attenuator Range 0 to -42dB, Mute

	Data			
	D3	D2	D1	D0
0dB *	0	0	0	0
-3dB	0	0	0	1
-6dB	0	0	1	0
-9dB	0	0	1	1
-12dB	0	1	0	0
-15dB	0	1	0	1
-18dB	0	1	1	0
-21dB	0	1	1	1
-24dB	1	0	0	0
-27dB	1	0	0	1
-30dB	1	0	1	0
-33dB	1	0	1	1
-36dB	1	1	0	0
-39dB	1	1	0	1
-42dB	1	1	1	0
Mute	1	1	1	1

*: Default Value

■ APPLICATION NOTES

The NJU72065 is a 1.2W monaural speaker amplifier with a built-in electronic volume. It operates from 2.7V supply. So it can output high power and it can reduce output coupling capacitor because it has a BTL amplifier. The voltage gain is set by the user-selected resister (Ri, Rf) and the built-in electronic volume. The NJU72065 equips with a standby mode. It reduces supply current and turns to mute at standby mode. It reduces pop noise at turning standby and active mode. All functions are controlled by I^2C BUS interface.

In this application note, the usage of this IC and its operation are discussed.

1. Operating Overview

Fig.1 and Fig.2 shows the NJU72065 block diagram. It comprises of pre-amplifier (Pre-Amp), electronic volume, I^2C BUS control circuit, two power amplifiers (Amp-A, Amp-B), a bias circuit (REF), and a thermal shutdown(TSD) circuit. The Pre-Amp uses external resistors and it has adjustable gain. The volume is controlled by I^2C BUS and it attenuates Pre-Amp's output signal from 0 to -42dB and Mute. The Amp-B is configured with a fixed gain of Av=-1 and produces the inverted signal of the OUTA terminal. The NJU72065 outputs twice voltage and four times power compared to a single-ended amplifier because it is BTL amplifier which speaker's load resistance is connected between the OUTA terminal and the OUTB terminal. When a standby mode is active, it stops all circuits except the I^2C BUS control circuit. As a result, the standby mode reduces the supply current. Time constant which is made up the external capacitor (Cb) and Internal resistance reduces disturbing pop noise at turning active and standby mode. For details, see 3. Pop Noise at turning active and standby mode. But Cb value depends on the turn-on time (standby to active time). For details, see 4. Turn on time / turn off time.

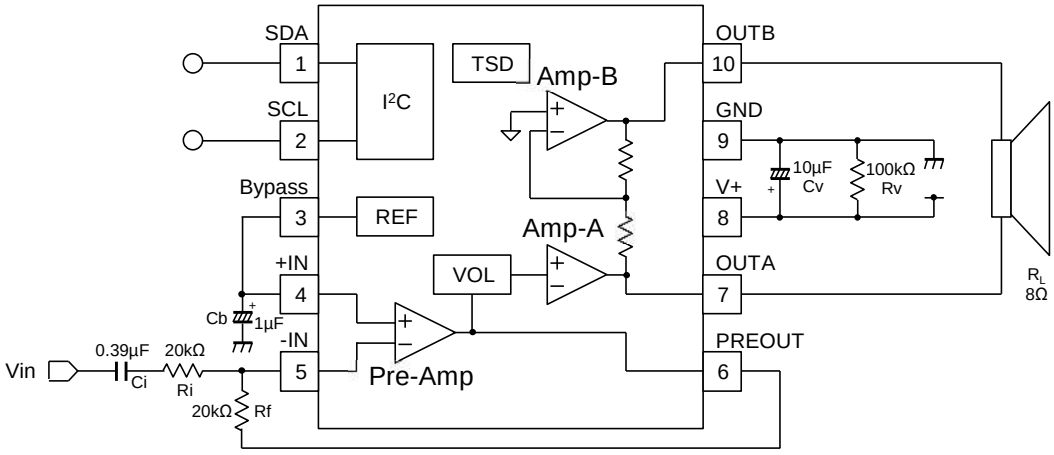


Fig.1 Block diagram and Application circuit (Single-end Input)

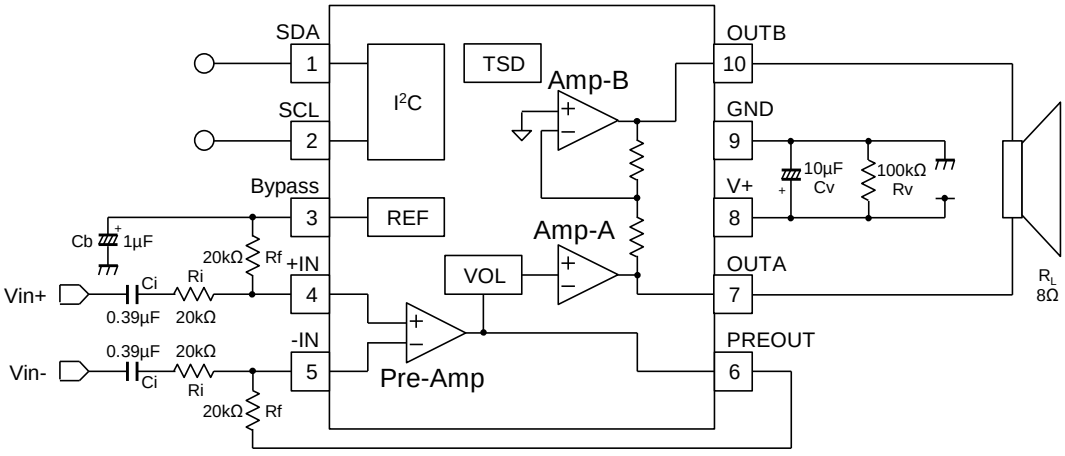


Fig. 2 Block diagram and Application circuit (Differential Input)

2. External Component

2.1 Bypass Capacitor

Power source bypass capacitor (Cv) reduces a noise and it stabilizes power source. Cv should have margin for temperature characteristics and the better characteristic in high frequency. Design to provide low impedance for the wiring between the IC and the capacitor. It is necessary to provide lower impedance in case that the NJU72065 uses high current like 4Ω loads. So it is recommended a ceramic chip capacitor which has low ESR.

2.2 Input Resistor and Feedback Resistor

The NJU72065's pre-amplifier gain depends on Input Resistor (Ri) and Feedback Resistor (Rf). The values of Ri and Rf affect output noise and disturbing pop noise in case that they increase.

So Ri affects frequency response. It is necessary to consider about 2.3 Input Coupling Capacitor and select Ri.

The NJU72065's BTL output voltage gain (Gv) is set by the following under the condition that the pre-amplifier voltage gain is $Gv_{\_PRE}$ and the EVR volume setting is $Gv_{\_EVR}$.

$$Gv = \frac{V_{OUTA} - V_{OUTB}}{V_{-IN} - V_{+IN}} = Gv_{\_PRE} + Gv_{\_EVR} = 20 \cdot Log\left(2 \cdot \frac{R_f}{R_i}\right) + Gv_{\_EVR}\,[dB]$$

$$\left(Gv \le +12\,[dB]\right)$$

2.3 Input Coupling Capacitor

The input coupling capacitor (Ci) is necessary for DC cut. Ci forms a HPF with Ri and low frequency signal is cut. Lower frequency signal is passed through in case that values of Ci and Ri increase, but pop noise may be loud.

The input coupling capacitor (Ci) is set by the following under the condition that the cutoff frequency is fc.

$$C_i = \frac{1}{2\pi \cdot R_i \cdot f_c}\,[F]$$

2.4 Bypass Capacitor for Reference Voltage

The capacitor (Cb) is connected to the Bypass terminal and it reduces a noise and it stabilizes reference voltage. The value of Cb causes pop noise, PSRR and turn on time. Pop noise and PSRR are improved in case that value of Cb is increases. See 3. Pop Noise at turning active and standby mode and 5. PSRR vs Cb, 7. Volume. But turn on time is longer in case that Cb increases. See 4. Turn on time / Turn off time.

2.5 Discharge resistor for Supply Voltage terminal

When power supply is turned off, it may cause initial condition abnormality in the case that turn on power supply again before the Supply Voltage terminal voltage drop to 0V. In such case, it is recommended that using a power supply IC with a discharge function to lower the power supply pin voltage to 0V immediately after turning off power supply or using a discharge resistor (Rv) of about 100kΩ between the Supply Voltage terminal and the GND terminal.

Table 1 shows recommendation value range of external component. It is merely recommendation. There is possibility in the using in case that their value varies from the recommendation. In the using, it should verify the characteristics.

Table 1. Function and recommendation value range of external components

Component	Function	Recommendation value	
		Default	Range
Cv	Bypass capacitor for power source	10uF	1uF<Cv
Ri	Input resistor	20kΩ	10kΩ<Ri<50kΩ
Rf	Feedback resistor	20kΩ	10kΩ<Rf<50kΩ
Ci	Input coupling capacitor	0.39uF	0.047uF<Ci
Cb	Bypass capacitor for reference voltage	1uF	0.1uF<Cb
R_L	Load resistor(speaker)	8Ω	4Ω<R_L

3. Pop Noise at turning active and standby mode

The NJU72065 has pop noise suppression circuit when it turns active and standby mode. But pop noise depends on the value of external components. This section shows the point of pop noise reduction.

3.1 Standby to Active (turn on)

The NJU72065 is BTL amplifier and it does not generate sound, if there is no difference voltage between two outputs at turning to active mode. But difference voltage which Pre-Amp(Amp-A) output voltage is higher than the reference voltage (the Bypass terminal voltage) and Amp-B output voltage is lower than the reference voltage (the Bypass terminal voltage) occurs and generates pop noise at turning to active mode because input coupling capacitor (Ci) is charged. The NJU72065 is designed that the amplifier operates after charged Ci and risen the -IN terminal voltage

Pop noise is low in case that difference voltage between the +IN terminal and the –IN terminal is low (in other words, Ci has been charged) at the moment amplifier operates. It is necessary to be careful to select Ci, input resistor (Ri) and feedback resistor (Rf) because charging time constant for Ci is large in case that they increase.

It is necessary that Ci decreases and bypass capacitor for reference voltage (Cb) increase for pop noise reduction. It is important to be careful to select the value of them because low frequency signal is cut in case that Ci decreases and turn on time is long in the case that Cb increases.

Table 2 to 6 shows the value of Cb for equivalent pop noise of application circuit which sets default value.

3.2 Active to Standby (turn off)

The NJU72065's output stops steeply at turning to standby mode. Pop noise is low under the condition of using BTL amplifier because Amp-A and Amp-B of outputs are turned off simultaneously. It is necessary to be careful in the case that the standby and active are switched at such short intervals that bypass capacitor for reference voltage (Cb) connected to the Bypass terminal is not discharged because normal amplifier startup operation described in 3.1 does not occur and pop noise occurs.

It is necessary to be careful under the condition of using single-end amplifier because pop noise occurs.

Table 2. The value of Cb at Ri=10kΩ

		Rf				
		10kΩ	20kΩ	30kΩ	40kΩ	50kΩ
Ci	0.047μF	0.1μF	0.33μF	0.33μF	0.33μF	0.33μF
	0.1μF	0.33μF	0.33μF	1μF	1μF	1μF
	0.39μF	1μF	1μF	2μF	2μF	3.3μF
	0.47μF	1μF	2μF	2μF	3.3μF	3.3μF
	1μF	2μF	3.3μF	4.7μF	10μF	10μF

Table 3. The value of Cb at Ri=20kΩ

		Rf				
		10kΩ	20kΩ	30kΩ	40kΩ	50kΩ
Ci	0.047μF	0.1μF	0.33μF	0.33μF	0.33μF	0.33μF
	0.1μF	0.33μF	0.33μF	1μF	1μF	1μF
	0.39μF	1μF	1μF	2μF	2μF	3.3μF
	0.47μF	1μF	2μF	2μF	3.3μF	3.3μF
	1μF	2μF	3.3μF	4.7μF	10μF	10μF

Table 4. The value of Cb at Ri=30kΩ

		Rf				
		10kΩ	20kΩ	30kΩ	40kΩ	50kΩ
Ci	0.047μF	0.1μF	0.33μF	0.33μF	0.33μF	0.33μF
	0.1μF	0.33μF	0.33μF	1μF	1μF	1μF
	0.39μF	1μF	1μF	2μF	2μF	3.3μF
	0.47μF	1μF	2μF	2μF	3.3μF	3.3μF
	1μF	2μF	3.3μF	4.7μF	10μF	10μF

Table 5. The value of Cb at Ri=40kΩ

		Rf				
		10kΩ	20kΩ	30kΩ	40kΩ	50kΩ
Ci	0.047μF	0.1μF	0.33μF	0.33μF	0.33μF	0.33μF
	0.1μF	0.33μF	0.33μF	1μF	1μF	1μF
	0.39μF	1μF	1μF	2μF	2μF	3.3μF
	0.47μF	1μF	2μF	2μF	3.3μF	3.3μF
	1μF	2μF	3.3μF	4.7μF	10μF	10μF

Table 6. The value of Cb at Ri=50kΩ

		Rf				
		10kΩ	20kΩ	30kΩ	40kΩ	50kΩ
Ci	0.047μF	0.1μF	0.33μF	0.33μF	0.33μF	0.33μF
	0.1μF	0.33μF	0.33μF	1μF	1μF	1μF
	0.39μF	1μF	1μF	2μF	2μF	3.3μF
	0.47μF	1μF	2μF	2μF	3.3μF	3.3μF
	1μF	2μF	3.3μF	4.7μF	10μF	10μF

4. Turn on time (standby to active time) / turn off time (active to standby time)

Pop noise and PSRR are improved in case that value of bypass capacitor for reference voltage (Cb) increases. But turn on time (standby to active time) is longer because Ci is charged. The NJU72065's output stops steeply at turning off (active to standby).

Fig.3 to 6 shows typical characteristics of Turn on time vs the value of Cb. Turn on time is prescribe time of stabilized output signal after receiving the acknowledge signal of DATA.

There is variation in turn on time because there is variation of the bypass terminal resistor.

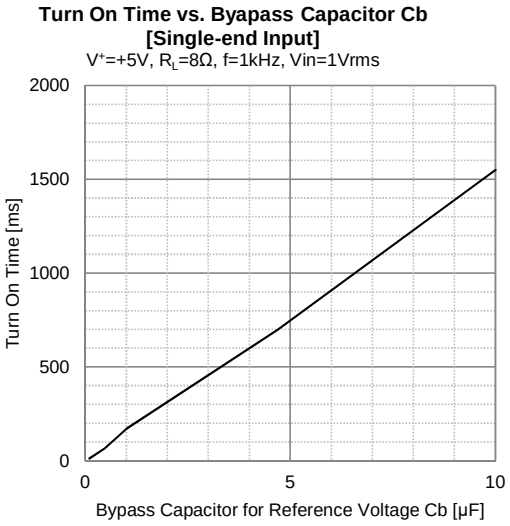


Fig. 3 Turn on time vs. Cb
(Single-end input, V^+=5V)

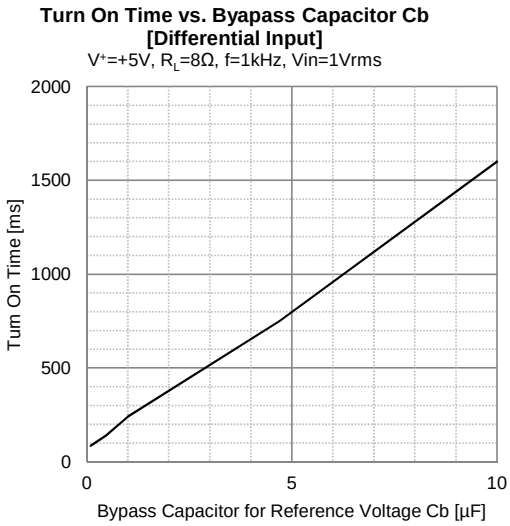


Fig. 4 Turn on time vs. Cb
(Differential input, V^+=5V)

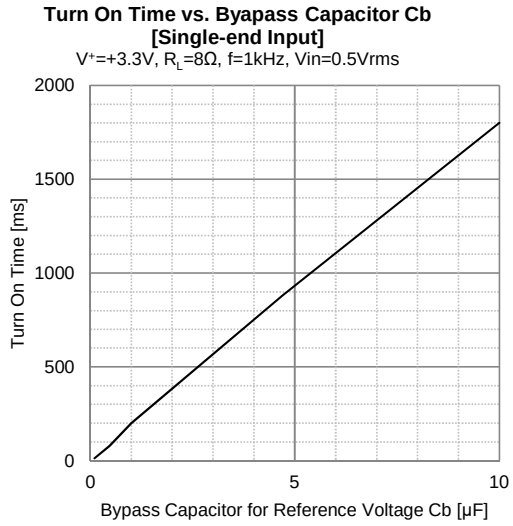


Fig. 5 Turn on time vs. Cb
(Single-end input, V^+=3.3V)

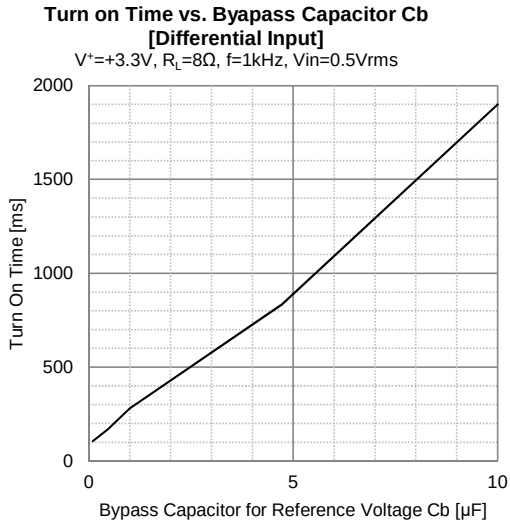


Fig. 6 Turn on time vs. Cb
(Differential input, V^+=3.3V)

5. PSRR vs Cb

PSRR is improved in case that value of bypass capacitor for reference voltage (Cb) increases. But the value of Cb causes pop noise and turn on time (standby to active time) too. It is important to consider when selects the value.

Fig. 7 to 10 shows typical characteristics of PSRR vs the value of Cb.

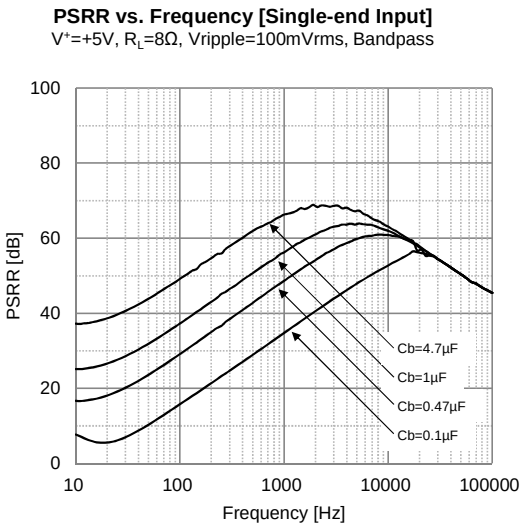


Fig. 7 PSRR vs. Cb
(Single-end input, V^+=5V)

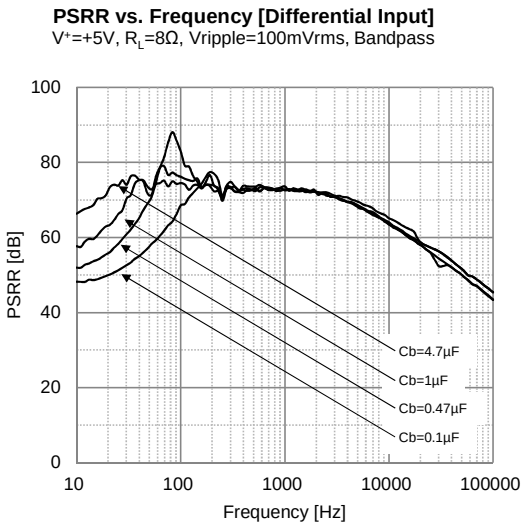


Fig. 8 PSRR vs. Cb
(Differential input, V^+=5V)

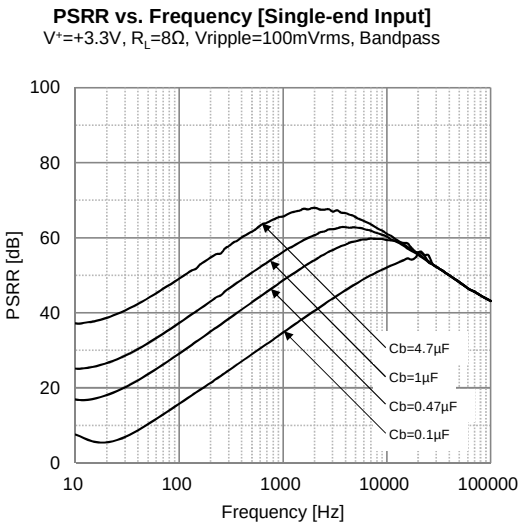


Fig. 9 PSRR vs. Cb
(Single-end input, V^+=3.3V)

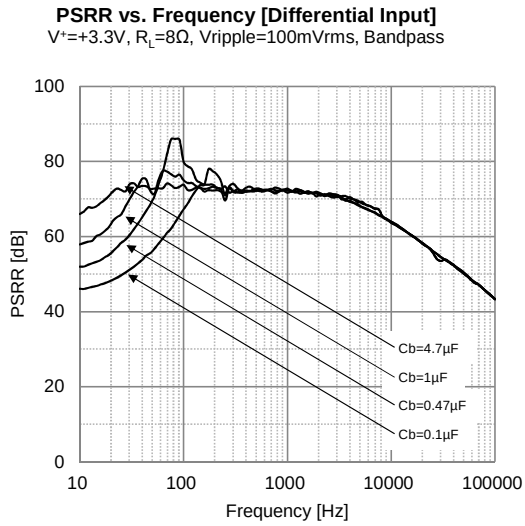


Fig. 10 PSRR vs. Cb
(Differential input, V^+=3.3V)

6. Standby current

The standby current depends on I²C BUS 's pull up voltage (V_{Pullup}). It should turn off the supply voltage in case of problem.

Fig. 11 to 12 shows typical characteristics of Standby current vs. V_{Pullup}.

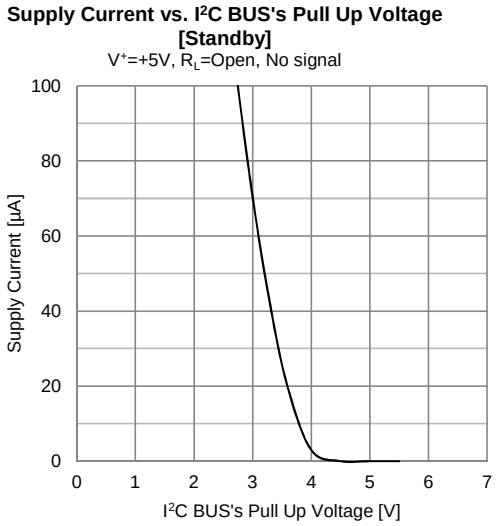


Fig. 11 Standby current vs. V_{Pullup} (V^+=5V)

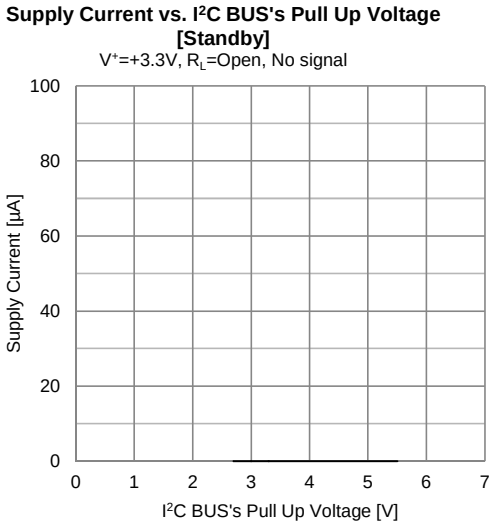


Fig. 12 Standby current vs. V_{Pullup} (V^+=3.3V)

7. Volume

The volume is controlled by I²C BUS and it attenuates Pre-Amp's output signal from 0 to -42dB and Mute. Mute attenuation depends on the value of bypass capacitor for reference voltage (Cb) and it is low in case that the value of Cb decreases. It should use the standby mode in case of problem.

Fig. 13 shows typical characteristics of Mute Level vs the value of Cb.

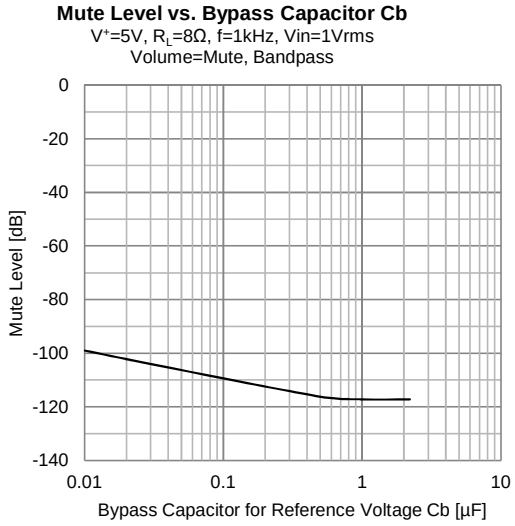


Fig. 13 Mute Level vs. Cb

8. Auxiliary functions

The NJU72065 has the auxiliary functions which suppress breaking itself when the use of an unexpected condition occurs. These auxiliary functions are not guarantee as they operate over absolute maximum ratings. It is essential to design as the auxiliary functions do not operate. Do not design when use the auxiliary functions.

8.1 Current Limit Circuit

The NJU72065 operates the current limit circuit when the current of over absolute maximum ratings flows through the OUTA terminal and the OUTB terminal. So the OUTA terminal and the OUTB terminal become high impedance. It is necessary to turn to standby mode by I^2C bus in case that it releases current limit.

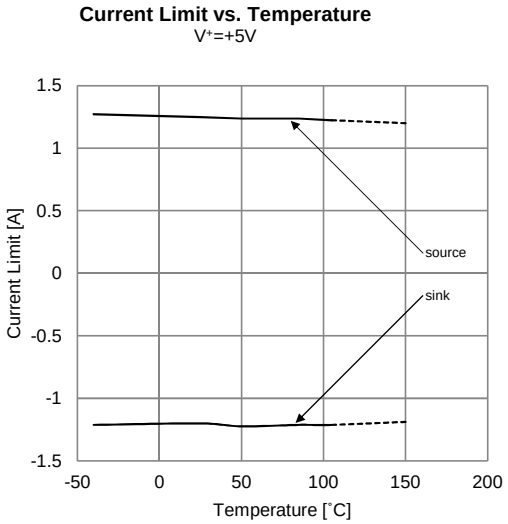


Fig. 14 Current Limit vs. Temperature (V^+=5V)

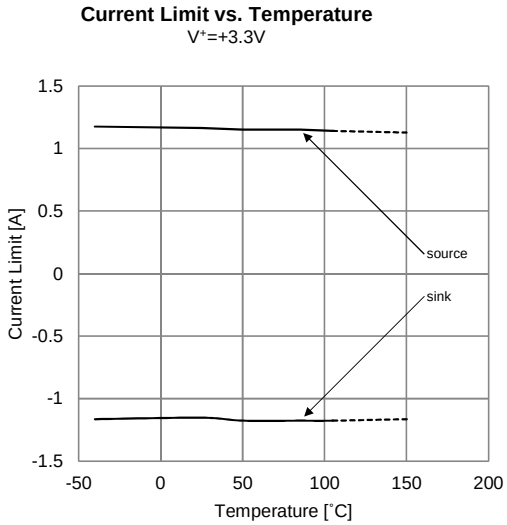


Fig. 15 Current Limit vs. Temperature (V^+=3.3V)

8.2 Thermal shutdown circuit

The NJU72065 operates the thermal shutdown circuit when the junction temperature is abnormally high temperature. So the OUTA terminal and the OUTB terminal become high impedance. The NJU72065's operation returns by itself in case that the junction temperature is normally.

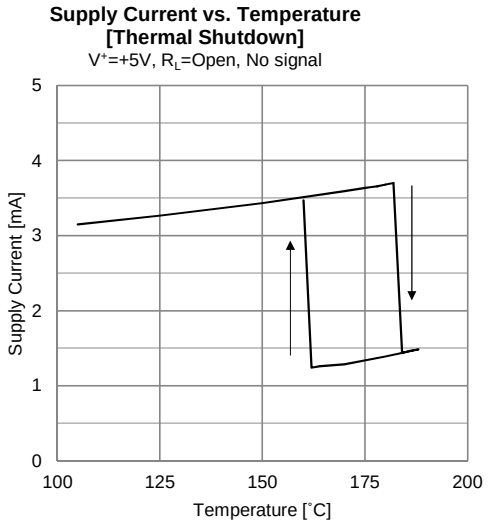


Fig. 16 Thermal Shutdown (V^+=5V)

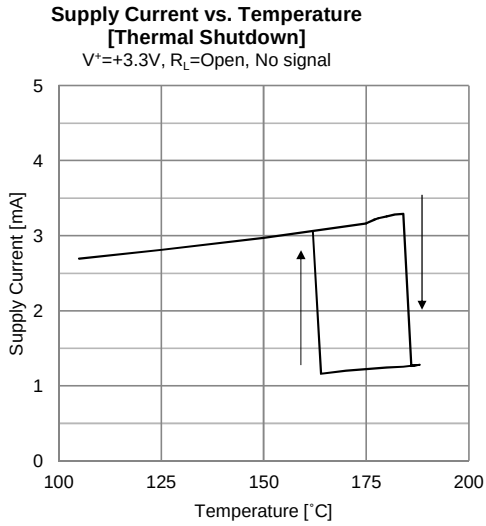


Fig. 17 Thermal Shutdown (V^+=3.3V)

9. Output power

9.1 Output Current and output power

It is important to consider that the NJU72065 define output current in absolute maximum rating. For example, maximum output power (Po_max) is set by the following under the condition that output current ($Io_{(rms)}$[Arms], Io[A]), load resistance (R_L) is 4Ω, Output signal is sine wave

$$P_{O\_\max} < I_{O(rms)}{}^{\wedge 2} \cdot R_L = \left(\frac{I_O}{\sqrt{2}}\right)^2 \cdot R_L = \left(\frac{0.6}{\sqrt{2}}\right)^2 \cdot 4 = 0.72\,[W]$$

9.2 Power dissipation and output power

IC is heated by own operation and it breaks when the junction temperature (Tj) exceeds the permissible value. The permissible value is power dissipation P_D and it is necessary to use no exceeding it.

Fig. 18 shows power dissipation (P_D) vs ambient temperature (Ta). The plots depends on following two points. The first point is P_D at Ta=25˚C which is power dissipation of the absolute maximum ratings. Power dissipation on Ta<25˚C is same value. The second point is 0W which means that the IC cannot permit heating. This point is gotten by maximum junction temperature Tjmax which is maximum storage temperature of this IC. Fig. 18 is drawn by connecting those points and the definition which P_D lower than 25˚C is constant. P_D on Ta≥25˚C is set by the following.

$$P_D = \frac{Tj\max - Ta}{\theta ja}\,[W] \quad (Ta \geq 25°C)$$

Θja is thermal resistance between Tj and Ta and it depends on package material (resin, frame and so on).

Power dissipation (P) of own operating is gotten by the following.

$$\begin{aligned} Power\ Dissipation\ P &= (Supply\ Voltage\ V^+) \cdot (Supply\ Current\ \ for\ V^+\ terminal\ I_{ALL}) \\ &\quad - (Output\ Power\ P_O) \\ &= (Supply\ Voltage\ V^+) \cdot (Supply\ Current\ \ for\ the\ NJU72065\ I_{DD} \\ &\quad + Supply\ Current\ \ for\ Load\ Resistance\ I_{R_L}) - (Output\ Power\ P_O) \end{aligned}$$

The NJU72065 should be operated under the condition that this power dissipation (P) is lower than power dissipation (P_D). It is recommended to consider under the condition and have an enough margin for stabilized operation.

In the designing, power dissipation (P) should be verified in the using but temporary value is read by Power Dissipation vs Output Power on the datasheet's typical characteristics. Fig.19 shows typical characteristics under the conditions that Ta=25˚C, V^+=5V, Gv=+6dB and R_L=8Ω BTL. The following are examples.

Ex. 1 How to get maximum ambient temperature Ta
in the case of request which is maximum output power Po.

The NJU72065RB2 is maximum junction temperature Tjmax=150˚C and MSOP10 (TVSP10) package's power dissipation P_D=700mW (4layer). Thermal resistance (θja) is gotten by the equation of power dissipation (P_D).

$$\theta ja = \frac{Tj\max - Ta}{P_D} = \frac{150 - 25}{0.7} = 178.6\,[°C/W]$$

Maximum ambient temperature Ta is set by the following under the conditions that V^+=5V, R_L=8Ω BTL and maximum output power Po=1.2W because maximum power dissipation (P) is approximately 0.65W by Fig. 19.

$$Ta = Tj\max - P_D \cdot \theta ja = 150 - 0.65 \cdot 178.6 = 33.9\,[°C]$$

Ex. 2 How to get maximum output power Po
in the case of request which is ambient temperature Ta.

Power dissipation (P_D) is gotten by the following under the conditions that Ta=60˚C and θja=178.6˚C/W which is set by Ex. 1.

$$P_D = \frac{Tj\max - Ta}{\theta ja} = \frac{150 - 60}{178.6} = 0.5\,[W]$$

Maximum output power (Po) is gotten approximately 0.2W or under by Fig. 19 under the conditions that V^+=5V, R_L=8Ω BTL, P_D=0.5W and Ta=60˚C.

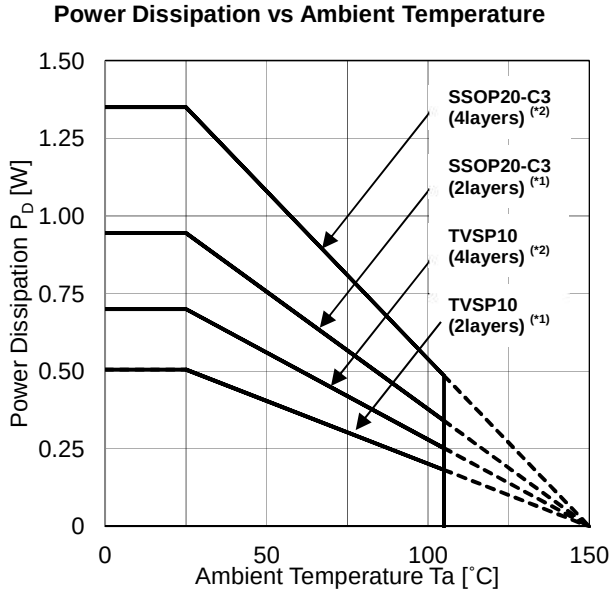


Fig. 18 Power Dissipation vs. Ambient Temperature

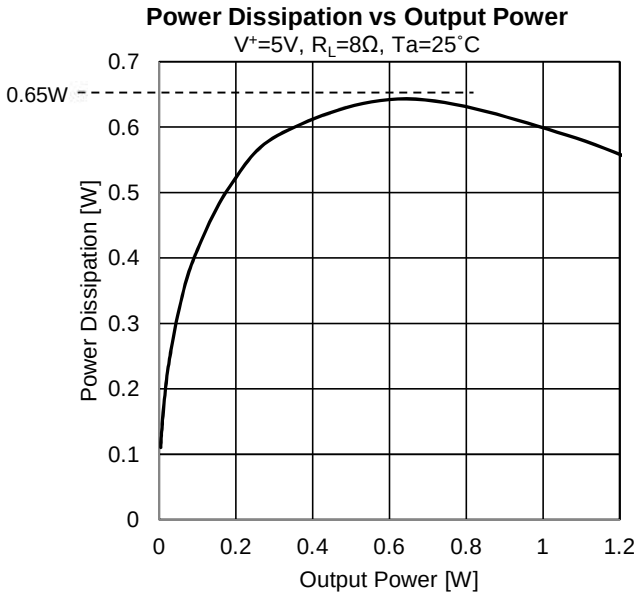


Fig. 19 Power Dissipation vs. Output Power

*1) EIA/JEDEC STANDARD Test board (76.2x114.3x1.6mm, 2layer, FR-4) mounting
*2) EIA/JEDEC STANDARD Test board (76.2x114.3x1.6mm, 4layer, FR-4) mounting

10. PCB layout

It is necessary to design a PCB appropriately in order to demonstrate the performance of IC. Power line, GND line and signal output line should be drawn wiring as low wiring resistance as possible. And all of the GND should be connect directly to the single point of power source bypass capacitor's GND

There is possibility that PSRR is low in case of 4 layer and over when the power plane is piled the wiring layer. It is recommended that the GND plane is inserted between the wiring layer and power plane.

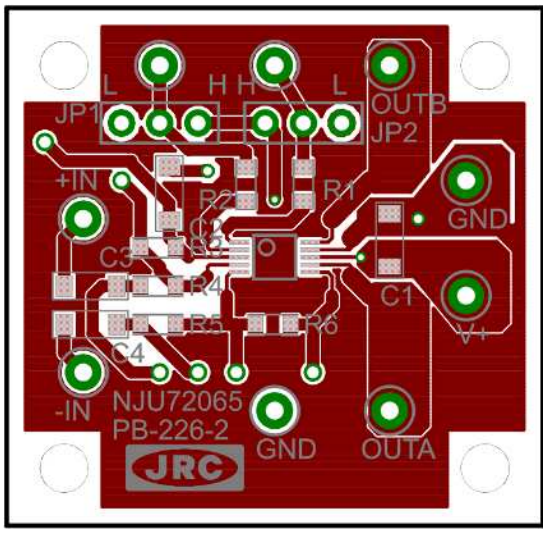


Fig. 20 Layout example: Top layer

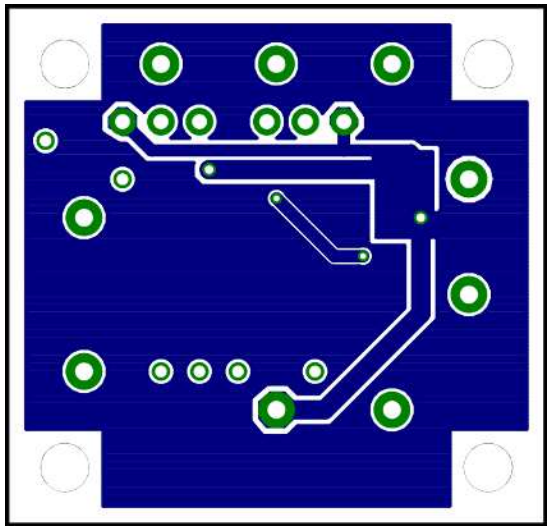
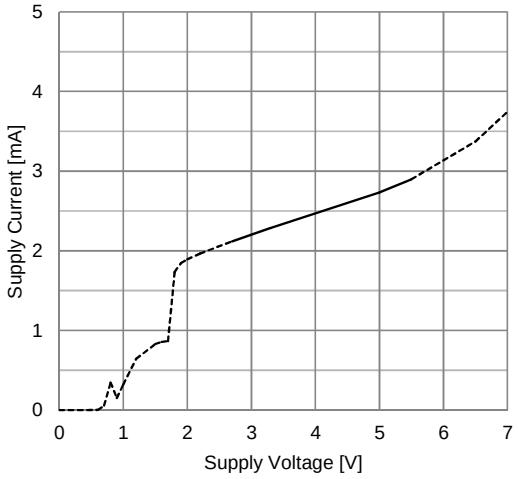


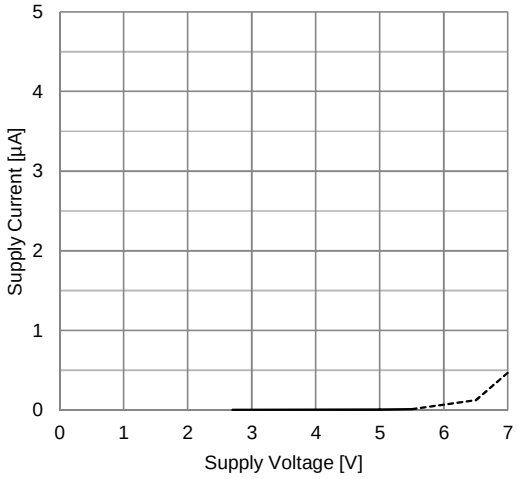
Fig. 21 Layout example: Bottom layer

■ TYPICAL CHARACTERISTICS

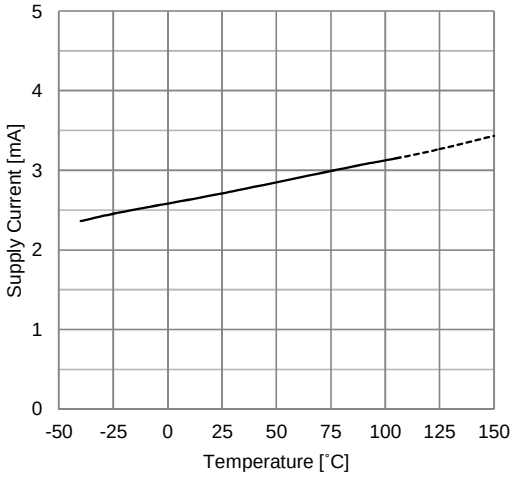
Supply Current vs. Supply Voltage
R_L=Open, No signal



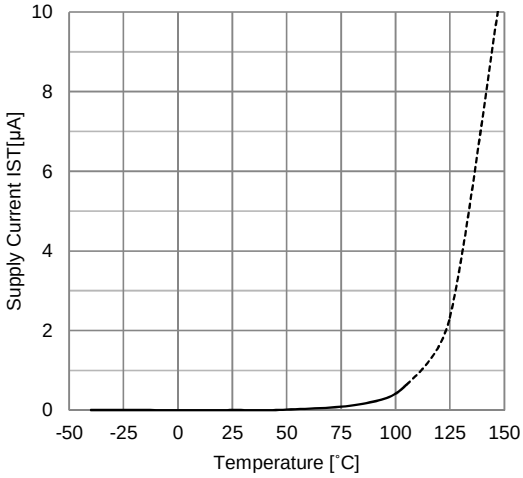
Supply Current vs. Supply Voltage [Standby]
R_L=Open, V_{Pullup}=V^+, No signal



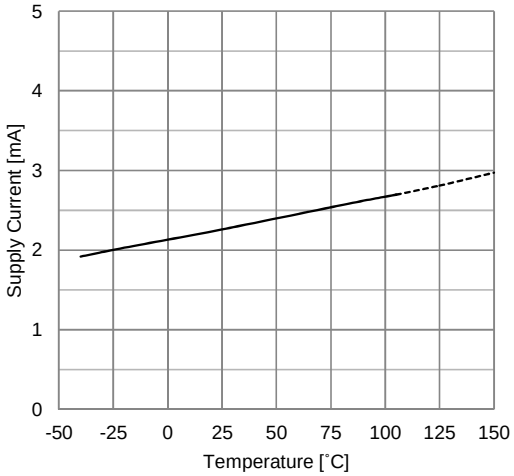
Supply Current vs. Temperature
V^+=+5V, R_L=Open, No signal



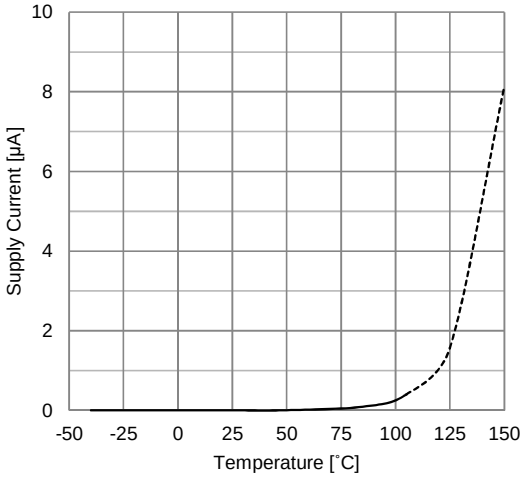
Supply Current vs. Temperature [Standby]
V^+=+5V, R_L=Open, V_{Pullup}=+5V, No signal



Supply Current vs. Temperature
V^+=+3.3V, R_L=Open, No signal

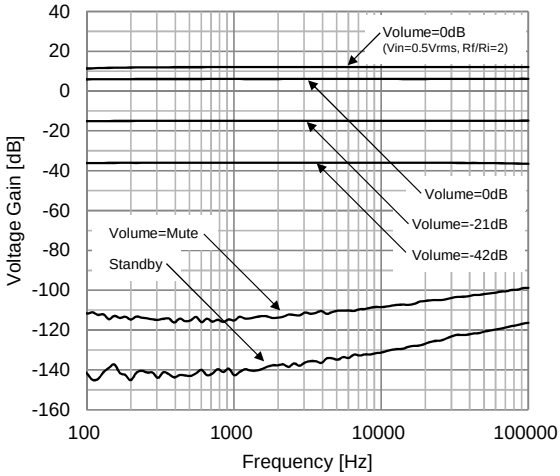


Supply Current vs. Temperature [Standby]
V^+=+3.3V, R_L=Open, V_{Pullup}=+3.3V, No signal

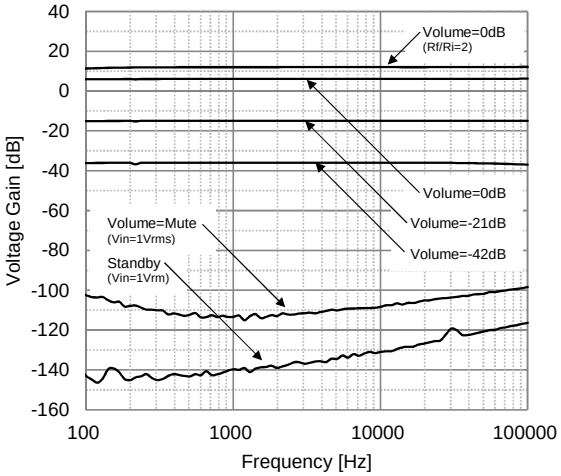


■ TYPICAL CHARACTERISTICS

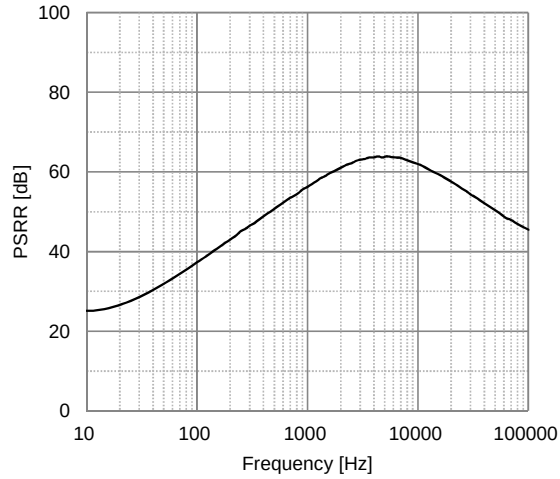
Voltage Gain vs. Frequency
V^+=5V, R_L=8Ω, Vin=1Vrms, Rf/Ri=1, Bandpass



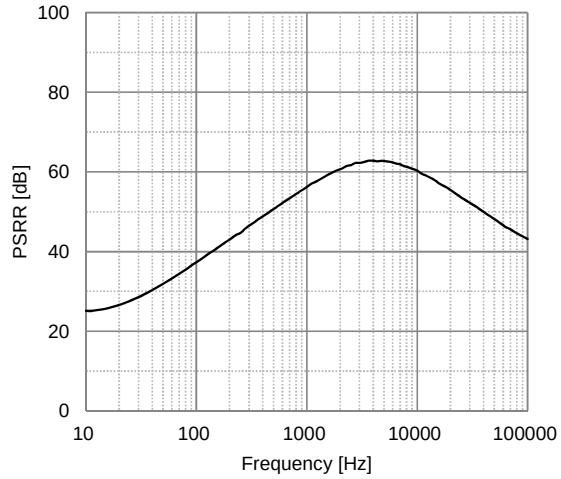
Voltage Gain vs. Frequency
V^+=+3.3V, R_L=8Ω, Vin=0.5Vrms, Rf/Ri=1, Bandpass



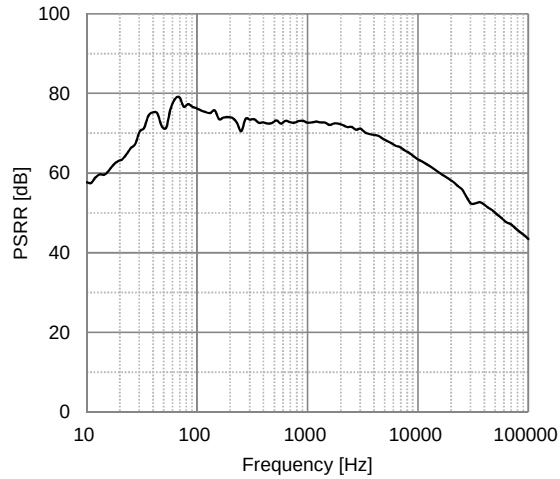
PSRR vs. Frequency [Single-end Input]
V^+=+5V, R_L=8Ω, Vripple=100mVrms, Bandpass



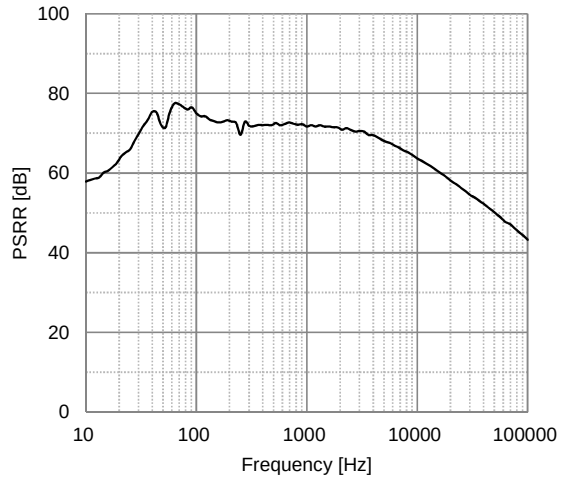
PSRR vs. Frequency [Single-end Input]
V^+=+3.3V, R_L=8Ω, Vripple=100mVrms, Bandpass



PSRR vs. Frequency [Differential Input]
V^+=+5V, R_L=8Ω, Vripple=100mVrms, Bandpass

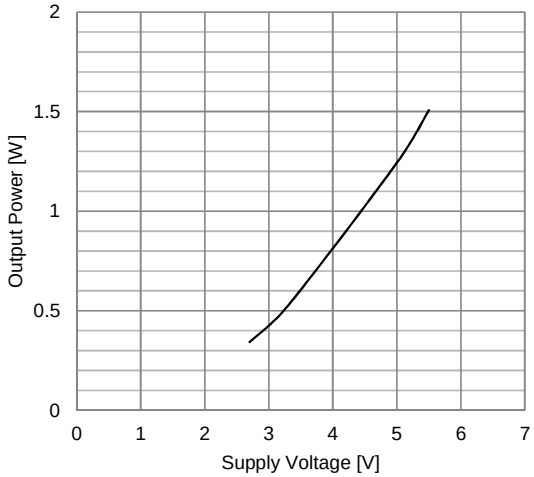


PSRR vs. Frequency [Differential Input]
V^+=+3.3V, R_L=8Ω, Vripple=100mVrms, Bandpass

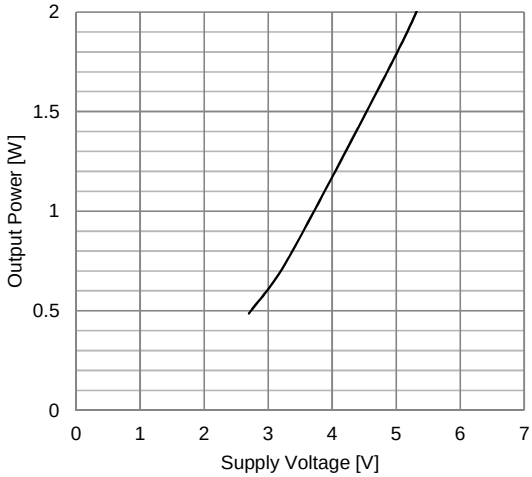


■ TYPICAL CHARACTERISTICS

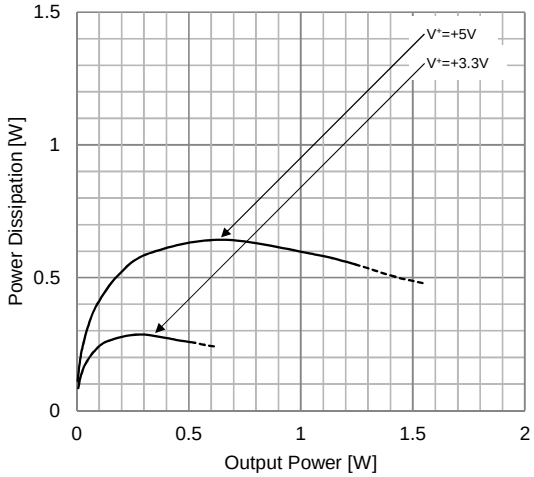
Output Power vs. Supply Voltage
R_L=8Ω, THD=1%



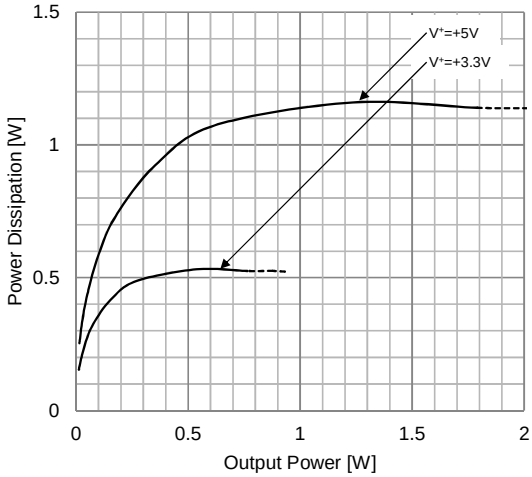
Output Power vs. Supply Voltage
R_L=4Ω, THD=1%



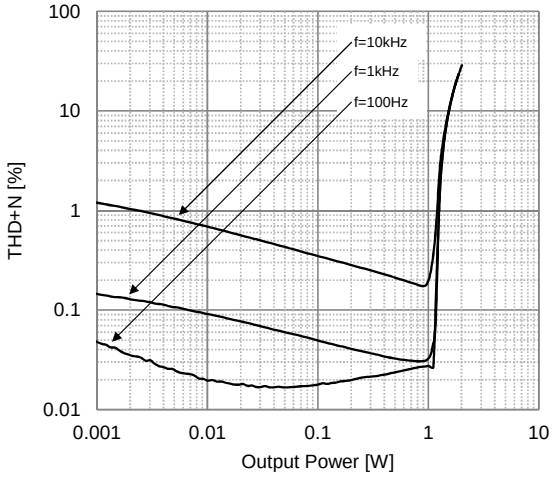
Power Dissipation vs. Output Power
R_L=8Ω, THD=1%



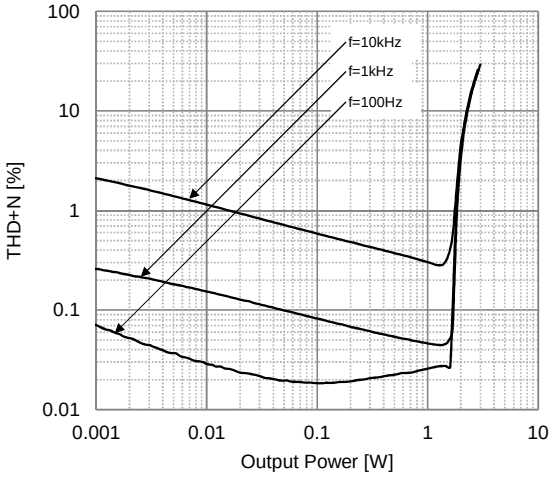
Power Dissipation vs. Output Power
R_L=4Ω, THD=1%



THD+N vs. Output Power [Single-end Input]
V^+=+5V, R_L=8Ω
BW: 22-22kHz(f=100Hz, 1kHz), 22-80kHz(f=10kHz)

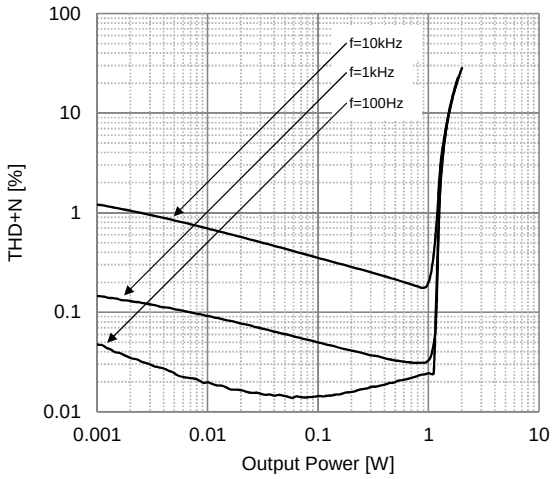


THD+N vs. Output Power [Single-end Input]
V+=+5V, R_L=4Ω
BW: 22-22kHz(f=100Hz, 1kHz), 22-80kHz(f=10kHz)

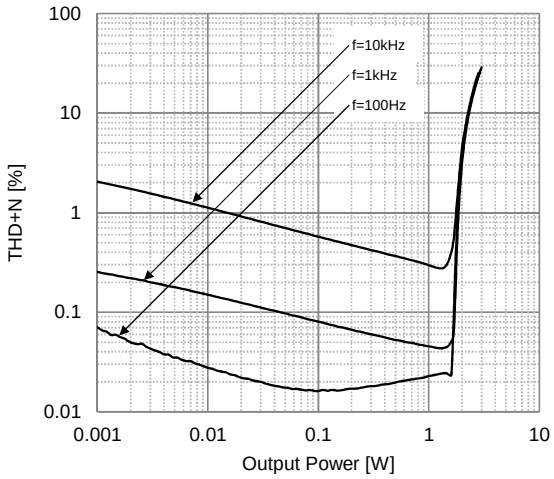


■ TYPICAL CHARACTERISTICS

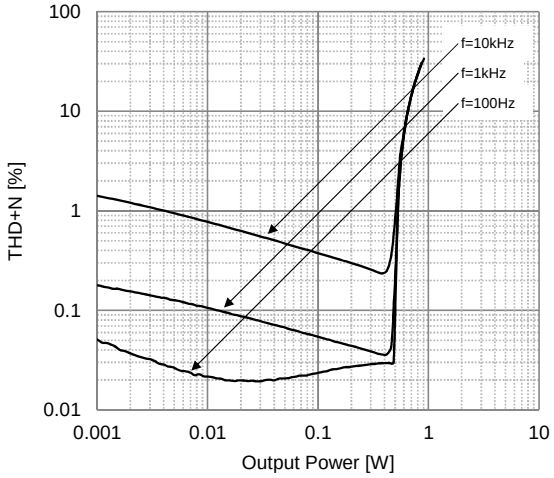
THD+N vs. Output Power [Differential Input]
V^+=+5V, R_L=8Ω
BW: 22-22kHz(f=100Hz, 1kHz), 22-80kHz(f=10kHz)



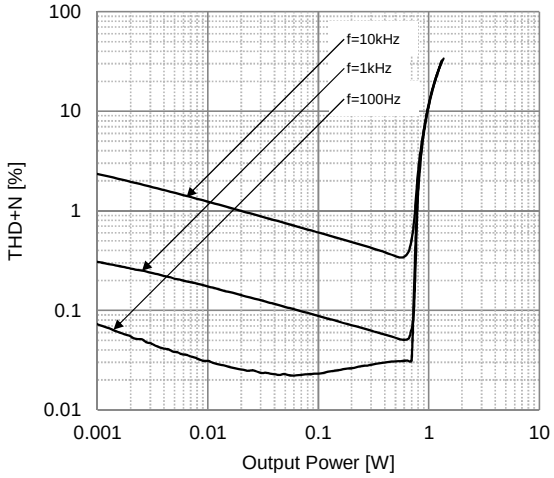
THD+N vs. Output Power [Differential Input]
V^+=+5V, R_L=4Ω
BW: 22-22kHz(f=100Hz, 1kHz), 22-80kHz(f=10kHz)



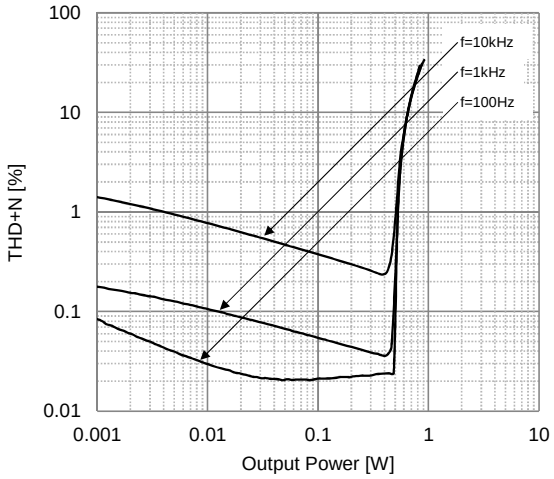
THD+N vs. Output Power [Single-end Input]
V^+=+3.3V, R_L=8Ω
BW: 22-22kHz(f=100Hz, 1kHz), 22-80kHz(f=10kHz)



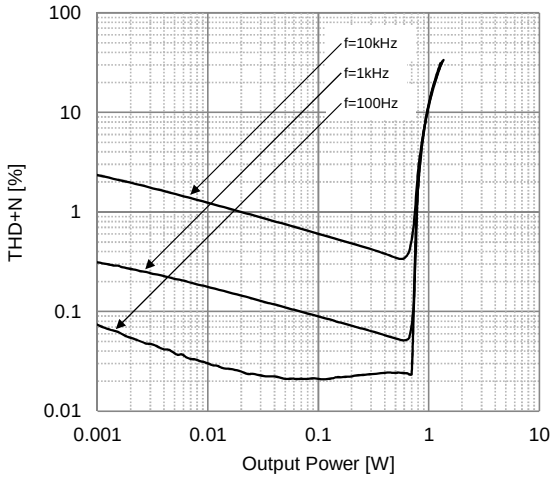
THD+N vs. Output Power [Single-end Input]
V^+=+3.3V, R_L=4Ω
BW: 22-22kHz(f=100Hz, 1kHz), 22-80kHz(f=10kHz)



THD+N vs. Output Power [Differential Input]
V^+=+3.3V, R_L=8Ω
BW: 22-22kHz(f=100Hz, 1kHz), 22-80kHz(f=10kHz)



THD+N vs. Output Power [Differential Input]
V^+=+3.3V, R_L=4Ω
BW: 22-22kHz(f=100Hz, 1kHz), 22-80kHz(f=10kHz)



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