

Initial Release

# Low Charge Injection, 8-Channel, High Voltage, Enhanced Analog Switch with Bleed Resistors

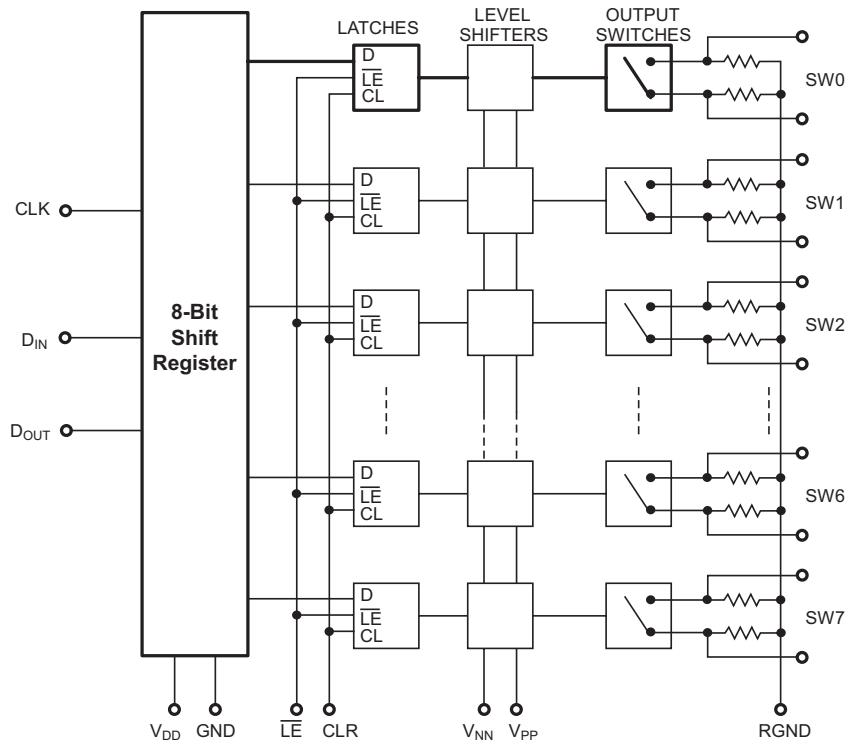
## Features

- HVCMOS technology for high performance
- Integrated bleed resistors on the outputs
- 8 Channels of high voltage analog switch
- 3.3V or 5V CMOS input logic level
- 20MHz data shift clock frequency
- Very low quiescent power dissipation- $10\mu\text{A}$
- Low parasitic capacitance
- DC to 10MHz analog signal frequency
- -60dB typical off-isolation at 5MHz
- CMOS logic circuitry for low power
- Excellent noise immunity
- Cascadable serial data register with latches
- Flexible operating supply voltages

## Applications

- Medical ultrasound imaging
- NDT metal flaw detection
- Piezoelectric transducer drivers
- Inkjet printer heads
- Optical MEMS modules

## Block Diagram



## General Description

The Supertex HV2301 is a low charge injection, 8-channel, high voltage analog switch integrated circuit (IC) with bleed resistors. The device can be used in applications requiring high voltage switching, controlled by low voltage control signals, such as medical ultrasound imaging, piezoelectric transducer driver, and printers. The built-in bleed resistors eliminate voltage built up on capacitive loads such as piezoelectric transducers. The HV2301 is an enhanced version of the HV232.

Input data is shifted into an 8-bit shift register that can then be retained in an 8-bit latch. To reduce any possible clock feed-through noise, the latch enable bar should be left high until all bits are clocked in. Data is clocked in during the rising edge of the clock. Using HVCMOS technology, this device combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

The device is suitable for various combinations of high voltage supplies, e.g.,  $V_{PP}/V_{NN}$ : +40V/-160V, +100V/-100V, and +160V/-40V.

## Ordering Information

Device	Package Options		
	48-Lead TQFP	28-Lead PLCC	32-Lead BCC
HV2301	HV2301FG-G	HV2301PJ-G	HV2301B1-G

-G indicates package is RoHS compliant ('Green')



## Absolute Maximum Ratings

Parameter	Value
$V_{DD}$ logic supply	-0.5V to +7V
$V_{PP}-V_{NN}$ differential supply	220V
$V_{PP}$ positive supply	-0.5V to $V_{NN}+200V$
$V_{NN}$ negative supply	+0.5V to -200V
Logic input voltage	-0.5V to $V_{DD}+0.3V$
Analog signal range	$V_{NN}$ to $V_{PP}$
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to 150°C
Power dissipation:	
48-Lead TQFP	1.0W
28-Lead PLCC	1.2W
32-Lead BCC	1.0W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

## Operating Conditions

Symbol	Parameter	Value
$V_{DD}$	Logic power supply voltage	3.0V to 5.5V
$V_{PP}$	positive high voltage supply	40V to $V_{NN}+200V$
$V_{NN}$	negative high voltage supply	-40V to -160V
$V_{IH}$	High level input voltage	0.9V to $V_{DD}$
$V_{IL}$	Low-level input voltage	0V to 0.1V
$V_{SIG}$	Analog signal voltage peak-to-peak	$V_{NN}+10V$ to $V_{PP}-10V$
$T_A$	Operating free air temperature	0°C to 70°C

Notes:

1. Power up/down sequence is arbitrary except GND must be powered up first and powered down last.
2.  $V_{SIG}$  must be  $V_{NN} \leq V_{SIG} \leq V_{PP}$  or floating during power up/down transition.
3. Rise and fall times of power supplies  $V_{DD}$ ,  $V_{PP}$  and  $V_{NN}$  should not be less than 1.0msec.

## DC Electrical Characteristics

(Over operating conditions unless otherwise specified)

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions	
		Min	Max	Min	Typ	Max	Min	Max			
$R_{ONS}$	Small signal switch on-resistance	-	30	-	26	38	-	48	$\Omega$	$I_{SIG} = 5\text{mA}$	$V_{PP} = +40\text{V}$
		-	25	-	22	27	-	32		$I_{SIG} = 200\text{mA}$	$V_{NN} = -160\text{V}$
		-	25	-	22	27	-	30		$I_{SIG} = 5\text{mA}$	$V_{PP} = +100\text{V}$
		-	18	-	18	24	-	27		$I_{SIG} = 200\text{mA}$	$V_{NN} = -100\text{V}$
		-	23	-	20	25	-	30		$I_{SIG} = 5\text{mA}$	$V_{PP} = +160\text{V}$
		-	22	-	16	25	-	27		$I_{SIG} = 200\text{mA}$	$V_{NN} = -40\text{V}$
$\Delta R_{ONS}$	Small signal switch on-resistance matching	-	20	-	5.0	20	-	20	%	$I_{SIG} = 5\text{mA}, V_{PP} = +100\text{V}, V_{NN} = -100\text{V}$	
$R_{ONL}$	Large signal switch on-resistance	-	-	-	15	-	-	-	$\Omega$	$V_{SIG} = V_{PP} - 10\text{V}, I_{SIG} = 1\text{A}$	
$R_{INT}$	Value of output bleed resistance	-	-	20	35	50	-	-	$\text{k}\Omega$	Output switch to RGND $I_{RINT} = 0.5\text{mA}$	
$I_{SOL}$	Switch off leakage per switch	-	5.0	-	1.0	10	-	15	$\mu\text{A}$	$V_{SIG} = V_{PP} - 10\text{V}, V_{NN} + 10\text{V}$	
$V_{OS}$	DC offset switch off	-	300	-	100	300	-	300	mV	No load	
	DC offset switch on	-	500	-	100	500	-	500	mV		
$I_{PPQ}$	Quiescent $V_{PP}$ supply current	-	-	-	10	50	-	-	$\mu\text{A}$	All switches off	
$I_{NNQ}$	Quiescent $V_{NN}$ supply current	-	-	-	-10	-50	-	-	$\mu\text{A}$	All switches off	
$I_{PPQ}$	Quiescent $V_{PP}$ supply current	-	-	-	10	50	-	-	$\mu\text{A}$	All switches on, $I_{SW} = 5\text{mA}$	
$I_{NNQ}$	Quiescent $V_{NN}$ supply current	-	-	-	-10	-50	-	-	$\mu\text{A}$	All switches on, $I_{SW} = 5\text{mA}$	
$I_{SW}$	Switch output peak current	-	3.0	-	3.0	2.0	-	2.0	A	$V_{SIG}$ duty cycle < 0.1%	
$f_{SW}$	Output switching frequency	-	-	-	-	50	-	-	kHz	Duty cycle = 50%	
$I_{PP}$	Average $V_{PP}$ supply current	-	4.0	-	-	5.0	-	5.5	mA	$V_{PP} = +40\text{V}$	$V_{NN} = -160\text{V}$
		-	3.5	-	-	3.5	-	3.5		$V_{PP} = +100\text{V}$	$V_{NN} = -100\text{V}$
		-	3.5	-	-	3.5	-	4.0		$V_{PP} = +160\text{V}$	$V_{NN} = -40\text{V}$
$I_{NN}$	Average $V_{NN}$ supply current	-	4.5	-	-	5.0	-	5.5	mA	$V_{PP} = +40\text{V}$	$V_{NN} = -160\text{V}$
		-	3.5	-	-	3.5	-	3.5		$V_{PP} = +100\text{V}$	$V_{NN} = -100\text{V}$
		-	3.5	-	-	3.5	-	4.0		$V_{PP} = +160\text{V}$	$V_{NN} = -40\text{V}$
$I_{DD}$	Average $V_{DD}$ supply current	-	4.0	-	-	4.0	-	4.0	mA	$f_{CLK} = 5\text{MHz}, V_{DD} = 5.0\text{V}$	
$I_{DDQ}$	Quiescent $V_{DD}$ supply current	-	10	-	-	10	-	10	$\mu\text{A}$	All logic inputs are static	
$I_{SOR}$	Data out source current	0.45	-	0.45	0.70	-	0.40	-	mA	$V_{OUT} = V_{DD} - 0.7\text{V}$	
$I_{SINK}$	Data out sink current	0.45	-	0.45	0.70	-	0.40	-	mA	$V_{OUT} = 0.7\text{V}$	
$C_{IN}$	Logic input capacitance	-	10	-	-	10	-	10	pF	---	

## AC Electrical Characteristics

(Over recommended operating conditions:  $V_{DD} = 5.0V$ ,  $t_R = t_F \leq 5ns$ , 50% duty cycle,  $C_{LOAD} = 20pF$  unless otherwise specified)

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
$t_{SD}$	Set up time before $\overline{LE}$ rises	25	-	25	-	-	25	-	ns	---
$t_{WLE}$	Time width of $\overline{LE}$	56	-	-	56	-	56	-	ns	$V_{DD} = 3.0V$
		12	-	-	12	-	12	-		$V_{DD} = 5.0V$
$t_{DO}$	Clock delay time to data out	-	120	-	95	140	-	167	ns	$V_{DD} = 3.0V$
		-	58	-	40	69	-	85		$V_{DD} = 5.0V$
$t_{WCL}$	Time width of CL	55	-	55	30	-	55	-	ns	---
$t_{SU}$	Set up time data to clock	39	-	47	30	-	58	-	ns	$V_{DD} = 3.0V$
		16	-	21	10	-	26	-		$V_{DD} = 5.0V$
$t_H$	Hold time data from clock	2	-	2	-	-	2	-	ns	$V_{DD} = 3.0$ or $5.0V$
$f_{CLK}$	Clock frequency	-	TBD	-	-	7.5	-	TBD	MHz	$V_{DD} = 3.0V$
		-	20	-	-	20	-	20		$V_{DD} = 5.0V$
$t_R, t_F$	Clock rise and fall times	-	50	-	-	50	-	50	ns	---
$t_{ON}$	Turn on time	-	5.0	-	-	5.0	-	5.0	μs	$V_{SIG} = V_{PP} - 10V$ , $R_{LOAD} = 10k\Omega$
$t_{OFF}$	Turn off time	-	5.0	-	-	5.0	-	5.0	μs	$V_{SIG} = V_{PP} - 10V$ , $R_{LOAD} = 10k\Omega$
dv/dt	Maximum $V_{SIG}$ slew rate	-	20	-	-	20	-	20	V/ns	$V_{PP} = +40V$ , $V_{NN} = -160V$
		-	20	-	-	20	-	20		$V_{PP} = +100V$ , $V_{NN} = -100V$
		-	20	-	-	20	-	20		$V_{PP} = +160V$ , $V_{NN} = -40V$
$K_O$	Off isolation	-30	-	-30	-33	-	-30	-	dB	$f = 5.0MHz$ , $1k\Omega/15pF$ load
		-58	-	-58	-	-	-58	-		$f = 5.0MHz$ , $50\Omega$ load
$K_{CR}$	Switch crosstalk	-60	-	-60	-70	-	-60	-	dB	$f = 5.0MHz$ , $50\Omega$ load
$I_{ID}$	Output switch isolation diode current	-	300	-	-	300	-	300	mA	300ns pulse width, 2.0% duty cycle
$C_{SG(OFF)}$	Off capacitance SW to GND	5.0	17	5.0	12	17	5.0	17	pF	0V, $f = 1.0MHz$
$C_{SG(ON)}$	On capacitance SW to GND	25	50	25	38	50	25	50	pF	0V, $f = 1.0MHz$
$\pm V_{SPK}$	Output voltage spike	-	-	-	-	150	-	-	mV	$V_{PP} = +40V$ , $V_{NN} = -160V$ , $R_{LOAD} = 50\Omega$
		-	-	-	-	150	-	-		$V_{PP} = +100V$ , $V_{NN} = -100V$ , $R_{LOAD} = 50\Omega$
		-	-	-	-	150	-	-		$V_{PP} = +160V$ , $V_{NN} = -40V$ , $R_{LOAD} = 50\Omega$
		-	-	-	-	150	-	-		$V_{PP} = +40V$ , $V_{NN} = -160V$ , $V_{SIG} = 0V$
		-	-	-	-	150	-	-		$V_{PP} = +100V$ , $V_{NN} = -100V$ , $V_{SIG} = 0V$
		-	-	-	-	150	-	-		$V_{PP} = +160V$ , $V_{NN} = -40V$ , $V_{SIG} = 0V$
QC	Charge injection	-	-	-	820	-	-	-	pC	$V_{PP} = +40V$ , $V_{NN} = -160V$ , $V_{SIG} = 0V$
		-	-	-	600	-	-	-		$V_{PP} = +100V$ , $V_{NN} = -100V$ , $V_{SIG} = 0V$
		-	-	-	350	-	-	-		$V_{PP} = +160V$ , $V_{NN} = -40V$ , $V_{SIG} = 0V$

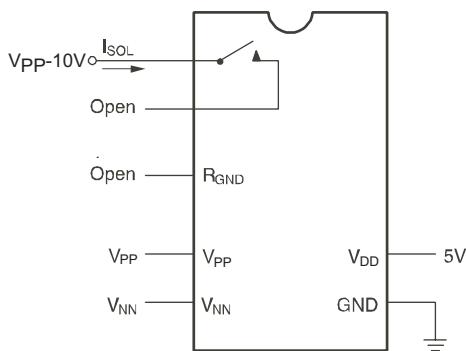
**Truth Table**

D0	D1	D2	D3	D4	D5	D6	D7	LE	CLR	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	Off							
H								L	L	On							
	L							L	L		Off						
	H							L	L		On						
		L						L	L			Off					
		H						L	L			On					
			L					L	L				Off				
			H					L	L				On				
				L				L	L					Off			
				H				L	L					On			
					L			L	L						Off		
					H			L	L						On		
						L		L	L							Off	
						H		L	L							On	
							L	L	L								Off
							H	L	L								On
X	X	X	X	X	X	X	X	H	L								Hold Previous State
X	X	X	X	X	X	X	X	X	H								All Switches Off

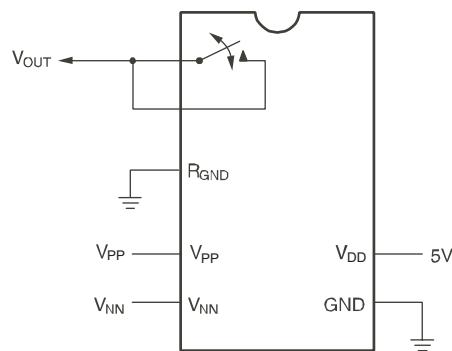
Notes:

1. The eight switches operate independently.
2. Serial data is clocked in on the L to H transition of the CLK.
3. The switches go to a state retaining their present condition at the rising edge of LE. When LE is low the shift register data flow through the latch.
4.  $D_{OUT}$  is high when data in the register 7 is high.
5. Shift register clocking has no effect on the switch states if LE is high.
6. The CLR clear input overrides all other inputs.

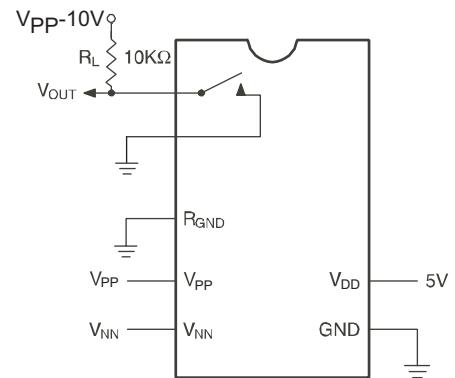
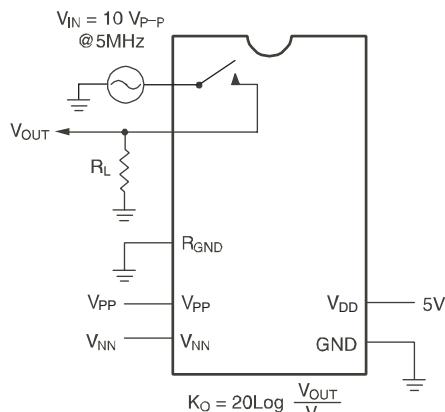
## Test Circuits



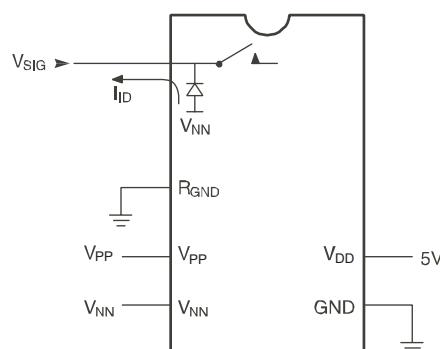
Switch OFF Leakage



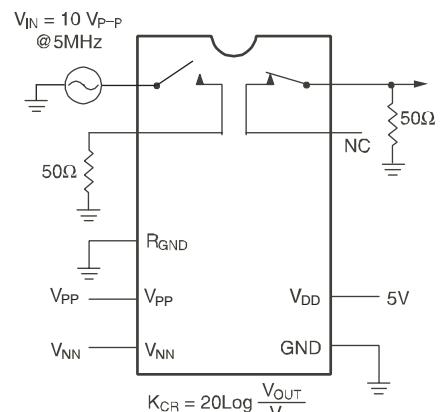
DC Offset ON/OFF

T<sub>ON</sub>/T<sub>OFF</sub> Test Circuit

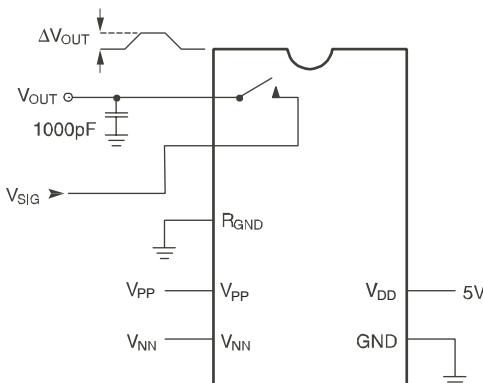
OFF Isolation



Isolation Diode Current

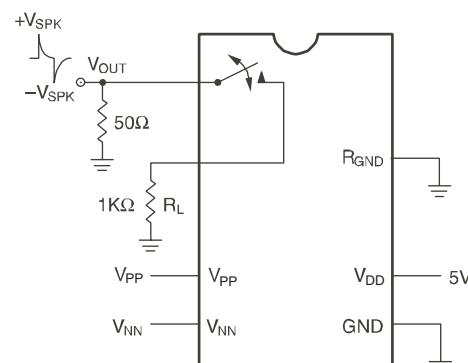


Crosstalk



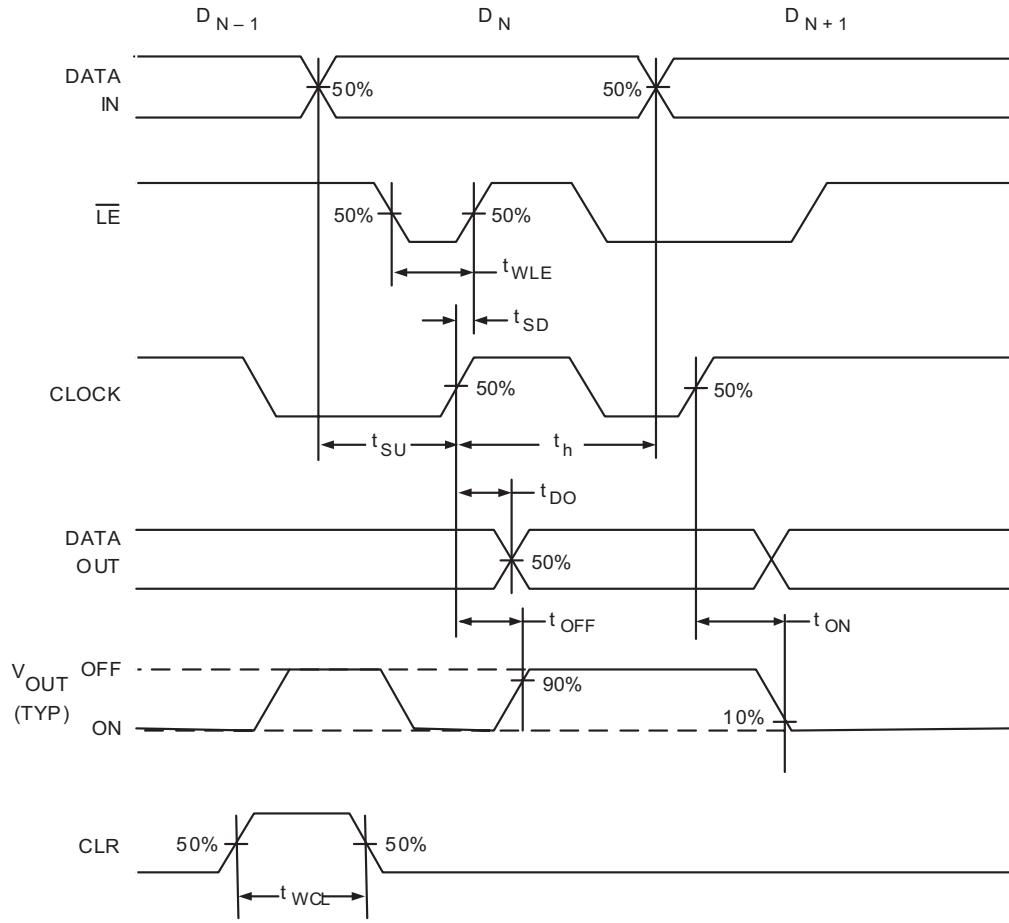
$$Q = 1000\text{pF} \times \Delta V_{OUT}$$

Charge Injection

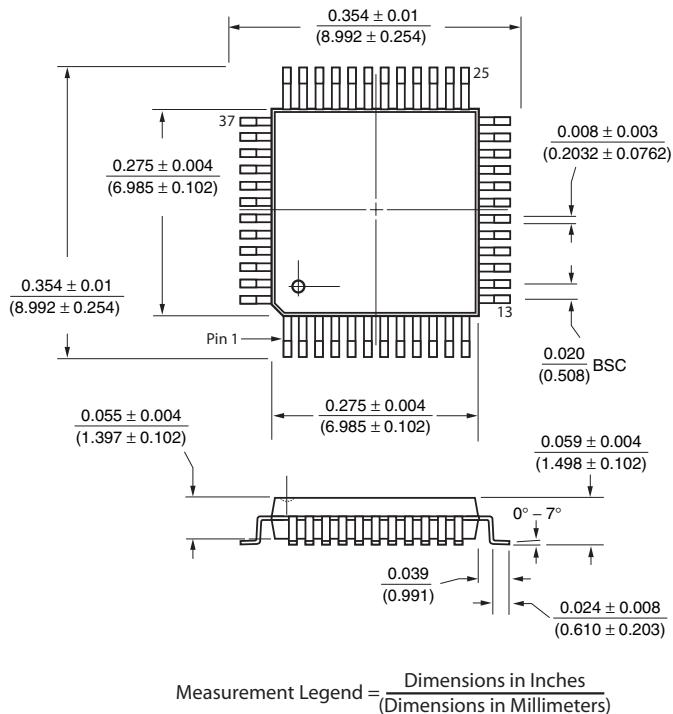


Output Voltage Spike

## Typical Waveforms



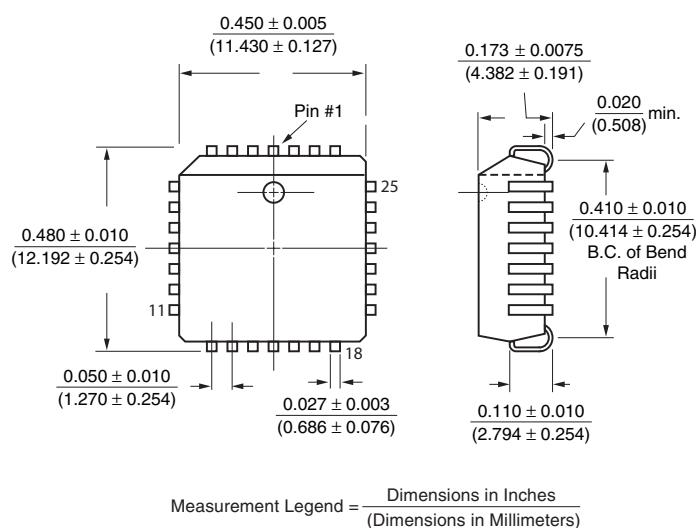
## 48-Lead TQFP (1.4mm) Package Outline (FG)



## Pin Configuration

Pin #	Pin Name	Pin #	Pin Name
1	SW5	25	V <sub>NN</sub>
2	NC	26	NC
3	SW4	27	RGND
4	NC	28	GND
5	SW4	29	V <sub>DD</sub>
6	NC	30	NC
7	NC	31	NC
8	SW3	32	NC
9	NC	33	D <sub>IN</sub>
10	SW3	34	CLK
11	NC	35	LE
12	SW2	36	CLR
13	NC	37	D <sub>OUT</sub>
14	SW2	38	NC
15	NC	39	SW7
16	SW1	40	NC
17	NC	41	SW7
18	SW1	42	NC
19	NC	43	SW6
20	SW0	44	NC
21	NC	45	SW6
22	SW0	46	NC
23	NC	47	SW5
24	V <sub>PP</sub>	48	NC

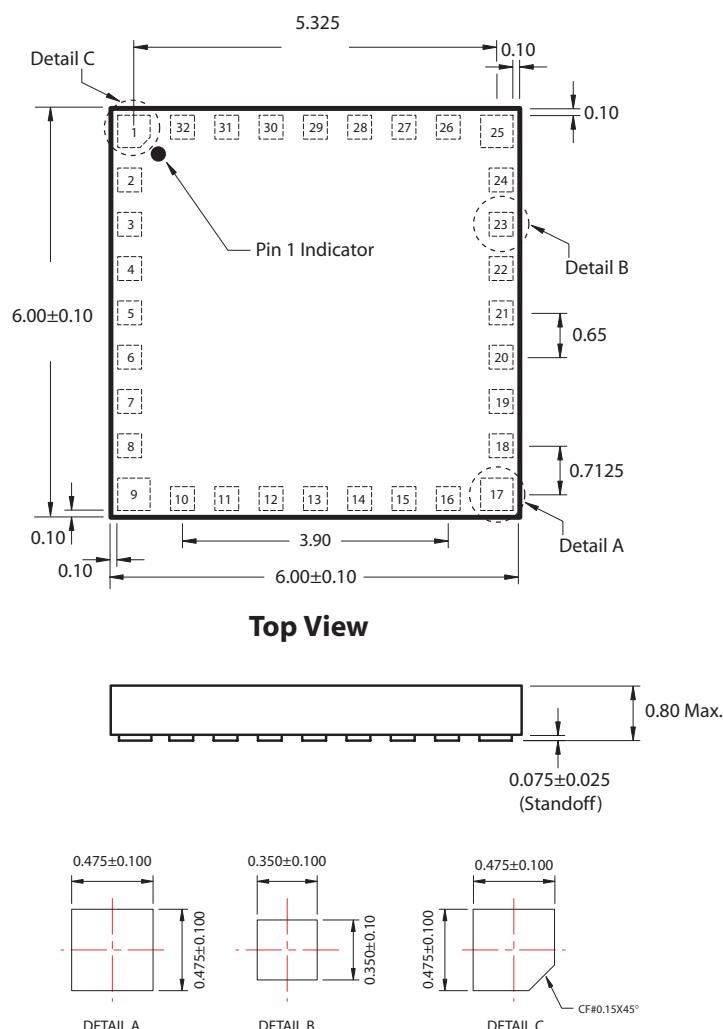
## 28-Lead PLCC Package Outline (PJ)



## Pin Configuration

Pin #	Pin Name	Pin #	Pin Name
1	SW3	15	NC
2	SW3	16	D <sub>IN</sub>
3	SW2	17	CLK
4	SW2	18	LE
5	SW1	19	CLR
6	SW1	20	D <sub>OUT</sub>
7	SW0	21	SW7
8	SW0	22	SW7
9	NC	23	SW6
10	V <sub>PP</sub>	24	SW6
11	RGND	25	SW5
12	V <sub>NN</sub>	26	SW5
13	GND	27	SW4
14	V <sub>DD</sub>	28	SW4

## 32-Lead BCC Package Outline (B1)



## Pin Configuration

Pin #	Pin Name	Pin #	Pin Name
1	NC	17	NC
2	SW5	18	V <sub>NN</sub>
3	SW5	19	RGND
4	SW4	20	GND
5	SW4	21	V <sub>DD</sub>
6	SW3	22	D <sub>IN</sub>
7	SW3	23	CLK
8	SW2	24	LE
9	SW2	25	CLR
10	NC	26	D <sub>OUT</sub>
11	SW1	27	NC
12	SW1	28	SW7
13	SW0	29	SW7
14	SW0	30	SW6
15	NC	31	SW6
16	V <sub>PP</sub>	32	NC

Note: All dimensions are in mm and angles are in degrees

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибуторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ Р В 0015-002 и ЭС РД 009

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