

VOLTAGE DETECTOR with Delay Function

■ GENERAL DESCRIPTION

The NJU7708/09 is a low quiescent current voltage detector with delay function featuring high precision detection voltage.

The detection voltage is internally fixed with an accuracy of 1.0%.

The NJU7708/09 are useful for preventing malfunction of microcomputer or DSP etc. through detect a drop in voltage of battery or power supply.

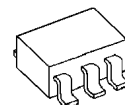
The delay function achieves set wait time when supply voltage is unstable. Moreover, the delay function can make a sequence that other devices in application work and stabilize before microcomputer or DSP works.

Delay time can be set by logical combination from 4-delay time.

NJU7708 is Nch. Open Drain and NJU7709 is a C-MOS output type.

Small packaging makes NJU7708 and NJU7709 suitable for space conscious applications.

■ PACKAGE OUTLINE

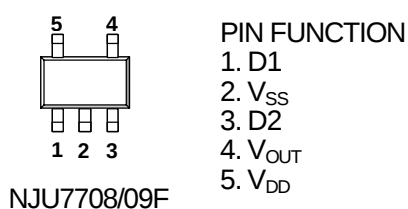


NJU7708/09F

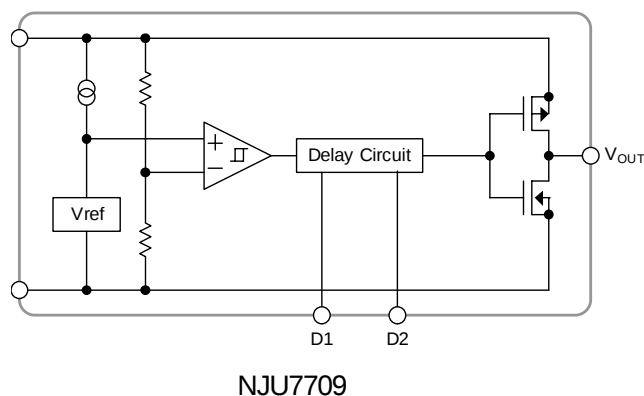
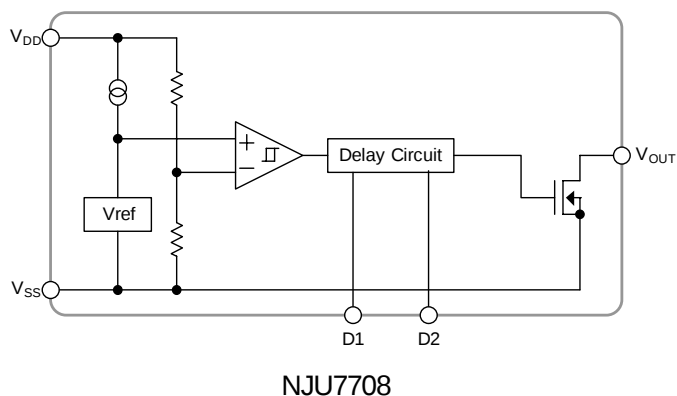
■ FEATURES

- | | |
|------------------------------------|---|
| ● High Precision detection Voltage | $\pm 1.0\%$ |
| ● Low Quiescent Current | $1.3\mu\text{A}$ |
| ● Detection Voltage Range | $1.3 \sim 6.0\text{V}$ (0.1V step) |
| ● Delay Time (Built-in Fixed Type) | 0ms/50ms/100ms/200ms: Logical selectable 4-delay time |
| ● Output Configuration | NJU7708: Nch. Open Drain Type
NJU7709: C-MOS Output Type |
| ● CMOS Technology | |
| ● Package Outline | SOT-23-5 |

■ PIN CONFIGURATION



■ EQUIVALENT CIRCUIT



■ DETECTION VOLTAGERANK LIST

Device Name	V _{DET}
NJU7708/09F15	1.5V
NJU7708/09F27	2.7V
NJU7708/09F42	4.2V
NJU7708/09F06	6.0V

■ LOGICAL TABLE OF DELAY TIME

D1	D2	DELAY
H	H	0ms
H	L	50ms
L	H	100ms
L	L	200ms

■ NJU7708

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Input Voltage	V _{DD}	+10	V
Output Voltage	V _{OUT}	V _{SS} -0.3 ~ +10	V
Output Current	I _{OUT}	50	mA
Power Dissipation	P _D	SOT-23-5 350(*1) 200(*2)	mW
Operating Temperature	Topr	-40 ~ +85	°C
Storage Temperature	Tstg	-40 ~ +125	°C

(*1) : Mounted on glass epoxy board based on EIA/JEDEC. (114.3x76.2x1.6mm: 2Layers)

(*2) : Device itself

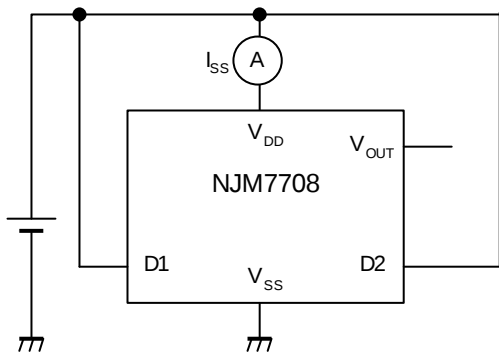
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Detection Voltage	V _{DET}		-1.0%	—	+1.0%	V
Hysteresis Voltage	V _{HYS}		70	90	130	V
Quiescent Current	I _{SS}	V _{DD} =V _{DET} +1V				
		V _{DET} =1.5V ~ 2.5V Version	—	1.0	1.7	μA
		V _{DET} =2.6V ~ 6.0V Version	—	1.3	2.2	μA
Output Current	I _{OUT}	Nch, V _{DS} =0.5V				
		V _{DD} =1.2V	0.75	2.0	—	mA
		V _{DD} =2.4V (≥2.7V Version)	4.5	7.0	—	mA
Output Leak Current	I _{LEAK}	V _{DD} =V _{OUT} =9V	—	—	0.1	μA
Detection Voltage Temperature Coefficient	ΔV _{DET} /ΔTa	Ta=0 ~ +85°C	—	±100	—	ppm/°C
Delay Time	td	V _{DD} =V _{DET} +1V				
		D1=H, D2=H	25	100	300	μs
		D1=H, D2=L	42.5	50	57.5	ms
		D1=L, D2=H	85	100	115	ms
		D1=L, D2=L	170	200	230	ms
Delay Time Change	V _{D1 H} / V _{D2 H}		1.5	—	V _{DD}	V
Terminal Input Voltage	V _{D1 L} / V _{D2 L}		0	—	0.3	V
Operating Voltage(*3)	V _{DD}	R _L =100kΩ	0.7	—	9	V

(*3): The minimum operating voltage(V_{OPL}) indicates the same value of the input voltage(V_{DD}) on condition that V_{OUT} becomes 10% or less of the input voltage(V_{DD}).

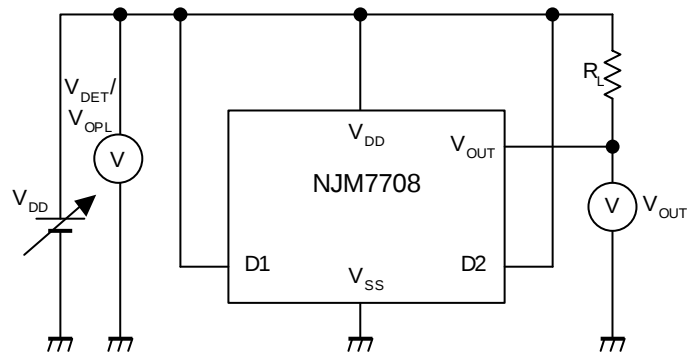
■ TEST CIRCUIT

● Quiescent Current TEST CIRCUIT

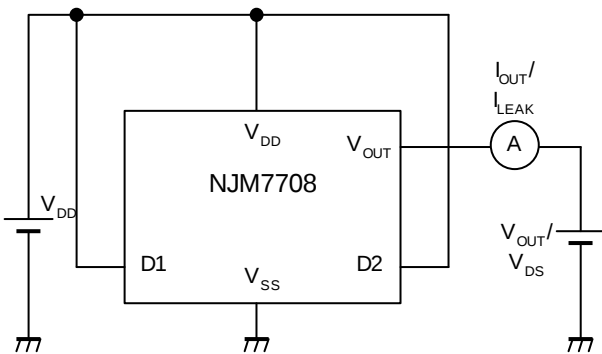


● Detection Voltage

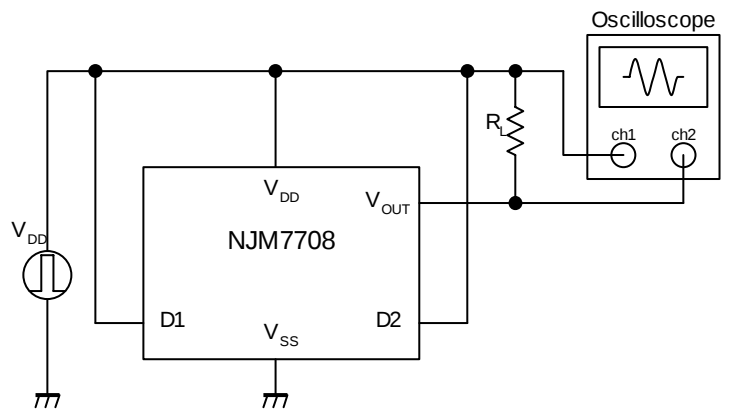
/Minimum Operating Voltage TEST CIRCUIT



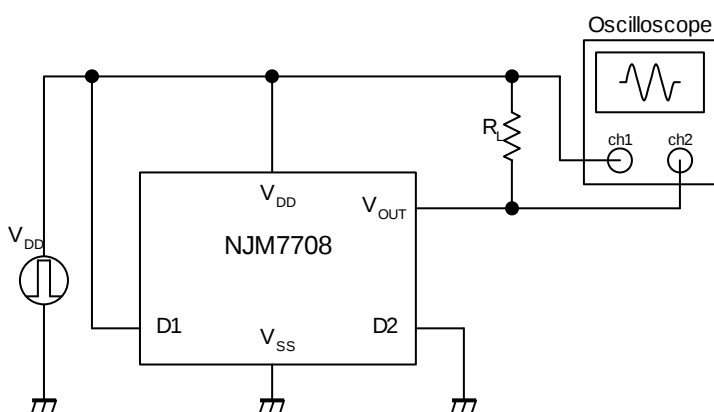
● Leak Current/Output Current TEST CIRCUIT



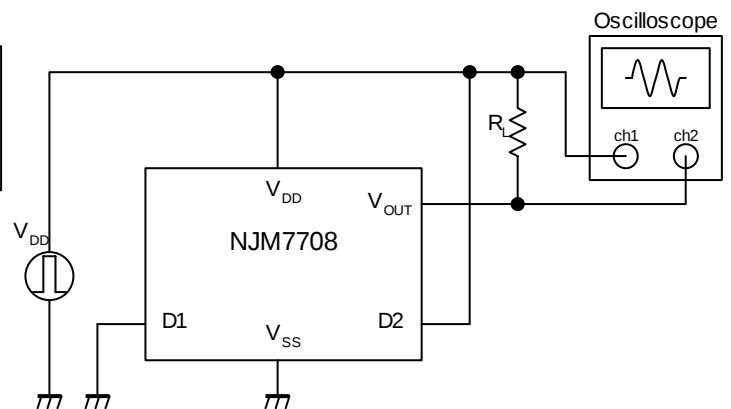
● Delay Time=0mS TEST CIRCUIT



● Delay Time=50mS TEST CIRCUIT

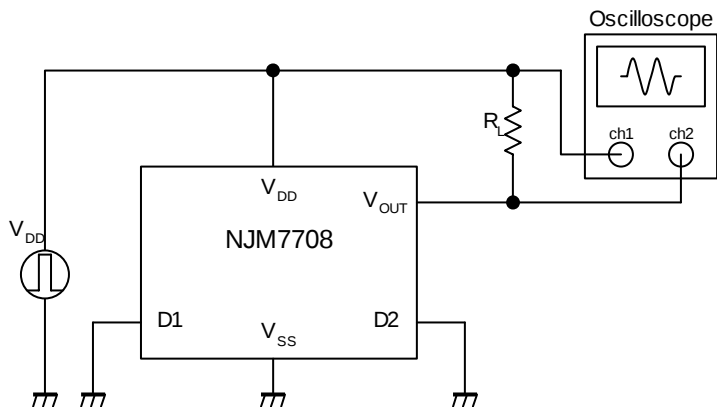


● Delay Time=100mS TEST CIRCUIT



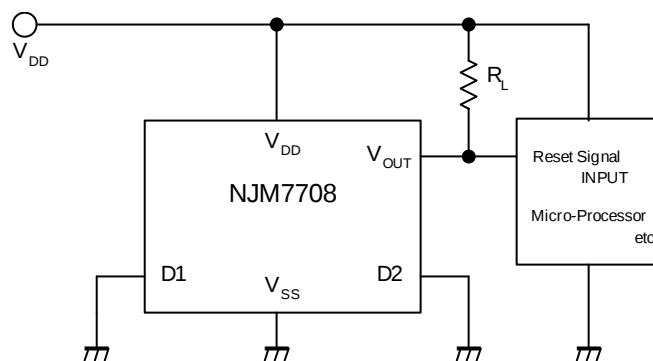
■ TEST CIRCUIT

● Delay Time=200mS TEST CIRCUIT

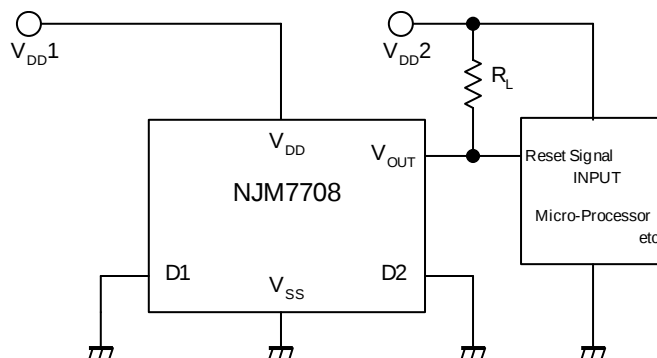


■ TYPICAL APPLICATION

① Power Supply Voltage Supervisory Circuit



② Power Supply Voltage Supervisory Circuit (Another Power Supply to Micro-Processor)



■ NJU7709

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Input Voltage	V_{DD}	+10	V
Output Voltage	V_{OUT}	$V_{SS}-0.3 \sim V_{DD}+0.3$	V
Output Current	I_{OUT}	50	mA
Power Dissipation	P_D	SOT-23-5 350(*4) 200(*5)	mW
Operating Temperature	Topr	-40 ~ +85	°C
Storage Temperature	Tstg	-40 ~ +125	°C

(*4) : Mounted on glass epoxy board based on EIA/JEDEC. (114.3x76.2x1.6mm: 2Layers)

(*5) : Device itself

■ ELECTRICAL CHARACTERISTICS

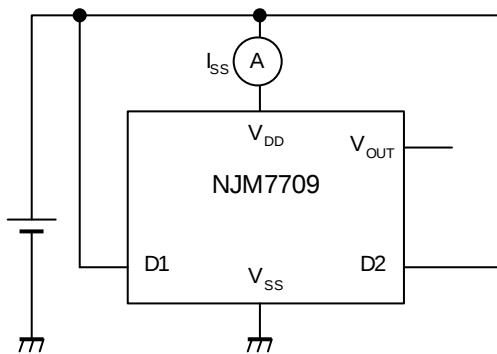
(Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Detection Voltage	V_{DET}		-1.0%	—	+1.0%	V
Hysteresis Voltage	V_{HYS}		70	90	130	V
Quiescent Current	I_{SS}	$V_{DD}=V_{DET}+1V$ $V_{DET}=1.5V \sim 1.9V$ Version $V_{DET}=2.0V \sim 6.0V$ Version	— —	1.0 1.3	1.7 2.2	μA
Output Current	I_{OUT}	Nch, $V_{DS}=0.5V$ $V_{DD}=1.2V$ $V_{DD}=2.4V(\geq 2.7V$ Version) $V_{DD}=4.8V(\leq 3.9V$ Version) Pch, $V_{DS}=0.5V$ $V_{DD}=6.0V(4.0V \sim 5.6V$ Version) $V_{DD}=8.4V(\geq 5.7V$ Version)	0.75 4.5 2.0 2.5 3.0	2.0 7.0 3.5 4.0 5.0	— — — — —	mA
Detection Voltage Temperature Coefficient	$\Delta V_{DET}/\Delta Ta$	Ta=0 ~ +85°C	—	± 100	—	ppm/°C
Delay Time	td	$V_{DD}=V_{DET}+1V$, D1=H, D2=H D1=H, D2=L D1=L, D2=H D1=L, D2=L	25 42.5 85 170	100 50 100 200	300 57.5 115 230	μs ms ms ms
Delay Time Change Terminal Input Voltage	V_{D1_H}/V_{D2_H}		1.5	—	V_{DD}	V
	V_{D1_L}/V_{D2_L}		0	—	0.3	V
Operating Voltage (*6)	V_{DD}	$R_L=100k\Omega$	0.8	—	9	V

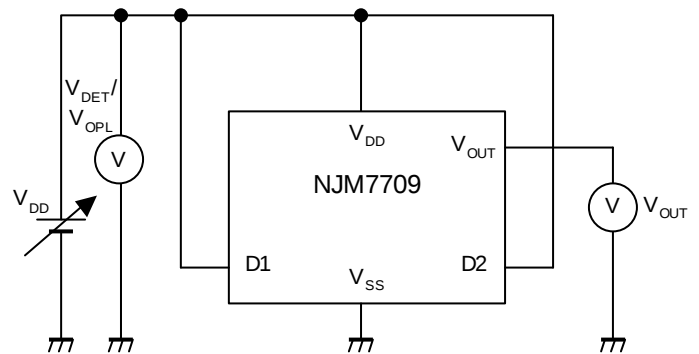
(*6): The minimum Operating Voltage(V_{OPL}) indicates the same value of the output voltage(V_{OUT}) on condition that V_{OUT} becomes 10% or less of the input voltage(V_{DD}).

■ TEST CIRCUIT

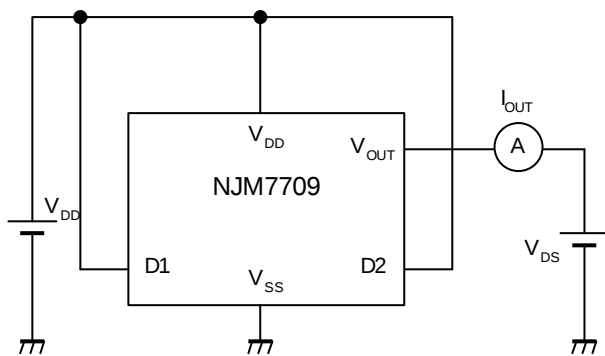
● Quiescent Current TEST CIRCUIT



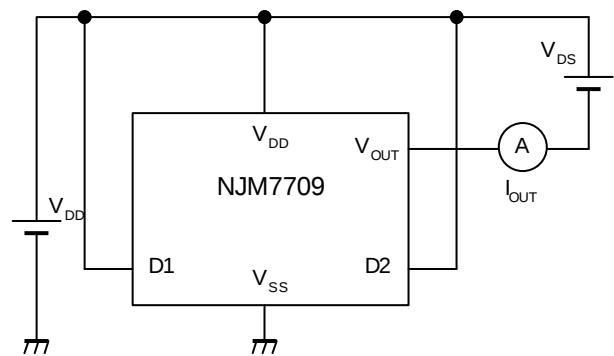
● Detection Voltage TEST CIRCUIT



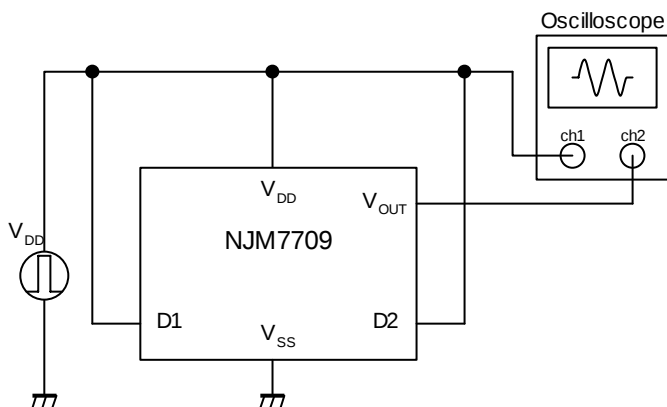
● Nch Output Current TEST CIRCUIT



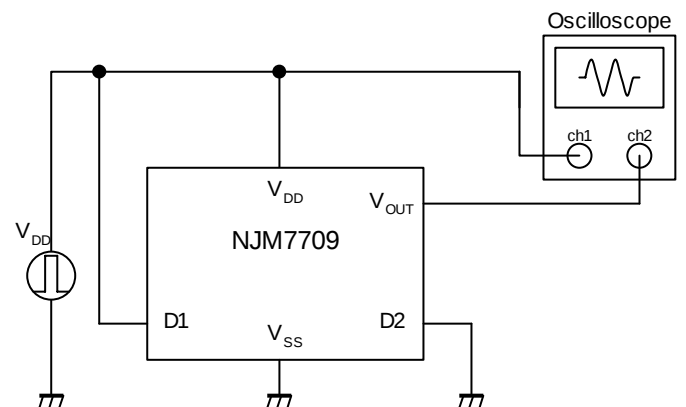
● Pch Output Current TEST CIRCUIT



● Delay Time=0mS TEST CIRCUIT

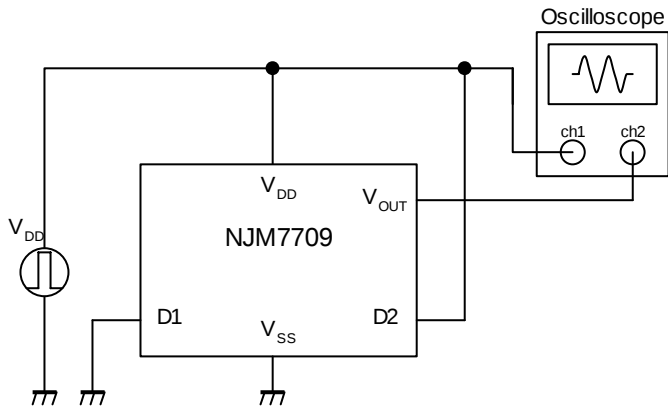


● Delay Time=50mS TEST CIRCUIT

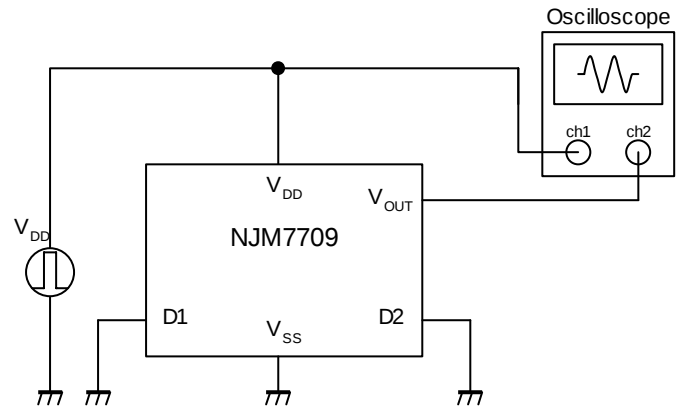


■ TEST CIRCUIT

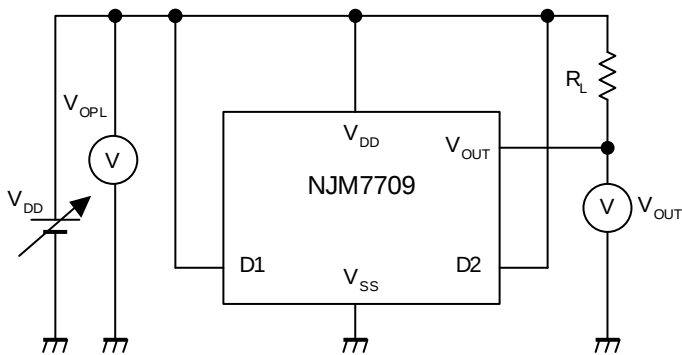
● Delay Time=100mS TEST CIRCUIT



● Delay Time=200mS TEST CIRCUIT

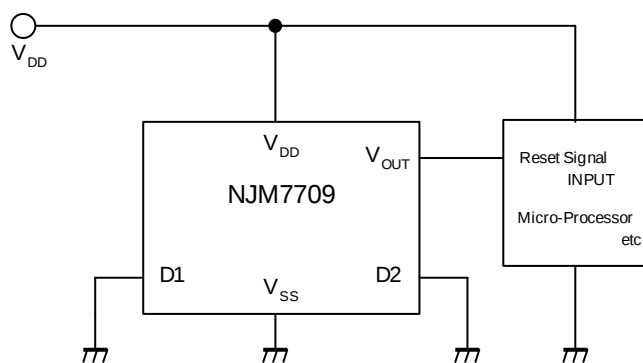


● Minimum Operating Voltage TEST CIRCUIT



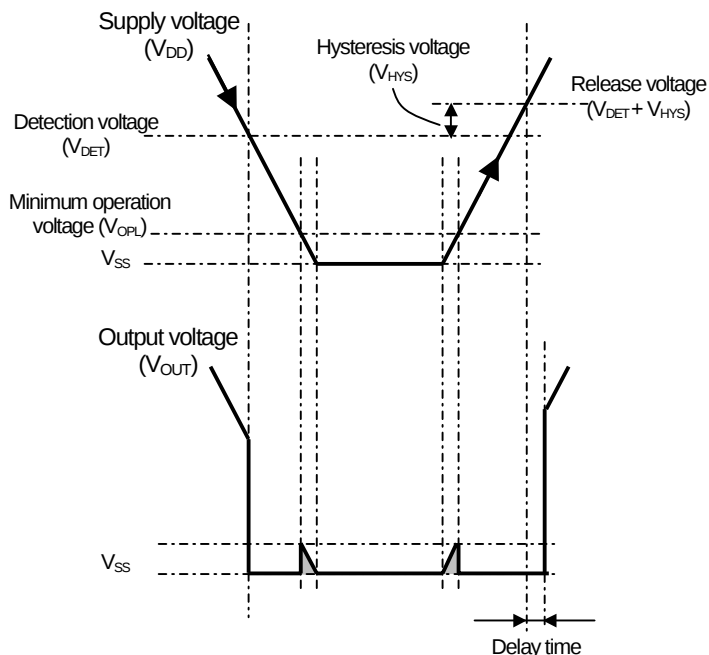
■ TYPICAL APPLICATION

① Power Supply Voltage Supervisory Circuit



■ FUNCTIONAL DESCRIPTION

(1) Basic Operation



- (1) When supply voltage (V_{DD}) drops below detection voltage (V_{DET}), Output voltage (V_{OUT}) changes "H" to "L" to alert reset state.
- (2) The reset state is kept while V_{DD} is lower than release voltage. The release voltage is a sum of V_{DET} and Hysteresis voltage (V_{HY}). Please refer to the (*7) below.
- (3) When V_{DD} becomes higher than the release voltage and reset release delay time fixed by logical select is past, then V_{OUT} changes from "L" to "H" to resume normal state.

(*7) V_{HY} is to avoid unstable V_{OUT} state caused by rapid voltage change at nearby V_{DET} .

(*8): C-MOS output product (NJU7709) : When V_{DD} less than V_{OP} , V_{OUT} is free of the shaded region.

(2) Description of Delay Time

Delay time can be set by logical combination of D1 and D2 (see " LOGICAL TABLE OF DELAY TIME " on page2).

[CAUTION]

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