

BUK9212-55B

N-channel TrenchMOS logic level FET Rev. 03 — 3 February 2011

Product data sheet

1. **Product profile**

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- AEC Q101 compliant
- Low conduction losses due to low on-state resistance
- Suitable for logic level gate drive sources
- Suitable for thermally demanding environments due to 185 °C rating

1.3 Applications

- 12 V and 24 V loads
- Automotive systems

- General purpose power switching
- Motors, lamps and solenoids

1.4 Quick reference data

Quick reference data Table 1.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{DS}	drain-source voltage	$T_j \ge 25 ^{\circ}\text{C}; T_j \le 185 ^{\circ}\text{C}$		-	-	55	V
I _D	drain current	V _{GS} = 5 V; T _{mb} = 25 °C; see <u>Figure 1</u> ; see <u>Figure 3</u>	[1]	-	-	75	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>		-	-	167	W
Static chara	acteristics						
R _{DSon}	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A};$ $T_j = 25 \text{ °C}; \text{ see } \frac{\text{Figure 12}}{\text{Figure 11}};$ see Figure 11		-	10.2	12	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A};$ $T_i = 25 \text{ °C}$		-	8.1	10	mΩ



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Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Avalanche	ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 75 A; $V_{sup} \le 55$ V; R_{GS} = 50 Ω ; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped	-	-	173	mJ
Dynamic ch	naracteristics					
Q_{GD}	gate-drain charge	$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A};$ $V_{DS} = 44 \text{ V}; T_j = 25 \text{ °C};$ see Figure 13	-	13	-	nC

^[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		_
2	D	drain[1]	mb	D D
3	S	source		
mb	D	mounting base; connected to drain	1 3	mbb076 S
			SOT428 (DPAK)	

^[1] It is not possible to make a connection to pin 2 of the SOT428 package.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9212-55B	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 185 °C	-	55	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	55	V
V_{GS}	gate-source voltage		-15	15	V
I _D	drain current	$T_{mb} = 25 ^{\circ}C; V_{GS} = 5 V; \text{ see } \frac{\text{Figure 1}}{};$	<u>[1]</u> _	83	Α
		see <u>Figure 3</u>	[2] _	75	Α
		T_{mb} = 100 °C; V_{GS} = 5 V; see <u>Figure 1</u>	<u>[1]</u> _	59	Α
I _{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \le 10 \mu s$; see Figure 3	-	335	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	167	W
T _{stg}	storage temperature		-55	185	°C
Tj	junction temperature		-55	185	°C
Source-drai	n diode				
Is	source current	T _{mb} = 25 °C	<u>[1]</u> -	83	Α
			[2] _	75	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$	-	335	Α
Avalanche r	uggedness				
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 75 A; $V_{sup} \le$ 55 V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped	-	173	mJ
		** *			

- [1] Current is limited by power dissipation chip rating.
- [2] Continuous current is limited by package.

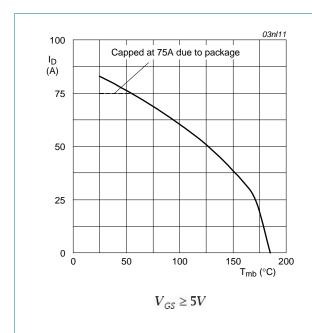


Fig 1. Normalized continuous drain current as a function of mounting base temperature

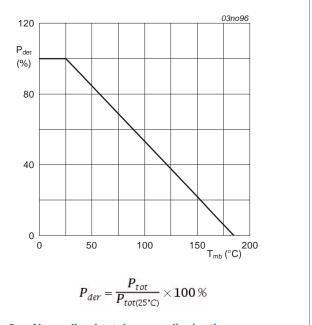
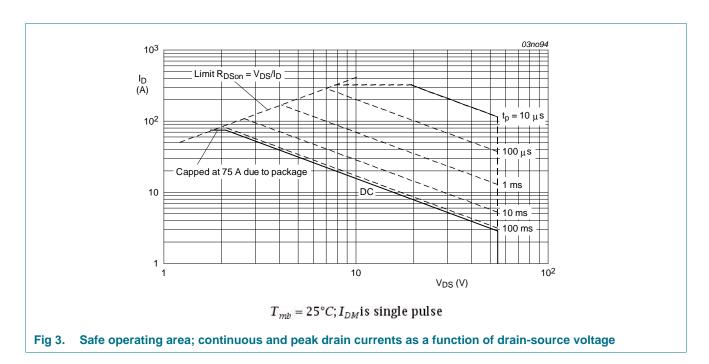


Fig 2. Normalized total power dissipation as a function of mounting base temperature

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5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	0.95	K/W
R _{th(j-a)}	thermal resistance from junction to ambient		-	71.4	-	K/W

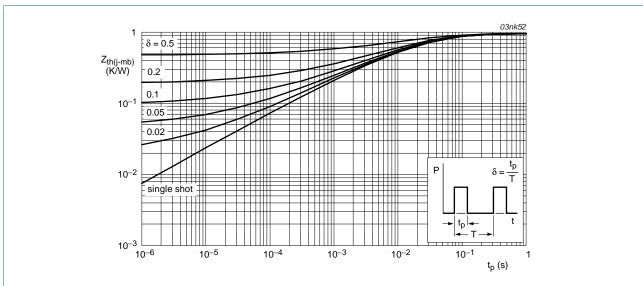


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static char	acteristics					
V _{(BR)DSS}	drain-source	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_i = 25 \text{ °C}$	55	-	-	V
	breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ °C}$	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = 25$ °C; see Figure 10	1.1	1.5	2	V
		I_D = 1 mA; V_{DS} = V_{GS} ; T_j = 185 °C; see Figure 10	0.4	-	-	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = -55$ °C; see Figure 10	-	-	2.3	V
I _{DSS}	drain leakage current	$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 185 ^{\circ}\text{C}$	-	-	500	μΑ
		$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.02	1	μΑ
I _{GSS}	gate leakage current	$V_{GS} = 15 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nA
		$V_{GS} = -15 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nA
R _{DSon}	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 185 °C;$ see <u>Figure 11</u> ; see <u>Figure 12</u>	-	-	25	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C}$	-	-	13	mΩ
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C};$ see Figure 12; see Figure 11	-	10.2	12	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^{\circ}\text{C}$	-	8.1	10	mΩ
Dynamic c	naracteristics					
Q _{G(tot)}	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 44 \text{ V}; V_{GS} = 5 \text{ V};$	-	32	-	nC
Q _{GS}	gate-source charge	T _j = 25 °C; see <u>Figure 13</u>	-	6	-	nC
Q_{GD}	gate-drain charge		-	13	-	nC
C _{iss}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$	-	2640	3519	pF
C _{oss}	output capacitance	T _j = 25 °C; see <u>Figure 14</u>	-	360	431	pF
C _{rss}	reverse transfer capacitance		-	160	220	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \Omega; V_{GS} = 5 \text{ V};$	-	19	-	ns
t _r	rise time	$R_{G(ext)} = 10 \Omega$; $T_j = 25 °C$	-	101	-	ns
t _{d(off)}	turn-off delay time	V_{DS} 30 V; $R_L = 1.2 \Omega$; $V_{GS} = 5$ V; $R_{G(ext)} = 10 \Omega$; $T_j = 25 ^{\circ}\text{C}$	-	96	-	ns
t _f	fall time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \Omega; V_{GS} = 5 \text{ V};$ $R_{G(ext)} = 10 \Omega; T_j = 25 \text{ °C}$	-	75	-	ns
L _D	internal drain inductance	measured from drain to center of die ; $T_j = 25 ^{\circ}\text{C}$	-	2.5	-	nΗ
L _S	internal source inductance	measured from source lead to source bond pad; $T_j = 25$ °C	-	7.5	-	nΗ
Source-dra	in diode	·				
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C};$ see <u>Figure 15</u>	-	0.85	1.2	V
t _{rr}	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s};$	-	55	-	ns
Q _r	recovered charge	$V_{GS} = -10 \text{ V}; V_{DS} = 30 \text{ V}; T_j = 25 \text{ °C}$	-	53	-	nC
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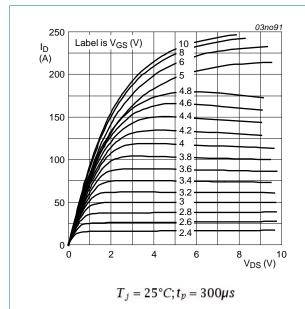


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

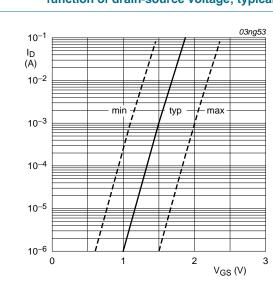
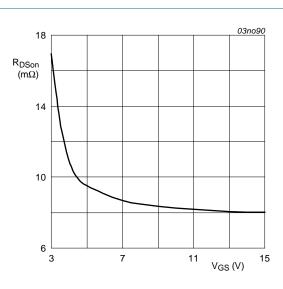


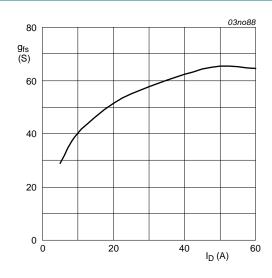
Fig 7. Sub-threshold drain current as a function of gate-source voltage

 $T_j = 25 \,^{\circ}C; V_{DS} = V_{GS}$



 $T_j = 25^{\circ}C; I_D = 25A$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values



 $T_j = 25^{\circ}C; V_{DS} = 25V$

Fig 8. Forward transconductance as a function of drain current; typical values

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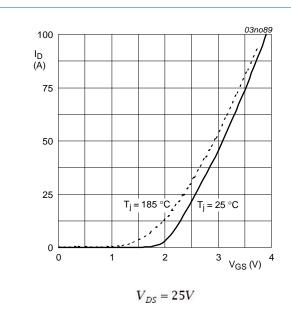


Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

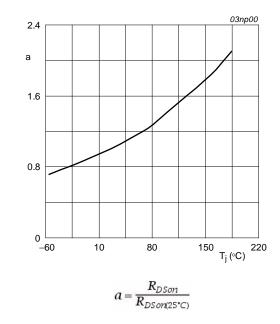
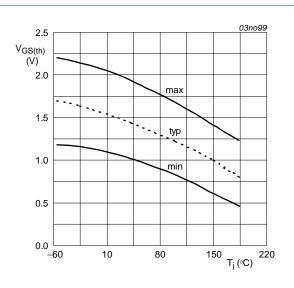
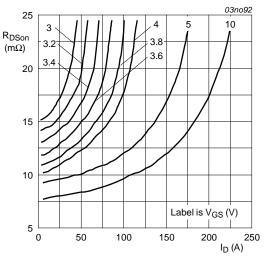


Fig 11. Normalized drain-source on-state resistance factor as a function of junction temperature



 $I_D = 1mA; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature



 $T_j = 25^{\circ}C; t_p = 300\mu s$

Fig 12. Drain-source on-state resistance as a function of drain current; typical values

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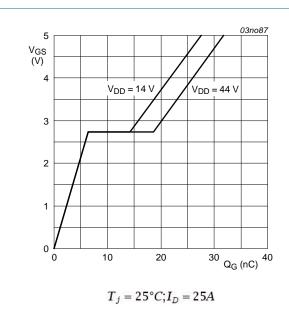
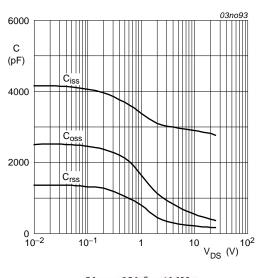


Fig 13. Gate-source voltage as a function of turn-on gate charge; typical values



 $V_{GS} = 0V; f = 1MHz$

Fig 14. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

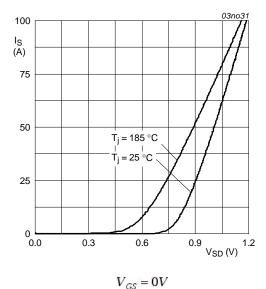


Fig 15. Source current as a function of source-drain voltage; typical values

7. Package outline

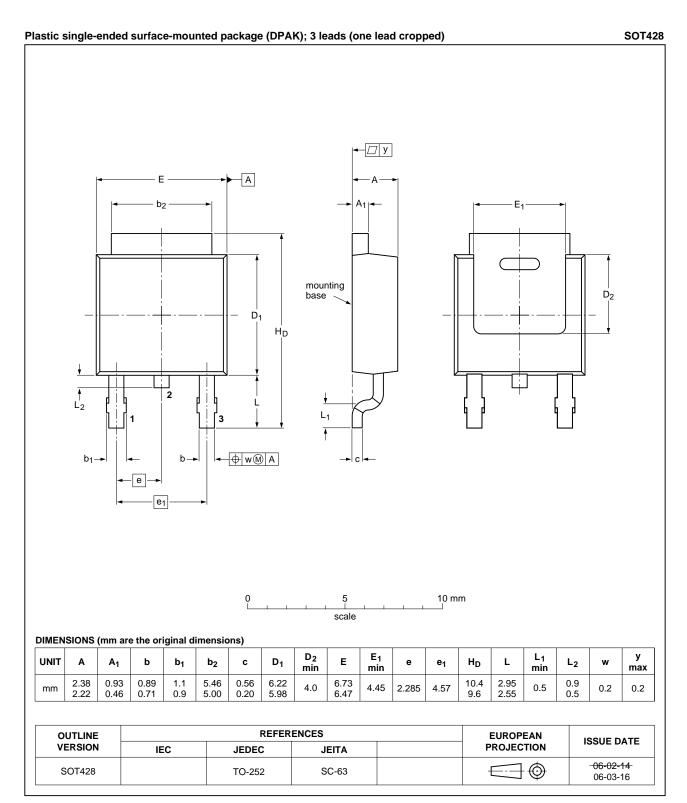


Fig 16. Package outline SOT428 (DPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9212-55B v.3	20110203	Product data sheet	-	BUK9212-55B v.2
Modifications:	of NXP Semico	onductors. /e been adapted to the new		the new identity guidelines appropriate.
BUK9212-55B v.2 (9397 750 12235)	20031212	Product data	-	-

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9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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