Hex Gate

The MC14572UB hex functional gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired. The chip contains four inverters, one NOR gate and one NAND gate.

Features

- Diode Protection on All Inputs
- Single Supply Operation
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- NOR Input Pin Adjacent to VSS Pin to Simplify Use As An Inverter
- NAND Input Pin Adjacent to V_{DD} Pin to Simplify Use As An Inverter
- NOR Output Pin Adjacent to Inverter Input Pin For OR Application
- NAND Output Pin Adjacent to Inverter Input Pin For AND Application
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable*
- This Device is Pb-Free and is RoHS Compliant

$\textbf{MAXIMUM RATINGS} \text{ (Voltages Referenced to V}_{SS}\text{)}$

Parameter	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	-0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	V _{in} , V _{out}	-0.5 to V _{DD} + 0.5	V
Input or Output Current (DC or Transient) per Pin	I _{in} , I _{out}	±10	mA
Power Dissipation, per Package (Note 1)	P _D	500	mW
Ambient Temperature Range	T _A	-55 to +125	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C
Lead Temperature (8-Second Soldering)	TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packagé: -7.0 mW/°C From 65°C To 125°C This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



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SOIC-16 D SUFFIX CASE 751B

PIN ASSIGNMENT

OUT_A	d	1●	16	V _{DD}
IN_A		2	15	IN 2 _F
OUT_B		3	14	IN 1 _F
IN_B		4	13	OUTF
OUT_C	d	5	12] IN _E
IN 1 _C		6	11	OUT _E
IN 2 _C	d	7	10] IN _D
V_{SS}		8	9	

MARKING DIAGRAM

A = Assembly Location

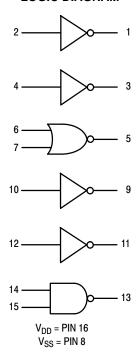
WL = Wafer Lot
 YY = Year
 WW = Work Week
 G = Pb-Free Package

ORDERING INFORMATION

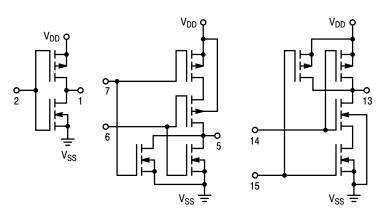
Device	Package	Shipping [†]		
MC14572UBDG	SOIC-16 (Pb-Free)	48 Units / Rail		
MC14572UBDR2G	SOIC-16 (Pb-Free)	2500/Tape & Reel		
NLV14572UBDR2G*	SOIC-16 (Pb-Free)	2500/Tape & Reel		

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

LOGIC DIAGRAM



CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

			- 55°C 25°C 125°C		5°C					
Characteristic	Symbol	V _{DD} Vdc	Min	Max	Min	Typ (Note 2)	Max	Min	Max	Unit
Output Voltage "0" Level V _{in} = V _{DD} or 0	V _{OL}	5.0 10 15	- - -	0.05 0.05 0.05	- - -	0 0 0	0.05 0.05 0.05	- - -	0.05 0.05 0.05	Vdc
V _{in} = 0 or V _{DD} "1" Level	V _{OH}	5.0 10 15	4.95 9.95 14.95	- - -	4.95 9.95 14.95	5.0 10 15	- - -	4.95 9.95 14.95	- - -	Vdc
Input Voltage "0" Level (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0 10 15	- - -	1.0 2.0 2.5	- - -	2.25 4.50 6.75	1.0 2.0 2.5	- - -	1.0 2.0 2.5	Vdc
"1" Level $(V_O = 0.5 \text{ or } 4.5 \text{ Vdc})$ $(V_O = 1.0 \text{ or } 9.0 \text{ Vdc})$ $(V_O = 1.5 \text{ or } 13.5 \text{ Vdc})$	V _{IH}	5.0 10 15	4.0 8.0 12.5	- - -	4.0 8.0 12.5	2.75 5.50 8.25	- - -	4.0 8.0 12.5	- - -	Vdc
Output Drive Current (V _{OH} = 2.5 Vdc) Source (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	ІОН	5.0 5.0 10 15	-1.2 -0.25 -0.62 -1.8	- - -	-1.0 -0.2 -0.5 -1.5	-1.7 -0.36 -0.9 -3.5	- - - -	-0.7 -0.14 -0.35 -1.1	- - - -	mAdc
$(V_{OL} = 0.4 \text{ Vdc})$ Sink $(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$	I _{OL}	5.0 10 15	0.64 1.6 4.2	- - -	0.51 1.3 3.4	0.88 2.25 8.8	- - -	0.36 0.9 2.4	- - -	mAdc
Input Current	I _{in}	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	-	_	_	_	5.0	7.5	_	_	pF
Quiescent Current (Per Package)	I _{DD}	5.0 10 15	- - -	0.25 0.5 1.0	- - -	0.0005 0.0010 0.0015	0.25 0.5 1.0	- - -	7.5 15 30	μAdc
Total Supply Current (Notes 3, 4) (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0 10 15			$I_{T} = (3)$.89 μA/kHz) .80 μA/kHz) .68 μA/kHz)	f + I _{DD}			μAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
 Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
 The formulas given are for the typical characteristics only at 25°C.
 To calculate total supply current at loads other than 50 pF: I_T(C_L) = I_T(50 pF) + (C_L – 50) Vfk where: I_T is in μA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.006.

SWITCHING CHARACTERISTICS (Type 5) ($C_L = 50 \text{ pF}, T_A = 25^{\circ}C$)

Characteristic	Symbol	V _{DD}	Min	Typ (Note 6)	Max	Unit
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	t _{TLH}	5.0 10 15	- - -	180 90 65	360 180 130	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t _{THL}	5.0 10 15	- - -	100 50 40	200 100 80	ns
Propagation Delay Time t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 5 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 17 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 15 \text{ ns}$	t _{PLH} , t _{PHL}	5.0 10 15	- - -	90 50 40	180 100 80	ns

^{5.} The formulas given are for the typical characteristics only at 25°C.
6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

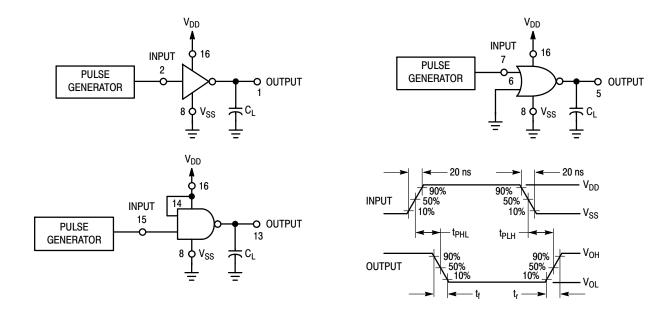
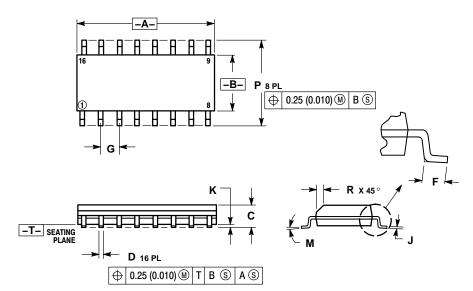


Figure 1. Switching Time Test Circuits and Waveforms

PACKAGE DIMENSIONS

SOIC-16 CASE 751B-05 ISSUE K

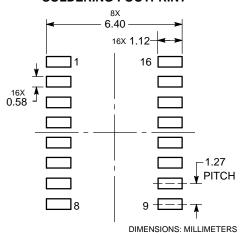


NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
 DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- DIMENSION D DOES NOT INCLUDE DAMBAR
 PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	9.80	10.00	0.386	0.393	
В	3.80	4.00	0.150	0.157	
C	1.35	1.75	0.054	0.068	
ם	0.35	0.49	0.014	0.019	
F	0.40	1.25	0.016	0.049	
G	1.27	BSC	0.050 BSC		
7	0.19	0.25	0.008	0.009	
K	0.10	0.25	0.004	0.009	
M	0°	7°	0°	7°	
P	5.80	6.20	0.229	0.244	
R	0.25	0.50	0.010	0.019	

SOLDERING FOOTPRINT



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