

General Description

The MAX504/MAX515 are low-power, voltage-output, 10-bit digital-to-analog converters (DACs) specified for single +5V power-supply operation. The MAX504 can also be operated with $\pm 5V$ supplies. The MAX515 draws only 140µA, and the MAX504 (with internal reference) draws only 260µA. The MAX515 comes in 8-pin DIP and SO packages, while the MAX504 comes in 14pin DIP and SO packages. Both parts have been trimmed for offset voltage, gain, and linearity, so no further adjustment is necessary.

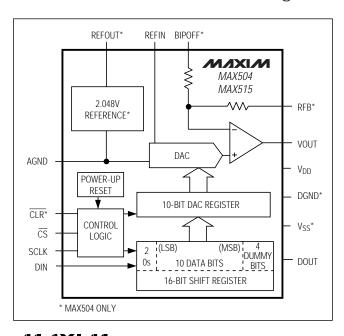
The MAX515's buffer is fixed at a gain of 2. The MAX504's internal op amp may be configured for a gain of 1 or 2, as well as for unipolar or bipolar output voltages. The MAX504 can also be used as a four-quadrant multiplier without external resistors or op amps.

For parallel data inputs, see the MAX503 data sheet. For a hardware and software compatible 12-bit upgrade, refer to the MAX531/MAX538/MAX539 data sheet.

Applications

Battery-Powered Test Instruments Digital Offset and Gain Adjustment Battery-Operated/Remote Industrial Controls Machine and Motion Control Devices Cellular Telephones

Functional Diagram



Features

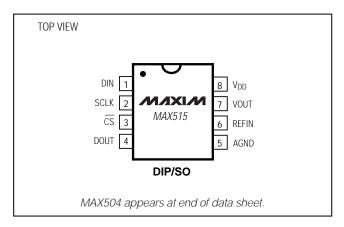
- ♦ Operate from Single +5V Supply
- Buffered Voltage Output
- ♦ Internal 2.048V Reference (MAX504)
- † 140µA Supply Current (MAX515)
- ♦ INL = ±1/2LSB (max)
- **♦** Guaranteed Monotonic Over Temperature
- **♦ Flexible Output Ranges:** 0V to VDD (MAX504/MAX515) Vss to V_{DD} (MAX504)
- **♦ 8-Pin SO/DIP (MAX515)**
- ♦ Power-On Reset
- Serial Data Output for Daisy-Chaining

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX504CPD	0°C to +70°C	14 Plastic DIP
MAX504CSD	0°C to +70°C	14 SO
MAX504EPD	-40°C to +85°C	14 Plastic DIP
MAX504ESD	-40°C to +85°C	14 SO
MAX515CPA	0°C to +70°C	8 Plastic DIP
MAX515CSA	0°C to +70°C	8 SO
MAX515EPA	-40°C to +85°C	8 Plastic DIP
MAX515ESA	-40°C to +85°C	8 SO

Refer to the MAX531/MAX538/MAX539 data sheet for military temperature or die equivalents.

Pin Configurations



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ABSOLUTE MAXIMUM RATINGS

Note 1: The output may be shorted to VDD, Vss, or AGND if the package power dissipation limit is not exceeded.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +5V Supply

 $(V_{DD} = 5V, V_{SS} = 0V, AGND = DGND = 0V, REFIN = 2.048V (external), RFB = BIPOFF = VOUT (MAX504), C_{REFOUT} = 33 \mu F (MAX504), R_L = 10 k\Omega$, $C_L = 100 pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution	N		10			Bits
Relative Accuracy (Note 2)	INL				±0.5	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic			±1	LSB
Unipolar Offset Error	Vos		0		3	LSB
Unipolar Offset Tempco	TCVos			3		ppm/°C
Unipolar Offset-Error Power-Supply Rejection Ratio	PSRR	4.5V ≤ V _{DD} ≤ 5.5V		0.1		LSB/V
Gain Error (Note 2)	GE				±1	LSB
Gain-Error Tempco				1		ppm/°C
Gain-Error Power-Supply Rejection Ratio	PSRR	4.5V ≤ V _{DD} ≤ 5.5V		0.1		LSB/V
VOLTAGE OUTPUT (Vout)						l
Output Valtage Dange		MAX504 (G = 1)	0		V _{DD} - 2	V
Output Voltage Range		MAX504 (G = 2), MAX515	0		V _{DD} - 0.4	V
Output Load Regulation		VOUT = 2V, $R_L = 2k\Omega$			0.5	LSB
Short-Circuit Current	Isc			12		mA
REFERENCE INPUT (REFIN)						
Voltage Range			0		V _{DD} - 2	V
Input Resistance		Code dependent, minimum at code 0101	40			kΩ
Input Capacitance		Code dependent (Note 3)	10		50	pF
AC Feedthrough		REFIN = 1kHz, 2Vp-p		-80		dB

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

 $(V_{DD}=5V,V_{SS}=0V,AGND=DGND=0V,REFIN=2.048V \ (external),RFB=BIPOFF=VOUT \ (MAX504),C_{REFOUT}=33\mu F \ (MAX504),R_{L}=10k\Omega,C_{L}=100pF,T_{A}=T_{MIN} \ to \ T_{MAX},unless \ otherwise \ noted.)$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE OUTPUT (REFOUT	-MAX504 Or	nly)	l			
		TA = +25°C	2.024	2.048	2.072	
Reference Output Voltage		MAX504C	2.015		2.081	V
		MAX504E	2.011		2.085	
Temperature Coefficient	TCREFOUT			30		ppm/°C
Resistance	Rrefout	(Note 4)		0.5	2	Ω
Power-Supply Rejection Ratio	PSRR	$4.5V \le V_{DD} \le 5.5V$		200		μV/V
Noise Voltage	en	0.1Hz to 10kHz		400		µVp-р
Required External Capacitor	CREFOUT		3.3			μF
DIGITAL INPUTS (DIN, SCLK, CS	S, CLR)		<u> </u>			
Input High	VIH		2.4			V
Input Low	VIL				0.8	V
Input Current	liN	VIN = 0V or VDD			±1	μΑ
Input Capacitance	CIN			8		pF
DIGITAL OUTPUT (DOUT)	•					
Output High	V _{OH}	ISOURCE = 2mA	V _{DD} - 1			V
Output Low	VoL	ISINK = 2mA			0.4	V
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate	SR	TA = +25°C	0.15	0.25		V/µs
Voltage-Output Settling Time		To $\pm 1/2$ LSB, VOUT = 2V		25		μs
Digital Feedthrough		$\overline{\text{CS}} = V_{\text{DD}}$, DIN = 100kHz		5		nV-s
Signal-to-Noise Plus Distortion	SINAD	REFIN = 1kHz, 2Vp-p (G = 1 or 2), code = 1111		68		dB
POWER SUPPLY	•		'			
Positive Supply Voltage	VDD		4.5		5.5	V
Power-Supply Current	I _{DD}	All inputs = 0V or V _{DD} , MAX504 output = no load MAX515		260 140	400 300	μΑ
SWITCHING CHARACTERISTICS	(Note 5)		'			
CS Setup Time	tcss		20			ns
SCLK Fall to CS Fall Hold Time	tCSH0		15			ns
SCLK Fall to CS Rise Hold Time	tCSH1		0			ns
SCLK High Width	tсн		35			ns
SCLK Low Width	tcL		35			ns
DIN Setup Time	t _{DS}		45			ns
DIN Hold Time	tDH		0			ns
DOUT Valid Propagation Delay	t _{DO}	$C_L = 50pF$			80	ns
CS High Pulse Width	tcsw		20			ns
CLR Pulse Width	tclr		25			ns
CS Rise to SCLK Rise Setup Time	tCS1		50			ns

ELECTRICAL CHARACTERISTICS—Dual ±5V Supplies (MAX504 Only)

 $(V_{DD}=5V,\,V_{SS}=-5V,\,AGND=DGND=0V,\,REFIN=2.048V\,\,(external),\,RFB=BIPOFF=VOUT,\,C_{REFOUT}=33\mu F,\,R_L=10k\Omega,\,C_L=100pF,\,T_A=T_{MIN}\,to\,T_{MAX},\,unless\,otherwise\,noted.)$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution	N		10			Bits
Relative Accuracy	INL				±0.5	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic			±1	LSB
Bipolar Offset Error	Vos	BIPOFF = REFIN			±3	LSB
Bipolar Offset Tempco	TCVos	BIPOFF = REFIN		3		ppm/°C
Offset-Error Power-Supply Rejection Ratio	PSRR	$4.5V \le V_{DD} \le 5.5V$, $-5.5V \le V_{SS} \le -4.5V$		0.1		LSB/V
Gain Error (Unipolar or Bipolar)	GE				±1	LSB
Gain-Error Tempco				1		ppm/°C
Gain-Error Power-Supply Rejection Ratio	PSRR	$4.5V \le V_{DD} \le 5.5V$, $-5.5V \le V_{SS} \le -4.5V$		0.1		LSB/V
REFERENCE INPUT (REFIN)						
Voltage Range			V _{SS} + 2		V _{DD} - 2	V
Input Resistance		Code dependent, minimum at code 0101	40			kΩ
Input Capacitance		Code dependent (Note 3)	10		50	рF
AC Feedthrough		REFIN = 1kHz, 2.0Vp-p		-80		dB
REFERENCE OUTPUT (REFOU	T—MAX504	Only)	•			
		$T_A = +25^{\circ}C$	2.024	2.048	2.072	
Reference Output Voltage		MAX504C	2.015		2.081	V
		MAX504E	2.011		2.085	
Temperature Coefficient	TCREFOUT			30		ppm/°C
Resistance	RREFOUT	(Note 4)		0.5	2	Ω
Power-Supply Rejection Ratio	PSRR	$4.5V \le V_{DD} \le 5.5V$		200		μV/V
Noise Voltage	en	0.1Hz to 10kHz		400		μVp-р
Required External Capacitor	CREFOUT		3.3			μF
DIGITAL INPUTS (DIN, SCLK, \overline{C}	S)					
Input High	VIH		2.4			V
Input Low	VIL				0.8	V
Input Current	I _{IN}	$V_{IN} = 0V \text{ or } V_{DD}$			±1	μΑ
Input Capacitance	CIN			8		рF
DIGITAL OUTPUT (DOUT)						
Output High	VoH	ISOURCE = 2mA	V _{DD} - 1			V
Output Low	Vol	I _{SINK} = 2mA		<u></u>	0.4	V

ELECTRICAL CHARACTERISTICS—Dual ±5V Supplies (MAX504 Only) (continued)

 $(V_{DD}=5V,\,V_{SS}=-5V,\,AGND=DGND=0V,\,REFIN=2.048V$ (external), RFB = BIPOFF = VOUT, CREFOUT = $33\mu F,\,R_L=10k\Omega,\,C_L=100pF,\,T_A=T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
VOLTAGE OUTPUT (VOUT)	1				'		
Output Valtage Dange		(G = 1)	Vss + 2		V _{DD} - 2	2 V	
Output Voltage Range		(G = 2)	V _{SS} + 0.4		V _{DD} - 0.4	V	
Output Load Regulation		VOUT = 2V, $R_L = 2k\Omega$			0.5	LSB	
Short-Circuit Current	Isc			12		mA	
DYNAMIC PERFORMANCE	1		<u>'</u>		'		
Voltage-Output Slew Rate	SR		0.15	0.25		V/µs	
Voltage-Output Settling Time		To $\pm 1/2$ LSB, VOUT = 2V		16		μs	
Digital Feedthrough		Step all 0s to all 1s		5		nV-s	
Ciarral ta Naisa Dhaa Diatantian	CINIAD	REFIN = $1kHz$, $2Vp-p$ (G = 1)		68		dB	
Signal-to-Noise Plus Distortion	SINAD	REFIN = 1kHz, 2Vp-p (G = 2)		68	68		
POWER SUPPLY	II.		'				
Positive Supply Voltage	V _{DD}		4.5		5.5	V	
Negative Supply Voltage	Vss		-5.5		0	V	
Positive Supply Current	IDD	All inputs = 0V or V _{DD} , no load		260	400	μΑ	
Negative Supply Current	Iss	All inputs = 0V or V _{DD} , no load		-120	-200	μΑ	
SWITCHING CHARACTERISTIC	S						
CS Setup Time	tcss		20			ns	
SCLK Fall to CS Fall Hold Time	tcsH0		15			ns	
SCLK Fall to CS Rise Hold Time	tcsH1		0			ns	
SCLK High Width	tсн		35			ns	
SCLK Low Width	tCL		35			ns	
DIN Setup Time	tDS		45			ns	
DIN Hold Time	tDH		0			ns	
DOUT Valid Propagation Delay	t _{DO}	$C_L = 50pF$			80	ns	
CS High Pulse Width	tcsw		20			ns	
CLR Pulse Width	tCLR		25			ns	
CS Rise to SCLK Rise Setup Time	tCS1		50			ns	

Note 2: In single-supply operation, INL and GE calculated from Code 3 to Code 1023.

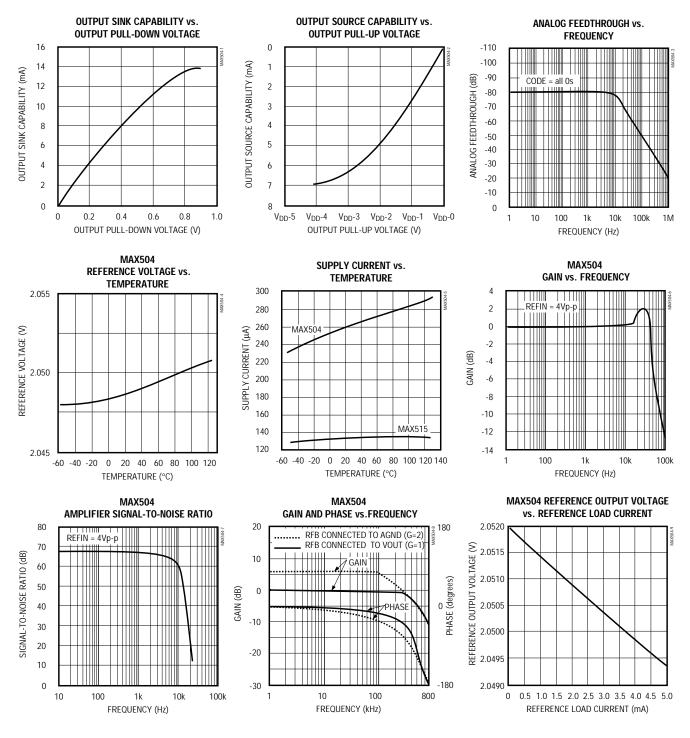
Note 3: Guaranteed by design.

Note 4: Tested at I_{OUT} = 100µA. The reference can typically source up to 5mA (see *Typical Operating Characteristics*).

Note 5: The timing characteristics limits for the MAX515 are guaranteed by design.

Typical Operating Characteristics

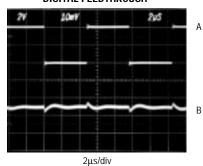
 $(V_{DD} = +5V, V_{RFFIN} = 2.048V, T_A = +25^{\circ}C, unless otherwise noted.)$



_Typical Operating Characteristics (continued)

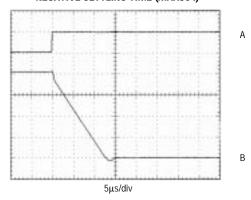
(VDD = +5V, VREFIN = 2.048V, TA = +25°C, unless otherwise noted.)

DIGITAL FEEDTHROUGH



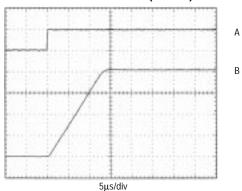
CS = HIGH A: DIN = 4Vp-p, 100kHz B: VOUT, 10mV/div

NEGATIVE SETTLING TIME (MAX504)



A: $\overline{\text{CS}}$ RISING EDGE, 5V/div B: VOUT, NO LOAD, 1V/div DUAL SUPPLY ±5V BIPOLAR CONFIGURATION V_{REFIN} = 2V

POSITIVE SETTLING TIME (MAX504)



A: $\overline{\text{CS}}$ RISING EDGE, 5V/div B: VOUT, NO LOAD, 1V/div DUAL SUPPLY ±5V BIPOLAR CONFIGURATION V_{REFIN} = 2V

Pin Description

PIN NAME **FUNCTION MAX504 MAX515** Bipolar offset/gain 1 **BIPOFF** resistor 2 1 DIN Serial data input Clear. Asynchronously sets 3 **CLR** DAC register to all 0s. 4 2 **SCLK** Serial clock input CS 5 3 Chip select, active low Serial data output for DOUT 6 4 daisy-chaining 7 **DGND** Digital ground 8 5 **AGND** Analog ground 9 6 REFIN Reference input Reference output, 2.048V. Connect to VDD 10 **REFOUT** if not used. Negative power supply 11 Vss **VOUT** 12 7 DAC output 8 13 V_{DD} Positive power supply 14 **RFB** Feedback resistor

Detailed Description

General DAC Discussion

The MAX504/MAX515 use an "inverted" R-2R ladder network with a single-supply CMOS op amp to convert 10-bit digital data to analog voltage levels (see *Functional Diagram*). The term "inverted" describes the ladder network because the REFIN pin in current-output DACs is the summing junction, or virtual ground, of an op amp. However, such use would result in the output voltage being the inverse of the reference voltage. The MAX504/MAX515's topology makes the output the same polarity as the reference input.

An internal reset circuit forces the DAC register to reset to all 0s on power-up. Additionally, a clear (CLR) pin, when held low, sets the DAC register to all 0s. CLR operates asynchronously and independently from the chip select (CS) pin.

Buffer Amplifier

The output buffer is a unity-gain stable, rail-to-rail output, BiCMOS op amp. Input offset voltage and CMRR are trimmed to achieve better than 10-bit performance. Settling time is 25µs to 0.01% of final value. The output is short-circuit protected and can drive a $2k\Omega$ load with more than 100pF load capacitance.

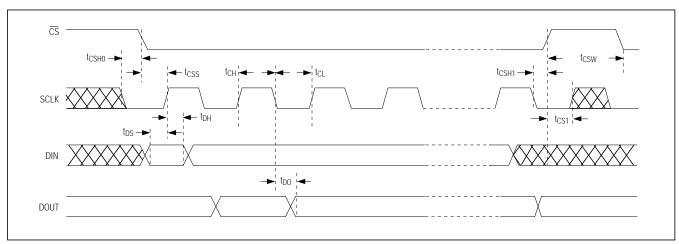


Figure 1. Timing Diagram

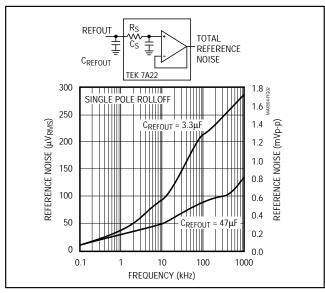


Figure 2. Reference Noise vs. Frequency

Internal Reference (MAX504 only)

The on-chip reference is laser trimmed to generate 2.048V at REFOUT. The output stage can source and sink current so REFOUT can settle to the correct voltage quickly in response to code-dependent loading changes. Typically, source current is 5mA and sink current is 100µA.

REFOUT connects the internal reference to the R-2R DAC ladder at REFIN. The R-2R ladder draws 50 μ A maximum load current. If any other connection is made to REFOUT, ensure that the total load current is less than 100 μ A to avoid gain errors.

For applications requiring very low-noise performance, connect a 33 μ F capacitor from REFOUT to AGND. If noise is not a concern, a lower value (3.3 μ F min) capacitor may be used. To reduce noise further, insert a buffered RC filter between REFOUT and REFIN (Figure 2). The reference bypass capacitor C_{REFOUT} is still required for reference stability. In applications not requiring the reference, connect REFOUT to V_{DD} (to save power and to eliminate the need for C_{REFOUT}) or use the MAX515 (no internal reference).

External Reference

An external reference in the range (Vss + 2V) to (VpD - 2V) may be used with the MAX504 in dual-supply operation. With the MAX515 or the MAX504 in single-supply use, the reference must be positive and may not exceed VpD - 2V. The reference voltage determines the DAC's full-scale output. The DAC input resistance is code dependent and is minimum (40k Ω) at code 0101... and virtually infinite at

code 0000.... REFIN's input capacitance is also code dependent and has a 50pF maximum value at several codes.

If an upgrade to the internal reference is required, the 2.5V MAX873A is suitable: ± 15 mV initial accuracy, TCV_{OUT} = 7ppm/°C (max).

Logic Interface

The MAX504/MAX515 logic inputs are designed to be compatible with TTL or CMOS logic levels. However, to achieve the lowest power dissipation, drive the digital inputs with rail-to-rail CMOS logic. With TTL logic levels, the power requirement increases by a factor of approximately 2.

Serial Clock and Update Rate

Figure 1 shows the MAX504/MAX515 timing. The maximum serial clock rate is given by $1/(t_{CH}+t_{CL})$, approximately 14MHz. The digital update rate is limited by the chip-select period, which is 16 x $(t_{CH}+t_{CL})+t_{CSW}$. This equals a 1.14 μ s, or 877kHz, update rate. However, the DAC settling time to 10 bits is 25 μ s, which may limit the update rate to 40kHz for full-scale step transitions.

_Applications Information

Refer to Figures 3a and 3b for typical operating connections.

Serial Interface

The MAX504/MAX515 use a three-wire serial interface that is compatible with SPI™, QSPI™ (CPOL = CPHA = 0), and Microwire™ standards as shown in Figures 4 and 5. The DAC is programmed by writing two 8-bit words (see Figure 1 and the Functional Diagram). 16 bits of serial data are clocked into the DAC in the following order: 4 fill (dummy) bits, 10 data bits, and 2 sub-LSB 0s. The 4 dummy bits are not normally needed, and are required only when DACs are daisy chained. The 2 sub-LSB 0s, however, are always needed, and allow hardware and software compatibility with the 12-bit MAX531/MAX538/MAX539. Transitions at CS should occur while SCLK is low. Data is clocked in on SCLK's rising edge while \overline{CS} is low. The serial input data is held in a 16-bit serial shift register. On \overline{CS} 's rising edge, the 10 data-bits are transferred to the DAC register and update the DAC. With $\overline{\text{CS}}$ high, data cannot be clocked into the MAX504/MAX514.

The MAX504/MAX515 inputs data in 16-bit blocks. The SPI and Microwire interfaces output data in 8-bit blocks, thereby requiring two write cycles to input data to the DAC. The QSPI interface allows variable data input from 8 to 16 bits, and can be loaded into the DAC in one write cycle.

SPI and QSPI are trademarks of Motorola, Inc., Microwire is a trademark of National Semiconductor Corp.



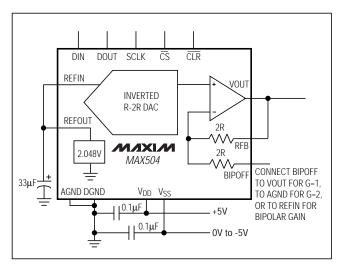


Figure 3a. MAX504 Typical Operating Circuit

Daisy-Chaining Devices

The serial output, DOUT, allows cascading of two or more DACs. The data at DIN appears at DOUT, delayed by 16 clock cycles plus one clock width. For low power, DOUT is a CMOS output that does not require an external pull-up resistor. DOUT does **not** go into a high-impedance state when $\overline{\text{CS}}$ is high. DOUT changes on SCLK's falling edge when $\overline{\text{CS}}$ is low. When $\overline{\text{CS}}$ is high, DOUT remains in the state of the last data bit.

Any number of MAX504/MAX515 DACs can be daisy-chained by connecting the DOUT of one device to the DIN of the next device in the chain. For proper timing, ensure that t_{CL} (SCLK low) is greater than t_{DO} + t_{DS} .

Unipolar Configuration

The MAX504 is configured for a gain of 1 (0V to VREFIN unipolar output) by connecting BIPOFF and RFB to VOUT (Figure 6). The converter operates from either single or dual supplies in this configuration. See Table 1 for the DAC-latch contents (input) vs. the analog VOUT (output). In this range, 1LSB = VREFIN ($^{2-10}$), where VREF is the voltage on REFIN.

A gain of 2 (0V to 2V_{REFIN} unipolar output) is set up by connecting BIPOFF to AGND and RFB to VOUT (Figure 7). Table 2 shows the DAC-latch contents vs. VOUT. The MAX504 operates from either single or dual supplies in this mode. In this range,

 $1LSB = (2)(V_{REFIN})(2^{-10}) = (V_{REFIN})(2^{-9}).$

The MAX515 is internally configured for unipolar gain of 2 operation.

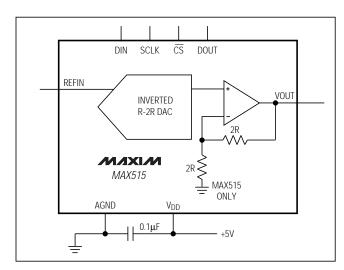


Figure 3b. MAX515 Typical Operating Circuit

Bipolar Configuration

A bipolar range is set up by connecting BIPOFF to REFIN and RFB to VOUT, and operating from dual $(\pm 5V)$ supplies (Figure 8). Table 3 shows the DAC-latch contents (input) vs. VOUT (output). In this range, 1LSB = V_{REFIN} (2 -9).

Four-Quadrant Multiplication

The MAX504 can be used as a four-quadrant multiplier by connecting BIPOFF to REFIN and RFB to VOUT, and using (1) an offset binary digital code, (2) bipolar power supplies, and (3) a bipolar analog input at REFIN within the range Vss + 2V to Vpd - 2V, as shown in Figure 9.

In general, a 10-bit DAC's output is (D)(VREFIN)(G), where "G" is the gain (1 or 2) and "D" is the binary representation of the digital input divided by 2^{10} or 1,024. This formula is precise for unipolar operation. However, for bipolar, offset binary operation, the MSB is really a polarity bit. No resolution is lost because the number of steps is the same. The output voltage, however, has been shifted from a range of, for example, 0V to 4.096V (G = 2) to a range of -2.048V to +2.048V.

Keep in mind that when using the DAC as a four-quadrant multiplier, the scale is skewed. Negative full scale is -V_{REFIN}, while positive full scale is +V_{REFIN} - 1LSB.

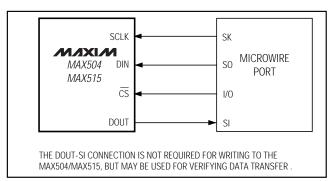


Figure 4. Microwire Connection

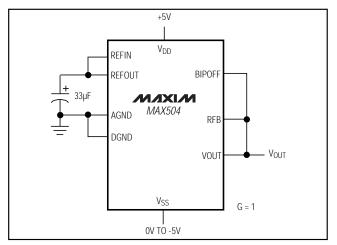


Figure 6. Unipolar Configuration (0V to +2.048V Output)

Table 1. Unipolar Binary Code Table (0V to VREFIN Output), Gain = 1

	INPUT	*	OUTPUT
1111	1111	11(00)	(V _{REFIN}) $\frac{1023}{1024}$
1000	0000	01(00)	(V _{REFIN}) $\frac{513}{1024}$
1000	0000	00(00)	$(V_{REFIN}) \frac{512}{1024} = +V_{REFIN}/2$
0111	1111	11(00)	(V _{REFIN}) 511 1024
0000	0000	01(00)	(V _{REFIN}) 1/1024
0000	0000	00(00)	OV

^{*} Write 10-bit data words with two sub-LSB 0s because the DAC input latch is 12 bits wide.

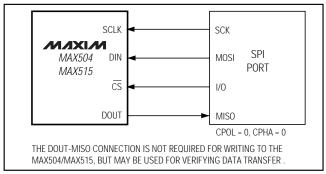


Figure 5. SPI/QSPI Connection

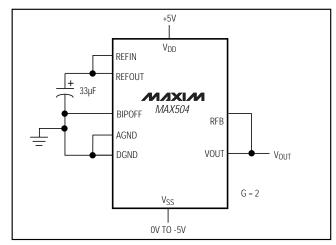


Figure 7. Unipolar Configuration (0V to +4.096V Output)

Table 2. Unipolar Binary Code Table (0V to 2VREFIN Output), Gain = 2

	INPUT	*	OUTPUT
1111	1111	11(00)	+2 (V _{REFIN}) $\frac{1023}{1024}$
1000	0000	01(00)	+2 (V _{REFIN}) $\frac{513}{1024}$
1000	0000	00(00)	+2 (V _{REFIN}) $\frac{512}{1024}$ = +V _{REFIN}
0111	1111	11(00)	+2 (V _{REFIN}) $\frac{511}{1024}$
0000	0000	01(00)	+2 (V _{REFIN}) 1/1024
0000	0000	00(00)	OV

^{*} Write 10-bit data words with two sub-LSB 0s because the DAC input latch is 12 bits wide.

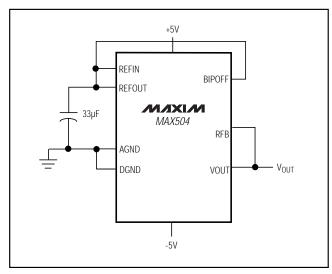


Figure 8. Bipolar Configuration (-2.048V to +2.048V Output)

Single-Supply Linearity

As with any amplifier, the MAX504/MAX515's output buffer offset can be positive or negative. When the offset is positive, it is easily accounted for (Figure 10). However, when the offset is negative, the buffer output cannot follow linearly when there is no negative supply. In that case, the amplifier output (VOUT) remains at ground until the DAC voltage is sufficient to overcome the offset and the output becomes positive.

Normally, linearity is measured after accounting for zero error and gain error. Since, in single-supply operation, the actual value of a negative offset is unknown, it cannot be accounted for during test. Additionally, the output buffer amplifier exhibits a nonlinearity near-zero output when operating with a single supply. To account for this nonlinearity in the MAX504/MAX515, linearity and gain error are measured from code 3 to code 1023. The output buffer's offset and nonlinearity do not affect monotonicity, and these DACs are guaranteed monotonic starting with code zero. In dual-supply operation, linearity and gain error are measured from code 0 to 1023.

Power-Supply Bypassing and Ground Management

Best system performance is obtained with printed circuit boards that use separate analog and digital ground planes. Wire-wrap boards are not recommended. The two ground planes should be connected together at the low-impedance power-supply source.

Table 3. Bipolar (Offset Binary) Code Table (-VREFIN to +VREFIN Output)

	INPUT	*	OUTPUT
1111	1111	11(00)	(+V _{REFIN}) 511 512
1000	0000	01(00)	(+V _{REFIN}) 1/512
1000	0000	00(00)	OV
0111	1111	11(00)	(-V _{REFIN}) 1/512
0000	0000	01(00)	(-V _{REFIN}) 511 512
0000	0000	00(00)	$(-V_{REFIN}) \frac{512}{512} = -V_{REFIN}$

^{*} Write 10-bit data words with two sub-LSB 0s because the DAC input latch is 12 bits wide.

DGND and AGND should be connected together at the chip. For the MAX504 in single-supply applications, connect Vss to AGND at the chip. The best ground connection may be achieved by connecting the DAC's DGND and AGND pins together and connecting that point to the system analog ground plane. If the DAC's DGND is connected to the system digital ground, digital noise may get through to the DAC's analog portion.

Bypass V_{DD} (and V_{SS} in dual-supply mode) with a 0.1 μ F ceramic capacitor connected between V_{DD} and AGND (and between V_{SS} and AGND). Mount it with short leads close to the device. Ferrite beads may also be used to further isolate the analog and digital power supplies.

Figures 11a and 11b illustrate the grounding and bypassing scheme described.

Saving Power

When the DAC is not being used by the system, minimize power consumption by setting the appropriate code to minimize load current. For example, in bipolar mode, with a resistive load to ground, set the DAC code to mid-scale (see Table 3). If there is no output load, minimize internal loading on the reference by setting the DAC to all 0s (on the MAX504, use CLR). Under this condition, REFIN is high impedance and the op amp operates at its minimum quiescent current.

Due to these low currents, the output settling time for a zero input code typically increases to $60\mu s$ ($100\mu s$ max).

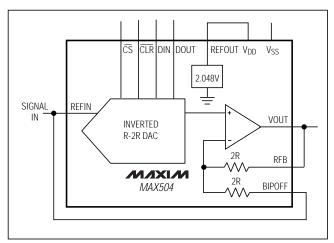


Figure 9. MAX504 Connected as Four-Quadrant Multiplier. The unused REFOUT is connected to V_{DD} .

AC Considerations

Digital Feedthrough

High-speed serial data at any of the digital input or output pins may couple through the DAC package and cause internal stray capacitance to appear at the DAC output as noise, even though $\overline{\text{CS}}$ is held high (see *Typical Operating Characteristics*). This digital feedthrough is tested by holding $\overline{\text{CS}}$ high transmitting 0101... from DIN to DOUT.

Analog Feedthrough

Because of internal stray capacitance, higher frequency analog input signals may couple to the output as shown in the Analog Feedthrough vs. Frequency graph in the *Typical Operating Characteristics*. It is tested by holding CS high, setting the DAC code to all 0s, and sweeping REFIN.

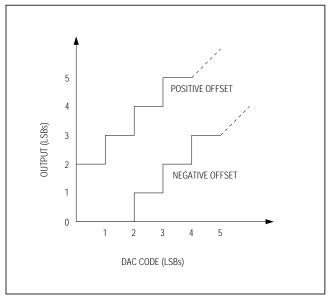


Figure 10. Single-Supply Offset

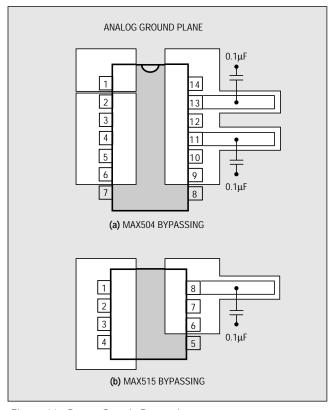
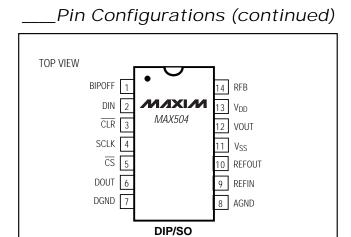


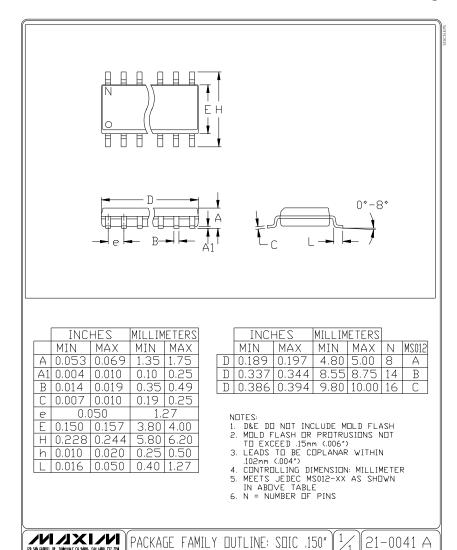
Figure 11. Power-Supply Bypassing



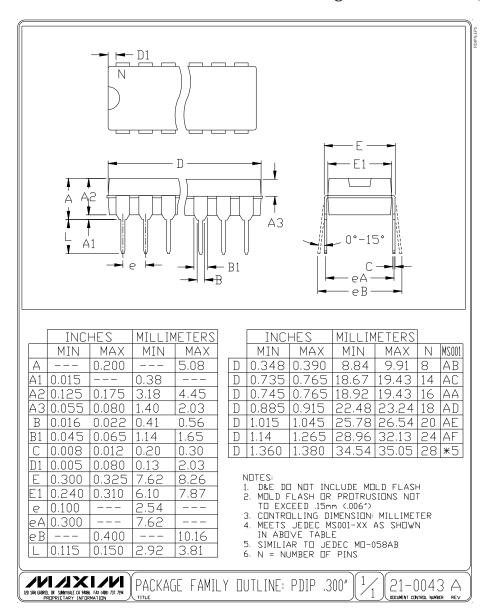
_____Chip Information
TRANSISTOR COUNT: 922

21-0041 A

Package Information



_Package Information (continued)



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