

NB3V110xC Series

3.3V/2.5V/1.8V LVCMOS Low Skew Fanout Buffer Family

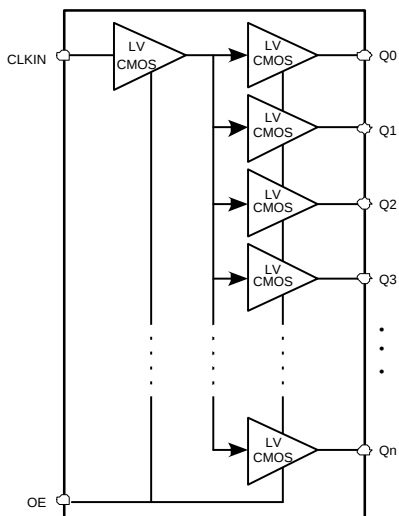
Description

The NB3V110xC are a modular, high-performance, low-skew, general purpose LVCMOS clock buffer family. The family of devices is designed with a modular approach. Four different fan-out variations, 1:2, 1:3, 1:4, 1:6 and 1:8, are available. All of the devices are pin compatible to each other for easy handling. All family members share the same high performing characteristics like low additive jitter, low skew, and wide operating temperature range. The NB3V110xC supports an asynchronous output enable control (OE) which switches the outputs into a low state when OE is low. The NB3V110xC devices operate in a 3.3 V, 2.5 V and 1.8 V environment and are characterized for operation from -40°C to 105°C.

Features

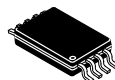
- Operating Temperature Range: -40°C to 105°C
- High-Performance 1:2, 1:3, 1:4, 1:6, 1:8 LVCMOS Clock Buffer
- Available in 8-, 14-, 16-Pin TSSOP and WDFN8 Packages
- Very Low Output-to-Output Skew < 50 ps
- Very Low Additive Jitter < 200 fs
- Supply Voltage: 3.3 V, 2.5 V or 1.8 V
- $f_{\max} = 250$ MHz for 3.3 V; $f_{\max} = 180$ MHz for 2.5 V;
 $f_{\max} = 133$ MHz for 1.8 V
- These Devices are Pb-Free and are RoHS Compliant

BLOCK DIAGRAM



ON Semiconductor®

www.onsemi.com



TSSOP-8
DT SUFFIX
CASE 948S



TSSOP-14
DT SUFFIX
CASE 948G

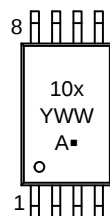


TSSOP-16
DT SUFFIX
CASE 948F

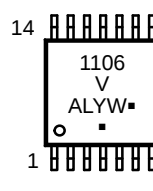


WDFN8, 2x2
MT SUFFIX
CASE 511AT

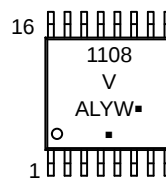
MARKING DIAGRAMS



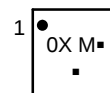
TSSOP-8



TSSOP-14



TSSOP-16



WDFN8

A = Assembly Location
M = Date Code
L = Wafer Lot
Y = Year
W, WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 9 of this data sheet.

NB3V110xC Series

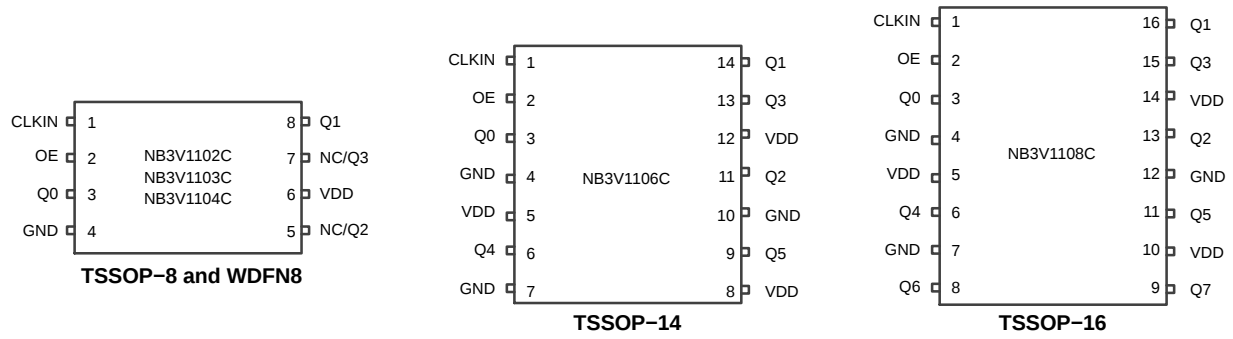


Figure 1. Pin Configuration

Table 1. PIN DESCRIPTION

	LVC MOS Clock Input	LVC MOS Clock Output Enable	LVC MOS Clock Output	Device Supply Voltage	Device Ground
Devices	CLKIN	OE	Q0, Q1, ... Q7	V _{DD}	GND
NB3V1102C	1	2	3, 8	6	4
NB3V1103C	1	2	3, 8, 5	6	4
NB3V1104C	1	2	3, 8, 5, 7	6	4
NB3V1106C	1	2	3, 14, 11, 13, 6, 9	5, 8, 12	4, 7, 10
NB3V1108C	1	2	3, 16, 13, 15, 6, 11, 8, 9	5, 10, 14	4, 7, 12

NOTE: Pins not mentioned in the table are NC.

Table 2. OUTPUT LOGIC TABLE

INPUTS		OUTPUTS
CLKIN	OE	Q _n
X	L	L
L	H	L
H	H	H

Table 3. ATTRIBUTES

Characteristic	Value	Unit
ESD Protection	Human Body Model (HBM) per ANSI/ESDA/JEDEC JS-001-2014 Charged Device Model (CDM) per ANSI/ESDA/JEDEC JS-002-2014	5000 1500 V V
Moisture Sensitivity, Indefinite Time Out of Dry Pack (Note 1)	Level 1	–
Meets or exceeds JEDEC Spec JESD78D (LU) IC Latchup Test		

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with a large copper heat spreader (20 mm², 2 oz.)

NB3V110xC Series

Table 4. ABSOLUTE MAXIMUM RATINGS (Note 2)
Over operating free-air temperature range (unless otherwise noted)

Symbol	Condition		Value	Unit
V_{DD}	Supply Voltage Range		–0.5 to 4.6	V
V_{IN}	Input Voltage Range (Note 3)		–0.5 to $V_{DD} + 0.5$	V
V_O	Output Voltage Range (Note 3)		–0.5 to $V_{DD} + 0.5$	V
I_{IN}	Input Current		± 20	mA
I_O	Continuous Output Current		± 50	mA
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	TSSOP–8	151.2*	°C/W
		TSSOP–14	104*	
		TSSOP–16	32*	
			110**	
		WDFN8	190**	
θ_{JC}	Thermal Resistance (Junction-to-Case top)	TSSOP–8	35	°C/W
		TSSOP–14	8.6	
		TSSOP–16	10	
		WDFN8	10	
T_J	Maximum Junction Temperature		125	°C
T_{STG}	Storage Temperature Range		–65 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with a large copper heat spreader (20 mm², 2 oz.)

3. For additional information, see Application Note AND8003/D.

*JEDEC51.7 four layer PCB with 100 sqmm, 2 oz with two 80x80x1oz ground planes.

**JEDEC51.3 two layer PCB with 100 sqmm, 2 oz.

NB3V110xC Series

Table 5. RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

Symbol	Condition		Min	Typ	Max	Unit
V _{DD}	Supply voltage range	3.3 V supply	3.0	3.3	3.6	V
		2.5 V supply	2.3	2.5	2.7	
		1.8 V supply	1.71	1.8	1.89	
V _{IL}	Low-level input voltage	V _{DD} = 3.0 V to 3.6 V			V _{DD} /2 – 600	mV
		V _{DD} = 2.3 V to 2.7 V			V _{DD} /2 – 400	
		V _{DD} = 1.71 V to 1.89 V			0.3xV _{DD}	V
V _{IH}	High-level input voltage	V _{DD} = 3.0 V to 3.6 V	V _{DD} /2 + 600			mV
		V _{DD} = 2.3 V to 2.7 V	V _{DD} /2 + 400			
		V _{DD} = 1.71 V to 1.89 V	0.7xV _{DD}			V
V _{th}	Input threshold voltage	V _{DD} = 2.3 V to 3.6 V	V _{DD} /2			V
		V _{DD} = 1.71 V to 1.89 V	V _{DD} /2			V
t _r / t _f	Input slew rate (Note 4)		1		4	V/ns
t _w	Minimum pulse width at CLKIN	V _{DD} = 3.0 V to 3.6 V	1.8			ns
		V _{DD} = 2.3 V to 2.7 V	2.75			
		V _{DD} = 1.71 V to 1.89 V	3.75			
f _{CLK}	LVCMOS clock Input Frequency	V _{DD} = 3.0 V to 3.6 V	DC		250	MHz
		V _{DD} = 2.3 V to 2.7 V	DC		180	
		V _{DD} = 1.71 V to 1.89 V	DC		133	
T _A	Operating free-air temperature		–40		105	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Guaranteed by Design.

NB3V110xC Series

Table 6. DEVICE CHARACTERISTICS Over recommended operating free-air temperature range (unless otherwise noted) (Note 5)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
OVERALL PARAMETERS FOR ALL VERSIONS						
I_{DD}	Static device current	OE = V_{DD} ; CLKIN = 0 V or V_{DD} ; I_O = 0 mA; V_{DD} = 3.6 V			0.2	mA
		OE = V_{DD} ; CLKIN = 0 V or V_{DD} ; I_O = 0 mA; V_{DD} = 2.7 V			0.2	
		OE = V_{DD} ; CLKIN = 0 V or V_{DD} ; I_O = 0 mA; V_{DD} = 1.89 V			0.2	
I_{PD}	Power down current	OE = 0 V; CLKIN = 0 V or V_{DD} ; I_O = 0 mA; V_{DD} = 3.6 V, 2.7 V or 1.89 V (For 1102C, 1103C, 1104C)			60	μ A
		OE = 0 V; CLKIN = 0 V or V_{DD} ; I_O = 0 mA; V_{DD} = 3.6 V, 2.7 V or 1.89 V (For 1106C, 1108C)			75	
C_{PD}	Power dissipation capacitance per output (Note 6)	V_{DD} = 3.3 V; f = 10 MHz		9		pF
		V_{DD} = 2.5 V; f = 10 MHz		9		
		V_{DD} = 1.8 V; f = 10 MHz		9		
I_I	Input leakage current at OE	V_I = 0 V or V_{DD} , V_{DD} = 3.6 V or 2.7 V			± 8	μ A
	Input leakage current at CLKIN				± 8	
	Input leakage current at OE, CLKIN	V_I = 0 V or V_{DD} , V_{DD} = 1.89 V			± 8	
R_{OUT}	Output impedance	V_{DD} = 3.3 V		40		Ω
		V_{DD} = 2.5 V		45		
		V_{DD} = 1.8 V		60		
f_{OUT}	Output frequency	V_{DD} = 3.0 V to 3.6 V	DC		250	MHz
		V_{DD} = 2.3 V to 2.7 V	DC		180	
		V_{DD} = 1.71 V to 1.89 V	DC		133	

OUTPUT PARAMETERS FOR $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$

V_{OH}	High-level output voltage	$V_{DD} = 3 \text{ V}$, $I_{OH} = -0.1 \text{ mA}$	2.9			V
		$V_{DD} = 3 \text{ V}$, $I_{OH} = -8 \text{ mA}$	2.5			
		$V_{DD} = 3 \text{ V}$, $I_{OH} = -12 \text{ mA}$	2.2			
V_{OL}	Low-level output voltage	$V_{DD} = 3 \text{ V}$, $I_{OL} = 0.1 \text{ mA}$			0.1	V
		$V_{DD} = 3 \text{ V}$, $I_{OL} = 8 \text{ mA}$			0.5	
		$V_{DD} = 3 \text{ V}$, $I_{OL} = 12 \text{ mA}$			0.8	
t_{PLH}, t_{PHL}	Propagation delay (Note 7)	CLKIN to Qn	0.8		2.0	ns
$t_{sk(o)}$	Output skew (Note 7)	Equal load of each output 85°C			50	ps
		Equal load of each output 105°C			60	
t_r/t_f	Rise and fall time	20%–80% ($V_{OH} - V_{OL}$)	0.12		0.8	ns
t_{DIS}	Output disable time (Note 7)	OE to Qn			6	ns
t_{EN}	Output enable time (Note 7)	OE to Qn			6	ns
$t_{sk(p)}$	Pulse skew; $t_{PLH(Qn)} - t_{PHL(Qn)}$ (Note 8)	To be measured with input duty cycle of 50%			180	ps
$t_{sk(pp)}$	Part-to-part skew	Under equal operating conditions for two parts			0.5	ns
$T_{jit(\phi)}$	Additive jitter rms	12 kHz...20 MHz $f_{OUT} = 100 \text{ MHz}$			100	fs
		12 kHz...20 MHz $f_{OUT} = 156.25 \text{ MHz}$				

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. All typical values are at respective nominal V_{DD} . For switching characteristics, outputs are terminated to 50 Ω to $V_{DD}/2$ (see Figure 2).

6. This is the formula for the power dissipation calculation.

$$P_{tot} = P_{stat} + P_{dyn} + P_{Cload} \text{ [W]} \quad P_{stat} = V_{DD} \times I_{DD} \text{ [W]}$$

$$P_{dyn} = C_{PD} \times V_{DD}^2 \times f \times n \text{ [W]}$$

$$P_{Cload} = C_{load} \times V_{DD}^2 \times f \times n \text{ [W]}$$

n = Number of switching output pins

7. With rail to rail input clock.

8. $t_{sk(p)}$ depends on output rise- and fall-time (t_r/t_f). The output duty-cycle can be calculated: $odc = (t_{w(OUT)} \pm t_{sk(p)})/t_{period}$; $t_{w(OUT)}$ is pulse-width of ideal output waveform and period is $1/f_{OUT}$.

NB3V110xC Series

Table 7. DEVICE CHARACTERISTICS (continued)

Over recommended operating free-air temperature range (unless otherwise noted) (Note 5)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
OUTPUT PARAMETERS FOR $V_{DD} = 2.5 \text{ V} \pm 0.2 \text{ V}$						
V_{OH}	High-level output voltage	$V_{DD} = 2.3 \text{ V}$, $I_{OH} = -0.1 \text{ mA}$	2.2			V
		$V_{DD} = 2.3 \text{ V}$, $I_{OH} = -8 \text{ mA}$	1.7			
V_{OL}	Low-level output voltage	$V_{DD} = 2.3 \text{ V}$, $I_{OL} = 0.1 \text{ mA}$			0.1	V
		$V_{DD} = 2.3 \text{ V}$, $I_{OL} = 8 \text{ mA}$			0.5	
t_{PLH} , t_{PHL}	Propagation delay (Note 10)	CLKIN to Qn		1.8		ns
$t_{sk(o)}$	Output skew (Note 10)	Equal load of each output 85°C			50	ps
		Equal load of each output 105°C			60	
t_r/t_f	Rise and fall time	20%–80% ($V_{OH} - V_{OL}$)	0.12		1.2	ns
t_{DIS}	Output disable time (Note 10)	OE to Qn			10	ns
t_{EN}	Output enable time (Note 10)	OE to Qn			10	ns
$t_{sk(p)}$	Pulse skew ; $t_{PLH(Qn)} - t_{PHL(Qn)}$ (Note 9)	To be measured with input duty cycle of 50%			220	ps
$t_{sk(pp)}$	Part-to-part skew	Under equal operating conditions for two parts			1.2	ns
$t_{jit(\phi)}$	Additive jitter rms	12 kHz...20 MHz $f_{OUT} = 100 \text{ MHz}$			150	fs
		12 kHz...20 MHz $f_{OUT} = 156.25 \text{ MHz}$			100	

OUTPUT PARAMETERS FOR $V_{DD} = 1.8 \text{ V} \pm 5\%$

V_{OH}	High-level output voltage	$V_{DD} = 1.71 \text{ V}$, $I_{OH} = -0.1 \text{ mA}$	1.6			V
		$V_{DD} = 1.71 \text{ V}$, $I_{OH} = -4 \text{ mA}$	$0.75 \times V_{DD}$			
V_{OL}	Low-level output voltage	$V_{DD} = 1.71 \text{ V}$, $I_{OL} = 0.1 \text{ mA}$			0.1	V
		$V_{DD} = 1.71 \text{ V}$, $I_{OL} = 4 \text{ mA}$			$0.25 \times V_{DD}$	
t_{PLH} , t_{PHL}	Propagation delay (Note 10)	CLKIN to Qn	1.8		3.5	ns
$t_{sk(o)}$	Output skew (Note 10)	Equal load of each output			75	ps
t_r/t_f	Rise and fall time	20%–80% ($V_{OH} - V_{OL}$)	0.17		1.2	ns
t_{DIS}	Output disable time (Note 10)	OE to Qn			10	ns
t_{EN}	Output enable time (Note 10)	OE to Qn			10	ns
$t_{sk(p)}$	Pulse skew ; $t_{PLH(Qn)} - t_{PHL(Qn)}$ (Note 9)	To be measured with input duty cycle of 50%			450	ps
$t_{sk(pp)}$	Part-to-part skew	Under equal operating conditions for two parts			1.2	ns
$t_{jit(\phi)}$	Additive jitter rms	12 kHz...20 MHz, $f_{OUT} = 100 \text{ MHz}$			200	fs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

9. $t_{sk(p)}$ depends on output rise- and fall-time (t_r/t_f). The output duty-cycle can be calculated: $odc = (t_{w(OUT)} \pm t_{sk(p)})/t_{period}$; $t_{w(OUT)}$ is pulse-width of ideal output waveform and t_{period} is $1/f_{OUT}$.

10. With rail to rail input clock.

NB3V110xC Series

PARAMETERS MEASUREMENT INFORMATION

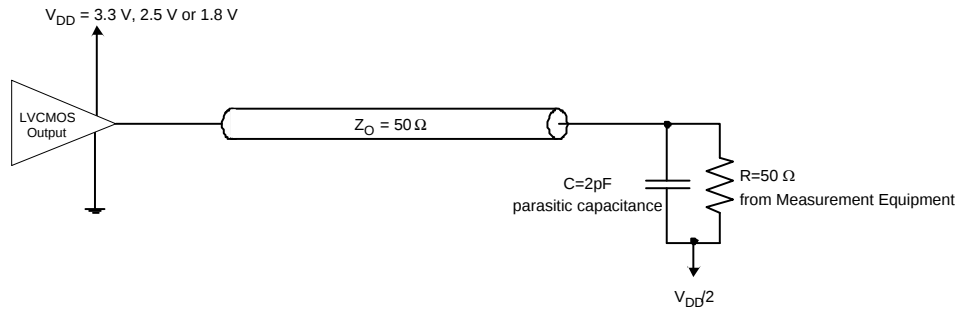


Figure 2. Test Load Circuit

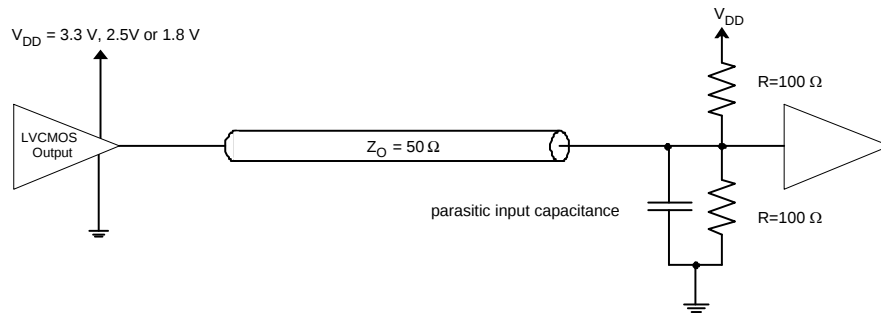


Figure 3. Application Load with $50\ \Omega$ Line Termination

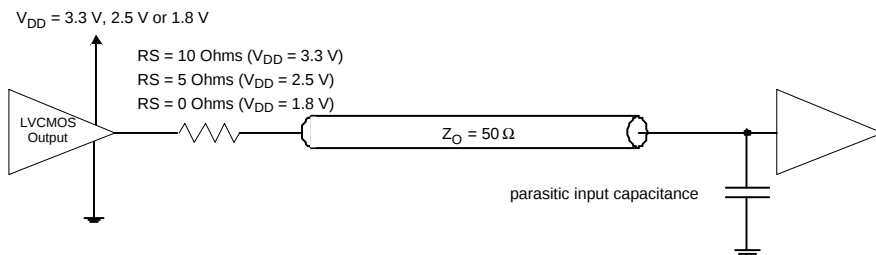


Figure 4. Application Load with Series Line Termination

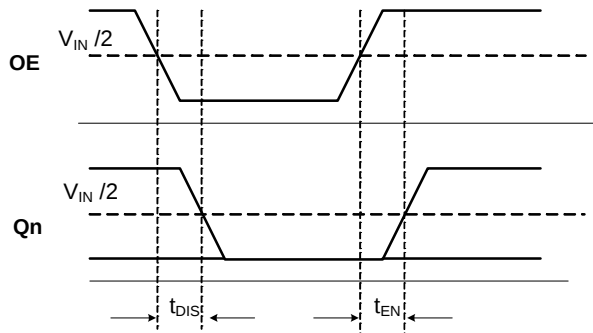


Figure 5. t_{DIS} and t_{EN} for Disable Low

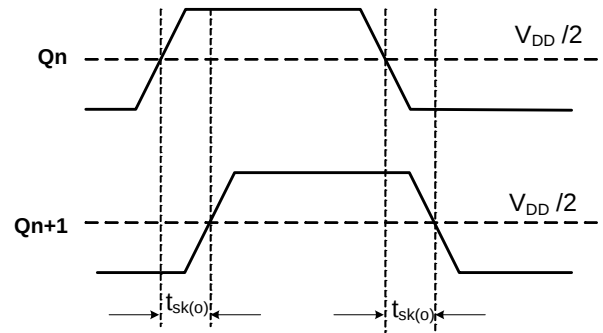


Figure 6. Output Skew $t_{sk(o)}$

NB3V110xC Series

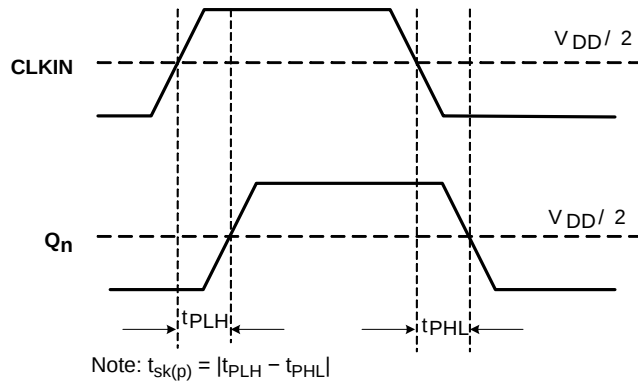


Figure 7. Pulse Skew $t_{sk(p)}$ and Propagation Delay t_{PLH}/t_{PHL}

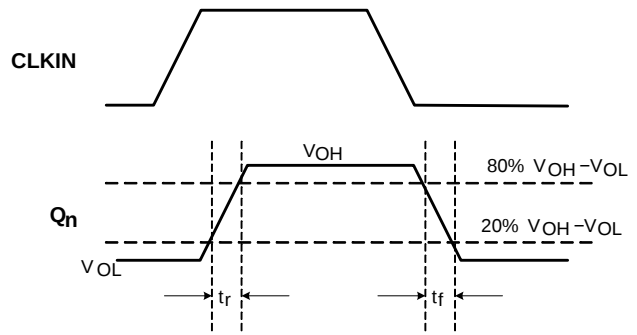


Figure 8. Rise/Fall Times t_r / t_f

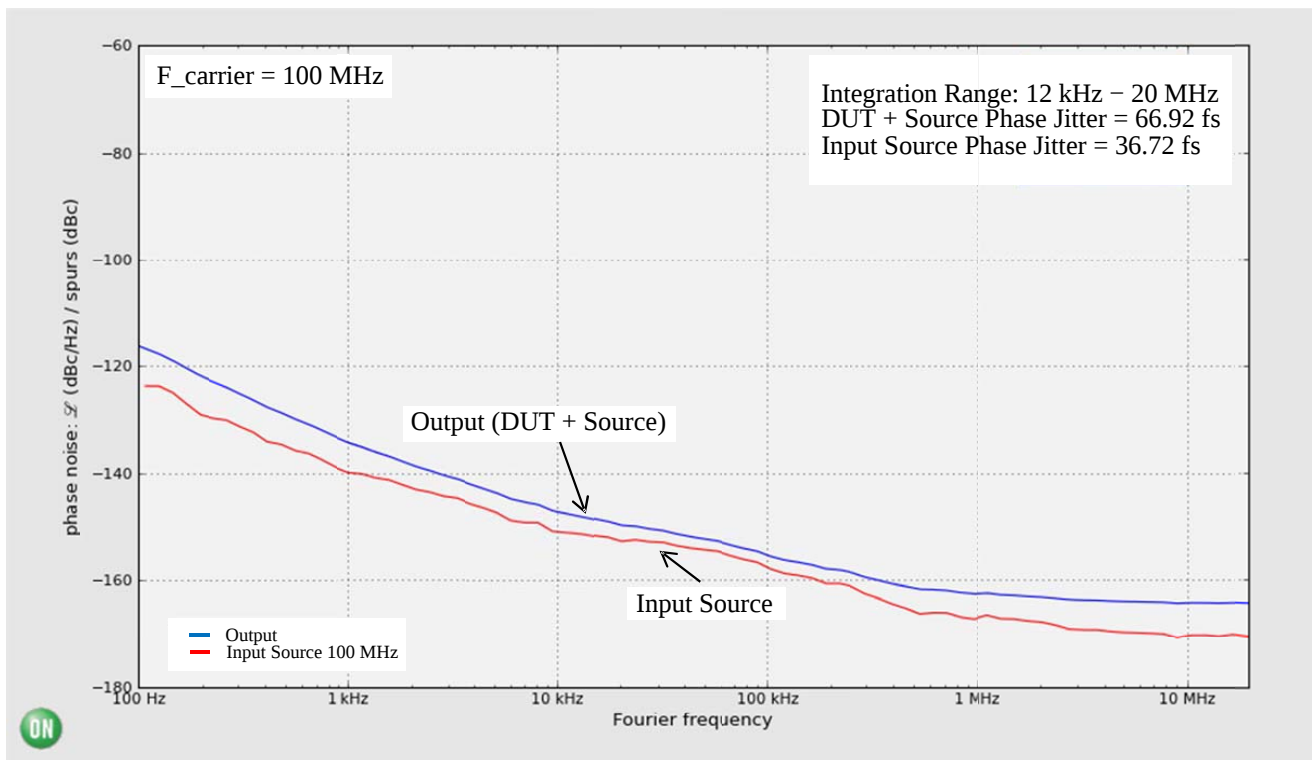


Figure 9. Typical NB3V110xC Phase Noise Plot at $f_{Carrier} = 100$ MHz, $V_{DD} = 3.3$ V, 25°C

The above phase noise data was captured using Agilent E5052A/B. The data displays the input phase noise and output phase noise used to calculate the additive phase jitter at a specified integration range. The additive RMS phase jitter contributed by the device (integrated between 12 kHz and 20 MHz) is 55.94 fs. The additive RMS phase jitter performance of the fan out buffer is highly dependent on the phase noise of the input source.

To obtain the most precise additive phase noise measurement, it is vital that the source phase noise be notably lower than that of the DUT. If the phase noise of the source is greater than the noise floor of the device under test, the source noise will dominate the additive phase jitter calculation and lead to an incorrect negative result for the additive phase noise within the integration range. The Figure above is a good example of the NB3V110xC source generator phase noise having a significantly lower floor than the DUT and results in an additive phase jitter of 55.94 fs.

$$\text{Additive RMS phase jitter} = \sqrt{\text{RMS phase jitter of output}^2 - \text{RMS phase jitter of input}^2}$$

$$55.94 \text{ fs} = \sqrt{66.92 \text{ fs}^2 - 36.72 \text{ fs}^2}$$

NB3V110xC Series

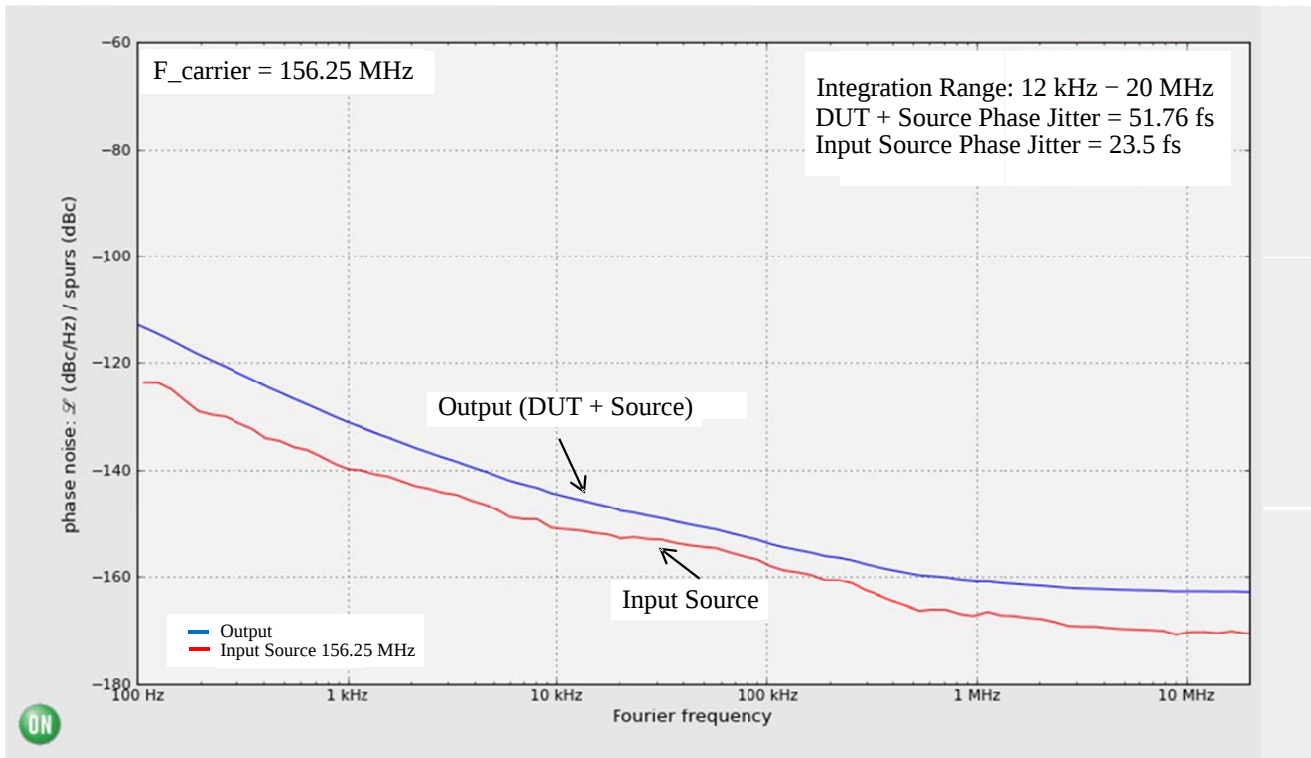


Figure 10. Typical NB3V110xC Phase Noise Plot at $f_{\text{carrier}} = 156.25 \text{ MHz}$, $V_{\text{CC}} = 3.3 \text{ V V}$, 25°C

The additive RMS phase jitter contributed by the device (integrated between 12 kHz and 20 MHz) is 46.11 fs.

$$\begin{aligned} \text{Additive RMS phase jitter} &= \sqrt{\text{RMS phase jitter of output}^2 - \text{RMS phase jitter of input}^2} \\ 46.11 \text{ fs} &= \sqrt{51.76 \text{ fs}^2 - 23.5 \text{ fs}^2} \end{aligned}$$

Figures 9 and 10 were created with measured data from Agilent-E5052A/B Signal Source Analyzer using ON Semiconductor Phase Noise Explorer web tool. This free application enables an interactive environment for advanced

phase noise and jitter analysis of timing devices and clock tree designs. To see the performance of NB3V110xC beyond conditions outlined in this datasheet, please visit the ON Semiconductor [Green Point Design Tools](#) homepage.

Table 8. ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NB3V1102CDTR2G	102	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
NB3V1103CDTR2G	103		
NB3V1104CDTR2G	104		
NB3V1102CMTTBG	02	WDFN8 (Pb-Free)	3000 / Tape & Reel
NB3V1104CMTTBG	04		
NB3V1106CDTR2G	1106 V	TSSOP-14 (Pb-Free)	2500 / Tape & Reel
NB3V1108CDTR2G	1108 V	TSSOP-16 (Pb-Free)	2500 / Tape & Reel

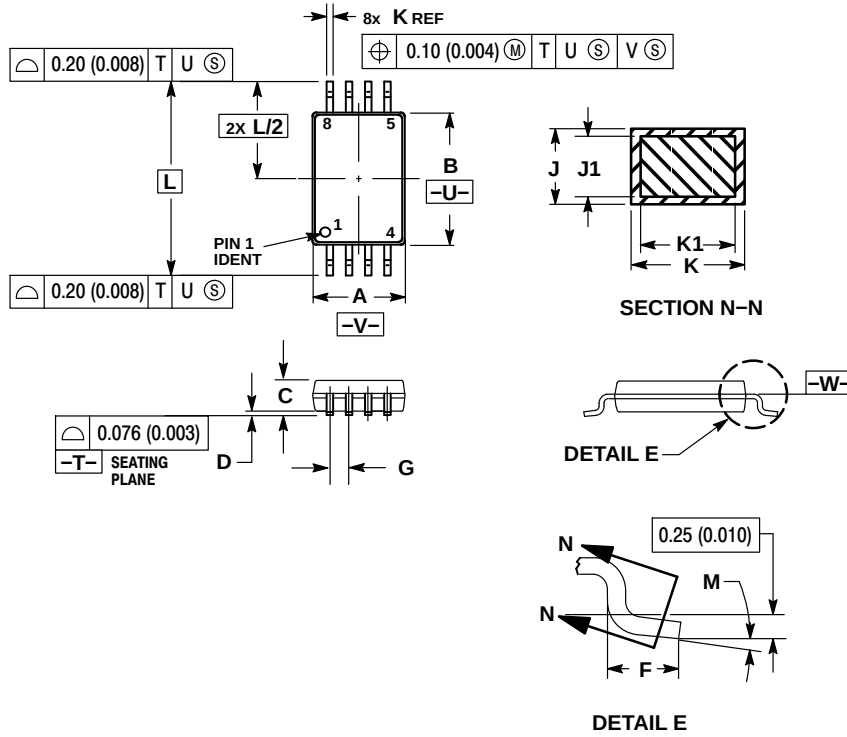
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NOTE: Please contact your ON Semiconductor sales representative for availability of parts in tube.

NB3V110xC Series

PACKAGE DIMENSIONS

TSSOP-8
CASE 948S
ISSUE C



NOTES:

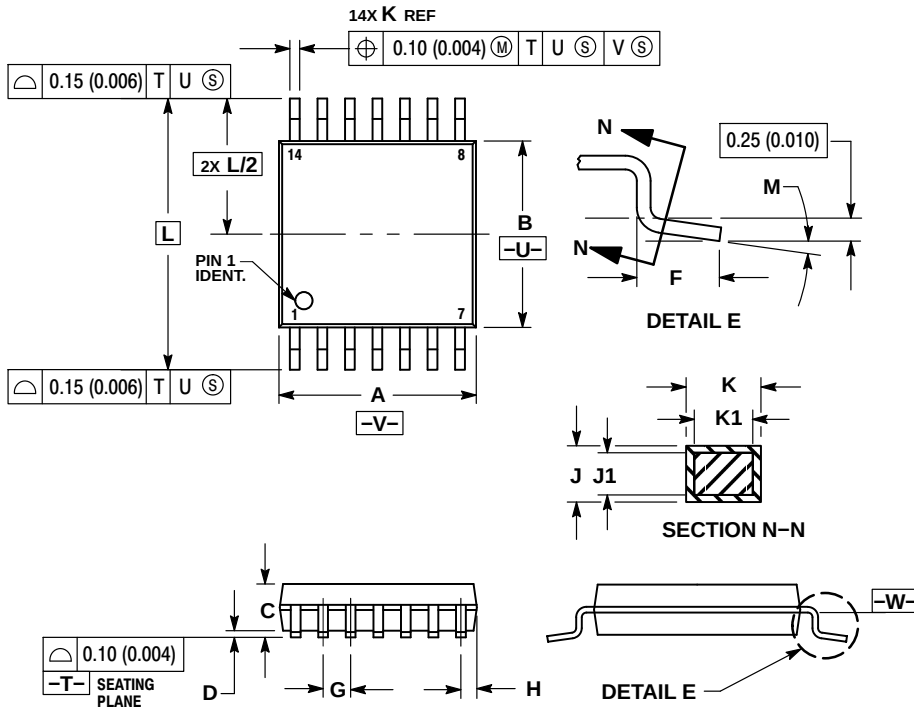
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	4.30	4.50	0.169	0.177
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.70	0.020	0.028
G	0.65 BSC		0.026 BSC	
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

NB3V110xC Series

PACKAGE DIMENSIONS

TSSOP-14 CASE 948G ISSUE B

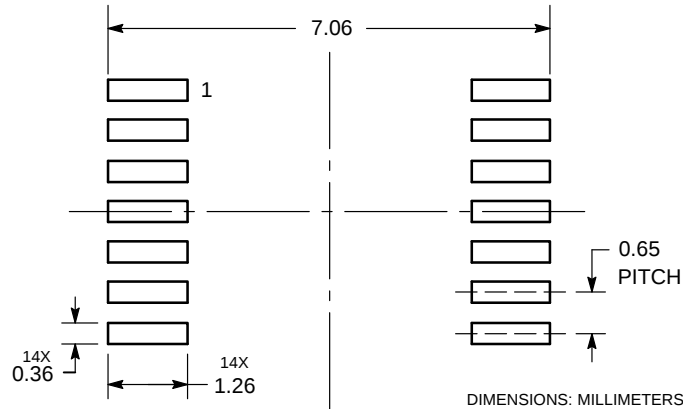


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

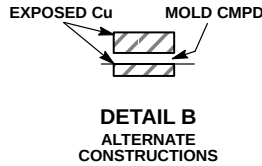
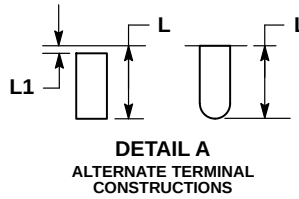
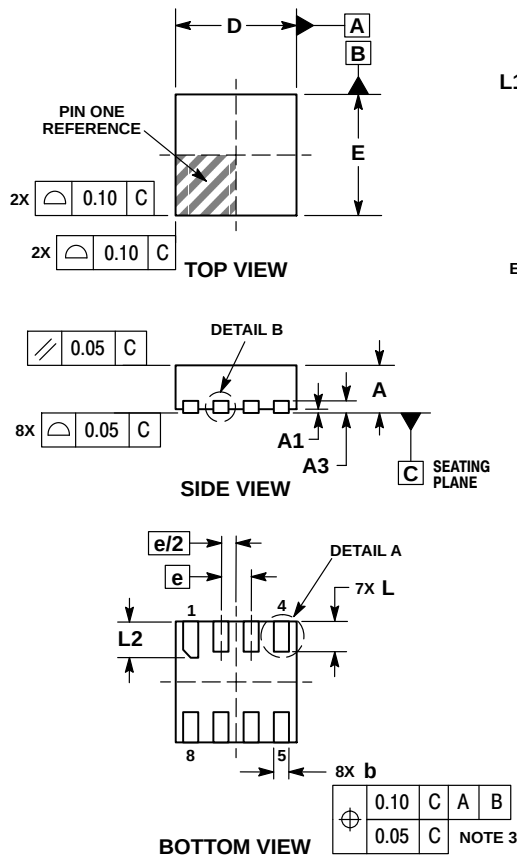
SOLDERING FOOTPRINT*



NB3V110xC Series

PACKAGE DIMENSIONS

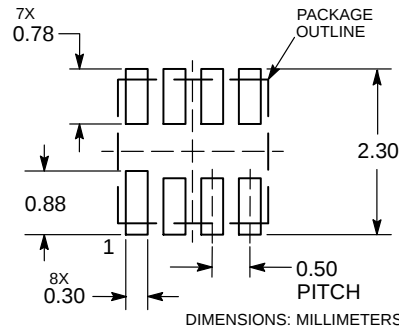
WDFN8 2x2, 0.5P
CASE 511AT
ISSUE O



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.

DIM	MILLIMETERS	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
E	2.00 BSC	
e	0.50 BSC	
L	0.40	0.60
L1	---	0.15
L2	0.50	0.70

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marketing.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

moschip.ru_4

moschip.ru_6

moschip.ru_9