Quad, 16-Bit, 2.4 GSPS, TxDAC+® Digital-to-Analog Converter

Data Sheet **AD9154**

FEATURES

- Supports input data rates up to 1 GSPS
- Proprietary, low spurious and distortion design
  - Single carrier LTE 20 MHz bandwidth (BW), ACLR = 77 dBc at 180 MHz IF
  - Six carrier GSM IMD = 78 dBc, 600 kHz carrier spacing at 180 MHz IF
  - SFDR = 72 dBc at 180 MHz IF, −6 dBFS single tone
- Flexible 8-lane JESD204B interface
- Multiple chip synchronization
  - Fixed latency
  - Data generator latency compensation
- Input signal power detection
- High performance, low noise phase-locked loop (PLL) clock multiplier
- Digital inverse sinc filter
- Digital quadrature modulation using a numerically controlled oscillator (NCO)
- Nyquist band selection—mix mode
- Selectable 1×, 2×, 4×, and 8× interpolation filters
- Low power: 2.11 W at 1.6 GSPS, full operating conditions
- 88-lead, exposed pad LFCSP

APPLICATIONS

- Wireless communications
  - Multicarrier LTE and GSM base stations
  - Wideband repeaters
  - Software defined radios
- Wideband communications
  - Point to point microwave radio
- Transmit diversity, multiple input/multiple output (MIMO)
- Instrumentation
- Automated test equipment

FUNCTIONAL BLOCK DIAGRAM

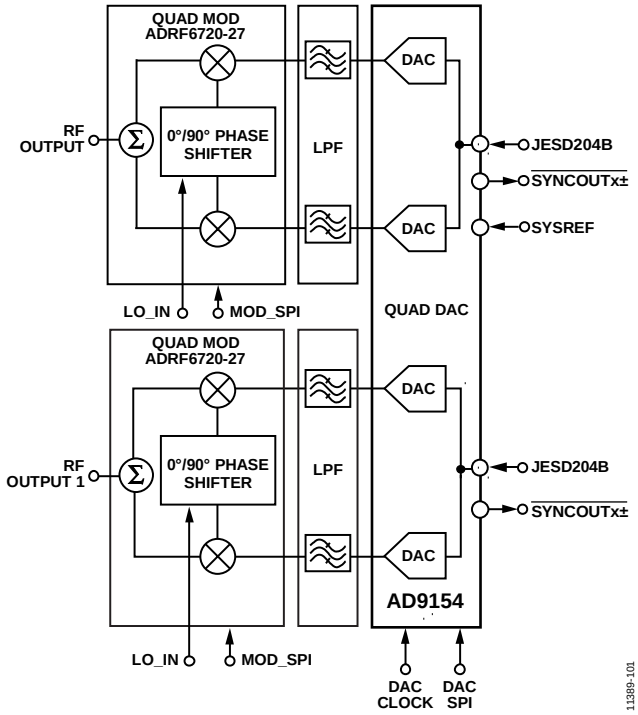

Figure 1.

GENERAL DESCRIPTION

The AD9154 is a quad, 16-bit, high dynamic range digital-to-analog converter (DAC) that provides a maximum sample rate of 2.4 GSPS, permitting multicarrier generation up to the Nyquist frequency in baseband mode. The AD9154 includes features optimized for direct conversion transmit applications, including complex digital modulation, input signal power detection, and gain, phase, and offset compensation. The DAC outputs are optimized to interface seamlessly with the ADRF6720-27 radio frequency quadrature modulator (AQM) from Analog Devices, Inc. In mix mode, the AD9154 DAC can reconstruct carriers in the second and third Nyquist zones. A serial port interface (SPI) provides the programming/readback of internal parameters. The full-scale output current can be programmed over a range of 4 mA to 20 mA. The AD9154 is available in two different 88-lead LFCSP packages.

PRODUCT HIGHLIGHTS

1. Ultrawide signal bandwidth enables emerging wideband and multiband wireless applications.
2. Advanced low spurious and distortion design techniques provide high quality synthesis of wideband signals from baseband to high intermediate frequencies.
3. JESD204B Subclass 1 support simplifies multichip synchronization.
4. Small package size with a 12 mm × 12 mm footprint.

Rev. B Document Feedback

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REVISION HISTORY

7/15—Rev. A to Rev. B

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Added Figure 34; Renumbered Sequentially 19
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3/15—Rev. 0 to Rev. A

Changes to Figure 1 and General Description Section 1

2/15—Revision 0: Initial Version

DETAILED FUNCTIONAL BLOCK DIAGRAM

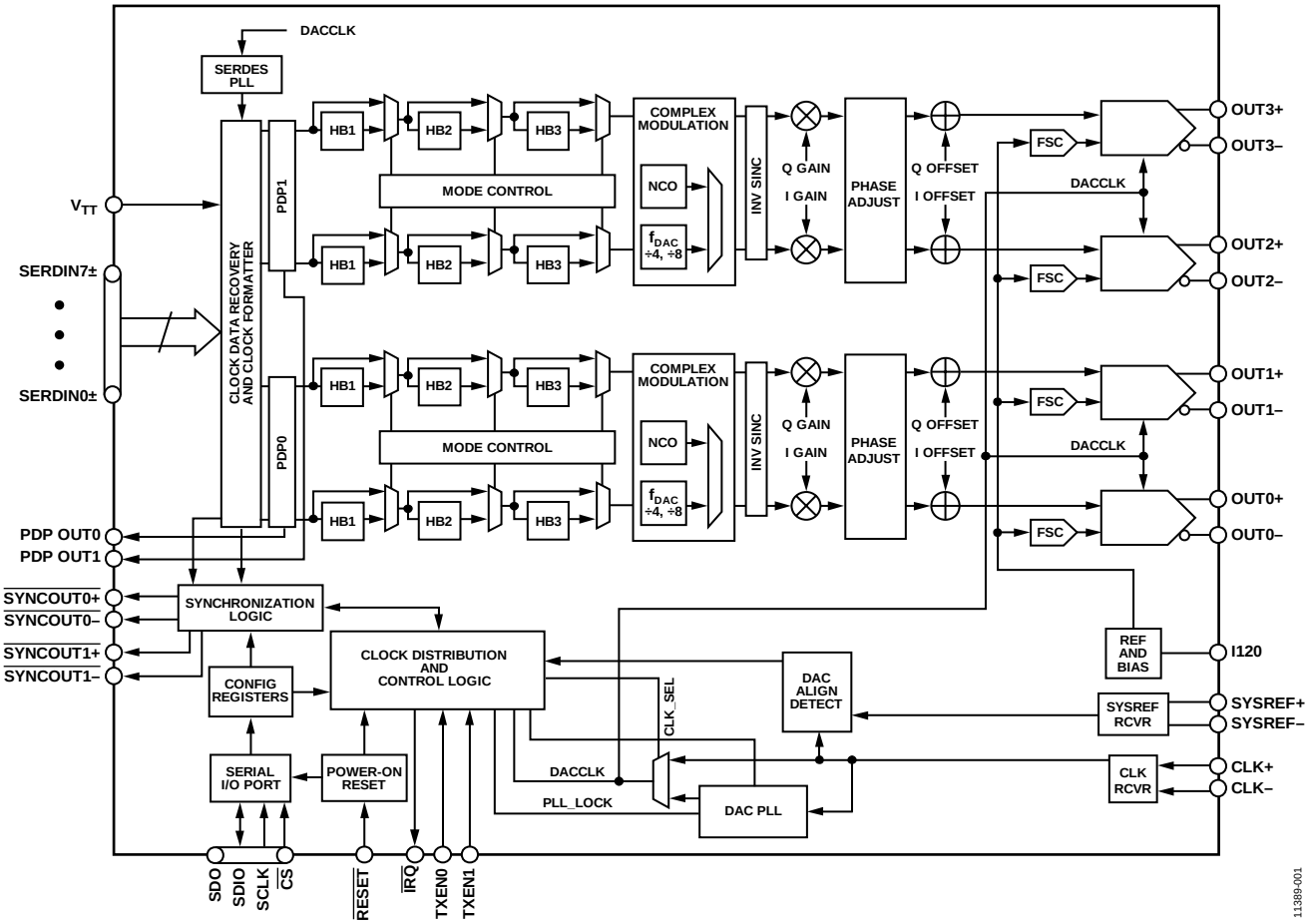


Figure 2. Detailed Functional Block Diagram

SPECIFICATIONS

DC SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION			16		Bits
ACCURACY					
Differential Nonlinearity (DNL)			±4.3		LSB
Integral Nonlinearity (INL)			±8.2		LSB
MAIN DAC OUTPUTS					
Gain Error	With internal reference	−8.0	−3.01	+8.0	% FSR
Offset Error[1]			2322		ppm
I/Q Gain Mismatch		−3.0	+0.54	+3.0	% FSR
Full-Scale Output Current	Based on a 4 kΩ external resistor between I120 and ground				
Maximum Setting		19.9	20.85	21.3	mA
Minimum Setting		3.9	4.17	4.4	mA
Output Compliance Range		2.0	2.8	3.37	V
Output Resistance			15		MΩ
Output Capacitance			3.0		pF
Full-Scale Current DAC Monotonicity			Guaranteed		
MAIN DAC TEMPERATURE DRIFT					
Gain[2]			−114		ppm/°C
REFERENCE					
Internal Reference Voltage			1.2		V
ANALOG SUPPLY VOLTAGES					
AVDD33	5%	3.13	3.3	3.47	V
PVDD12	5%	1.14	1.2	1.26	V
	2%	1.274	1.3	1.326	V
CVDD12	5%	1.14	1.2	1.26	V
	2%	1.274	1.3	1.326	V
DIGITAL SUPPLY VOLTAGES					
SIOVDD33	5%	3.13	3.3	3.47	V
V_{TT}		1.1	1.2	1.37	V
DVDD12	5%	1.14	1.2	1.26	V
	2%	1.274	1.3	1.326	V
SVDD12	5%	1.14	1.2	1.26	V
	2%	1.274	1.3	1.326	V
IOVDD	5%	1.71	1.8	3.47	V
POWER CONSUMPTION					
2× Interpolation Mode, JESD204B Mode 4, Dual Link, 8 SERDES Lanes	f_{DAC} = 1.6 GSPS, NCO on, IF_{OUT} = 40 MHz, PLL on, DAC full-scale current = 20 mA		2.11	2.63	W
AVDD33			159	185	mA
PVDD12			152	174	mA
CVDD12			355	397	mA
SVDD12	Includes V_{TT}		541.9	682	mA
DVDD12			264.5	442	mA
SIOVDD33 + IOVDD			10.6	11.4	mA

[1] Offset error is a measure of how far from full-scale range (FSR) the DAC output current is at 25°C (in ppm).
[2] Gain drift is a measure of the slope of the DAC output current across its full temperature range (in ppm/°C).

DIGITAL SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CMOS INPUT LOGIC LEVEL						
Input Voltage (V_{IN}) Logic						
High		1.8 V ≤ IOVDD ≤ 3.3 V	0.7 × IOVDD			V
Low		1.8 V ≤ IOVDD ≤ 3.3 V			0.3 × IOVDD	V
CMOS OUTPUT LOGIC LEVEL						
Output Voltage (V_{OUT}) Logic						
High		1.8 V ≤ IOVDD ≤ 3.3 V	0.7 × IOVDD			V
Low		1.8 V ≤ IOVDD ≤ 3.3 V			0.3 × IOVDD	V
MAXIMUM DAC UPDATE RATE[1]		1× interpolation[2] (see Table 4)	1096			MSPS
		2× interpolation[3]	2192			MSPS
		4× interpolation	2400			MSPS
		8× interpolation	2400			MSPS
ADJUSTED DAC UPDATE RATE		1× interpolation	1096			MSPS
		2× interpolation	1096			MSPS
		4× interpolation	600			MSPS
		8× interpolation	300			MSPS
INTERFACE[4]						
Number of JESD204B Lanes				8		Lanes
JESD204B Serial Interface Speed						
Minimum		Per lane			1.44	Gbps
Maximum		Per lane, SVDD12 = 1.3 V ± 2%	10.96			Gbps
DAC CLOCK INPUT (CLK±)						
Differential Peak-to-Peak Voltage			400	1000	2000	mV
Common-Mode Voltage		Self biased input, ac-coupled		600		mV
Maximum Clock Rate, DAC Clock Sourced Directly from CLK±			2400			MHz
PLL Multiplier Mode Clock Input Frequency[5]		6.0 GHz ≤ f_{VCO} ≤ 12.0 GHz	35		1000	MHz
SYSREF INPUT (SYSREF±)						
Differential Peak-to-Peak Voltage			400	1000	2000	mV
Common-Mode Voltage			0		2000	mV
SYSREF± Frequency[6]					$f_{DATA}/(K \times (F/S))$	Hz
SYSREF± TO DAC CLOCK[7]		SYSREF± differential swing = 0.4 V, slew rate = 1.3 V/ns, (ac-coupled, and 0 V, 0.6 V, 1.25 V, 2.0 V dc-coupled common-mode voltages)				
Setup Time	t_{SSD}		111			ps
Hold Time	t_{HSD}		145			ps
SPI		See timing diagrams shown in Figure 39 and Figure 40				
Maximum Clock Rate	SCLK	IOVDD = 1.8 V	10			MHz
Minimum SCLK Pulse Width						
High	t_{PWH}				8	ns
Low	t_{PWL}				12	ns
SDIO to SCLK						
Setup Time	t_{DS}		5			ns
Hold Time	t_{DH}		2			ns
SDO to SCLK						
Data Valid Window	t_{DV}		25			ns

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
$\overline{CS}$ to SCLK						
Setup Time	$t_{S\overline{CS}}$		5			ns
Hold Time	$t_{HCS\overline{CS}}$		2			ns

[1] See Table 3 for detailed specifications for DAC update rate conditions.
[2] Maximum speed for 1× interpolation is limited by the JESD204B interface. See Table 4 for details.
[3] Maximum speed for 2× interpolation is limited by the JESD204B interface. See Table 4 for details.
[4] See Table 4 for detailed specifications for JESD204B speed conditions.
[5] CLK+/CLK– serve as a reference oscillator input for the on-chip PLL clock multiplier when in use.
[6] K, F, and S are JESD204B transport layer parameters. See Table 42 for the full definitions.
[7] See Table 5 for detailed specifications for SYSREF to DAC clock timing conditions.

MAXIMUM DAC UPDATE RATE SPEED SPECIFICATIONS BY SUPPLY

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
MAXIMUM DAC UPDATE RATE	DVDD12, CVDD12, PVDD12 = 1.2 V ± 5%	1.93			GSPS
	DVDD12, CVDD12, PVDD12 = 1.2 V ± 2%	2.07			GSPS
	DVDD12, CVDD12, PVDD12 = 1.3 V ± 2%	2.4			GSPS

JESD204B SERIAL INTERFACE SPEED SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLOCK AND DATA RECOVERY (CDR) HALF RATE MODE	SVDD12 = 1.2 V ± 5%	5.74		9.04	Gbps
	SVDD12 = 1.2 V ±2%	5.74		9.65	Gbps
	SVDD12 = 1.3 V ± 2%	5.74		10.96	Gbps
CDR FULL RATE MODE	SVDD12 = 1.2 V ± 5%	2.87		4.79	Gbps
	SVDD12 = 1.2 V ±2%	2.87		4.93	Gbps
	SVDD12 = 1.3 V ± 2%	2.87		5.73	Gbps
CDR OVERSAMPLING MODE	SVDD12 = 1.2 V ± 5%	1.44		2.39	Gbps
	SVDD12 = 1.2 V ±2%	1.44		2.50	Gbps
	SVDD12 = 1.3 V ± 2%	1.44		2.93	Gbps

SYSREF TO DAC CLOCK TIMING SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, SYSREF± common-mode voltages = 0.0 V, 0.6 V, 1.25 V, and 2.0 V, unless otherwise noted.

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SYSREF	Differential swing = 0.4 V, slew rate = 1.3 V/ns				
Setup Time	AC-coupled	89			ps
	DC-coupled	111			ps
Hold Time	AC-coupled	105			ps
	DC-coupled	145			ps
	Differential swing = 0.7 V, slew rate = 2.28 V/ns				
Setup Time	AC-coupled	71			ps
	DC-coupled	81			ps
Hold Time	AC-coupled	97			ps
	DC-coupled	118			ps
	Differential swing = 1.0 V, slew rate = 3.26 V/ns				
Setup Time	AC-coupled	58			ps
	DC-coupled	64			ps
Hold Time	AC-coupled	92			ps
	DC-coupled	108			ps

DIGITAL INPUT DATA TIMING SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = 25°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 6.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LATENCY					
Interface, Excluding Transport Layer Delay Buffer			17		PClock[1] cycles
Interpolation	With or without modulation				
1×			94		DAC clock cycles
2×			130		DAC clock cycles
4×			250		DAC clock cycles
8×			474		DAC clock cycles
Inverse Sinc			17		DAC clock cycles
Fine Modulation			20		DAC clock cycles
Coarse Modulation					
$f_S/8$			8		DAC clock cycles
$f_S/4$			4		DAC clock cycles
Digital Phase Adjust			12		DAC clock cycles
Digital Gain Adjust			12		DAC clock cycles
Power-Up Time					
Dual A Only	Register 0x011 from 0x60 to 0x00		30		µs
Dual B Only	Register 0x011 from 0x18 to 0x00		30		µs
All DACs	Register 0x011 from 0x78 to 0x00		30		µs

[1] PClock is the AD9154 internal processing clock running at the JESD204B lane rate ÷ 40.

LATENCY VARIATION SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = 25°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 7.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DAC LATENCY VARIATION					
Subclass 1					
PLL Off			0	1	DACCLK cycles
PLL On		−1		+1	DACCLK cycles

JESD204B INTERFACE ELECTRICAL SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 8.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
JESD204B DATA INPUTS						
Input Leakage Current		T_A = 25°C				
Logic High		Input level = 1.2 V ± 0.25 V, V_{TT} = 1.2 V		10		µA
Logic Low		Input level = 0 V		−4		µA
Unit Interval	UI		94		714	ps
Common-Mode Voltage	V_{RCM}	AC-coupled V_{TT} = SVDD12[1]	−0.05		+1.85	V
Differential Voltage	R_V_{DIFF}		110		1050	mV
V_{TT} Source Impedance	Z_{TT}	At dc			30	Ω
Differential Impedance	Z_{RDIFF}	At dc	80	100	120	Ω
Differential Return Loss	RL_{RDIF}			8		dB
Common-Mode Return Loss	RL_{RCM}			6		dB
DIFFERENTIAL OUTPUTS ($\overline{SYNCOUT}$±)[2]						
Output Offset Voltage	V_{OS}		1.19		1.27	V
DETERMINISTIC LATENCY						
Fixed					17	PClock[3] cycles
Variable					2	PClock[3] cycles
SYSREF± TO LOCAL MULTIFRAME CLOCK (LMFC) DELAY				4		DAC clock cycles

[1] As measured on the input side of the ac coupling capacitor.
[2] IEEE Standard 1596.3 LVDS compatible.
[3] PClock is the AD9154 internal processing clock; its frequency is equal to the JESD204B lane rate ÷ 40.

AC SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = 25°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 9.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)	−6 dBFS single tone				
f_{DAC} = 1966.08 MSPS	f_{OUT} = 20 MHz		76		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 150 MHz		73		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 180 MHz		72		dBc
TWO-TONE THIRD INTERMODULATION DISTORTION (IMD)	−6 dBFS				
f_{DAC} = 983.04 MSPS	f_{OUT} = 30 MHz		87		dBc
f_{DAC} = 983.04 MSPS	f_{OUT} = 150 MHz		77		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 30 MHz		86		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 180 MHz		78		dBc
NOISE SPECTRAL DENSITY (NSD), SINGLE TONE	0 dBFS				
f_{DAC} = 983.04 MSPS	f_{OUT} = 150 MHz		−164		dBm/Hz
f_{DAC} = 1966.08 MSPS	f_{OUT} = 180 MHz		−163		dBm/Hz
5 MHz BW LTE FIRST ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER	0 dBFS, PLL off				
f_{DAC} = 1966.08 MSPS	f_{OUT} = 50 MHz		79		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 150 MHz		77		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 180 MHz		77		dBc
5 MHz BW LTE SECOND ACLR, SINGLE CARRIER	0 dBFS, PLL off				
f_{DAC} = 1966.08 MSPS	f_{OUT} = 50 MHz		82		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 150 MHz		81		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 180 MHz		81		dBc

ABSOLUTE MAXIMUM RATINGS

Table 10.

Parameter	Rating
I120 to Ground	−0.3 V to AVDD33 + 0.3 V
SERDINx±, V_{TT}, $\overline{\text{SYNCOUTx}}$±, and TXENx	−0.3 V to SIOVDD33 + 0.3 V
OUTx±	−0.3 V to AVDD33 + 0.3 V
SYSREF±	GND − 0.5 V
CLK± to Ground	−0.3 V to PVDD12 + 0.3 V
$\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, $\overline{\text{CS}}$, SCLK, SDIO, SDO, and PDP OUTx to Ground	−0.3 V to IOVDD + 0.3 V
LDO_BYP1	−0.3 V to SVDD12 + 0.3 V
LDO_BYP2	−0.3 V to PVDD12 + 0.3 V
Ambient Operating Temperature (T_A)	−40°C to +85°C
Junction Temperature	125°C
Storage Temperature	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

The exposed pad (EPAD) must be soldered to the ground plane for the 88-lead LFCSP. The EPAD provides an electrical, thermal, and mechanical connection to the board.

Typical θ_{JA}, θ_{JB}, and θ_{JC} values are specified for a 4-layer, JESD51-7 high effective thermal conductivity test board for leaded surface-mount packages. θ_{JA} is obtained in still air conditions (JESD51-2). Airflow increases heat dissipation, effectively reducing θ_{JA}. θ_{JB} is obtained following double-ring cold plate test conditions (JESD51-8). θ_{JC} is obtained with the test case temperature monitored at the bottom of the exposed pad.

Ψ_{JT} and Ψ_{JB} are thermal characteristic parameters obtained with θ_{JA} in still air test conditions.

Junction temperature (T_J) can be estimated using the following equations:

$$T_J = T_T + (\Psi_{JT} \times P),$$

or

$$T_J = T_B + (\Psi_{JB} \times P)$$

where:
T_T is the temperature measured at the top of the package.
P is the total device power dissipation.
T_B is the temperature measured at the board.

Table 11. Thermal Resistance

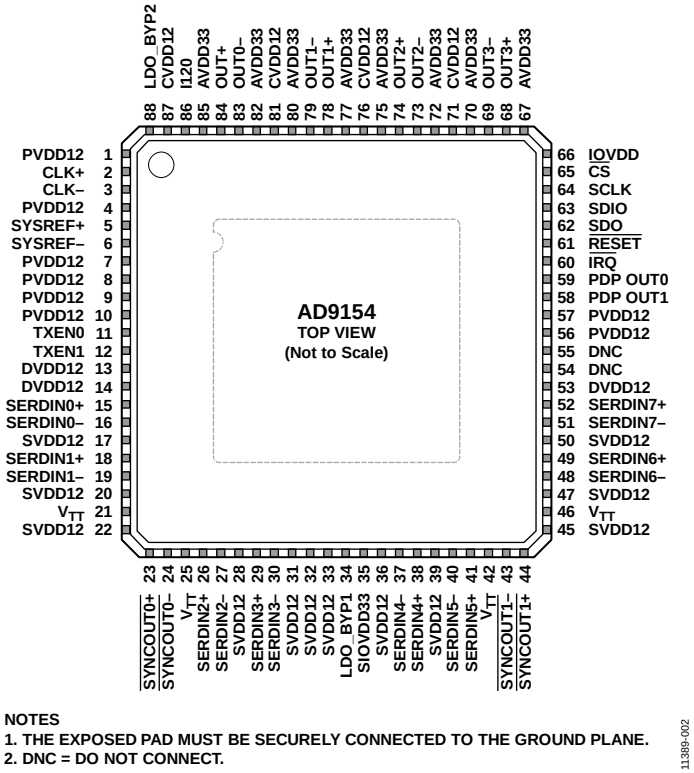
Package	θ_{JA}	θ_{JB}	θ_{JC}	Ψ_{JT}	Ψ_{JB}	Unit
88-Lead LFCSP[1]	22.6	5.59	1.17	0.1	5.22	°C/W

[1] The exposed pad must be securely connected to the ground plane.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD MUST BE SECURELY CONNECTED TO THE GROUND PLANE.
2. DNC = DO NOT CONNECT.

11389-002

Figure 3. Pin Configuration

Table 12. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4, 7, 8, 9, 10, 56, 57	PVDD12	1.2 V Clock Supplies.
2	CLK+	PLL Reference/Clock Input, Positive. When the PLL is used, this pin is the positive reference clock input. When the PLL is not used, this pin is the positive device clock input. This pin is self biased and must be ac-coupled.
3	CLK–	PLL Reference/Clock Input, Negative. When the PLL is used, this pin is the negative reference clock input. When the PLL is not used, this pin is the negative device clock input. This pin is self biased and must be ac-coupled.
5	SYSREF+	Timing Reference Input, Positive. This pin is used in JESD204B Subclass 1 systems and is self biased, ac-coupled, or dc-coupled.
6	SYSREF–	Timing Reference Input, Negative. This pin is used in JESD204B Subclass 1 systems and is self biased, ac-coupled, or dc-coupled.
11	TXEN0	Transmit enable for DAC0 and DAC1. CMOS levels are determined with respect to IOVDD.
12	TXEN1	Transmit Enable for DAC2 and DAC3. CMOS levels are determined with respect to IOVDD.
13, 14, 53	DVDD12	1.2 V Digital Supplies.
15	SERDIN0+	Serial Channel Input 0, Positive. CML compliant. SERDIN0+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
16	SERDIN0–	Serial Channel Input 0, Negative. CML compliant. SERDIN0– is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
17, 20, 22, 28, 31, 32, 33, 36, 39, 45, 47, 50	SVDD12	1.2 V JESD204B Receiver Supplies.
18	SERDIN1+	Serial Channel Input 1, Positive. CML compliant. SERDIN1+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
19	SERDIN1–	Serial Channel Input 1, Negative. CML compliant. SERDIN1– is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
21, 25, 42, 46	V_{TT}	1.2 V Termination Voltage Pins.

Pin No.	Mnemonic	Description
23	$\overline{\text{SYNCOUT0+}}$	Positive LVDS Synchronization Output Signal for Channel Link 0.
24	$\overline{\text{SYNCOUT0–}}$	Negative LVDS Synchronization Output Signal for Channel Link 0.
26	SERDIN2+	Serial Channel Input 2, Positive. CML compliant. SERDIN2+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
27	SERDIN2–	Serial Channel Input 2, Negative. CML compliant. SERDIN2– is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
29	SERDIN3+	Serial Channel Input 3, Positive. CML compliant. SERDIN3+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
30	SERDIN3–	Serial Channel Input 3, Negative. CML compliant. SERDIN3– is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
34	LDO_BYP1	LDO SERDES Bypass. This pin requires a 1 Ω resistor in series with a 1 µF capacitor to ground.
35	SIOVDD33	SERDES Ports Input/Output Supply.
37	SERDIN4–	Serial Channel Input 4, Negative. CML compliant. SERDIN4– is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
38	SERDIN4+	Serial Channel Input 4, Positive. CML compliant. SERDIN4+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
40	SERDIN5–	Serial Channel Input 5, Negative. CML compliant. SERDIN5– is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
41	SERDIN5+	Serial Channel Input 5, Positive. CML compliant. SERDIN5+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
43	$\overline{\text{SYNCOUT1–}}$	Negative LVDS Synchronization Output Signal for Channel Link 1.
44	$\overline{\text{SYNCOUT1+}}$	Positive LVDS Synchronization Output Signal for Channel Link 1.
48	SERDIN6–	Serial Channel Input 6, Negative. CML compliant. SERDIN6– is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
49	SERDIN6+	Serial Channel Input 6, Positive. CML compliant. SERDIN6+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
51	SERDIN7–	Serial Channel Input 7, Negative. CML compliant. SERDIN7– is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
52	SERDIN7+	Serial Channel Input 7, Positive. CML compliant. SERDIN7+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
54, 55	DNC	Do Not Connect. Do not connect to this pin.
58	PDP OUT1	Power Detection and Protection (PDP) Indicator for DAC2 and DAC3.
59	PDP OUT0	PDP Indicator for DAC0 and DAC1.
60	$\overline{\text{IRQ}}$	Interrupt Request (Active Low, Open Drain).
61	$\overline{\text{RESET}}$	Reset (Active Low). CMOS levels with are determined with respect to IOVDD.
62	SDO	Serial Port Data Output. CMOS levels with are determined with respect to IOVDD.
63	SDIO	Serial Port Data Input/Output. CMOS levels with are determined with respect to IOVDD.
64	SCLK	Serial Port Clock Input. CMOS levels with are determined with respect to IOVDD.
65	$\overline{\text{CS}}$	Serial Port Chip Select (Active Low). CMOS levels with are determined with respect to IOVDD.
66	IOVDD	CMOS Input/Output and SPI Pin Supply.
67, 70, 72, 75, 77, 80, 82, 85	AVDD33	3.3 V Analog Supplies for the DAC Cores.
68	OUT3+	DAC3 Positive Current Output.
69	OUT3–	DAC3 Negative Current Output.
71, 76, 81, 87	CVDD12	1.2 V Clock Supplies.
73	OUT2–	DAC2 Negative Current Output.
74	OUT2+	DAC2 Positive Current Output.
78	OUT1+	DAC1 Positive Current Output.
79	OUT1–	DAC1 Negative Current Output.
83	OUT0–	DAC0 Negative Current Output.
84	OUT0+	DAC0 Positive Current Output.
86	I120	Output Current Generation Pin for DAC Full-Scale Current. Tie a 4 kΩ resistor from this pin to ground.
88	LDO_BYP2	LDO Clock Bypass for the DAC PLL. Tie a 1 Ω resistor in series with a 1 µF capacitor from this pin to ground.
	EPAD	Exposed Pad. The exposed pad must be securely connected to the ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

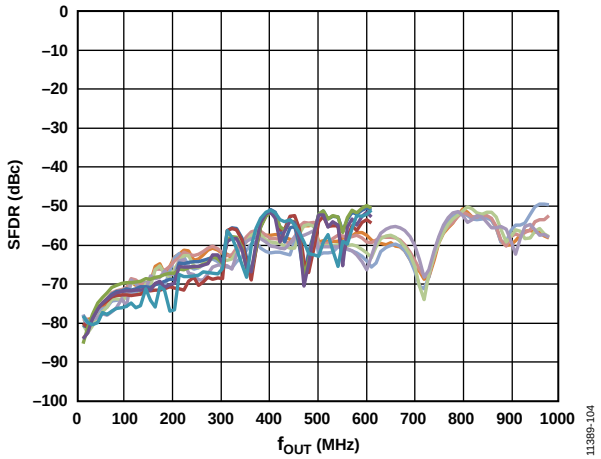


Figure 4. Single Tone (0 dBFS) SFDR vs. f_{OUT} in the First Nyquist Zone over f_{DAC} = 1966.08 MHz and 1228.80 MHz, All Four DAC Outputs

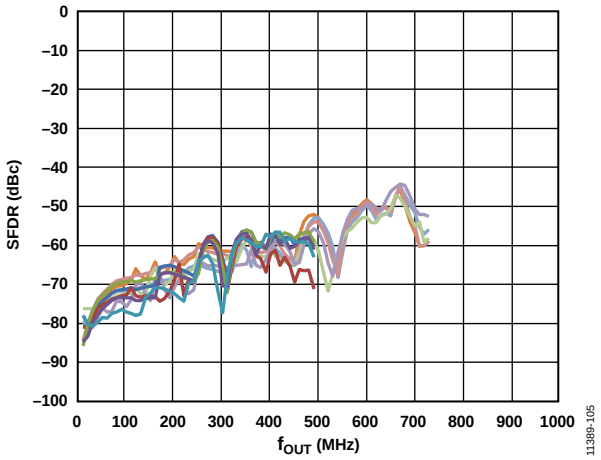


Figure 5. Single Tone (0 dBFS) SFDR vs. f_{OUT} in the First Nyquist Zone over f_{DAC} = 1474.56 MHz and 983.04 MHz, All Four DAC Outputs

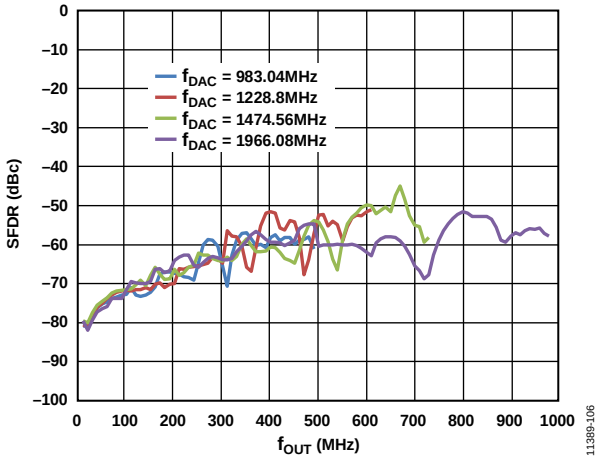


Figure 6. Single Tone (0 dBFS) SFDR vs. f_{OUT} in the First Nyquist Zone over f_{DAC} = 1966.08 MHz, 1474.56 MHz, 1228.8 MHz, and 983.04 MHz

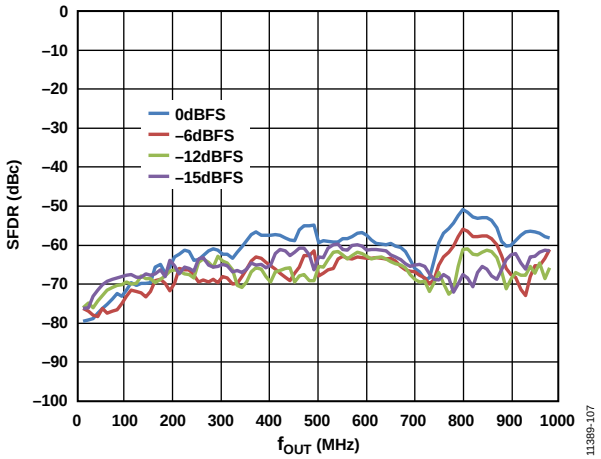


Figure 7. Single Tone SFDR vs. f_{OUT} in the First Nyquist Zone over Digital Back Off, f_{DAC} = 1966.08 MHz

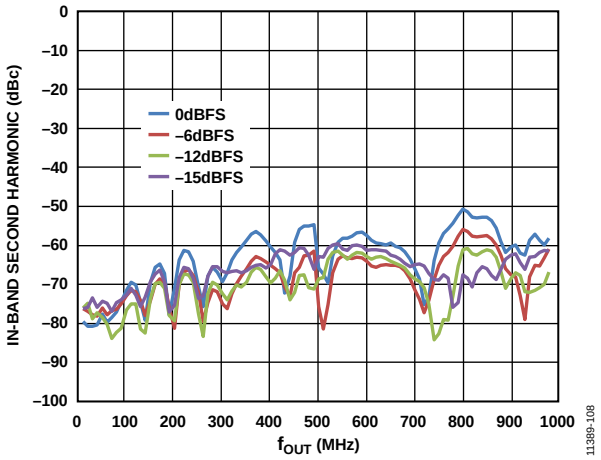


Figure 8. In-Band Second Harmonic vs. f_{OUT} in the First Nyquist Zone over Digital Back Off, f_{DAC} = 1966.08 MHz

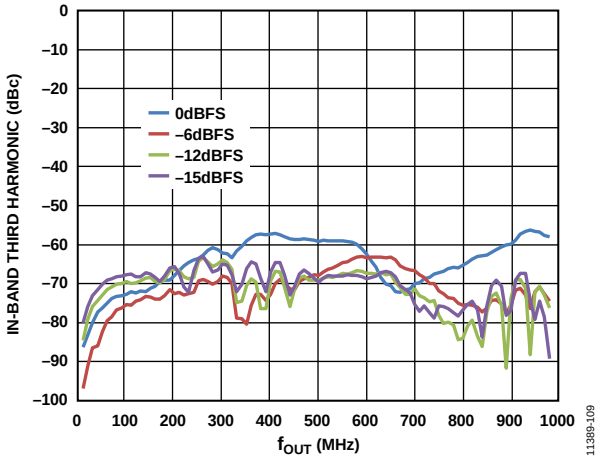


Figure 9. In-Band Third Harmonic vs. f_{OUT} in the First Nyquist Zone, f_{DAC} = 1966.08 MHz

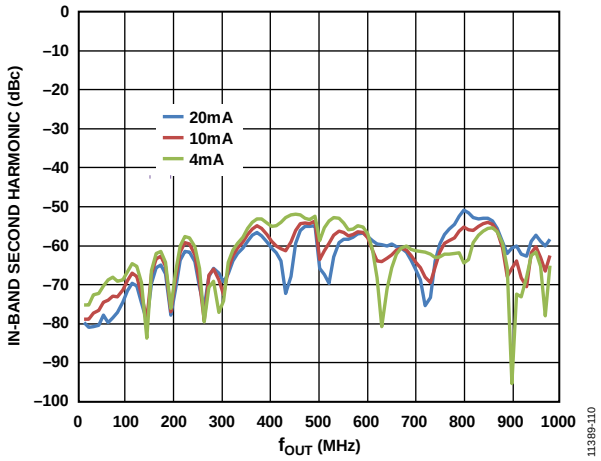


Figure 10. In-Band Second Harmonic vs. f_{OUT} in the First Nyquist Zone over Analog Full-Scale Current, f_{DAC} = 1966.08 MHz

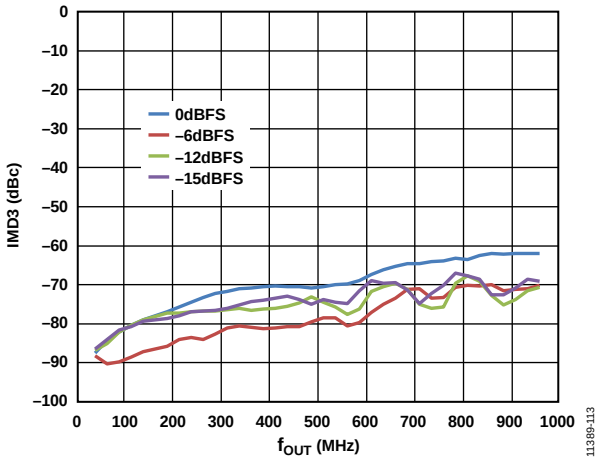


Figure 13. Two-Tone Third Harmonic (IMD3) vs. f_{OUT} over Digital Backoff

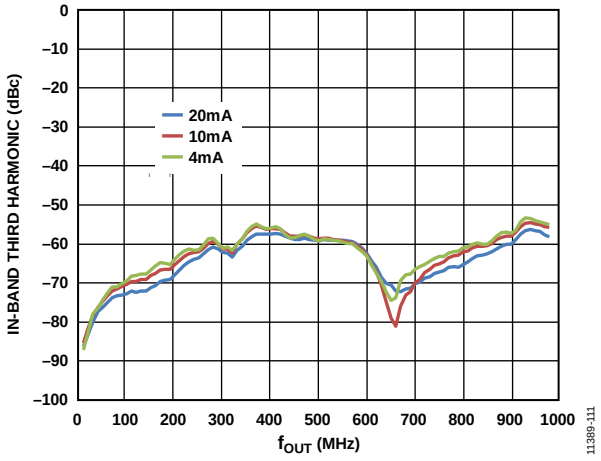


Figure 11. In-Band Third Harmonic vs. f_{OUT} in the First Nyquist Zone over Analog Full-Scale Current, f_{DAC} = 1966.08 MHz

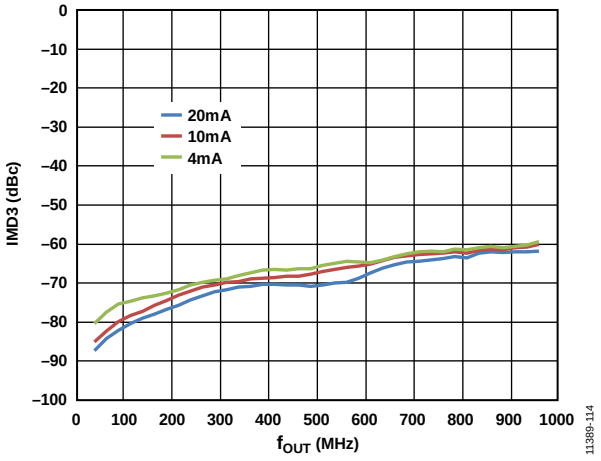


Figure 14. Two-Tone Third Harmonic (IMD3) vs. f_{OUT} over Analog Full-Scale Current, f_{DAC} = 1966.08 MHz

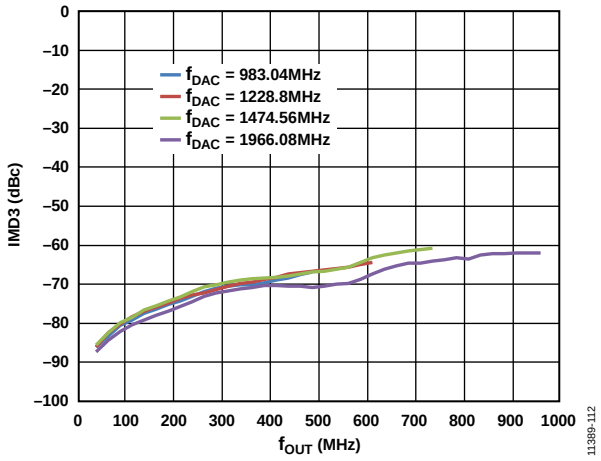


Figure 12. Two-Tone Third Harmonic (IMD3) vs. f_{OUT}, f_{DAC} = 1966.08 MHz, 1474.56 MHz, 1228.8 MHz, and 983.04 MHz

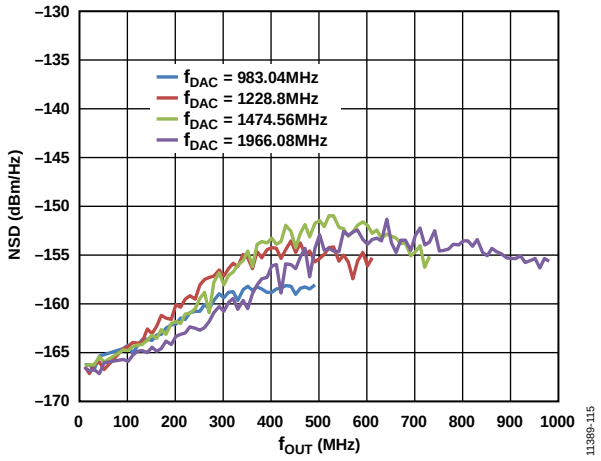


Figure 15. Single Tone (0 dBFS) NSD vs. f_{OUT} over f_{DAC} = 1966.08 MHz, 1474.56 MHz, 1228.8 MHz, and 983.04 MHz at 70 MHz

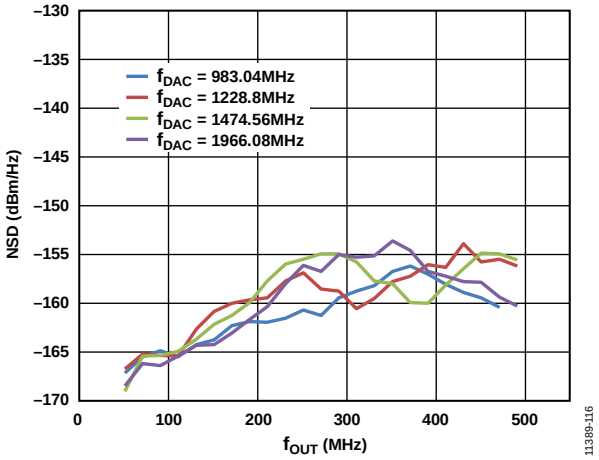


Figure 16. Single Tone (0 dBFS) NSD vs. f_{OUT} over f_{DAC}, 20 MHz Offset from Carrier

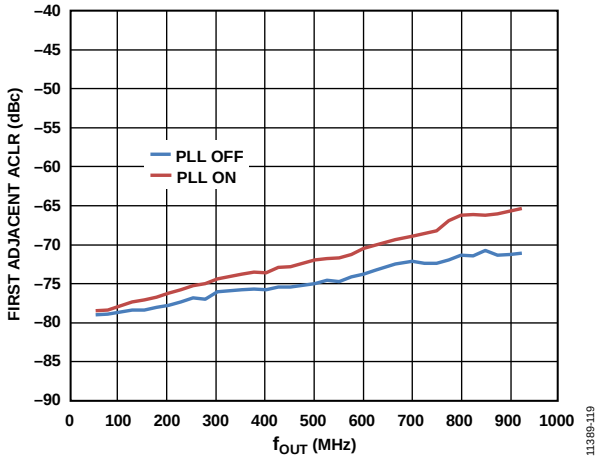


Figure 19. 1-Channel (1C) 5 MHz BW LTE, First Adjacent ACLR vs. f_{OUT}, PLL On and Off

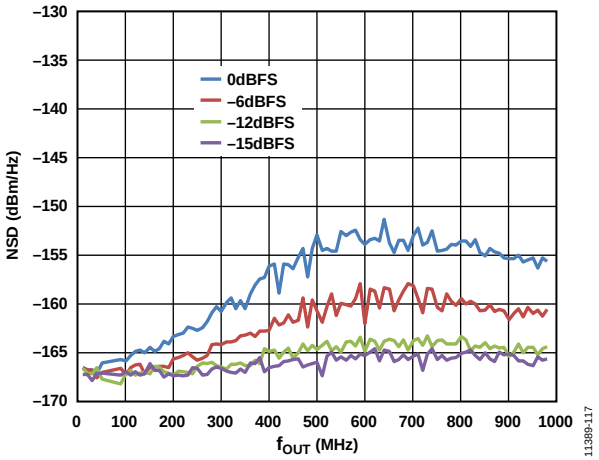


Figure 17. Single Tone NSD vs. f_{OUT} over Digital Back Off, f_{DAC} = 1966.08 MHz, Measured at 70 MHz

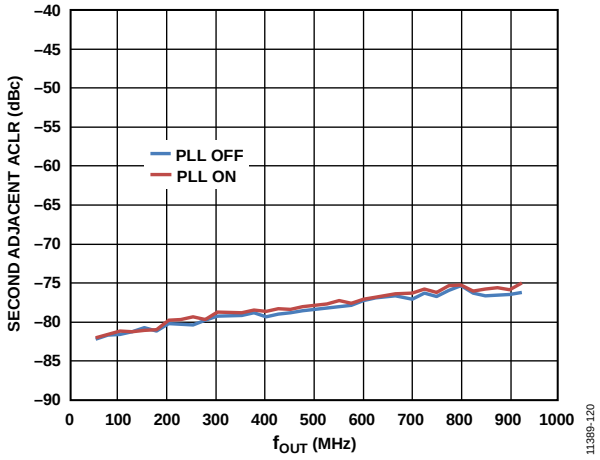


Figure 20. 1C 5 MHz BW LTE, Second Adjacent ACLR vs. f_{OUT}, PLL On and Off

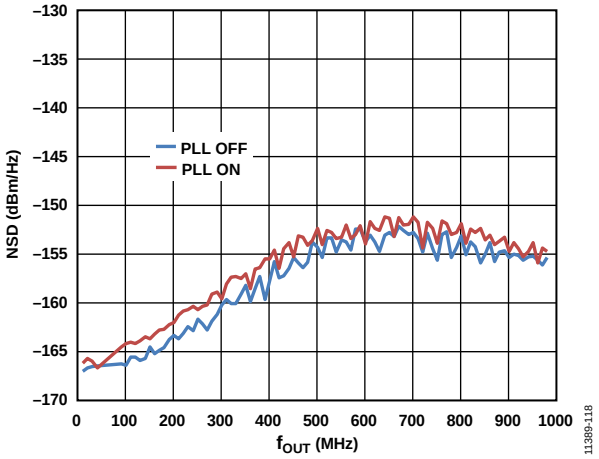


Figure 18. Single Tone NSD vs. f_{OUT}, f_{DAC} = 1966.08 MHz, Measured at 70 MHz, PLL On and Off

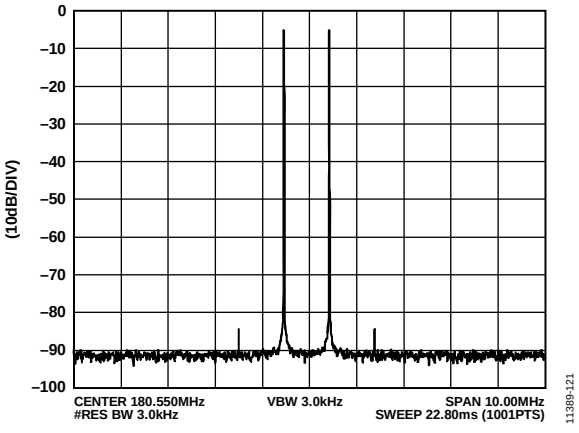


Figure 21. Two-Tone, Third IMD Performance, IF = 180 MHz, f_{DAC} = 1966.08 MHz

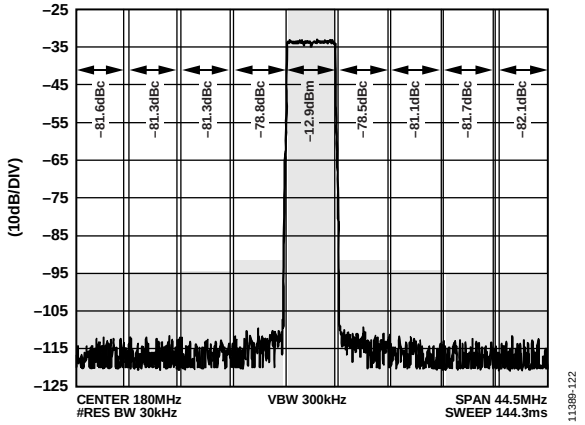


Figure 22. 1C 5 MHz BW LTE ACLR Performance, IF = 180 MHz, f_{DAC} = 1966.08 MHz

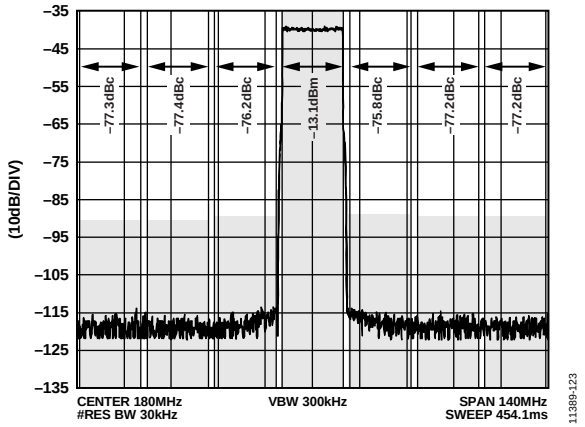


Figure 23. 1C 20 MHz BW LTE ACLR Performance, IF = 180 MHz, f_{DAC} = 1966.08 MHz

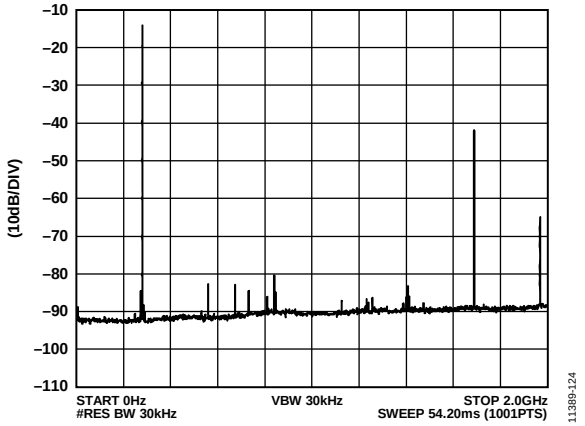


Figure 24. Single Tone f_{DAC} = 1966.08 MHz, f_{OUT} = 280 MHz, −14 dBFS

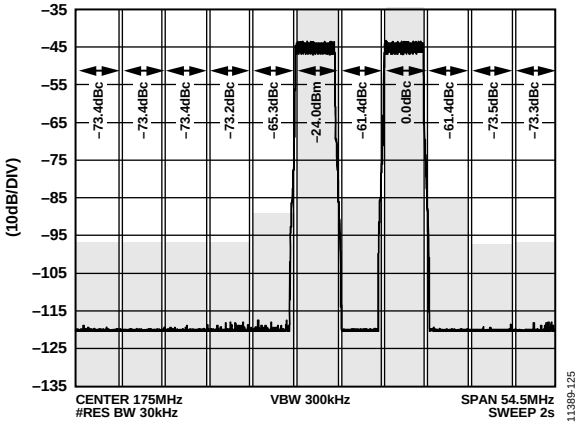


Figure 25. 2-Channel (2C) 5 MHz BW with 5 MHz Gap, LTE ACLR Performance, IF = 180 MHz, f_{DAC} = 1966.08 MHz (Total LTE Carrier Power is 20.982 dBm)

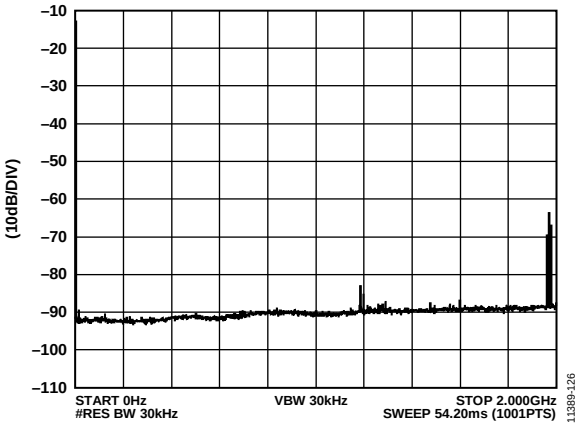


Figure 26. Single Tone SFDR f_{DAC} = 1966.08 MHz, 4× Interpolation, f_{OUT} = 10 MHz, −14 dBFS

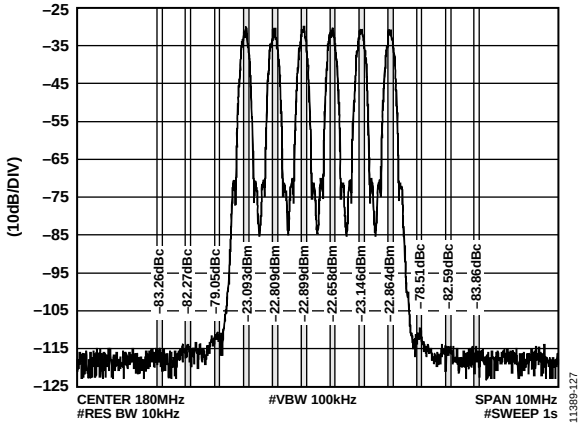


Figure 27. 6-Channel (6C) Spaced by 600 kHz GSM, Enhanced Data Rates for GSM Evolution (EDGE) Adjacent Channel Power (ACP) IMD Performance, IF = 180 MHz, f_{DAC} = 1966.08 MHz

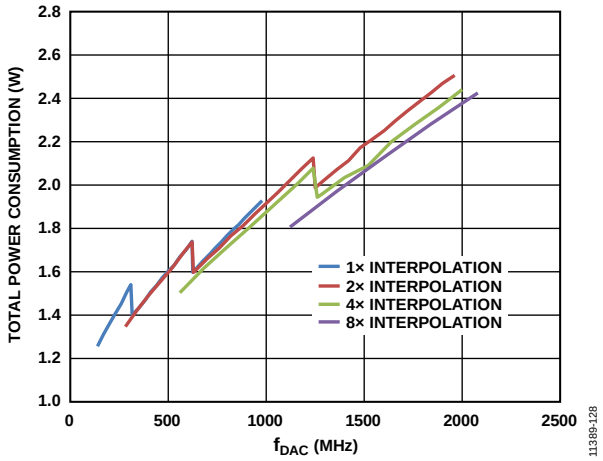


Figure 28. Total Power Consumption vs. f_{DAC} over Interpolation

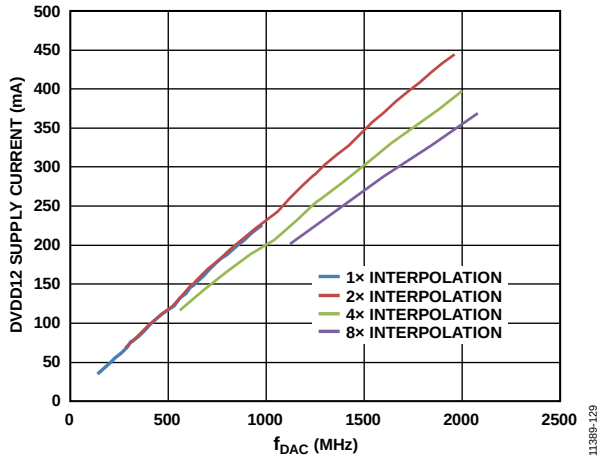


Figure 29. DVDD12 Supply Current vs. f_{DAC} over Interpolation

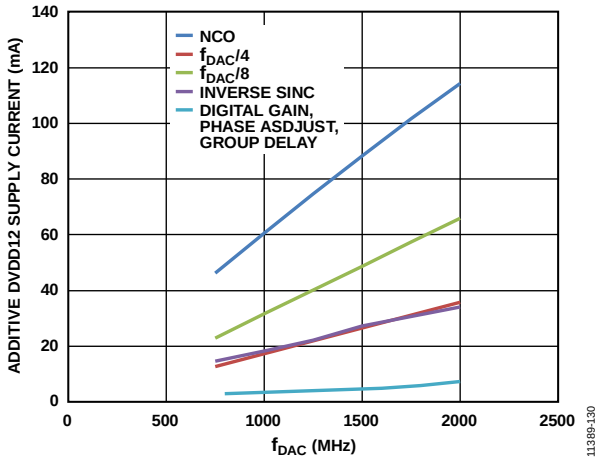


Figure 30. Additive DVDD12 Supply Current vs. f_{DAC} over Digital Functions

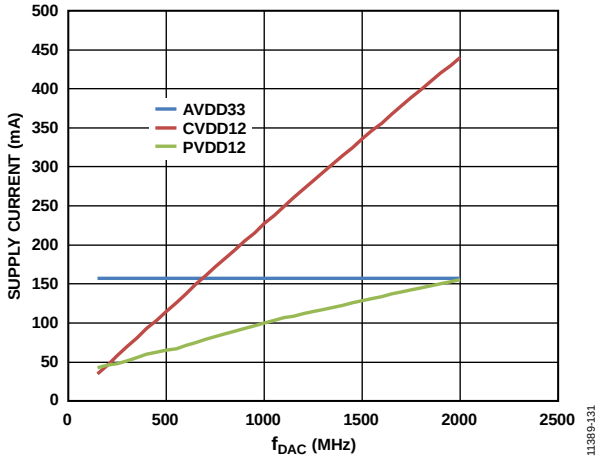


Figure 31. AVDD33, CVDD12, and PVDD12 Supply Current vs. f_{DAC}

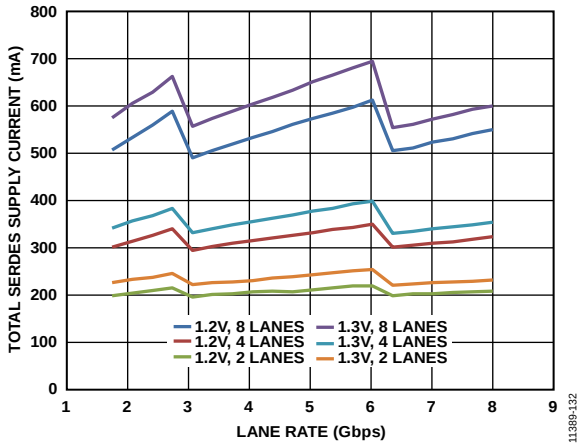


Figure 32. Total SERDES Supply Current (SVDD12) vs. Lane Rate: 2, 4, and 8 Lanes

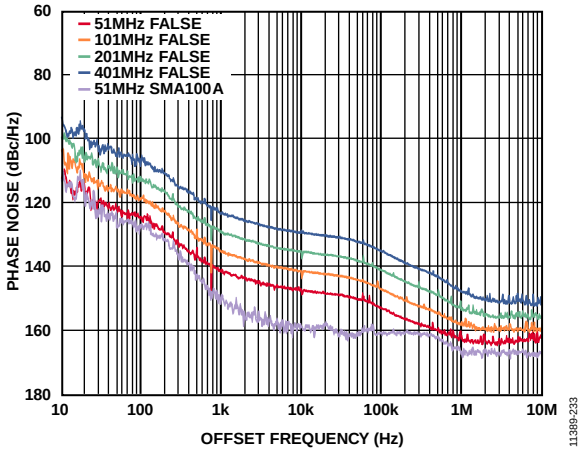


Figure 33. Single Tone Phase Noise vs. Offset Frequency at Four Different f_{OUT} Rates, f_{DAC} = 2.0 GHz, PLL Off

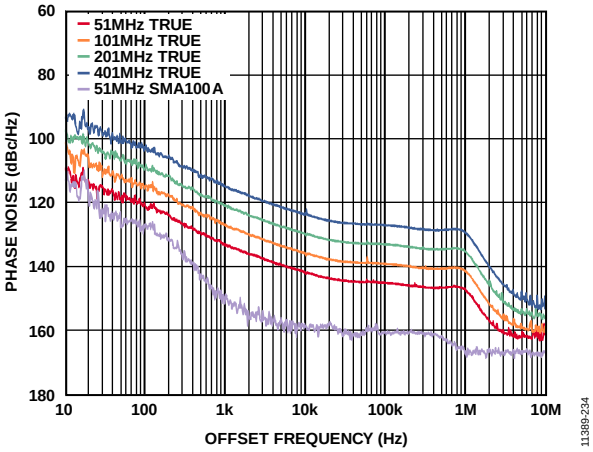


Figure 34. Single Tone Phase Noise vs. Offset Frequency at Four Different f_{OUT} Rates, f_{DAC} = 2.0 GHz, PLL On

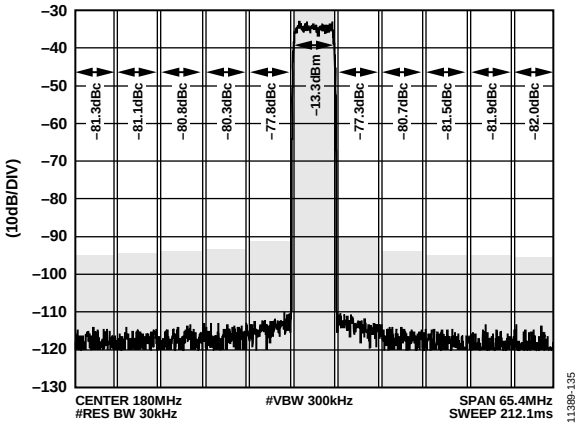


Figure 35. 1C 256 Point Quadrature Amplitude Modulation (QAM) Signal ACLR Performance, IF = 180 MHz, f_{DAC} = 1966.08 MHz

TERMINOLOGY

Integral Nonlinearity (INL)
INL is the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Offset Error
Offset error is a measure of how far from full-scale range (FSR) the DAC output current is at 25°C (in ppm).

Gain Error
Gain error is the difference between the actual and ideal output span. The actual span is determined by the difference between the output when the input is at its minimum code and the output when the input is at its maximum code.

Output Compliance Range
The output compliance range is the range of allowable voltages at the output of a current output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient value (25°C) to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of FSR per degree Celsius.

Settling Time
Settling time is the time required for the output to reach and remain within a specified error band around its final value, measured from the start of the output transition.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels, between the peak amplitude of the output signal and the peak spurious signal within the dc to Nyquist frequency of the DAC. Typically, energy in this band is rejected by the interpolation filters. This specification, therefore, defines how well the interpolation filters work and the effect of other parasitic coupling paths on the DAC output.

Interpolation Filter
If the digital inputs to the DAC are sampled at a multiple rate of f_{DATA} (interpolation rate), a digital filter can be constructed that has a sharp transition band near $f_{DATA}/2$. Images that typically appear around f_{DAC} (output data rate) can be greatly suppressed.

Adjacent Channel Leakage Ratio (ACLR)
ACLR is the ratio in decibels relative to the carrier (dBc) between the measured power within a channel relative to its adjacent channel.

Complex Image Rejection
In a single sideband upconversion, two images are created around the second IF frequency; the desired signal is on one of these images. The other signal is unwanted, and a complex modulator rejects this unwanted image.

Adjusted DAC Update Rate
The adjusted DAC update rate the DAC update rate divided by the selected interpolation factor.

Physical Lane
Physical Lane x refers to SERDINx±.

Logical Lane
Logical Lane x refers to physical lanes after optionally being remapped by the crossbar block (Register 0x308 to Register 0x30B).

Link Lane
Link Lane x refers to logical lanes considered per link. When paging Link 0 (Register 0x300, Bit 2 = 0), Link Lane x = Logical Lane x. When paging Link 1 (Register 0x300, Bit 2 = 1, dual link only), Link Lane x = Logical Lane x + 4.

THEORY OF OPERATION

The AD9154 is a 16-bit, quad DAC with a SERDES interface. Figure 2 shows a detailed functional block diagram of the AD9154. Eight high speed serial lanes carry data into the AD9154.

The clock for the input data is derived from the device clock (as called out in the JESD204B specification). This device clock can be sourced with a phase-locked loop (PLL) reference clock used by the on-chip PLL to generate a DAC clock or a high fidelity direct external DAC sampling clock. The device can be configured to operate in one-, two-, four-, or eight-lane modes, depending on the required input data rate. The quad DAC can be configured as a dual link device with each JESD204B link providing data for a dual DAC pair to add application flexibility.

The signal processing datapath of the AD9154 offers four interpolation modes (1×, 2×, 4×, and 8×) through three half-band filters. An inverse sinc filter compensates for DAC output sinc roll-off. A digital inphase and quadrature modulator upcoverts a pair of DAC input signals to an IF frequency within the first Nyquist zone of the DAC programmed into an NCO. Gain, phase, dc offset, and group delay adjustments can programmably predistort the DAC input signals to improve LO feedthrough and unwanted sideband cancellation performance of an analog quadrature modulator following the AD9154 in a transmitter signal chain.

The AD9154 DAC cores provide a differential current output with a nominal full-scale current of 20 mA. The differential current outputs are optimized for integration with the Analog Devices ADRF6720-27 wideband quadrature modulator. The AD9154 has a mechanism for multichip synchronization, as well as a mechanism for achieving deterministic latency (latency locking). The latency for each DAC remains constant from link establishment to link establishment. The AD9154 makes use of the JESD204B Subclass 1 SYSREF signal to establish multichip synchronization.

The various functional blocks and the data interface must be set up in a specific sequence for proper operation (see the Device Setup Guide section). This data sheet describes the various blocks of the AD9154 in detail, including descriptions of the JESD204B interface, the control parameters, and the various registers used to set up and monitor the device. The recommended start-up routine reliably sets up the data link.

SERIAL PORT OPERATION

The serial port interface (SPI) is a flexible, synchronous serial communications port that allows easy interfacing with many industry-standard microcontrollers and microprocessors. The interface facilitates read/write access to all registers that configure the AD9154. MSB first or LSB first transfer formats are supported. The SPI is configurable as a 4-wire interface or a 3-wire interface in which the input and output share a single-pin I/O, SDIO.

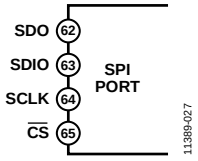


Figure 36. SPI Pins

There are two phases to a communication cycle with the AD9154. Phase 1 is the instruction cycle (the writing of an instruction byte into the device), coincident with the first 16 SCLK rising edges. The instruction word provides the serial port controller with information regarding the data transfer cycle, Phase 2 of the communication cycle. The Phase 1 instruction word defines whether the upcoming data transfer is a read or write, along with the starting register address for the following data transfer.

A logic high on the $\overline{CS}$ pin, followed by a logic low, resets the serial port timing to the initial state of the instruction cycle. From this state, the next 16 rising SCLK edges represent the instruction bits of the current input/output (I/O) operation.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the device and the system controller. Phase 2 of the communication cycle is a transfer of one or more data bytes. Eight × N SCLK cycles are needed to transfer N bytes during the transfer cycle. Registers change immediately upon writing to the last bit of each transfer byte, except for the frequency tuning word (FTW) and numerically controlled oscillator (NCO) phase offsets, which change only when the frequency tuning word FTW_UPDATE_REQ bit is set.

DATA FORMAT

The instruction byte contains the information shown in Table 13.

Table 13. Serial Port Instruction Word

I15 (MSB)	I[14:0]
R/$\overline{W}$	A[14:0]

R/$\overline{W}$, Bit 15 of the instruction word, determines whether a read or a write data transfer occurs after the instruction word write. Logic 1 indicates a read operation, and Logic 0 indicates a write operation.

A14 to A0, Bit 14 to Bit 0 of the instruction word, determine the register accessed during the data transfer portion of the communication cycle. For multibyte transfers, A[14:0] is the starting address. The device generates the remaining register addresses based on the address increment bits. If the address increment bits are set high (Register 0x000, Bit 5 and Bit 2), multibyte SPI writes start on A[14:0] and increment by 1 every eight bits sent/received. If the address increment bits are set to 0, the address decrements by 1 every eight bits.

SERIAL PORT PIN DESCRIPTIONS

Serial Clock (SCLK)

The serial clock pin synchronizes data to and from the device and runs the internal state machines. The maximum frequency of SCLK is specified in Table 2. All data input is registered on the rising edge of SCLK. All data is driven out on the falling edge of SCLK.

Chip Select ($\overline{CS}$)

An active low input starts and gates a communication cycle. It allows the use of more than one device on the same serial communications lines. The SDIO pin goes to a high impedance state when this input is high. During the communication cycle, chip select must stay low.

Serial Data I/O (SDIO)

This pin is a bidirectional data line. In 4-wire mode, this pin acts as the data input and SDO acts as the data output.

SERIAL PORT OPTIONS

The serial port can support both MSB first and LSB first data formats. The LSB first bits (Register 0x000, Bit 6 and Bit 1) control this functionality. The default is MSB first (the LSB first bits = 0).

When the LSB first bits = 0 (MSB first), the instruction and data bits must be written from MSB to LSB. R/$\overline{W}$ is followed by A[14:0] as the instruction word, and D[7:0] is the data-word. When the LSB first bits = 1 (LSB first), the opposite is true. A[0:14] is followed by R/$\overline{W}$, which is subsequently followed by D[0:7].

The serial port supports a 3-wire or 4-wire interface. When the SDO active bits = 1 (Register 0x000, Bit 4 and Bit 3), a 4-wire interface with a separate input pin (SDIO) and output pin (SDO) is used. When the SDO active bits = 0, the SDO pin is unused and the SDIO pin is used for both input and output.

Multibyte data transfers can be performed as well. Hold the $\overline{CS}$ pin low for multiple data transfer cycles (eight SCLKs) after the first data transfer word following the instruction cycle. The first eight SCLKs following the instruction cycle read from or write to the register provided in the instruction cycle. For each additional eight SCLK cycles, the address is either incremented or decremented and the read/write occurs on the new register. Set the direction of the address using the address increment bits (Register 0x000, Bit 5 and Bit 2). When the address increment bits = 1, the multicycle addresses are incremented. When the address increment bits = 0, the addresses are decremented. A new write cycle can always be initiated by bringing $\overline{CS}$ high and then low again.

During writes to Register 0x0000 only, the chip tests the first nibble following the address phase, ignoring the second nibble. This is completed independently from the LSB first bit and ensures that there are extra clock cycles following the soft reset bits (Register 0x000, Bit 0 and Bit 7).

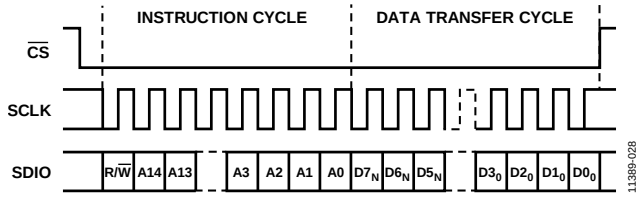


Figure 37. Serial Register Interface Timing, MSB First, Address Increment Bits = 0

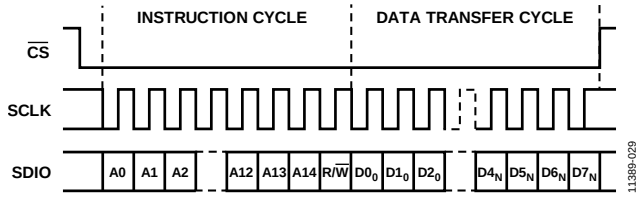


Figure 38. Serial Register Interface Timing, LSB First, Address Increment Bits = 1

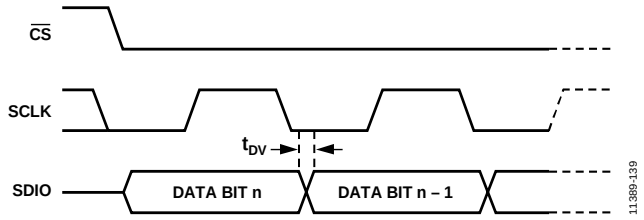


Figure 39. Timing Diagram for Serial Port Register Read

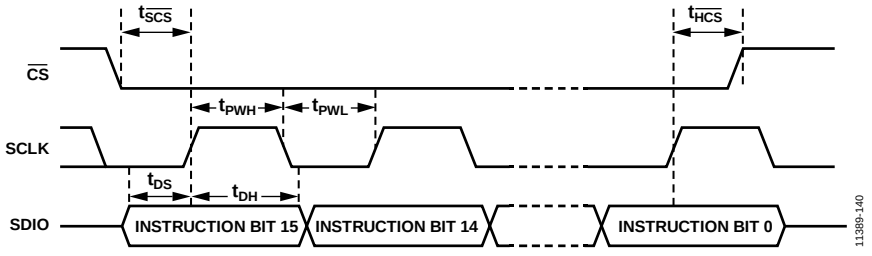


Figure 40. Timing Diagram for Serial Port Register Write

CHIP INFORMATION

Register 0x003 to Register 0x006 contain chip information, as shown in Table 14.

Table 14. Chip Information

Information	Description
Chip Type	The product is a high speed DAC represented by a code of 0x04 in Register 0x003.
Product ID	8 MSBs in Register 0x005 and 8 LSBs in Register 0x004. The product ID is 0x9154.
Product Grade	Register 0x006, Bits[7:4]. The product grade is 0x8.
Device Revision	Register 0x006, Bits[3:0]. The device revision is 0x9.

DEVICE SETUP GUIDE

Follow these steps to properly set up the AD9154:

1. Set up the SPI interface, power up necessary circuit blocks, make required writes to the configuration registers, and set up the DAC clocks (see Step 1: Start Up the DAC).
2. Set the digital features of the AD9154 (see Step 2: Digital Datapath).
3. Set up the JESD204B links (see Step 3: Transport Layer).
4. Set up the physical layer of the SERDES interface (see Step 4: Physical Layer).
5. Set up the data link layer of the SERDES interface (see Step 5: Data Link Layer).
6. Check for errors (see Step 6: Error Monitoring).
7. Enable any additional datapath features needed as described in Table 19.

A specific working start-up sequence example is given in the Example Start-Up Sequence section.

The register writes listed in Table 15 to Table 22 are necessary writes to set up the AD9154. Consider printing out this setup guide and filling in the Value column with appropriate variable values for the conditions of the desired application.

The value notation 0x without a specified value setting indicates register settings that must be filled in by the user. To fill in the unknown register values, select the correct settings for each variable listed in the Variable column of Table 15 to Table 22. The Description column describes how to set variables, or provides a link to a section where this procedure is described. Register settings with specified values are fixed settings to be used in all cases.

A variable is noted by concatenating multiple terms. For example, PdDACs is a variable corresponding to the value that is determined for Register 0x011[6:3] in the Device Setup Guide section.

STEP 1: START UP THE DAC

This section describes how to set up the SPI interface, power up necessary circuit blocks, as well as the required writes to the configuration registers, and how to set up the DAC clocks.

Table 15. Power-Up and DAC Initialization Settings

Addr.	Bit No.	Value[1]	Variable	Description
0x000		0xBD		Soft reset.
0x000		0x3C		Deassert reset, set 4-wire SPI.
0x011		0x		
	7	0		Power-up band gap.
	[6:3]		PdDACs	PdDACs = 0 if all four DACs are being used. If not, see the DAC Power-Down Setup section.
0x080	[7:6]		PdClocks	PdClocks = 0 if all four DACs are being used. If not, see the DAC Power-Down Setup section.
	1	0x1	DUTY_EN	Always set DUTY_EN = 1
0x081		0x	PdSysref	PdSysref = 0x00 for Subclass 1. PdSysref = 0x10 for Subclass 0. See the Subclass Setup section for details on subclass.

[1] 0x denotes a register value that the user must fill in. See the Variable and Description columns for information on selecting the appropriate register value.

The registers in Table 16 must be written to and the values changed from default for the device to work correctly. These registers must be written to after any soft reset, hard reset, or on a power-up.

Table 16. Required Device Configurations

Addr.	Value	Description
0x12D	0x8B	Digital datapath configuration
0x146	0x01	Digital datapath configuration
0x333	0x01	JESD interface configuration

If using the optional DAC PLL, also set the registers in Table 17.

Table 17. Optional DAC PLL Configuration Procedure

Addr.	Value[1]	Variable	Description
0x087	0x62		Optimal DAC PLL loop filter settings
0x088	0xC9		Optimal DAC PLL loop filter settings
0x089	0x0E		Optimal DAC PLL loop filter settings
0x08A	0x12		Optimal DAC PLL CP settings
0x08D	0x7B		Optimal DAC LDO settings for DAC PLL
0x1B0	0x00		Power DAC PLL blocks when power machine disabled
0x1B5	0xC9		Optimal DAC PLL VCO settings
0x1B9	0x24		Optimal DAC PLL calibration options settings
0x1BC	0x0D		Optimal DAC PLL block control settings
0x1BE	0x02		Optimal DAC PLL VCO power control settings
0x1BF	0x8E		Optimal DAC PLL VCO calibration settings
0x1C0	0x2A		Optimal DAC PLL lock counter length setting
0x1C1	0x2A		Optimal DAC PLL charge pump setting
0x1C4	0x7E		Optimal DAC PLL varactor settings
0x1C5	0x06		Optimal DAC PLL VCO settings
0x08B	0x	LODivMode	See the DAC PLL Setup section
0x08C	0x	RefDivMode	See the DAC PLL Setup section
0x085	0x	BCount	See the DAC PLL Setup section
Various	0x	LookUpVals	See the DAC PLL Setup section
0x083	0x10		Enable DAC PLL[2]

[1] 0x denotes a register value that the user must fill in. See the Variable and Description columns for information on selecting the appropriate register value.
[2] Verify that Register 0x084[1] reads back 1 after enabling the DAC PLL to indicate that the DAC PLL has locked.

STEP 2: DIGITAL DATAPATH

The digital datapath selects interpolation mode and the data format. Additional digital datapath capabilities are shown in Table 19.

Table 18. Digital Datapath Settings

Addr.	Bit No.	Value[1]	Variable	Description
0x112		0x	InterpMode	Select the interpolation mode; see the Interpolation section.
0x110	7	0x	DataFmt	DataFmt = 0 if twos complement; DataFmt = 1 if unsigned binary.

[1] 0x denotes a register value that the user must fill in. See the Variable and Description columns for information on selecting the appropriate register value.

There are a number of signal processing functions to be enabled if needed; these are in addition to the interpolation mode.

Table 19. Digital Datapath Signal Processing Functions

Feature	Default	Description
Digital Modulation	Off	Modulates the data with a desired IF carrier. See the Digital Datapath section.
Inverse Sinc	On	Improves pass-band flatness. See the Digital Datapath section.
Digital Gain	0 dB	Multiplies data by a factor to compensate inverse sinc usage or balance I/Q amplitude. See the Digital Datapath section.
Phase Adjust	Off	Used to balance I/Q phase. See the Digital Datapath section.
DC Offset	Off	Used to cancel LO leakage. See the Digital Datapath section.
Group Delay	0	Used to control overall latency. See the Digital Datapath section.
Downstream Protection	Off	Used to protect downstream components. See the Digital Datapath section.

STEP 3: TRANSPORT LAYER

This section describes how to set up the JESD204B links. The desired JESD204B operating mode determines the parameters. See the JESD204B Setup section for details.

Table 20. Transport Layer Settings

Addr.	Bit No.	Value[1]	Variable	Description
0x200		0x00		Power up the interface.
0x201		0x	UnusedLanes	See the JESD204B Setup section.
0x300		0x		
	6		CheckSumMode	See the JESD204B Setup section.
	3		DualLink	See the JESD204B Setup section.
	2		CurrentLink	See the JESD204B Setup section.
0x450		0x	DID	Set DID to match the device ID sent by the transmitter.
0x451		0x	BID	Set BID to match the bank ID sent by the transmitter.
0x452		0x	LID	Set LID to match the lane ID sent by the transmitter.
0x453		0x		
	7		Scrambling	See the JESD204B Setup section.
	[4:0]		$L - 1^2$	See the JESD204B Setup section.
0x454		0x	$F - 1^2$	See the JESD204B Setup section.
0x455		0x	$K - 1^2$	See the JESD204B Setup section.
0x456		0x	$M - 1^2$	See the JESD204B Setup section.
0x457		0x	$N - 1^2$	N = 16.
0x458		0x		
	5		Subclass	See the JESD204B Setup section.
	[4:0]		$Np - 1^2$	Np = 16.

Addr.	Bit No.	Value[1]	Variable	Description
0x459		0x		
	[7:5]		JESDVer	JESDVer = 1 for JESD204B, JESDVer = 0 for JESD204A.
	[4:0]		S – 1[2]	See the JESD204B Setup section.
0x45A	7	0x	HD	See the JESD204B Setup section.
	[4:0]		CF	CF = 0
0x45D		0x	Lane0Checksum	See the JESD204B Setup section.
0x46C		0x	Lanes	Deskew lanes.
0x476		0x	F	See the JESD204B Setup section.
0x47D		0x	Lanes	Enable lanes. See the JESD204B Setup section.

[1] 0x denotes a register value that the user must fill in. See the Variable and Description columns for information on selecting the appropriate register value.
[2] This JESD204B link parameter is programmed in n – 1 notation as noted. For example, if the setup requires L = 8 (8 lanes per link), program L – 1 or 7 into Register 0x453, Bits[4:0].

If using dual link, perform writes from Register 0x300 to Register 0x47D with CurrentLink = 0, and then repeat the same set of register writes with CurrentLink = 1. Write to Register 0x200 and Register 0x201 only once.

STEP 4: PHYSICAL LAYER

This section describes how to set up the physical layer of the SERDES interface. In this section, the input termination settings are configured along with the CDR sampling and SERDES PLL.

Table 21. Device Configurations and Physical Layer Settings

Addr.	Bit No.	Value[1]	Variable	Description
0x2A7		0x01		Autotune PHY setting
0x2AE		0x01		Autotune PHY setting
0x314		0x01		SERDES SPI configuration
0x230		0x		
	5		Halfrate	Set up the CDR; see the SERDES Clocks Setup section
	[4:2]	0x2		
	[2:1]		OvSmp	Set up the CDR; see the SERDES Clocks Setup section
0x206		0x00		Reset the CDR
0x206		0x01		Release the CDR reset
0x289		0x		
	2	1		SERDES PLL configuration
	[1:0]		PLLDiv	Set the CDR oversampling for PLL; see the SERDES Clocks Setup section
0x284		0x62		Optimal SERDES PLL loop filter
0x285		0xC9		Optimal SERDES PLL loop filter
0x286		0x0E		Optimal SERDES PLL loop filter
0x287		0x12		Optimal SERDES PLL CP
0x28A		0x7B		Optimal SERDES PLL VCO LDO
0x28B		0x00		Optimal SERDES PLL PD
0x290		0x89		Optimal SERDES PLL VCO
0x291		0x4C		Optimal SERDES PLL VCO
0x294		0x24		Optimal SERDES PLL CP
0x296		0x1B		Optimal SERDES PLL VCO
0x297		0x0D		Optimal SERDES PLL VCO
0x299		0x02		Optimal SERDES PLL PD
0x29A		0x8E		Optimal SERDES PLL VCO
0X29C		0x2A		Optimal SERDES PLL CP
0x29F		0x7E		Optimal SERDES PLL VCO
0x2A0		0x06		Configure SERDES PLL VCO
0x280		0x01		Enable SERDES PLL[2]
0x268		0x		
	[7:6]		EqMode	See the Equalization Mode Setup section
	[5:0]	0x22		Required value (default)

[1] 0x denotes a register value that the user must fill in. See the Variable and Description columns for information on selecting the appropriate register value.
[2] Verify that Register 0x281, Bit 0 reads back 1 after enabling the SERDES PLL to indicate that the SERDES PLL has locked.

STEP 5: DATA LINK LAYER

This section describes how to set up the data link layer of the SERDES interface. This section deals with SYSREF processing, setting deterministic latency, and establishing the link.

Table 22. Data Link Layer Settings

Address	Bit No.	Value[1]	Variable	Description
0x301		0x	Subclass	See the JESD204B Setup section.
0x304		0x	LMFCDel	See the Link Latency Setup section.
0x305		0x	LMFCDel	See the Link Latency section.
0x306		0x	LMFCVar	See the Link Latency Setup section.
0x307		0x	LMFCVar	See the Link Latency Setup section.
0x03A		0x01		Set sync mode = one-shot sync; see the Syncing LMFC Signals section for other sync options.
0x03A		0x81		Enable the sync machine.
0x03A		0xC1		Arm the sync machine.
SYSREF±				If Subclass = 1, ensure that at least one SYSREF± edge is sent to the device.[2]
0x308 to 0x30B		0x	XBarVals	If remapping lanes, set up crossbar; see the Crossbar Setup section.
0x334		0x	InvLanes	Invert the polarity of desired logical lanes. Bit x of InvLanes must be a 1 for each Logical Lane x to invert.
0x300		0x		Enable the links.
	6		CheckSum Mode	See the JESD204B Setup section.
	3		DualLink	See the JESD204B Setup section.
	[1:0]		EnLinks	EnLinks = 3 if DualLink = 1 (enables Link 0 and Link 1); EnLinks = 1 if DualLink = 0 (enables Link 0 only).

[1] 0x denotes a register value that the user must fill in. See the Variable and Description columns for information on selecting the appropriate register value.
[2] Verify that Register 0x03B, Bit 3 reads back 1 after sending at least one SYSREF± edge to the device to indicate that the LMFC sync machine has properly locked.

STEP 6: ERROR MONITORING

For JESD204B error monitoring, see the JESD204B Error Monitoring section. For other error checks, see the Interrupt Request Operation section.

DAC PLL SETUP

This section explains how to select appropriate LODivMode, RefDivMode, and BCount in the Step 1: Start Up the DAC section. These parameters depend on the desired DAC clock frequency (f_{DACCLK}) and DAC reference clock frequency (f_{REF}). When using the DAC PLL, the reference clock signal is applied to the CLK± differential pins, Pin 2 and Pin 3.

Table 23. DAC PLL LODivMode Settings

DAC Frequency Range (MHz)	LODIVMODE, Register 0x08B[1:0]
1500 to 2400	1
750 to 1500	2
420 to 750	3

Table 24. DAC PLL RefDivMode Settings

DAC PLL Reference Frequency (f_{REF}) (MHz)	Divide by (RefDivFactor)	REFDIVMODE, Register 0x08C[2:0]
35 to 80	1	0
80 to 160	2	1
160 to 320	4	2
320 to 640	8	3
640 to 1000	16	4

The VCO frequency (f_{VCO}) is related to the DAC clock frequency according to the following equation:

$$f_{VCO} = f_{DACCLK} \times 2^{LODivMode + 1}$$

where 6 GHz ≤ f_{VCO} ≤ 12 GHz.

BCount must be between 6 and 127 and is calculated based on f_{DACCLK} and f_{REF} as follows:

$$BCount = floor((f_{DACCLK})/(2 \times f_{REF}/RefDivFactor))$$

where $RefDivFactor = 2^{RefDivMode}$ (see Table 24).

Finally, to finish configuring the DAC PLL, set the VCO control registers up as described in Table 80 based on the VCO frequency (f_{VCO}).

For more information on the DAC PLL, see the DAC Input Clock Configurations section.

INTERPOLATION

The transmit path can use zero to three cascaded interpolation filters, which each provide a 2× increase in output data rate and a low-pass function. Table 25 shows the different interpolation modes and the respective usable bandwidth, along with the maximum f_{DATA} rate attainable.

Table 25. Interpolation Modes and Their Usable Bandwidth

Interpolation Mode	InterpMode	Usable Bandwidth
1× (bypass)	0x00	0.5× f_{DATA}
2×	0x01	0.4 × f_{DATA}
4×	0x03	0.4 × f_{DATA}
8×	0x04	0.4 × f_{DATA}

The usable bandwidth is defined for 1×, 2×, 4×, and 8× modes as the frequency band over which the filters have a pass-band ripple of less than ±0.001 dB and an image rejection of greater than 85 dB. For more information, see the Interpolation section.

JESD204B SETUP

This section explains how to select a JESD204B operating mode for a desired application. This in turn defines appropriate values for CheckSumMode, UnusedLanes, DualLink, CurrentLink, Scrambling, L, F, K, M, N, Np, Subclass, S, HD, Lane0Checksum, and Lanes needed for the Step 3: Transport Layer section.

Note that DualLink, Scrambling, L, F, K, M, N, Np, S, HD, and Subclass must have the same settings on the transmit side.

For a summary of how a JESD204B system works and what each parameter means, see the JESD204B Serial Data Interface section.

Available Operating Modes

Table 26. JESD204B Operating Modes (Single Link Only)

	Mode			
Parameter	**0**	**1**	**2**	**3**
M (Converter Count)	4	4	4	4
L (Lane Count)	8	8	4	2
S ((Samples per Converter) per Frame)	1	2	1	1
F ((Octets per Frame) per Lane)	1	2	2	4

Table 27. JESD204B Operating Modes (Single or Dual Link)

	Mode					
Parameter	**4**	**5**	**6**	**7**	**9**	**10**
M (Converter Count)	2	2	2	2	1	1
L (Lane Count)	4	4	2	1	2	1
S ((Samples per Converter) per Frame)	1	2	1	1	1	1
F ((Octets per Frame) per Lane)	1	2	2	4	1	2

For a particular application, the number of converters to use (M) and the f_{DATA} (DataRate) are known. The LaneRate and number of lanes (L) can be traded off as follows:

$$DataRate = (DACRate)/(InterpolationFactor)$$
$$LaneRate = (20 \times DataRate \times M)/L$$

where *LaneRate* is specified in Table 4.

Octets per frame per lane (F) and samples per convertor per frame (S) define how the data is packed. If F = 1, the high density (HD) setting must be set to 1 (HD = 1). Otherwise, set HD = 0.

Both the converter resolution (N) and the bits per sample (Np) must be set to 16. K must be set to 32 for Mode 0, Mode 4 and Mode 9. Other modes may use either K = 16 or K = 32.

DualLink

DualLink sets up two independent JESD204B links; each link can be reset independently. If DualLink is desired, set it to 1; if a single link is desired, set DualLink to 0. Note that Link 0 and Link 1 must have identical parameters. The operating modes available when using dual link mode are shown in Table 26. In addition to these operating modes, the modes in Table 27 may also be used when using single link mode.

Scrambling

Scrambling is a feature that makes the spectrum of the link data independent. This avoids spectral peaking and provides some protection against data dependent errors caused by frequency selective effects in the electrical interface. Set Scrambling to 1 if scrambling is being used, or to 0 if it is not.

Subclass

Subclass determines whether the latency of the device is deterministic, meaning it requires an external synchronization signal. See the Subclass Setup section for more information.

CurrentLink

To configure Link 0 or Link 1, set CurrentLink to either 0 or 1, respectively.

Lanes

Lanes enables and deskews particular lanes in two thermometer coded registers.

$$Lanes = (2^L) - 1$$

UnusedLanes

UnusedLanes turns off unused circuit blocks to save power. Each physical lane not being used (SERDINx±) must be powered off by writing a 1 to the corresponding bit of Register 0x201.

For example, if using Mode 6 in dual link mode and sending data on SERDIN0±, SERDIN1±, SERDIN4±, and SERDIN5±, set UnusedLanes = 0xCC to power off Physical Lane 2, Physical Lane 3, Physical Lane 6, and Physical Lane 7.

CheckSumMode

CheckSumMode must match the checksum mode used on the transmit side. If the checksum used is the sum of fields in the link configuration table, CheckSumMode = 0. If summing the registers containing the packed link configuration fields, CheckSumMode = 1. For more information on the how to calculate the two checksum modes, see the Lane0Checksum section.

Lane0Checksum

Lane0Checksum is used for error checking purposes to ensure that the transmitter is set up as expected.

If CheckSumMode = 0, the checksum is the lower 8 bits of the sum of the L − 1, M − 1, K − 1, N − 1, Np − 1, S − 1, Scrambling, HD, Subclass, and JESDVer variables.

If CheckSumMode = 1, Lane0Checksum is the lower 8 bits of the sum of Register 0x450 to Register 0x45A. Select whether to sum by fields or by registers, matching the setting on the transmitter.

DAC Power-Down Setup

As described in the Step 1: Start Up the DAC section, PdDACs must be set to 0 if all four converters are being used. If fewer than four converters are in use, the unused converters can be powered down. Use Table 28 determine which DACs are powered down based on the number of converters per link (M) and whether the device is in DualLink mode.

Table 28. DAC Power-Down Configuration Settings

M (Converters per Link)	DualLink	DACs to Power Down				PdDACs
		0	1	2	3	
1	0	0	1	1	1	0b0111
1	1	0	1	1	0	0b0110
2	0	0	0	1	1	0b0011
2	1	0	0	0	0	0b0000
4	0	0	0	0	0	0b0000

When using M = 1 in DualLink mode, set the I_TO_Q bit high to ensure data entering DAC Dual B is sent to the DAC 3 output.

PdClocks

If both DACs in DAC Dual B (DAC2 and DAC3) are powered down, the clock for DAC Dual B can be powered down. In this case, Register 0x080, Bits[7:6] = 0x1; otherwise, Register 0x080, Bits[7:6] = 0x0.

SERDES Clocks Setup

This section describes how to select the appropriate Halfrate, OvSmp, and PLLDiv settings in the Step 4: Physical Layer section. These parameters depend solely on the lane rate. The lane rate is established in the JESD204B Setup section.

Table 29. SERDES Lane Rate Configuration Settings

Lane Rate (Gbps) (see Table 4)	Halfrate	OvSmp	PLLDiv
CDR Oversampling Mode	0	1	2
CDR Full Rate Mode	0	0	1
CDR Half Rate Mode	1	0	0

Halfrate and OvSmp set how the clock detect and recover (CDR) circuit samples. See the SERDES PLL section for an explanation of how this circuit blocks works and the role of PLLDiv in the block.

EQUALIZATION MODE SETUP

Set EqMode = 1 for a low power setting. Select this mode if the insertion loss in the printed circuit board (PCB) is less than 12 dB. For insertion losses greater than 12 dB but less than 17.5 dB, set EqMode = 0. See the Equalization section for more information.

LINK LATENCY SETUP

This section describes the steps necessary to guarantee multichip deterministic latency in Subclass 1 and guarantee synchronization of links within a device in Subclass 0. Use this section to fill in LMFCDel, LMFCVar, and Subclass in the Step 5: Data Link Layer section. For more information, see the Syncing LMFC Signals section.

Subclass Setup

The AD9154 supports JESD204B Subclass 0 and Subclass 1 operation.

Subclass 1

Subclass 1 mode achieves deterministic latency and allows the synchronization of links to within the limits called out in Table 7. It requires an external SYSREF± signal accurately phase aligned to the DAC clock.

Subclass 0

Subclass 0 mode does not require any signal on the SYSREF± pins; leave these pins disconnected.

Subclass 0 still requires that all lanes arrive within the same LMFC cycle and the dual DACs must be synchronized to each other (they are synchronized to an internal clock instead of the SYSREF± signal when in Subclass 0 mode).

Set Subclass to 0 or 1 as desired.

Link Delay Setup

LMFCVar and LMFCDel impose delays such that all lanes in a system arrive in the same LMFC cycle.

The unit used internally for delays is the period of the internal processing clock (PClock), with a rate 1/40th of the lane rate. Delays that are not in PClock cycles must be converted before they are used.

Some useful internal relationships are defined below:

$$PClockPeriod = 40/LaneRate$$

The PClockPeriod is used to convert from time to PClock cycles when needed.

PClockFactor = 4/F (Frames per PClock)

The PClockFactor is used to convert from units of PClock cycles to frame clock cycles, which is required to set LMFCDel in Subclass 1.

PClocksPerMF= K/PClockFactor (PClocks per LMFC Cycle)

where *PClocksPerMF* is the number of PClock cycles in a multiframe cycle.

The values for PClockFactor and PClockPerMF are given per JESD204B mode in Table 30 and Table 31.

Table 30. PClockFactor and PClockPerMF Per LMFC

JESD204B Mode ID	0	1	2	3
PClockFactor	4	2	2	1
PClockPerMF (K = 32)	8	16	16	32
PClockPerMF (K = 16)	Not applicable	8	8	16

Table 31. PClockFactor and PClockPerMF Per LMFC

JESD204B Mode ID	4	5	6	7	9	10
PClockFactor	4	2	2	1	4	2
PClockPerMF (K = 32)	8	16	16	32	8	16
PClockPerMF (K = 16)	N/A[1]	8	8	16	N/A[1]	8

[1] N/A means not applicable.

With Known Delays

LMFCVar and LMFCDel can be calculated directly with information about all the system delays.

RxFixed (the fixed receiver delay in PClock cycles) and RxVar (the variable receiver delay in PClock cycles) are found in Table 8. TxFixed (the fixed transmitter delay in PClock cycles) and TxVar (the variable receiver delay in PClock cycles) can be found in the data sheet of the transmitter used. PCBFixed (the fixed PCB trace delay in PClock cycles) is extracted from the software. Because PCBFixed is generally much smaller than a PClock cycle, it can be omitted. For both the PCB and transmitter delays, convert the delays into PClock cycles.

For each lane,

MinDelayLane = floor(*RxFixed + TxFixed + PCBFixed*)
FALL_COUNT_DelayLane = ceiling(*RxFixed + RxVar + TxFixed + TxVar + PCBFixed*))

where, across lanes, links, and devices:
MinDelayLane is the minimum of all *MinDelayLane* values.
FALL_COUNT_Delay is the maximum of all *FALL_COUNT_DelayLane* values.

For safety, add a guard band of 1 PClock cycle to each end of the link delay, as shown in the following equations:

LMFCVar = (*FALL_COUNT_Delay* + 1) − (*MinDelay* − 1)

Note that if LMFCVar must be more than 10, the AD9154 cannot tolerate the variable delay in the system.

For Subclass 1,

LMFCDel = ((*MinDelay* − 1) × *PClockFactor*) % *K*

For Subclass 0,

LMFCDel = (*MinDelay* − 1) % *PClockPerMF*

Program the same LMFCDel and LMFCVar across all links and devices.

See the Link Delay Setup Example, With Known Delays section for an example calculation.

Without Known Delays

If comprehensive delay information is not available or known, the AD9154 can read back the link latency between the $LMFC_{RX}$ and the last arriving LMFC boundary in PClock cycles. Use this information to calculate LMFCVar and LMFCDel.

For each link on each device,

1. Power up the board.
2. Follow the steps in Table 15 through Table 22 in the Device Setup Guide section.
3. Set the subclass and perform a sync. For a one-shot sync, perform the writes in Table 32. See the Syncing LMFC Signals section for alternate sync modes.
4. Record DYN_LINK_LATENCY_0 (Register 0x302) as a value of Delay for that link and power cycle.
5. Record DYN_LINK_LATENCY_1 (Register 0x303) as a value of Delay for that link and power cycle.

Repeat Step 1 through Step 5 twenty times for each device in the system. Keep a single list of the Delay values across all runs and devices.

Table 32. Register Configuration and Procedure for One-Shot Sync

Addr.	Bit. No.	Value[1]	Variable	Description
0x301		0x	Subclass	Set subclass
0x03A		0x01		Set sync mode = one-shot sync
0x03A		0x81		Enable the sync machine
0x03A		0xC1		Arm the sync machine
SYSREF±				If Subclass = 1, ensure that at least one SYSREF± edge is sent to the device
0x300		0x		Enable the links
	6		ChkSmMd	See the JESD204B Setup section
	3		Dual Link	See the JESD204B Setup section
	[1:0]		EnLinks	EnLinks = 3 if in DualLink mode to enable Link 0 and Link 1; EnLinks = 1 if not in DualLink mode to enable Link 0

[1] 0x denotes a register value that the user must fill in. See the Variable and Description columns for information on selecting the appropriate register value.

Use the list of delay values to calculate LMFCDel and LMFCVar, but note that some of the delay values may need to be remapped first.

The maximum possible value for DYN_LINK_LATENCY_x is one less than the number of PClocks in a multiframe (PClocksPerMF). A rollover condition may be encountered, meaning the set of recorded delay values may roll over the edge of a multiframe. If so, Delay values may be near both 0 and PClocksPerMF. If this occurs, add PClocksPerMF to the set of values near 0.

For example, for Delay value readbacks of 6, 7, 0, and 1, the 0 and 1 Delay values must be remapped to 8 and 9, making the new set of Delay values 6, 7, 8, and 9.

Across power cycles, links, and devices,

- MinDelay is the minimum of all delay measurements.
- FALL_COUNT_Delay is the maximum of all delay measurements.

For safety, add a guard band of 1 PClock cycle to each end of the link delay and calculate LMFCVar and LMFCDel with the following equation:

$$LMFCVar = (FALL_COUNT_Delay + 1) - (MinDelay - 1)$$

Note that if LMFCVar must be more than 10, the AD9154 cannot tolerate the variable delay in the system.

For Subclass 1,

$$LMFCDel = ((MinDelay - 1) \times PClockFactor) \% K$$

For Subclass 0

$$LMFCDel = (MinDelay - 1) \% PClockPerMF$$

Program the same LMFCDel and LMFCVar across all links and devices.

See the Link Delay Setup Example, Without Known Delay section for an example calculation.

CROSSBAR SETUP

Registers 0x308 to Register 0x30B allow arbitrary mapping of physical lanes (SERDINx±) to logical lanes used by the SERDES deframers.

Table 33. Crossbar Registers

Address	Bits	Logical Lane
0x308	[2:0]	XBARVAL0
0x308	[5:3]	XBARVAL1
0x309	[2:0]	XBARVAL2
0x309	[5:3]	XBARVAL3
0x30A	[2:0]	XBARVAL4
0x30A	[5:3]	XBARVAL5
0x30B	[2:0]	XBARVAL6
0x30B	[5:3]	XBARVAL7

Write each XBARVALy with the number (x) of the desired physical lane (SERDINx±) from which to get data. By default, all logical lanes use the corresponding physical lane as their data source. For example, by default, XBARVAL0 = 0, meaning Logical Lane 0 receives data from Physical Lane 0 (SERDIN0±). If instead the user wants to use SERDIN4± as the source for Logical Lane 0, the user must write XBARVAL0 = 4.

JESD204B SERIAL DATA INTERFACE

JESD204B OVERVIEW

The JESD204B Setup section explains how to select a JESD204B operating mode. This section presents an overview of the inner workings of the AD9154 JESD204B receiver implementation.

The AD9154 has eight JESD204B data ports that receive data. The eight JESD204B ports can be configured as part of a single JESD204B link or as part of two separate JESD204B links (dual link mode) that share a single system reference (SYSREF±) and device clock (CLK±).

The JESD204B hardware protocol stack consists of three layers: the physical layer, the data link layer, and the transport layer. These sections of the hardware are described in subsequent sections, including information for configuring every aspect of the interface. Figure 41 shows the communication layers implemented in the AD9154 serial data interface to recover the clock and deserialize, descramble, and deframe the data before it is sent to the digital signal processing section of the device.

The physical layer establishes a reliable channel between the transmitter and the receiver, the data link layer unpacks the data into frames of octets and descrambles the data, and the transport layer receives the descrambled JESD204B frames and converts them to DAC input samples.

A number of JESD204B parameters (L, F, K, M, N, Np, S, and HD) define how the data is packed and instruct the device on how to turn the serial data into samples. These parameters are defined in detail in the Transport Layer section.

Only certain combinations of parameters are supported. Each supported combination is called a JESD204B operating mode. In total, there are 10 single link modes supported by the AD9154, as described in Table 34. In dual link mode, there are six supported modes, as described in Table 35.

Each of these tables shows the associated clock rates when the lane rate is 10 Gbps.

For a particular application, the number of converters to use (M) and the DataRate are known. The LaneRate and number of lanes (L) can be traded off as follows:

$$DataRate = (DACRate)/(InterpolationFactor)$$
$$LaneRate = (20 \times DataRate \times M)/L$$

where *LaneRate* must be between 1.42 Gbps and 10.64 Gbps.

Achieving and recovering synchronization of the lanes is very important. To simplify the interface to the transmitter, the AD9154 designates a master synchronization signal for each JESD204B link. In single link mode, SYNCOUT0± is the master signal for all lanes; in dual link mode, SYNCOUT0± is the master signal for Link 0, and SYNCOUT1± is used as the master signal for Link 1. If any lane in a link loses synchronization, a resynchronization request is sent to the transmitter via the SYNCOUT signal of the link. The transmitter stops sending data and instead sends synchronization characters to all lanes in that link until resynchronization is achieved.

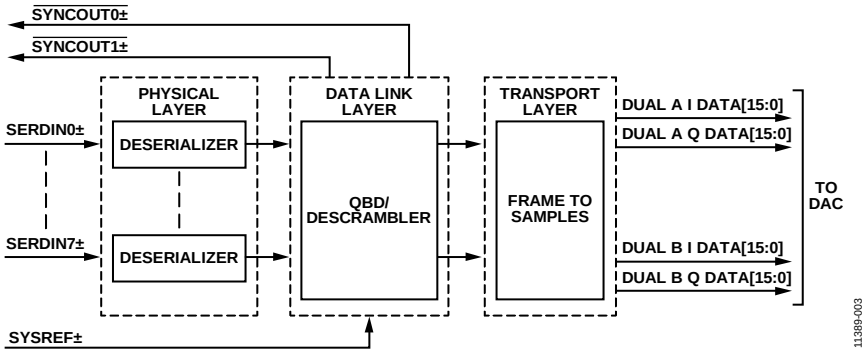


Figure 41. Functional Block Diagram of Serial Link Receiver

Table 34. Single Link JESD204B Operating Modes

	Mode									
Parameter	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**9**	**10**
M (Converter Counts)	4	4	4	4	2	2	2	2	1	1
L (Lane Counts)	8	8	4	2	4	4	2	1	2	1
S (Samples per Converter per Frame)	1	2	1	1	1	2	1	1	1	1
F (Octets per Frame per Lane)	1	2	2	4	1	2	2	4	1	2
Example Clocks for 10 Gbps Lane Rate										
PClock (MHz)	250	250	250	250	250	250	250	250	250	250
Frame Clock (MHz)	1000	500	500	250	1000	500	500	250	1000	500
Sample Clock (MHz)	1000	1000	500	250	1000	1000	500	250	1000	500

Table 35. Dual Link JESD204B Operating Modes for Link 0 and Link 1

	Mode					
Parameter	**4**	**5**	**6**	**7**	**9**	**10**
M (Converter Counts)	2	2	2	2	1	1
L (Lane Counts)	4	4	2	1	2	1
S (Samples per Converter per Frame)	1	2	1	1	1	1
F (Octets/Frame per Lane)	1	2	2	4	1	2
Example Clock for 10 Gbps Lane Rate						
PClock (MHz)	250	250	250	250	250	250
Frame Clock (MHz)	1000	500	500	250	1000	500
Sample Clock (MHz)	1000	1000	500	250	1000	500

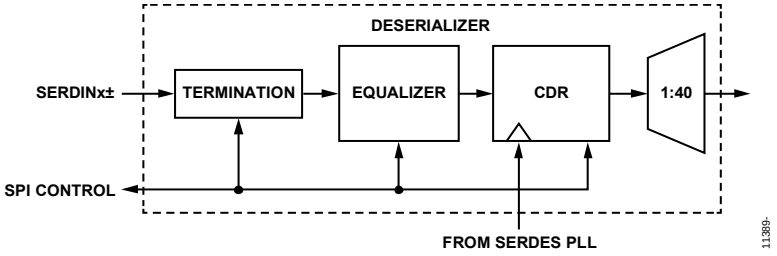


Figure 42. Deserializer Block Diagram

PHYSICAL LAYER

The physical layer of the JESD204B interface, hereafter referred to as the deserializer, has eight identical channels. Each channel consists of the terminators, an equalizer, a CDR circuit, and the 1:40 demux function (see Figure 42).

JESD204B data is input to the AD9154 via the SERDINx± 1.2 V differential input pins as per the JESD204B specification.

Power-Down Unused PHYs

Note that any unused and enabled lanes unnecessarily consume extra power. Each lane that is not in use (SERDINx±) must be powered off by writing a 1 to the corresponding bit of PHY_PD (Register 0x201).

Interface Power-Up and Input Termination

Before using the JESD204B interface, it must be powered up by setting Register 0x200[0] = 0. In addition, each physical lane that is not being used (SERDINx±) must be powered down. To do so, set the corresponding Bit x for Physical Lane x in Register 0x201 to 0 if the physical lane is being used, and to 1 if it is not being used.

The AD9154 autocalibrates the input termination to 50 Ω. Register 0x2A7 controls autocalibration for PHY 0, PHY 1, PHY 6, and PHY 7. Register 0x2AE controls autocalibration for PHY 2, PHY 3, PHY 4, and PHY 5. The PHY termination autocalibration routine is shown in Table 36.

Table 36. PHY Termination Autocalibration Routine

Address	Value	Description
0x2A7	0x01	Autotune PHY terminations
0x2AE	0x01	Autotune PHY terminations

The input termination voltage of the DAC is sourced externally via the V_{TT} pins (Pin 21, Pin 25, Pin 42, and Pin 46). Set V_{TT} by connecting it to SVDD12. It is recommended that the JESD204B inputs be ac-coupled to the JESD204B transmit device using 100 nF capacitors.

Receiver Eye Mask

The AD9154 complies with the JESD204B specification regarding the receiver eye mask and can capture data that complies with this mask without equalization. With equalization enabled, the AD9154 can reliably capture from signals with much smaller eye openings. Figure 43 shows the receiver eye mask normalized to the data rate interval with a 600 mV V_{TT} swing. See the JESD204B specification for more information regarding the eye mask and permitted receiver eye opening.

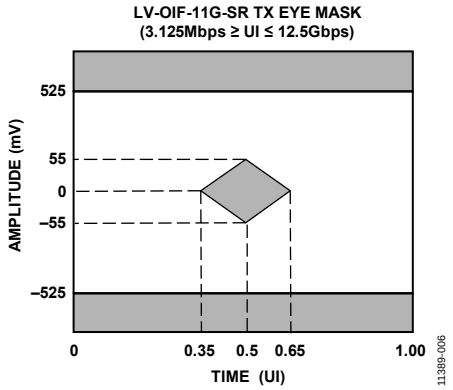


Figure 43. Receiver Eye Mask

Equalization

To compensate for signal integrity distortions for each PHY channel due to insertion loss caused by PCB trace characteristics, the AD9154 employs an easy to use, low power equalizer on each JESD204B channel. The AD9154 equalizers can compensate for insertion losses far greater than required by the JESD204B specification. The equalizers have two modes of operation determined by the EQ_POWER_MODE register setting in Register 0x268, Bits[7:6]. In low power mode (Register 0x268, Bits[7:6] = 2b'01) and operating at the maximum lane rate, the equalizer can compensate for up to 12 dB of insertion loss. In normal mode (Register 0x268, Bits[7:6] = 2b'00), the equalizer can compensate for up to 17.5 dB of insertion loss. This performance is shown in Figure 44 as an overlay to the JESD204B specification for insertion loss. Figure 44 shows the equalization performance at 10.0 Gbps, near the maximum baud rate for the AD9154.

Figure 45 and Figure 46 are provided as points of reference for hardware designers and show the insertion loss for various lengths of well laid out stripline and microstrip transmission lines on FR-4 material.

Low power mode is recommended if the insertion loss of the JESD204B PCB channels is less than that of the most lossy supported channel for lower power mode (shown in Figure 44). If the insertion loss is greater than that, but still less than that of the most lossy supported channel for normal mode (shown in Figure 44), use normal mode. At 10 Gbps operation, the equalizer in normal mode consumes about 4 mW more power per lane used than in low power equalizer mode. Note that either mode can be used in conjunction with transmitter preemphasis to ensure functionality and/or to optimize for power.

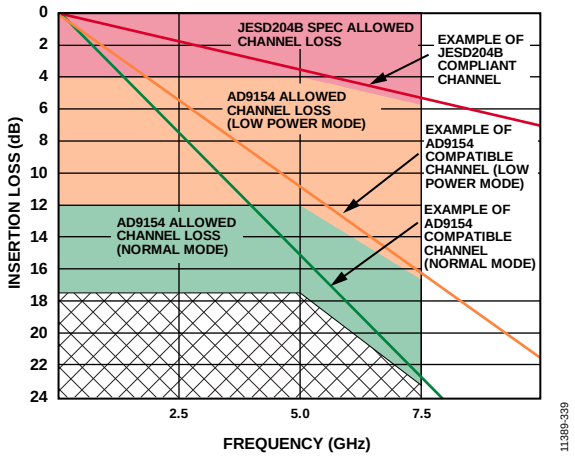


Figure 44. Insertion Loss Allowed

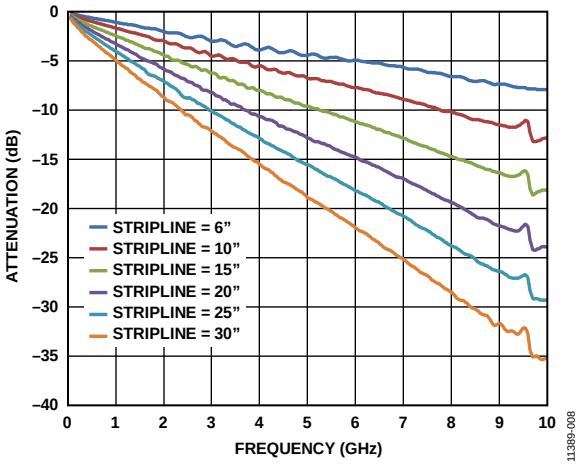


Figure 45. Insertion Loss of 50 Ω Striplines on FR-4

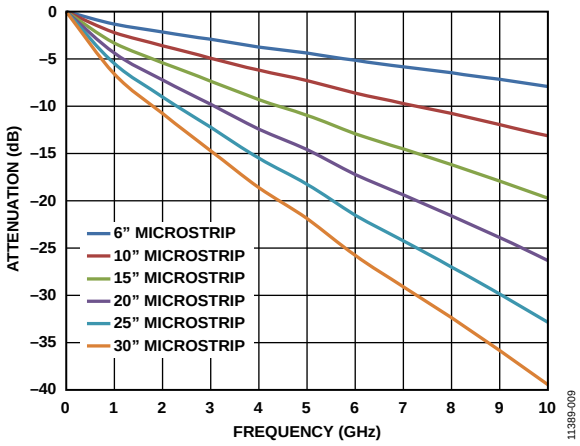


Figure 46. Insertion Loss of 50 Ω Microstrips on FR-4

Clock Multiplication Relationships

The following clocks rates are used throughout the rest of the JESD204B section. The relationship between any of the clocks can be derived from the following equations:

$$DataRate = (DACRate)/(InterpolationFactor)$$

$$LaneRate = (20 \times DataRate \times M)/L$$

$$ByteRate = LaneRate/10$$

where:
M is the JESD204B parameter for converters per link.
L is the JESD204B parameter for lanes per link.
F is the JESD204B parameter for octets per frame per lane.

This comes from 8-bit/10-bit encoding, where each byte is represented by 10 bits.

$$PClockRate = ByteRate/4$$

The processing clock is used for a quad-byte decoder.

$$FrameRate = ByteRate/F$$

where *F* is defined as (bytes per frame) per lane.

$$PClockFactor = FrameRate/PClockRate = 4/F$$

SERDES PLL

Functional Overview of the SERDES PLL

The independent SERDES PLL uses integer-N techniques to achieve clock synthesis. The entire SERDES PLL is integrated on chip, including the VCO and the loop filter. The SERDES PLL VCO operates over the range of 5.65 GHz to 12 GHz.

In the SERDES PLL, a VCO divider block divides the VCO clock by 2 to generate a 2.825 GHz to 6 GHz quadrature clock for the deserializer cores. This clock is the input to the CDR block described in the Clock and Data Recovery section.

The reference clock to the SERDES PLL is always running at a frequency of f_{REF} = 1/40 of the lane rate = PClockRate. This clock is divided by a DivFactor to deliver a clock to the PFD block that is between 35 MHz and 80 MHz. Table 37 includes the respective SERDES_PLL_DIV_MODE register settings for each of the desired DivFactor options available.

Table 37. SERDES PLL Divider Settings

LaneRate (Gbps) (see Table 4)	Divide by (DivFactor)	SPI_CDR_OVERSAMP Register 0x289, Bits[1:0]
CDR Oversampling Mode	1	2
CDR Full Rate Mode	2	1
CDR Half Rate Mode	4	0

Register 0x280 controls the synthesizer enable and recalibration.

To enable the SERDES PLL, first set the PLL divider register according to Table 37, then enable the SERDES PLL by writing Register 0x280, Bit 0 to 1.

Confirm that the SERDES PLL is working by reading Register 0x281. If Register 0x281, Bit 0 = 1, the SERDES PLL is locked. If Register 0x281, Bit 3 = 1, the SERDES PLL is successfully calibrated. If Register 0x281, Bit 4 or Register 0x281, Bit 5 are high, the PLL hits the upper or lower end of its calibration band and must be recalibrated by writing 0 and then 1 to Register 0x280, Bit 2.

SERDES PLL Fixed Register Writes

To optimize the SERDES PLL across all operating conditions, the following register writes to the following locations are recommended: 0x284, 0x285, 0x286, 0x287, 0x28A, 0x28B, 0x290, 0x291, 0x294, 0x296, 0x297, 0x299, 0x29A, 0x29C, 0x29F, and 0x2A0 as shown in Table 21.

SERDES PLL IRQ

SERDES PLL lock and lost signals are available as IRQ events. Use Register 0x01F, Bit 3 and Bit2 to enable these signals, and then use Register 0x023, Bit 3 and Bit 2 to read back their statuses and reset the IRQ signals. See the Interrupt Request Operation section for more information.

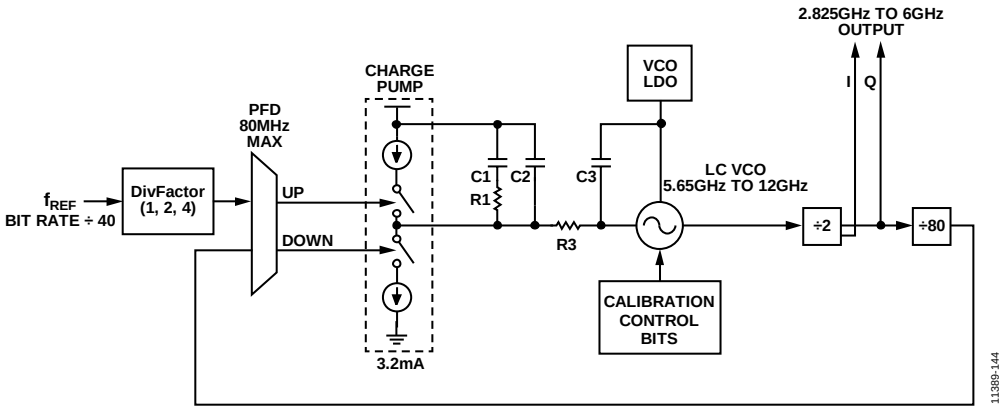


Figure 47. SERDES PLL Synthesizer Block Diagram Including VCO Divider Block

Clock and Data Recovery

The deserializer is equipped with a CDR circuit. Instead of recovering the clock from the JESD204B serial lanes, the CDR recovers the clocks from the SERDES PLL. The 2.825 GHz to 6 GHz output from the SERDES PLL, shown in Figure 47, is the input to the CDR.

Select a CDR sampling mode to generate the lane rate clock inside the device. If the desired lane rate is greater than 5.65 GHz, half rate CDR operation must be used. If the desired lane rate is less than 5.65 GHz, disable half rate operation. If the lane rate is less than 2.825 GHz, disable half rate and enable 2× oversampling to recover the appropriate lane rate clock. Table 38 breaks down the CDR sampling settings that must be set dependent on the LaneRate.

Table 38. CDR Operating Modes

LaneRate (Gbps) (See Table 4)	HALFRATE, Register 0x230, Bit 5	CDR_OVERSAMP, Register 0x230, Bit 1
CDR Oversampling Mode	0	1
CDR Full Rate Mode	0	0
CDR Half Rate Mode	1	0

The CDR circuit synchronizes the phase used to sample the data on each serial lane independently. This independent phase adjustment per serial interface ensures accurate data sampling and eases the implementation of multiple serial interfaces on a PCB.

After configuring the CDR circuit, reset it and then release the reset by writing 1 and then 0 to Register 0x206, Bit 0.

DATA LINK LAYER

The data link layer of the AD9154 JESD204B interface accepts the deserialized data from the PHYs and deframes and descrambles them so that data octets are presented to the transport layer to be put into DAC samples. The architecture of the data link layer is shown in Figure 48. It consists of a synchronization FIFO for each lane, a crossbar switch, a deframer, and descrambler.

The AD9154 can operate as a single link or dual link, high speed JESD204B serial data interface. When operating in dual link mode, configure both links with the same JESD204B parameters because they share a common device clock and system reference. All eight lanes of the JESD204B interface handle link layer communications such as code group synchronization, frame alignment, and frame synchronization.

The AD9154 decodes 8-bit/10-bit control characters, allowing marking of the start and end of the frame and alignment between serial lanes. Each AD9154 serial interface link can issue a synchronization request by setting its $\overline{\text{SYNCOUT0±}}$/$\overline{\text{SYNCOUT1±}}$ signal low. The synchronization protocol follows Section 4.9 of the JESD204B standard. When a stream of four consecutive /K/ symbols is received, the AD9154 deactivates the synchronization request by setting the $\overline{\text{SYNCOUT0±}}$/$\overline{\text{SYNCOUT1±}}$ signal high at the next internal LMFC rising edge. Then, it waits for the transmitter to issue a lane alignment sequence (ILAS). During the ILAS sequence, all lanes are aligned using the /A/ to /R/ character transition as described in the JESD204B Serial Link Establishment section. Elastic buffers hold early arriving lane data until the alignment character of the latest lane arrives. At this point, the buffers for all lanes are released and all lanes are aligned (see Figure 49).

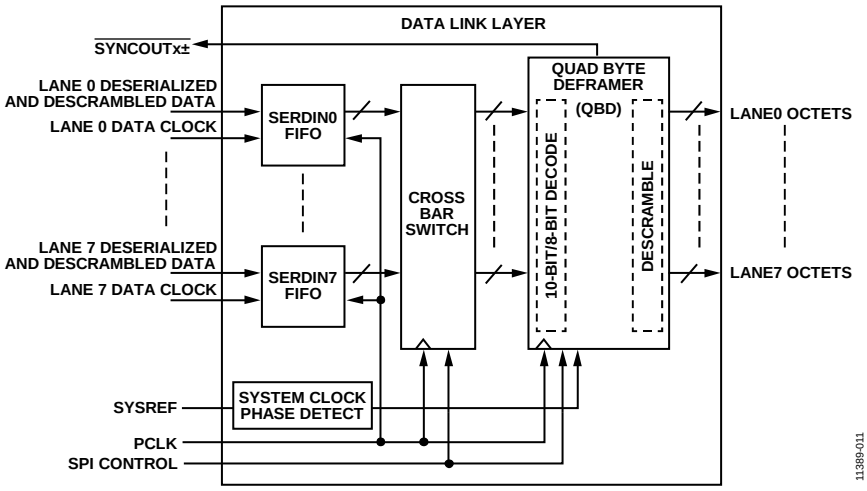


Figure 48. Data Link Layer Block Diagram

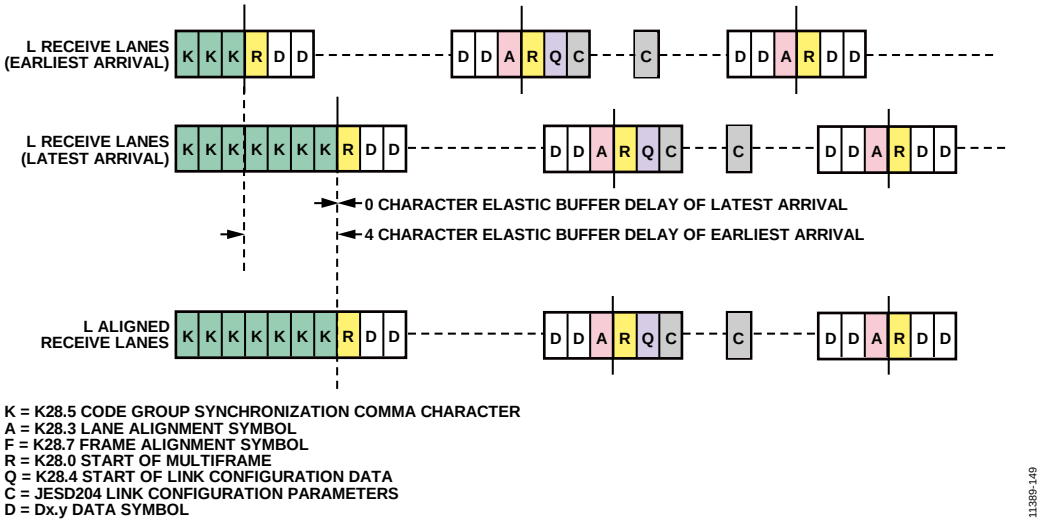


Figure 49. Lane Alignment During ILAS

JESD204B Serial Link Establishment

A brief summary of the high speed serial link establishment process for Subclass 1 is provided. See Section 5.3.3 of the JESD204B specifications document for complete details.

Step 1: Code Group Synchronization

Each receiver must locate K (K28.5) characters in its input data stream. After four consecutive K characters are detected on all link lanes, the receiver block deasserts the $\overline{\text{SYNCOUTx±}}$ signal to the transmitter block at the LMFC edge.

The transmitter captures the change in the $\overline{\text{SYNCOUTx±}}$ signal, and at a future transmitter LMFC rising edge, starts the initial ILAS.

Step 2: Initial Lane Alignment Sequence

The main purposes of this phase are to align all the lanes of the link and verify the parameters of the link.

Before the link is established, write each of the link parameters to the receiver device to designate how data is sent to the receiver block.

The ILAS consists of four or more multiframes. The last character of each multiframe is a multiframe alignment character, /A/. The first, third, and fourth multiframes are populated with predetermined data values. Note that Section 8.2 of the JESD204B specifications document describes the data ramp expected during ILAS. By default, the AD9154 does not require this ramp. Register 0x47E[0] can be set high to require the data ramp. The deframer uses the final /A/ of each lane to align the ends of the multiframes within the receiver. The second multiframe contains an R (K.28.0), Q (K.28.4), and then data corresponding to the link parameters. Additional multiframes can be added to the ILAS if needed by the receiver. By default, the AD9154 uses four multiframes in the ILAS (this can be changed in Register 0x478). If using Subclass 1, exactly four multiframes must be used.

After the last /A/ character of the last ILAS, the multiframe data begins streaming. The receiver adjusts the position of the /A/ character such that it aligns with the internal LMFC of the receiver at this point.

Step 3: Data Streaming

In this phase, data is streamed from the transmitter block to the receiver block.

Optionally, data can be scrambled. Scrambling does not start until the very first octet following the ILAS.

The receiver block processes and monitors the data it receives for errors, including

- Bad running disparity (8-bit/10-bit error)
- Not in table (8-bit/10-bit error)
- Unexpected control character
- Bad ILAS
- Interlane skew error (through character replacement)

If any of these errors exist, they are reported back to the transmitter in one of a few ways (see the JESD204B Error Monitoring section for details):

- Signal assertion. Resynchronization ($\overline{\text{SYNCOUTx±}}$ signal pulled low) is requested at each error for the last two errors. For the first three errors, an optional resynchronization request can be asserted when the error counter reaches a set error threshold.
- For the first three errors, each multiframe with an error in it causes a small pulse of programmable width on $\overline{\text{SYNCOUTx±}}$.
- Errors can optionally trigger an IRQ event, which can be sent to the transmitter.

See to the JESD204B Test Modes section for various test modes for verifying the link integrity.

Lane FIFO

The FIFOs in front of the crossbar switch and deframer synchronize the samples sent on the high speed serial data interface with the deframer clock by adjusting the phase of the incoming data. The FIFO absorbs timing variations between the data source and the deframer; this allows up to two PClock cycles of drift from the transmitter. The FIFO_STATUS_REG_0 register and FIFO_STATUS_REG_1 register (Register 0x30C and Register 0x30D, respectively) can be monitored to identify whether the FIFOs are full or empty.

Lane FIFO IRQ

An aggregate lane FIFO error bit is also available as an IRQ event. Use Register 0x01F[1] to enable the FIFO error bit, and then use Register 0x023[1] to read back its status and reset the IRQ signal. See the Interrupt Request Operation section for more information.

Crossbar Switch

Register 0x308 to Register 0x30B allow arbitrary mapping of physical lanes (SERDINx±) to logical lanes used by the SERDES deframers.

Table 39. Crossbar Registers

Address	Bits	Logical Lane
0x308	[2:0]	XBARVAL0
0x308	[5:3]	XBARVAL1
0x309	[2:0]	XBARVAL2
0x309	[5:3]	XBARVAL3
0x30A	[2:0]	XBARVAL4
0x30A	[5:3]	XBARVAL5
0x30B	[2:0]	XBARVAL6
0x30B	[5:3]	XBARVAL7

Write each XBARVALx with the number (x) of the desired physical lane (SERDINx±) from which to get data. By default, all logical lanes use the corresponding physical lane as their data source. For example, by default XBARVALx = 0, so Logical Lane 0 gets data from Physical Lane 0 (SERDIN0±). If instead the user wants to use SERDIN4± as the source for Logical Lane 0, the user must write XBARVALx = 4.

Lane Inversion

Register 0x334 allows the inversion of desired logical lanes, which can be used to ease routing of the SERDINx± signals. For each Logical Lane x, set Bit x of Register 0x334 to 1 to invert the lane.

Deframers

The AD9154 consists of two quad byte deframers (QBDs). Each deframer takes in the 8-bit/10-bit encoded data from the deserializer (via the crossbar switch), decodes it, and descrambles it into JESD204B frames before passing it to the transport layer to be converted to DAC samples. The deframer processes four symbols (or octets) per processing clock (PClock) cycle.

In single link mode, Deframer 0 is used exclusively and Deframer 1 remains inactive. In dual link mode, both QBDs are active and must be configured separately using the SEL_REG_MAP_1 bit (Register 0x300[2]) to select the link to be configured. The DUALLINK bit (Register 0x300[3]) =1 for dual link, or 0 for single link.

Each deframer uses the JESD204B parameters that the user has programmed into the register map to identify how the data has been packed and how to unpack it. The JESD204B parameters are discussed in detail in the Transport Layer section; many of the parameters are also needed in the transport layer to convert JESD204B frames into samples.

Descrambler

The AD9154 provides an optional descrambler block using a self synchronous descrambler with a polynomial: $1 + x^{14} + x^{15}$.

Enabling data scrambling reduces the spectral peaks produced when the same data octets repeat from frame to frame. It also makes the spectrum data independent so that possible frequency selective effects on the electrical interface do not cause data dependent errors. Descrambling of the data is enabled by setting the SCR bit (Register 0x453[7]) to 1.

Syncing LMFC Signals

The first step in guaranteeing synchronization across links and devices begins with syncing the LMFC signals. Each DAC dual (DAC Dual A = DAC0/DAC1 and DAC Dual B = DAC2/DAC3) has its own LMFC signal. In Subclass 0, the LMFC signals for each of the two links are synchronized to an internal processing clock. In Subclass 1, all LMFC signals (for all duals and devices) are synchronized to an external SYSREF signal.

SYSREF Signal

The SYSREF± signal is a differential source synchronous input that synchronizes the LMFC signals in both the transmitter and receiver in a JESD204B Subclass 1 system to achieve deterministic latency.

The SYSREF± signal is an active high signal sampled by the device clock rising edge. It is best practice that the device clock and the SYSREF± signals be generated by the same source, such as a device from the AD9516-0, AD9516-1, AD9516-2, AD9516-3, AD9516-4, and AD9516-5 family of clock generators, so that the phase alignment between the signals is fixed. When designing for optimum deterministic latency operation, consider the timing distribution skew of the SYSREF± signal in a multipoint link system (multichip).

The AD9154 supports a single pulse or step, or a periodic SYSREF± signal. The periodicity can be continuous, strobed, or gapped periodic.

To avoid this common-mode current draw, use a 50% duty-cycle periodic SYSREF± signal with ac coupling capacitors. If ac-coupled, the ac coupling capacitors combine with the resistors shown in Figure 50 to create a high-pass filter with an RC time constant of τ = RC. Select C such that τ > 4/SYSREF frequency. In addition, the edge rate must be sufficiently fast—at least 1.3 V/ns is recommended per Table 5.

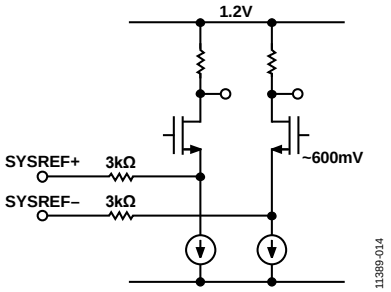


Figure 50. SYSREF± Input Circuit

LMFC Synchronization Modes Overview

The AD9154 supports various LMFC sync processing modes. These modes are one-shot, continuous, windowed continuous, and monitor modes. All sync processing modes perform a phase check to see that the LMFC is phase aligned to an alignment edge. In Subclass 1, the SYSREF± pulse acts as the alignment edge; in Subclass 0, an internal processing clock acts as the alignment edge. If the signals are not in phase, a clock rotation occurs to align the signals. The sync modes are described in the following sections. See the LMFC Synchronization Procedure section for details on the procedure for syncing the LMFC signals.

One-Shot Sync Mode (SYNCMODE = 0x1)

In one-shot sync mode, a phase check occurs on only the first alignment edge received after the sync machine is armed. If the phase error is larger than a specified window error tolerance, a phase adjustment occurs. Though an LMFC synchronization occurs only once, the SYSREF± signal can still be continuous.

Continuous Sync Mode (SYNCMODE = 0x2)

Continuous mode must only be used in Subclass 1 with a periodic SYSREF± signal. In continuous mode, a phase check/alignment occurs on every alignment edge.

Continuous mode differs from the one-shot mode in two ways. First, no SPI cycle is required to arm the device; the alignment edge seen after continuous mode is enabled results in a phase check. Second, a phase check (and when necessary, clock rotation) occurs on every alignment edge in continuous mode. The one caveat to the previous statement is that when a phase rotation cycle is underway, subsequent alignment edges are ignored until the logic lane is ready again.

The maximum acceptable phase error (in DAC clock cycles) between the alignment edge and the LMFC edge is set in the error window tolerance register. If continuous sync mode is used with a nonzero error window tolerance, then a phase check occurs on every SYSREF± pulse, but an alignment occurs only if the phase error is greater than the specified error window tolerance. If the jitter of the SYSREF± signal violates the setup and hold time specifications given in Table 5, and therefore causes phase error uncertainty, the error tolerance can be increased to avoid constant clock rotations. Note that this means that the latency is less deterministic by the size of the window. If the error window tolerance must be set above 3, Subclass 0 with a one-shot sync is recommended.

For debug purposes, SYNCARM (Register 0x03A, Bit 6) informs the user that alignment edges are being received in continuous mode. Because the SYNCARM bit is self cleared after an alignment edge is received, the user can arm the sync (SYNCARM (Register 0x03A, Bit 6) = 1), and then read back SYNCARM. If SYNCARM = 0, the alignment edges are being received and phase checks are occurring. Arming the sync machine in this mode does not affect the operation of the device.

One-Shot Then Monitor Sync Mode (SYNCMODE = 0x9)

In one-shot then monitor mode, the user can monitor the phase error in real time. Use this sync mode with a periodic SYSREF± signal. A phase check and alignment occurs on the first alignment edge received after the sync machine is armed. On all subsequent alignment edges, the phase is monitored and reported, but no clock phase adjustment occurs.

The phase error can be monitored on the CURRERR_L register, (Register 0x03C, Bits[7:0]). Immediately after an alignment occurs, CURRERRx = 0 to indicate that there is no difference between the alignment edge and the LMFC edge. On every subsequent alignment edge, the phase is checked. If the alignment is lost, the phase error is reported in the CURRERR_L register in DAC clock cycles. If the phase error is beyond the selected window tolerance (Register 0x034, Bits[2:0]), one bit of Register 0x03D, Bits[7:6] is set high, depending on whether the phase error is on low or high side.

When an alignment occurs, snapshots of the last phase error (Register 0x03C, Bits[3:0]) and the corresponding error flags (Register 0x03D, Bit 7 and Bit 6]) are placed into readable registers for reference (Register 0x038 and Register 0x039, respectively).

LMFC Synchronization Procedure

The procedure for enabling the LMFC sync is as follows:

1. Set Register 0x008 to 0x03 to sync the LMFC for both DAC duals (DAC0/DAC1 and DAC2/DAC3)
2. Set the desired sync processing mode. The sync processing mode settings are listed in Table 40.
3. For Subclass 1, set the error window according to the uncertainty of the SYSREF± signal relative to the DAC clock and the tolerance of the application for deterministic latency uncertainty. The sync window tolerance settings are given in Table 41.
4. Enable sync by writing 1 to SYNCENABLE (Register 0x03A, Bit 7).

5. If in one-shot mode, arm the sync machine by writing 1 to SYNCARM (Register 0x03A, Bit 6).
6. If in Subclass 1, ensure that at least one SYSREF± pulse is sent to the device.
7. Check the status by reading the following bit fields:
   a) REF_BUSY (Register 0x03B, Bit 7) = 0 to indicate that the sync logic is no longer busy.
   b) REF_LOCK (Register 0x03B, Bit 3) = 1 to indicate that the signals are aligned. This bit updates on every phase check.
   c) REF_WLIM (Register 0x03B, Bit 1) = 0 to indicate that the phase error is not beyond the specified error window. This bit updates on every phase check.
   d) REFROTA (Register 0x03B, Bit 2) = 1 if the phases were not aligned before the sync and an alignment occurred, this indicates that a clock alignment occurred. This bit is sticky and can be cleared only by writing to the SYNCCLRSTKY control bit (Register 0x03A, Bit 5).
   e) REF_TRIP (Register 0x03B, Bit 0) = 1 to indicate alignment edge received and phase check occurred. This bit is sticky and can be cleared only by writing to the SYNCCLRSTKY control bit (Register 0x03A, Bit 5).

Table 40. Sync Processing Modes

Sync Processing Mode	SYNCMODE (Register 0x03A, Bits[3:0])
One-shot	0x01
Continuous	0x02
One-shot then monitor	0x09

Table 41. Sync Window Tolerance

Sync Error Window Tolerance	ERRWINDOW (Register 0x034, Bits[2:0])
±1/2 DAC clock cycles	0x00
±1 DAC clock cycles	0x01
±2 DAC clock cycles	0x02
±3 DAC clock cycles	0x03

LMFC Sync IRQ

The sync status bits (REFLOCK, REFROTA, REFTRIP, and REFWLIM) are available as IRQ events.

Use Register 0x021, Bits[3:0] to enable the sync status bits for DAC Dual A (DAC0 and DAC1), and then use Register 0x025, Bits[3:0] to read back their statuses and reset the IRQ signals.

Use Register 0x022, Bits[3:0] to enable the sync status bits for DAC Dual B (DAC2 and DAC3), and then use Register 0x026, Bits[3:0] read back their statuses and reset the IRQ signals.

Deterministic Latency

JESD204B systems contain various clock domains distributed throughout each system. Data traversing from one clock domain to a different clock domain can lead to ambiguous delays in the JESD204B link. These ambiguities lead to nonrepeatable latencies across the link from power cycle to power cycle with each new link establishment. Section 6 of the JESD204B specification addresses the issue of deterministic latency with mechanisms defined as Subclass 1 and Subclass 2.

The AD9154 supports JESD204B Subclass 0 and Subclass 1 operation, but not Subclass 2. Write the subclass to Register 0x301, Bits[2:0] and once per link to Register 0x458, Bits[7:5].

Subclass 0

This mode does not require any signal on the SYSREF± pins, which can be left disconnected.

Subclass 0 still requires that all lanes arrive within the same LMFC cycle and the dual DACs must be synchronized to each other.

Minor Subclass 0 Caveats

Because the AD9154 requires an ILAS, the nonmultiple converter single lane (NMCDA-SL) case from the JESD204A specification is only supported when using the optional ILAS.

Error reporting using $\overline{\text{SYNCOUTx±}}$ is not supported when using Subclass 0 with F = 1.

Subclass 1

This mode gives deterministic latency and allows links to be synced to within ½ a DAC clock period. It requires an external SYSREF± signal that is accurately phase aligned to the DAC clock.

Deterministic Latency Requirements

Several key factors are required for achieving deterministic latency in a JESD204B Subclass 1 system.

- The SYSREF± signal distribution skew within the system must be less than the desired uncertainty.
- The SYSREF± setup and hold time requirements must be met for each device in the system.
- The total latency variation across all lanes, links and devices must be ≤10 PClock periods. This includes both variable delays and the variation in fixed delays from lane to lane, link to link, and device to device in the system.

Link Delay

The link delay of a JESD204B system is the sum of fixed and variable delays from the transmitter, channel and receiver, as shown in Figure 53.

For proper functioning, all lanes on a link must be read during the same LMFC period. Section 6.1 of the JESD204B specification states that the LMFC period must be larger than the maximum link delay.

For the AD9154, this is not necessarily the case; instead, the AD9154 uses a local LMFC for each link ($LMFC_{Rx}$) that can be delayed from the SYSREF aligned LMFC. Because the LMFC is periodic, this can account for any amount of fixed delay. As a result, the LMFC period must only be larger than the variation in the link delays, and the AD9154 can achieve proper performance with a smaller total latency. Figure 51 and Figure 52 show a case where the link delay is larger than an LMFC period. Note that it can be accommodated by delaying $LMFC_{Rx}$.

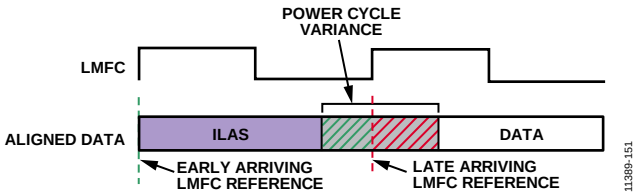


Figure 51. Link Delay > LMFC Period Example

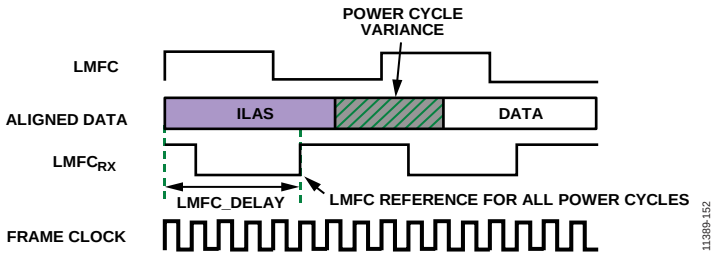


Figure 52. LMFC DELAY to Compensate for Link Delay > LMFC

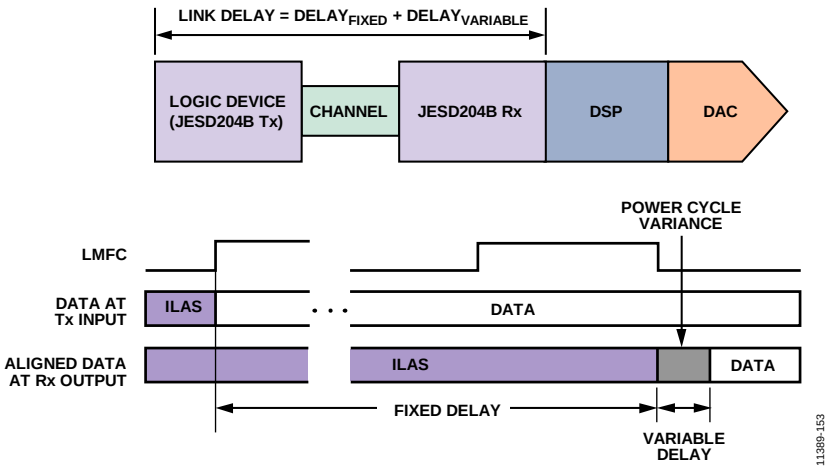


Figure 53. JESD204B Link Delay = Fixed Delay + Variable Delay

The method for setting the LMFCDel and LMFCVar is described in the Link Delay Setup section.

Setting LMFCDel appropriately ensures that all the corresponding data samples arrive in the same LMFC period. Then LMFCVar is written into the receive buffer delay (RBD) to absorb all link delay variation. This ensures that all data samples have arrived before reading. By setting these to fixed values across runs and devices, deterministic latency is achieved.

The RBD described in the JESD204B specification takes values from 1 to K frame clock cycles, while the RBD of the AD9154 takes values from 0 PClock cycles to 10 PClock cycles. As a result, up to 10 PClock cycles of total delay variation can be absorbed. Because LMFCVar is in PClock cycles, and LMFCDel is in frame clock cycles, a conversion between these two units is needed. The PClockFactor, or number of frame clock cycles per PClock cycle, is equal to 4/F. For more information on this relationship, see the Clock Multiplication Relationships section.

Two examples follow that show how to determine LMFCVar and LMFCDel. After they are calculated, write LMFCDel into both Register 0x304 and Register 0x305 for all devices in the system, and write LMFCVar to both Register 0x306 and Register 0x307 for all devices in the system.

Link Delay Setup Example, With Known Delays

All the known system delays can be used to calculate LMFCVar and LMFCDel as described in the Link Delay Setup section.

The example shown in Figure 54 is demonstrated in the following steps according to the procedure outlined in the Link Delay Setup section. Note that this example is in Subclass 1 to achieve deterministic latency, which has a PClockFactor (4/F) of 2 frame clock cycles per PClock cycle, and uses K = 32 (frames per multiframe). Because PCBFixed < PClockPeriod, PCBFixed is negligible in this example and is not included in the calculations.

1. Find the receiver delays using Table 8.
   RxFixed = 17 PClock cycles
   RxVar = 2 PClock cycles
2. Find the transmitter delays. The equivalent table in the example JESD204B core (implemented on a GTH or GTX transceiver on a Virtex-6 FPGA) states that the delay is 56 ± 2 byte clock cycles.
   Because the PClockRate = ByteRate/4 as described in the Clock Multiplication Relationships section, the transmitter delays in PClock cycles are:
   TxFixed = 54/4 = 13.5 PClock cycles
   TxVar = 4/4 = 1 PClock cycle
3. Calculate MinDelayLane as follows:
   MinDelayLane = *floor*(*RxFixed* + *TxFixed* + *PCBFixed*)
   = *floor*(17 + 13.5 + 0)
   = *floor*(30.5)
   MinDelayLane = 30
4. Calculate FALL_COUNT_DelayLane as follows:
   FALL_COUNT_DelayLane = ceiling(*RxFixed* + *RxVar* + *TxFixed* + *TxVar* + *PCBFixed*))
   = ceiling(17 + 2 + 13.5 + 1 + 0)
   = ceiling(33.5)
   FALL_COUNT_DelayLane = 34
5. Calculate LMFCVar as follows:
   LMFCVar = (*FALL_COUNT_DelayLane* + 1) − (*MinDelay* − 1)
   = (34 + 1) − (30 − 1) = 35 − 29
   LMFCVar = 6 PClock cycles
6. Calculate LMFCDel as follows:
   LMFCDel = ((*MinDelay* − 1) × *PClockFactor*) % K
   = ((30 − 1) × 2) % 32 = (29 × 2) % 32
   = 58 % 32
   LMFCDel = 26 frame clock cycles
7. Write LMFCDel to both Register 0x304 and Register 0x305 for all devices in the system. Write LMFCVar to both Register 0x306 and Register 0x307 for all devices in the system.

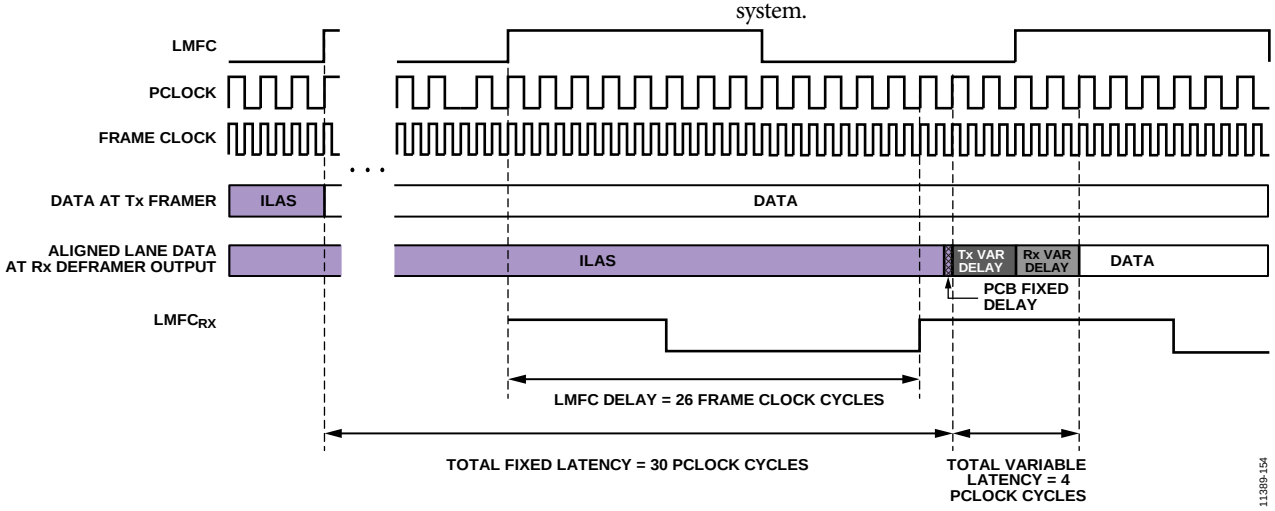


Figure 54. LMFC_DELAY Calculation Example

Link Delay Setup Example, Without Known Delay

If the system delays are not known, the AD9154 can read back the link latency between $LMFC_{RX}$ for each link and the SYSREF aligned LMFC. This information is used to calculate LMFCVar and LMFCDel, as shown in the Without Known Delays section.

Figure 56 shows how DYN_LINK_LATENCY_x (Register 0x302 and Register 0x303) provides a readback showing the delay (in PClock cycles) between $LMFC_{RX}$ and the transition from ILAS to the first data sample. By repeatedly power-cycling and taking this measurement, the minimum and maximum delays across power cycles can be determined and used to calculate LMFCVar and LMFCDel.

The example shown in Figure 56 is demonstrated in the following steps according to the procedure outlined in the Without Known Delays section. Note that this example is in Subclass 1 to achieve deterministic latency, which has a PClockFactor (FrameClockRate/ PClkRate) of 2 and uses K = 16; therefore PClocksPerMF = 8.

1. In Figure 56, for Link A, Link B, and Link C, the system containing the AD9154 (including the transmitter) is power cycled and configured 20 times. The AD9154 is configured as described in the Device Setup Guide section. As the point of this exercise is to determine LMFCDel and LMFCVar, the LMFCDel is programmed to 0 and the DYN_ LINK_LATENCY_x is read from Register 0x302 and Register 0x303 for Link 0 and Link 1, respectively. The variation in the link latency over the 20 runs is shown in Figure 56 in gray.
   - Link A gives readbacks of 6, 7, 0, and 1. Note that the set of recorded delay values rolls over the edge of a multiframe at the boundary K/PClockFactor = 8. Add PClocksPerMF = 8 to low set. Delay values range from 6 to 9.
   - Link B gives Delay values from 5 to 7.
   - Link C gives Delay values from 4 to 7.
2. Calculate the minimum of all Delay measurements across all power cycles, links, and devices:
   MinDelay = min(all *Delay* values) = 4
3. Calculate the maximum of all Delay measurements across all power cycles, links, and devices:
   FALL_COUNT_Delay = max(all *Delay* values) = 9
4. Calculate the total Delay variation (with guard band) across all power cycles, links, and devices:
   LMFCVar = (*FALL_COUNT_Delay* + 1) − (*MinDelay* − 1)
   = (9 + 1) − (4 − 1) = 10 − 3 = 7 PClock cycles
5. Calculate the minimum delay in frame clock cycles (with guard band) across all power cycles, links, and devices:
   LMFCDel = ((*MinDelay* − 1) × *PClockFactor*) % K
   = ((4 − 1) × 2) % 16 = (3 × 2) % 16
   = 6 % 16 = 6 frame clock cycles
6. Write LMFCDel to both Register and Register 0x305 for all devices in the system. Write LMFCVar to both Register 0x306 and Register 0x307 for all devices in the system.

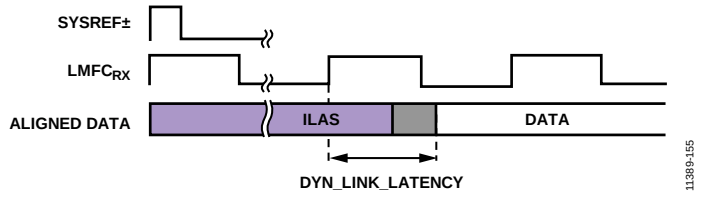


Figure 55. DYN_LINK_LATENCY Illustration

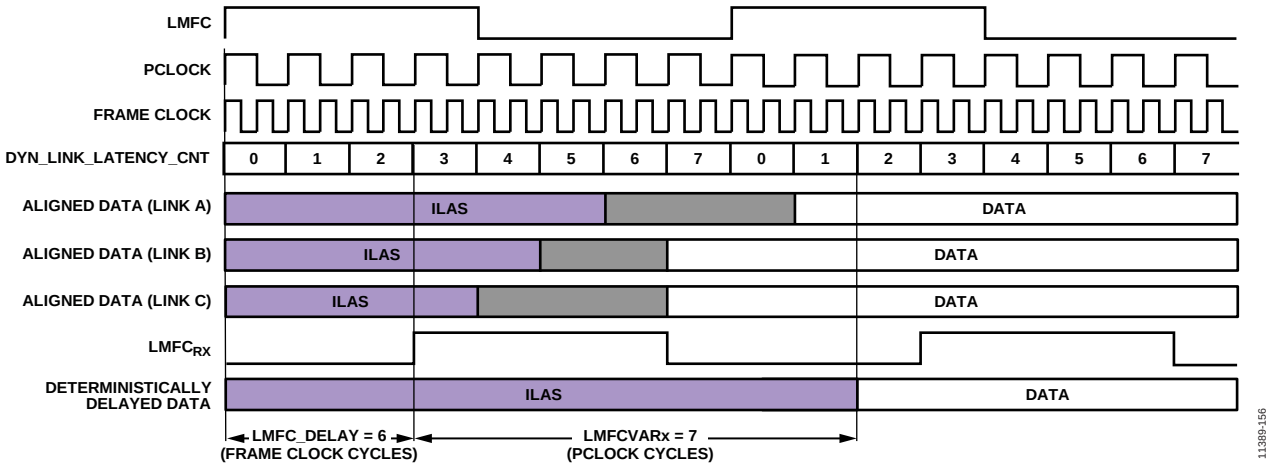


Figure 56. Multilink Synchronization Settings, Derived Method Example

TRANSPORT LAYER

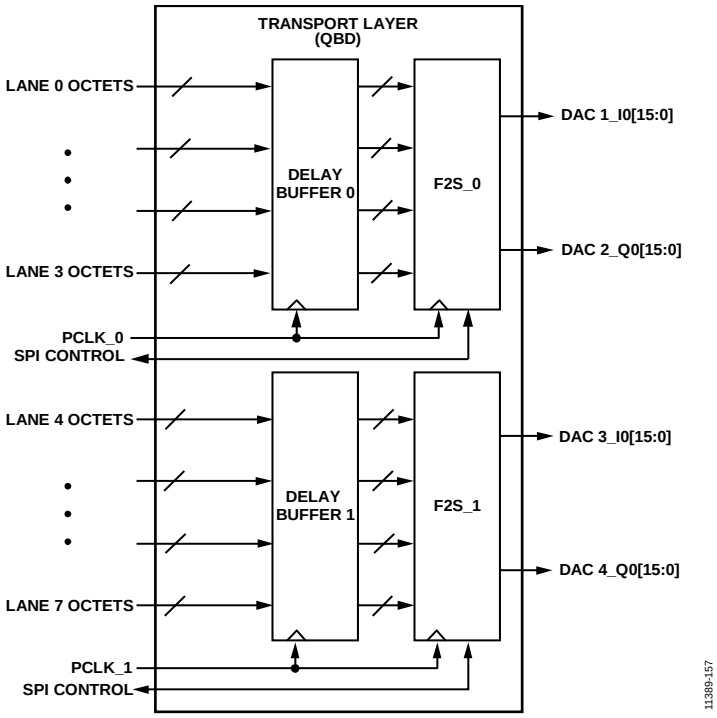


Figure 57. Transport Layer Block Diagram

The transport layer receives the descrambled JESD204B frames and converts them to DAC samples based on the programmed JESD204B parameters shown in Table 42. A number of device parameters are defined in Table 43.

Table 42. JESD204B Transport Layer Parameters

Parameter	Description
F	Number of octets per frame per lane: 1, 2, or 4.
K	Number of frames per multiframe. K = 32 if F = 1, K = 16 or 32 otherwise.
L	Number of lanes per converter device (per link), as follows. 1, 2, 4, or 8 (single link mode). 1, 2, or 4 (dual link mode).
M	Number of converters per device (per link), as follows. 1, 2, or 4 (single link mode). 1 or 2 (dual link mode).
S	Number of samples per converter, per frame: 1 or 2.

Table 43. JESD204B Device Parameters

Parameter	Description
CF	Number of control words per device clock per link. Not supported, must be 0.
CS	Number of control bits per conversion sample. Not supported, must be 0.
HD	High density user data format. Used when samples must be split across lanes. Set to 1 when F = 1, otherwise 0.
N	Converter resolution = 16.
N Prime (N')	Total number of bits per sample = 16.

Certain combinations of these parameters, called JESD204B operating modes, are supported by the AD9154. See Table 44 and Table 45 for a list of supported modes, along with their associated clock relationships.

Table 44. Single Link JESD204B Operating Modes

	Mode									
Parameter	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**9**	**10**
M (Converter Count)	4	4	4	4	2	2	2	2	1	1
L (Lane Count)	8	8	4	2	4	4	2	1	2	1
S (Samples per Converter per Frame)	1	2	1	1	1	2	1	1	1	1
F (Octets per Frame, per Lane)	1	2	2	4	1	2	2	4	1	2
K[1] (Frames per Multiframe)	32	16/32	16/32	16/32	32	16/32	16/32	16/32	32	16/32
HD (High Density)	1	0	0	0	1	0	0	0	1	0
N (Converter Resolution)	16	16	16	16	16	16	16	16	16	16
NP (Bits per Sample)	16	16	16	16	16	16	16	16	16	16
Example Clocks for 10 Gbps Lane Rate										
PClock Rate (MHz)	250	250	250	250	250	250	250	250	250	250
Frame Clock Rate (MHz)	1000	500	500	250	1000	500	500	250	1000	500
Data Rate (MHz)	1000	1000	500	250	1000	1000	500	250	1000	500

[1] K must be 32 in Mode 0, Mode 4, and Mode 9. K can be 16 or 32 in all other modes.

Table 45. Dual Link JESD204B Operating Modes for Link 0 and Link 1

	Mode					
Parameter	**4**	**5**	**6**	**7**	**9**	**10**
M (Converter Count)	2	2	2	2	1	1
L (Lane Count)	4	4	2	1	2	1
S (Samples per Converter per Frame)	1	2	1	1	1	1
F (Octets per Frame per Lane)	1	2	2	4	1	2
K[1] (Frames per Multiframe)	32	16/32	16/32	16/32	32	16/32
HD (High Density)	1	0	0	0	1	0
N (Converter Resolution)	16	16	16	16	16	16
NP (Bits per Sample)	16	16	16	16	16	16
Example Clocks for 10 Gbps Lane Rate						
PClock Rate (MHz)	250	250	250	250	250	250
Frame Clock Rate (MHz)	1000	500	500	250	1000	500
Data Rate (MHz)	1000	1000	500	250	1000	500

[1] K must be 32 in Mode 4 and Mode 9. K can be 16 or 32 in all other modes.

Configuration Parameters

The AD9154 modes refer to the link configuration parameters for L, K, M, N, NP, S, and F. Table 46 provides the description and addresses for these settings.

Table 46. Configuration Parameters

JESD204B Setting	Description	Address [Bits]
L – 1	Number of lanes – 1.	0x453[4:0]
F[1] – 1	Number of ((octets per frame) per lane) – 1.	0x454[7:0]
K – 1	Number of frames per multiframe – 1.	0x455[4:0]
M – 1	Number of converters – 1.	0x456[7:0]
N – 1	Converter bit resolution – 1.	0x457[4:0]
NP – 1	Bit packing per sample – 1.	0x458[4:0]
S – 1	Number of ((samples per converter) per frame) – 1.	0x459[4:0]
HD	High density format. Set to 1 if F = 1. Leave at 0 if F ≠ 1.	0x45A[7]
F[1]	F parameter, in ((octets per frame) per lane).	0x476[7:0]
DID	Device ID. Match the device ID sent by the transmitter.	0x450[7:0]
BID	Bank ID. Match the bank ID sent by the transmitter.	0x451[3:0]
LID0	Lane ID for Lane 0. Match the lane ID sent by the transmitter on Logical Lane 0.	0x452[4:0]
JESDVER	JESD Version. Match the version sent by the transmitter (0x0 = JESD204A, 0x1 = JESD204B).	0x459[7:5]

[1] F must be programmed in two places: Register 0x454, Bits[7:0] and Register 0x459, Bits[7:0].

Data Flow Through the JESD204B Receiver

The link configuration parameters determine how the serial bits on the JESD204B receiver interface are deframed and passed on to the DACs as data samples. Figure 58 shows a detailed flow of the data through the various hardware blocks for Mode 4 (L = 4, M = 2, S = 1, F = 1). Simplified flow diagrams for all other modes are provided in Figure 59 through Figure 67.

Single and Dual Link Configuration

The AD9154 uses the settings contained in Table 44 and Table 45. Mode 0 to Mode 10 can be used for single link operation. Mode 4 to Mode 10 can also be used for dual link operation.

To use dual link mode, set DUALLINK (Register 0x300, Bit 3) to 1. In dual link mode, Link 1 must be programmed with identical parameters to Link 0. To write to Link 1, set SEL_REG_MAP_1 (Register 0x300, Bit 2) to 1.

If single link mode is being used, a small amount of power can be saved by powering down the output buffer for SYNCOUT1±, which can be done by setting Register 0x203, Bit 0 = 1.

Checking Proper Configuration

As a convenience, the AD9154 provides some quick configuration checks. Register 0x030, Bit 5 is high if an illegal LMFCDELx is used. Register 0x030, Bit 3 is high if an unsupported combination of L, M, F, or S is used. Register 0x030, Bit 2 is high if an illegal K is used. Register 0x030, Bit 1 is high if an illegal SUBCLASSV is used.

Deskewing and Enabling Logical Lanes

After proper configuration, the logical lanes must be deskewed and enabled to capture data.

Set Bit x in Register 0x46C to 1 to deskew Logical Lane x and to 0 if that logical lane is not being used. Then, set Bit x in Register 0x47D to 1 to enable Logical Lane x and to 0 if that logical lane is not being used.

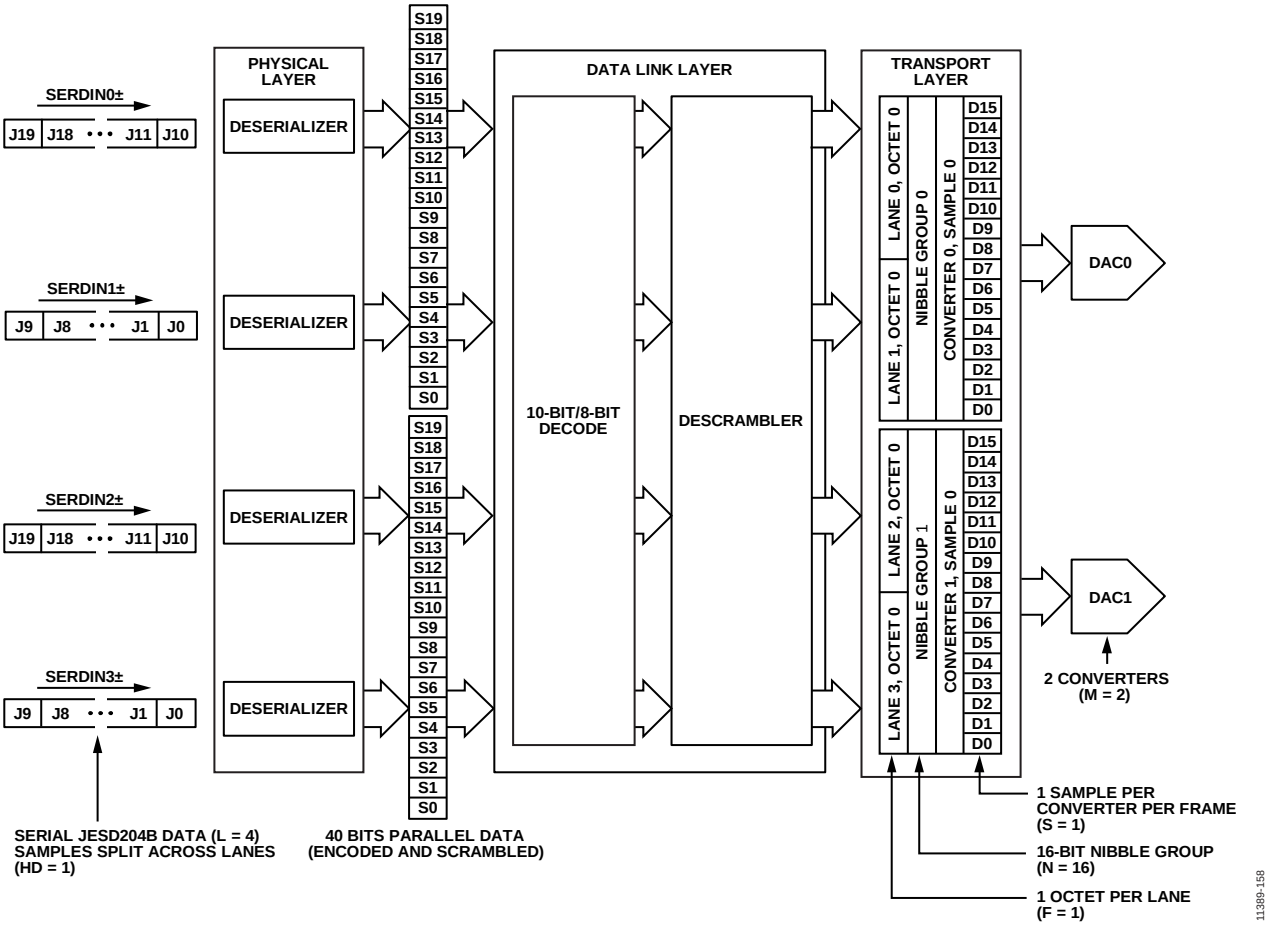


Figure 58. JESD204B Mode 4 Data Deframing

Mode Configuration Maps

Table 47 through Table 56 contain the SPI configuration maps for each mode shown in Figure 59 through Figure 67. Figure 59 through Figure 67 show the associated data flow through the deframing process of the JESD204B receiver for each of the modes. Mode 0 to Mode 10 apply to single link operation. Mode 4 to Mode 10 also apply to dual link operation. Register 0x300 must be set accordingly for single or dual link operation.

Additional details regarding all the SPI registers can be found in the Register Summary and Register Details sections.

Table 47. SPI Configuration Map—Register Settings for JESD204B Parameters for Mode 0

Address	Setting	Description
0x453	0x07 or 0x87	Register 0x453, Bit 7 = 0 or 1: scrambling disabled or enabled; Register 0x453[4:0] = 0x7: L = 8 lanes per link
0x454	0x00	Register 0x454, Bits[7:0] = 0x00: F = 1 octet per frame
0x455	0x1F	Register 0x455, Bits[4:0] = 0x1F: K = 32 frames per multiframe
0x456	0x03	Register 0x456, Bits[7:0] = 0x03: M = 4 converters per link
0x457	0x0F	Register 0x457, Bits[7:6] = 0x0: always set $\overline{CS}$ = 0; Register 0x457, Bits[4:0] = 0xF: N = 16, always set to 16-bit resolution
0x458	0x0F or 0x2F	Register 0x458, Bits[7:5] = 0x0 or 0x1: Subclass 0 or Subclass 1; Register 0x458, Bits[4:0] = 0xF: NP = 16 bits per sample
0x459	0x20	Register 0x459, Bits[7:5] = 0x1: JESD204B version; Register 0x459, Bits[4:0] = 0x0: S = 1 sample per converter per frame
0x45A	0x80	Register 0x45A, Bit 7 = 1: HD = 1; Register 0x45A, Bits[4:0] = 0x00: always set CF = 0
0x46C	0xFF	Register 0x46C, Bits[7:0] = 0xFF: Deskew Link Lane 0 to Link Lane 7
0x476	0x01	Register 0x476, Bits[7:0] = 0x01: F = 1 octet per frame
0x47D	0xFF	Register 0x47D, Bits[7:0] = 0xFF: Enable Link Lane 0 to Link Lane 7

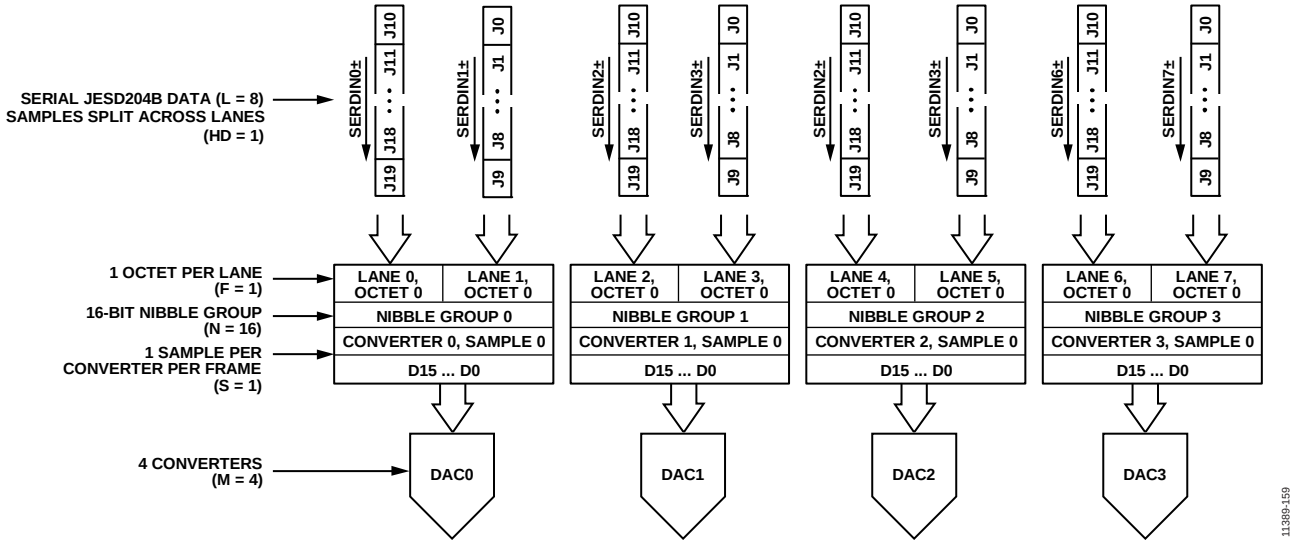


Figure 59. JESD204B Mode 0 Data Deframing

Table 48. SPI Configuration Map—Register Settings for JESD204B Parameters for Mode 1

Address	Setting	Description
0x453	0x07 or 0x87	Register 0x453, Bit 7 = 0 or 1: scrambling disabled or enabled; Register 0x453, Bits[4:0] = 0x7: L = 8 lanes per link
0x454	0x01	Register 0x454, Bits[7:0] = 0x01: F = 2 octets per frame
0x455	0x0F or 0x1F	Register 0x455, Bits[4:0] = 0x0F or 0x1F: K = 16 or 32 frames per multiframe
0x456	0x03	Register 0x456, Bits[7:0] = 0x03: M = 4 converters per link
0x457	0x0F	Register 0x457, Bits[7:6] = 0x0: always set CS = 0; Register 0x457, Bits[4:0] = 0x0F: N = 16, always set to 16-bit resolution
0x458	0x0F or 0x2F	Register 0x458, Bits[7:5] = 0x0 or 0x1: Subclass 0 or Subclass 1, Register 0x458, Bits[4:0] = 0xF: NP = 16 bits per sample
0x459	0x21	Register 0x459, Bits[7:5] = 0x1: set to JESD204B version, Register 0x459, Bits[4:0] = 0x1: S = 2 samples per converter per frame
0x45A	0x00	Register 0x45A, Bit 7 = 0: HD = 0; Register 0x45A, Bits[4:0] = 0x00: always set CF = 0
0x46C	0xFF	Register 0x46C, Bits[7:0] = 0xFF: deskew Link Lane 0 to Link Lane 7
0x476	0x02	Register 0x476, Bits[7:0] = 0x02: F = 2 octets per frame
0x47D	0xFF	Register 0x47D, Bits[7:0] = 0xFF: 8 lanes enabled, set one bit per lane to enable

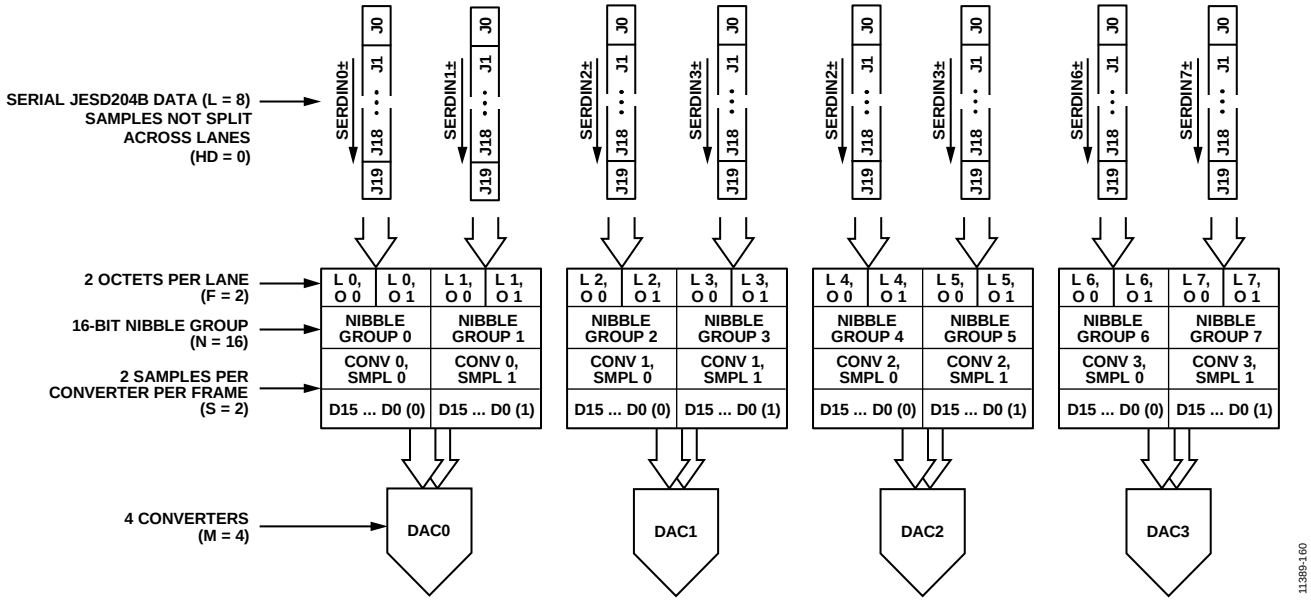


Figure 60. JESD204B Mode 1 Data Deframing

Table 49. SPI Configuration Map—Register Settings for JESD204B Parameters for Mode 2

Address	Setting	Description
0x453	0x03 or 0x83	Register 0x453, Bit 7 = 0 or 1: scrambling disabled or enabled; Register 0x453, Bits[4:0] = 0x3: L = 4 lanes per link
0x454	0x01	Register 0x454, Bits[7:0] = 0x01: F = 2 octets per frame
0x455	0x0F or 0x1F	Register 0x455, Bits[4:0] = 0x0F or 0x1F: K = 16 or 32 frames per multiframe
0x456	0x03	Register 0x456, Bits[7:0] = 0x03: M = 4 converters per link
0x457	0x0F	Register 0x457, Bits[7:6] = 0x0: always set CS = 0; Register 0x457, Bits[4:0] = 0x0F: N = 16, always set to 16-bit resolution
0x458	0x0F or 0x2F	Register 0x458, Bits[7:5] = 0x0 or 0x1: Subclass 0 or Subclass 1, Register 0x458, Bits[4:0] = 0xF: NP = 16 bits per sample
0x459	0x20	Register 0x459, Bits[7:5] = 0x1: set to JESD204B version, Register 0x459, Bits[4:0] = 0x0: S = 1 sample per converter per frame
0x45A	0x00	Register 0x45A, Bit 7 = 0: HD = 0; Register 0x45A, Bits[4:0] = 0x00: always set CF = 0
0x46C	0x0F	Register 0x46C, Bits[7:0] = 0xFF: Deskew Link Lane 0 to Link Lane 3
0x476	0x02	Register 0x476, Bits[7:0] = 0x02: F = 2 octets per frame
0x47D	0x0F	Register 0x47D, Bits[7:0] = 0x0F: enable Link Lane 0 to Link Lane 3

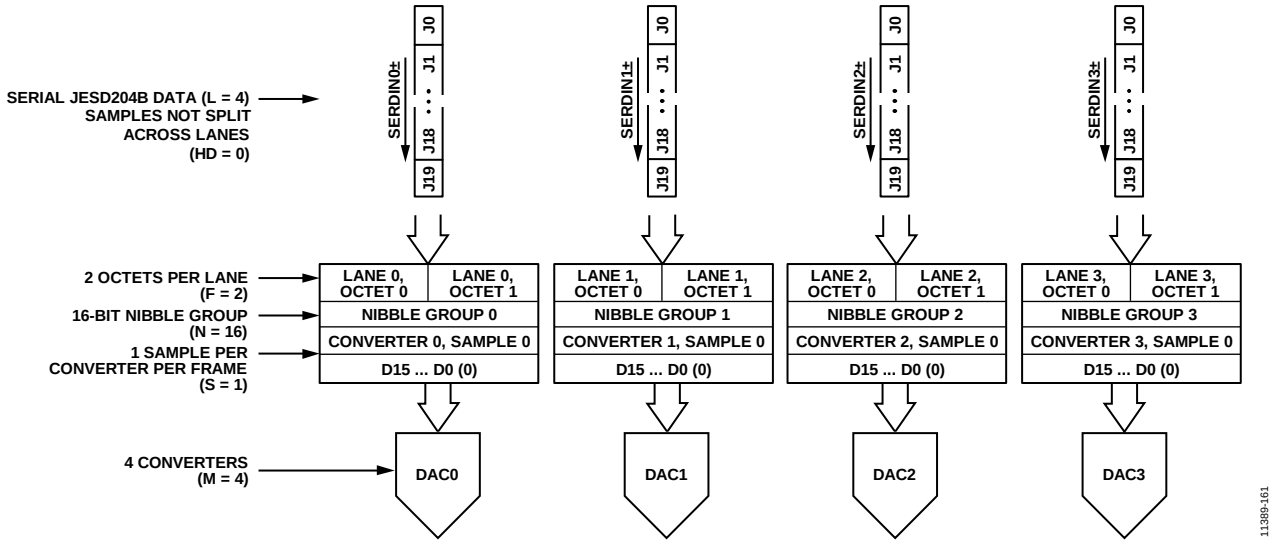


Figure 61. JESD204B Mode 2 Data Deframing

Table 50. SPI Configuration Map—Register Settings for JESD204B Parameters for Mode 3

Address	Setting	Description
0x453	0x01 or 0x81	Register 0x453, Bit 7 = 0 or 1: scrambling disabled or enabled; Register 0x453, Bits[4:0] = 0x1: L = 2 lanes per link
0x454	0x03	Register 0x454, Bits[7:0] = 0x03: F = 4 octets per frame
0x455	0x0F or 0x1F	Register 0x455, Bits[4:0] = 0x0F or 0x1F: K = 16 or 32 frames per multiframe
0x456	0x03	Register 0x456, Bits[7:0] = 0x03: M = 4 converters per link
0x457	0x0F	Register 0x457, Bits[7:6] = 0x0: always set CS = 0; Register 0x457, Bits[4:0] = 0x0F: N = 16, always set to 16-bit resolution
0x458	0x0F or 0x2F	Register 0x458, Bits[7:5] =0x0 or 0x1: Subclass 0 or Subclass 1, Register 0x458, Bits[4:0] = 0xF: NP = 16 bits per sample
0x459	0x20	Register 0x459, Bits[7:5] = 0x1: set to JESD204B version, Register 0x459, Bits[4:0] = 0x0: S = 1 sample per converter per frame
0x45A	0x00	Register 0x45A, Bit 7 = 0: HD = 0; Register 0x45A, Bits[4:0] = 0x00: always set CF = 0
0x46C	0x03	Register 0x46C, Bits[7:0] = 0xFF: deskew Link Lane 0 and Link Lane 1
0x476	0x04	Register 0x476, Bits[7:0] = 0x04: F = 4 octets per frame
0x47D	0x03	Register 0x47D, Bits[7:0] = 0x03: enable Link Lane 0 and Link Lane 1

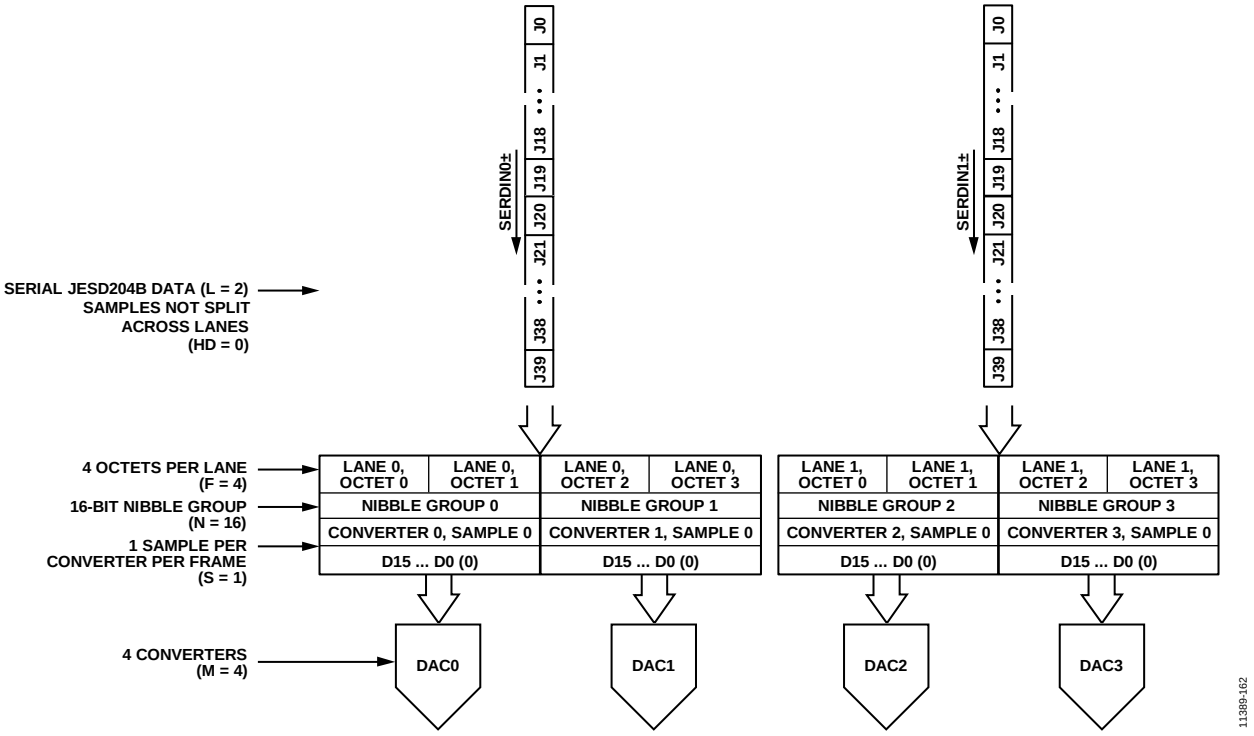


Figure 62. JESD204B Mode 3 Data Deframing

Table 51. SPI Configuration Map—Register Settings for JESD204B Parameters for Mode 4

Address	Setting	Description
0x453	0x03 or 0x83	Register 0x453, Bit 7 = 0 or 1: scrambling disabled or enabled; Register 0x453, Bits[4:0] = 0x3: L = 4 lanes per link
0x454	0x00	Register 0x454, Bits[7:0] = 0x00: F = 1 octet per frame
0x455	0x0F or 0x1F	Register 0x455, Bits[4:0] = 0x0F or 0x1F: K =16 or 32 frames per multiframe
0x456	0x01	Register 0x456, Bits[7:0] = 0x01: M = 2 converters per link
0x457	0x0F	Register 0x457, Bits[7:6] = 0x0: always set CS = 0; Register 0x457, Bits[4:0] = 0x0F: N = 16, always set to 16-bit resolution
0x458	0x0F or 0x2F	Register 0x458, Bits[7:5] = 0x0 or 0x1: Subclass 0 or Subclass 1, Register 0x458, Bits[4:0] = 0xF: NP = 16 bits per sample
0x459	0x20	Register 0x459, Bits[7:5] = 0x1: set to JESD204B version, Register 0x459, Bits[4:0] = 0x0: S = 1 sample per converter per frame
0x45A	0x01	Register 0x45A, Bit 7 = 1: HD = 1; Register 0x45A, Bits[4:0] = 0x00: always set CF = 0
0x46C	0x0F	Register 0x46C, Bits[7:0] = 0xFF: deskew Link Lane 0 to Link Lane 3
0x476	0x01	Register 0x476, Bits[7:0] = 0x01: F = 1 octet per frame
0x47D	0x0F	Register 0x47D, Bits[7:0] = 0x0F: Enable Link Lane 0 to Link Lane 3

See Figure 58 for an illustration of the AD9154 JESD204B Mode 4 data deframing process.

Table 52. SPI Configuration Map—Register Settings for JESD204B Parameters for Mode 5

Address	Setting	Description
0x453	0x03 or 0x83	Register 0x453, Bit 7 = 0 or 1: scrambling disabled or enabled; Register 0x453, Bits[4:0] = 0x3: L = 4 lanes per link
0x454	0x01	Register 0x454, Bits[7:0] = 0x01: F = 2 octets per frame
0x455	0x0F or 0x1F	Register 0x455, Bits[4:0] = 0x0F or 0x1F: K = 16 or 32 frames per multiframe
0x456	0x01	Register 0x456, Bits[7:0] = 0x01: M = 2 converters per link
0x457	0x0F	Register 0x457, Bits[7:6] = 0x0: always set CS = 0; Register 0x457, Bits[4:0] = 0x0F: N = 16, always set to 16-bit resolution
0x458	0x0F or 0x2F	Register 0x458, Bits[7:5] = 0x0 or 0x1: Subclass 0 or Subclass 1, Register 0x458, Bits[4:0] = 0xF: NP = 16 bits per sample
0x459	0x21	Register 0x459, Bits[7:5] = 0x1: set to JESD204B version, Register 0x459, Bits[4:0] = 0x1: S = 2 samples per converter per frame
0x45A	0x00	Register 0x45A, Bit 7 = 0: HD = 0; Register 0x45A, Bits[4:0] = 0x00: always set CF = 0
0x46C	0x0F	Register 0x46C, Bits[7:0] = 0xFF: deskew Link Lane 0 to Link Lane 3
0x476	0x02	Register 0x476, Bits[7:0] = 0x02: F = 2 octets per frame
0x47D	0x0F	Register 0x47D, Bits[7:0] = 0x0F: Enable Link Lane 0 to Link Lane 3

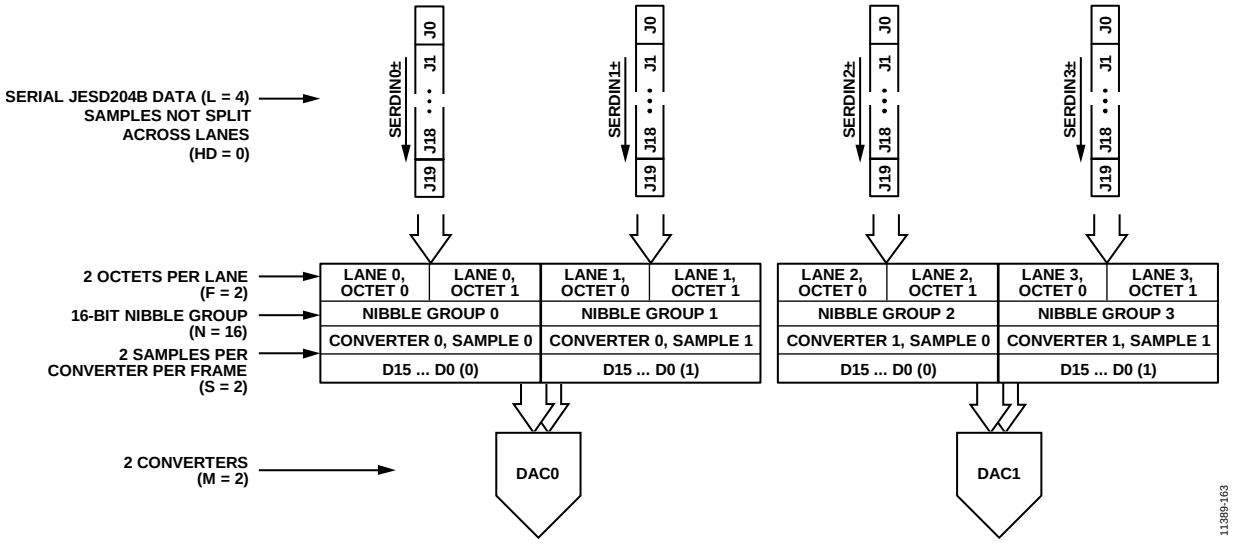


Figure 63. JESD204B Mode 5 Data Deframing

Table 53. SPI Configuration Map—Register Settings for JESD204B Parameters for Mode 6

Address	Setting	Description
0x453	0x01 or 0x81	Register 0x453, Bit 7 = 0 or 1: scrambling disabled or enabled, Register 0x453, Bits[4:0] = 0x1: L = 2 lanes per link
0x454	0x01	Register 0x454, Bits[7:0] = 0x01: F = 2 octets per frame
0x455	0x0F or 0x1F	Register 0x455, Bits[4:0] = 0x0F or 0x1F: K = 16 or 32 frames per multiframe
0x456	0x01	Register 0x456, Bits[7:0] = 0x01: M = 2 converters per link
0x457	0x0F	Register 0x457, Bits[7:6] = 0x0: always set CS = 0; Register 0x457, Bits[4:0] = 0x0F: N = 16, always set to 16-bit resolution
0x458	0x0F or 0x2F	Register 0x458, Bits[7:5] = 0x0 or 0x1: Subclass 0 or Subclass 1, Register 0x458, Bits[4:0] = 0xF: NP = 16 bits per sample
0x459	0x20	Register 0x459, Bits[7:5] = 0x1: set to JESD204B version, Register 0x459, Bits[4:0] = 0x0: S = 1 sample per frame
0x45A	0x00	Register 0x45A, Bit 7 = 0: HD = 0; Register 0x45A, Bits[4:0] = 0x00: always set CF = 0
0x46C	0x03	Register 0x46C, Bits[7:0] = 0xFF: deskew Link Lane 0 and Link Lane 1
0x476	0x02	Register 0x476, Bits[7:0] = 0x02: F = 2 octets per frame
0x47D	0x03	Register 0x47D, Bits[7:0] = 0x03: Enable Link Lane 0 and Link Lane 1

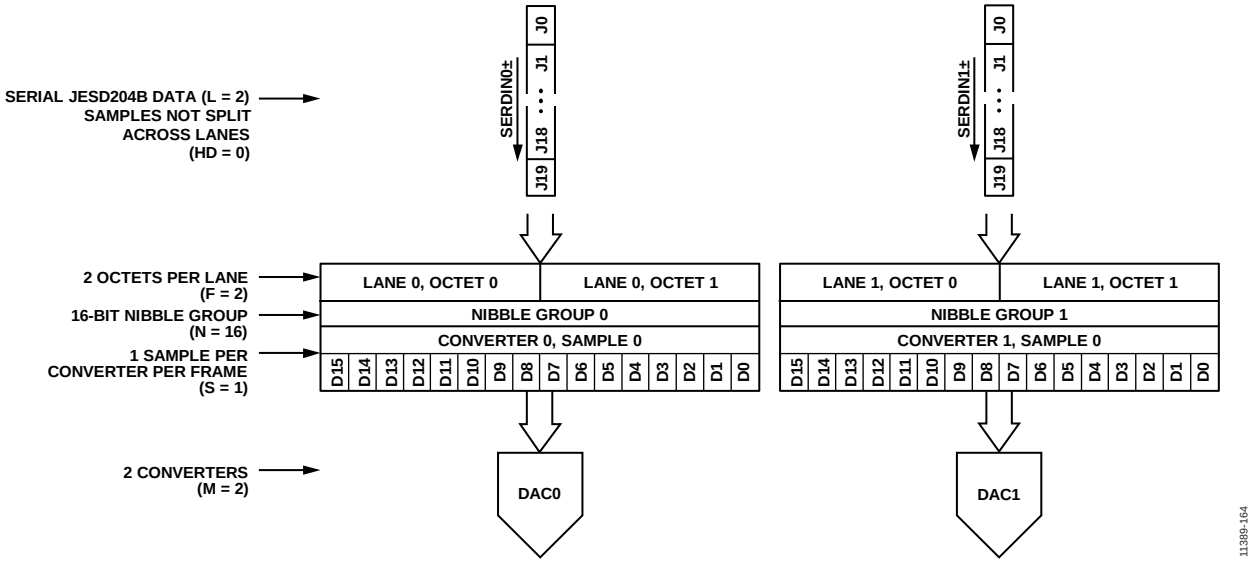


Figure 64. JESD204B Mode 6 Data Deframing

Table 54. SPI Configuration Map—Register Settings for JESD204B Parameters for Mode 7

Address	Setting	Description
0x453	0x00 or 0x80	Register 0x453, Bit 7 = 0 or 1: scrambling disabled or enabled, Register 0x453, Bits[4:0] = 0x0: L = 1 lane per link
0x454	0x03	Register 0x454, Bits[7:0] = 0x03: F = 4 octets per frame
0x455	0x0F or 0x1F	Register 0x455, Bits[4:0] = 0x0F or 0x1F: K = 16 or 32 frames per multiframe
0x456	0x01	Register 0x456, Bits[7:0] = 0x01: M = 2 converters per link
0x457	0x0F	Register 0x457, Bits[7:6] = 0x0: always set CS = 0; Register 0x457, Bits[4:0] = 0x0F: N = 16, always set to 16-bit resolution
0x458	0x0F or 0x2F	Register 0x458, Bits[7:5] = 0x0 or 0x1: Subclass 0 or Subclass 1, Register 0x458, Bits[4:0] = 0xF: NP = 16 bits per sample
0x459	0x20	Register 0x459, Bits[7:5] = 0x1: set to JESD204B version, Register 0x459, Bits[4:0] = 0x0: S = 1 sample per converter per frame
0x45A	0x00	Register 0x45A, Bit 7 = 0: HD = 0; Register 0x45A, Bits[4:0] = 0x00: always set CF = 0
0x46C	0x01	Register 0x46C, Bits[7:0] = 0xFF: Deskew Link Lane 0
0x476	0x04	Register 0x476, Bits[7:0] = 0x04: F = 4 octets per frame
0x47D	0x01	Register 0x47D, Bits[7:0] = 0x01: Enable Link Lane 0

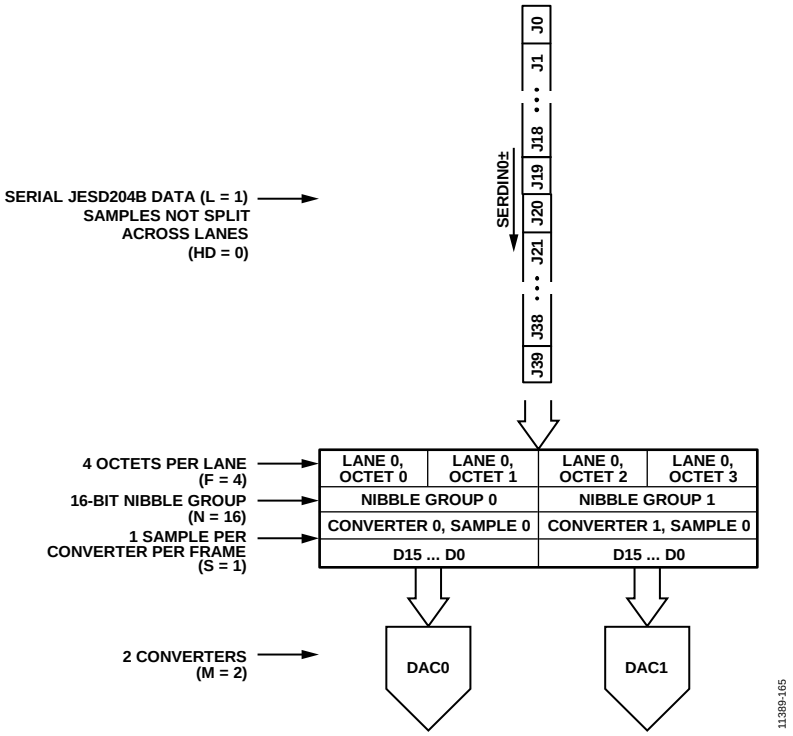


Figure 65. JESD204B Mode 7 Data Deframing

Table 55. SPI Configuration Map—Register Settings for JESD204B Parameters for Mode 9

Address	Setting	Description
0x453	0x01 or 0x81	Register 0x453, Bit 7 = 0 or 1: scrambling disabled or enabled, Register 0x453, Bits[4:0] = 0x1: L = 2 lanes per link
0x454	0x00	Register 0x454, Bits[7:0] = 0x00: F = 1 octet per frame
0x455	0x1F	Register 0x455, Bits[4:0] = 0x1F: K = 32 frames per multiframe
0x456	0x00	Register 0x456, Bits[7:0] = 0x00: M = 1 converter per link
0x457	0x0F	Register 0x457, Bits[7:6] = 0x0: always set CS = 0; Register 0x457, Bits[4:0] = 0x0F: N = 16, always set to 16-bit resolution
0x458	0x0F or 0x2F	Register 0x458, Bits[7:5] = 0x0 or 0x1: Subclass 0 or Subclass 1, Register 0x458, Bits[4:0] = 0xF: NP = 16 bits per sample
0x459	0x20	Register 0x459, Bits[7:5] = 0x1: Set to JESD204B version, Register 0x459, Bits[4:0] = 0x0: S = 1 sample per converter per frame
0x45A	0x01	Register 0x45A, Bit 7 = 1: HD = 1; Register 0x45A, Bits[4:0] = 0x00: always set CF = 0
0x46C	0x03	Register 0x46C, Bits[7:0] = 0xFF: Deskew Link Lane 0 and Link Lane 1
0x476	0x01	Register 0x476, Bits[7:0] = 0x01: F = 1 octet per frame
0x47D	0x03	Register 0x47D, Bits[7:0] = 0x03: Enable Link Lane 0 and Link Lane 1

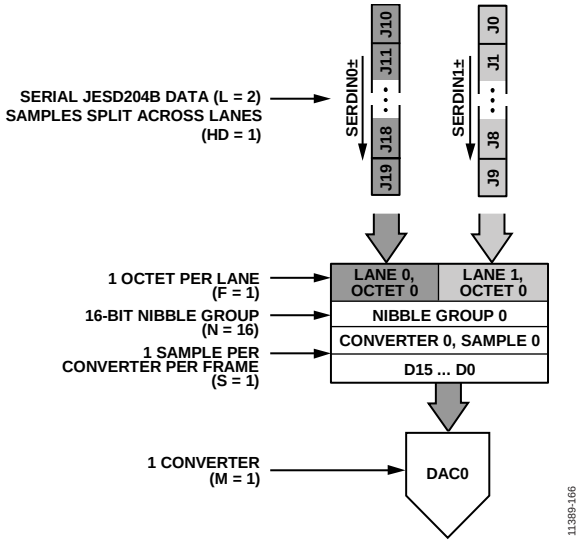


Figure 66. JESD204B Mode 9 Data Deframing

Table 56. SPI Configuration Map—Register Settings for JESD204B Parameters for Mode 10

Address	Setting	Description
0x453	0x00 or 0x80	Register 0x453, Bit 7 = 0 or 1: scrambling disabled or enabled, Register 0x453, Bits[4:0] = 0x0: L = 1 lane per link
0x454	0x01	Register 0x454, Bits[7:0] = 0x01: F = 2 octets per frame
0x455	0x0F or 0x1F	Register 0x455, Bits[4:0] = 0x0F or 0x1F: K = 16 or 32 frames per multiframe
0x456	0x00	Register 0x456, Bits[7:0] = 0x00: M = 1 converter per link
0x457	0x0F	Register 0x457, Bits[7:6] = 0x0: always set CS = 0; Register 0x457, Bits[4:0] = 0x0F: N = 16, always set to 16-bit resolution
0x458	0x0F or 0x2F	Register 0x458, Bits[7:5] = 0x0 or 0x1: Subclass 0 or Subclass 1, Register 0x458, Bits[4:0] = 0xF: NP = 16 bits per sample
0x459	0x20	Register 0x459, Bits[7:5] = 0x1: set to JESD204B version, Register 0x459, Bits[4:0] = 0x0: S = 1 sample per converter per frame
0x45A	0x00	Register 0x45A, Bit 7 = 0: HD = 0; Register 0x45A, Bits[4:0] = 0x00: always set CF = 0
0x46C	0x01	Register 0x46C, Bits[7:0] = 0x01: Deskew Link Lane 0 to Link Lane 7
0x476	0x02	Register 0x476, Bits[7:0] = 0x02: F = 2 octets per frame
0x47D	0x01	Register 0x47D, Bits[7:0] = 0x01: Enable Link Lane 0

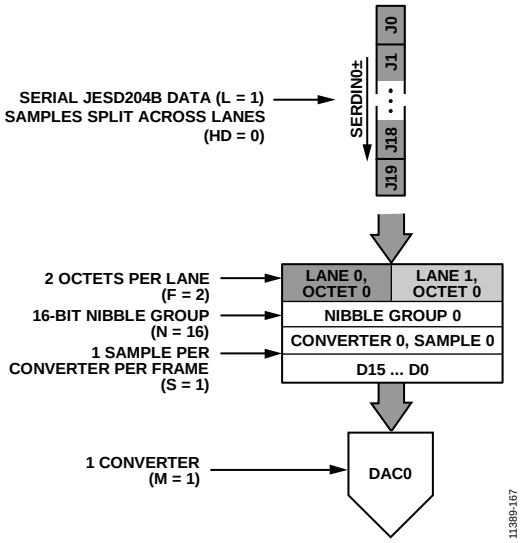


Figure 67. JESD204B Mode 10 Data Deframing

JESD204B TEST MODES

PHY PRBS Testing

The JESD204B receiver on the AD9154 includes a pseudorandom binary sequence (PRBS) pattern checker on the back end of its physical layer. This functionality enables bit error rate (BER) testing of each physical lane of the JESD204B link. The PHY PRBS pattern checker does not require that the JESD204B link be established. It can synchronize with a PRBS7, PRBS15, or PRBS31 data pattern. PRBS pattern verification can be performed on multiple lanes at once. The error counts for failing lanes are reported for one JESD204B lane at a time. The process for performing PRBS testing on the AD9154 is as follows:

1. Start sending a PRBS7, PRBS15, or PRBS31 pattern from the JESD204B transmitter.
2. Select and write the appropriate PRBS pattern to Register 0x316, Bits[3:2], as shown in Table 57.
3. Enable the PHY test for all lanes being tested by writing to PHY_TEST_EN (Register 0x315). Each bit of Register 0x315 enables the PRBS test for the corresponding lane. For example, writing a 1 to Bit 0 enables the PRBS test for Physical Lane 0.
4. Toggle PHY_TEST_RESET (Register 0x316, Bit 0) from 0 to 1, then back to 0.
5. Set PHY_PRBS_ERROR_THRESHOLD (Register 0x319 to Register 0x317) as desired.
6. Write a 0 and then a 1 to PHY_TEST_START (Register 0x316, Bit 1). The rising edge of PHY_TEST_START starts the test.
7. Wait 500 ms.
8. Stop the test by writing 0 to PHY_TEST_START (Register 0x316, Bit 1).
9. Read the PRBS test results.
   a. Each bit of PHY_PRBS_TEST_STATUS (Register 0x31D) corresponds to one SERDES lane. 0 = fail, 1 = pass.
   b. The number of PRBS errors seen on each failing lane can be read by writing the lane number to check (0 to 7) in the PHY_SRC_ERR_CNT (Register 0x316, Bits[6:4]) and reading PHY_PRBS_ERR_COUNT (Register 0x31A to Register 0x31C). The maximum error count is 2^{24-1}. If all bits of Register 0x31A to Register 0x31C are high, the maximum error count on the selected lane has been exceeded.

Table 57. PHY PRBS Pattern Selection

PHY_PRBS_PAT_SEL Setting (Register 0x316[3:2])	PRBS Pattern
0b00 (default)	PRBS7
0b01	PRBS15
0b10	PRBS31

Transport Layer Testing

The JESD204B receiver in the AD9154 supports the short transport layer (STPL) test as described in the JESD204B standard. Use this test to verify the data mapping between the JESD204B transmitter and receiver.

The STPL test ensures that each sample from each converter is mapped appropriately according to the number of converters (M) and the number of samples per converter (S). As specified in the JESD204B standard, the converter manufacturer specifies what test samples are transmitted. Each sample must have a unique value. For example, if M = 2 and S = 2, four unique samples are transmitted repeatedly until the test is stopped. The expected sample must be programmed into the device and the expected sample is compared to the received sample one sample at a time until all have been tested. The process for performing this test on the AD9154 is described as follows:

1. Synchronize the JESD204B link.
2. Enable the STPL test at the JESD204B Tx.
3. Select Converter 0 Sample 0 for testing. Write SHORT_TPL_M_SEL (Register 0x32C, Bits[3:2]) = 0 and SHORT_TPL_SP_SEL (Register 0x32C, Bits[5:4]) = 0.
4. Set the expected test sample for Converter 0, Sample 0. Program the expected 16-bit test sample into the SHORT_TPL_REF_SP_x registers (Register 0x32E and Register 0x32D).
5. Enable the STPL test. Write 1 to SHORT_TPL_TEST_EN (Register 0x32C, Bit 0).
6. Toggle the STPL reset, SHORT_TPL_TEST_RESET (Register 0x32C, Bit 1), from 0 to 1, then back to 0.
7. Check for failures. Read SHORT_TPL_FAIL (Register 0x32F, Bit 0), 0 = pass, 1 = fail.
8. Repeat Steps 3 to Step 7 for each sample of each converter. $Conv_0Sample_0$ through $Conv_{M-1}Sample_{S-1}$.

Repeated CGS and ILAS Test

As per Section 5.3.3.8.2 of the JESD204B specification, the AD9154 can check that a constant stream of /K28.5/ characters is being received, or that a CGS followed by a constant stream of ILAS is being received.

To run a repeated CGS test, send a constant stream of /K28.5/ characters to the AD9154 SERDES inputs. Next, set up the device and enable the links as described in the Device Setup Guide section. Ensure that the /K28.5/ characters are being received by verifying that the $\overline{\text{SYNCOUTx}}\pm$ signal has been deasserted and that CGS has passed for all enabled link lanes by reading Register 0x470. Program Register 0x300, Bit 2 = 0 to monitor the status of lanes on Link 0, and Register 0x300, Bit 2 = 1 to monitor the status of lanes on Link 1 for dual link mode.

To run the CGS followed by a repeated ILAS sequence test, follow the Device Setup Guide section, but before performing the last write (enabling the links), enable the ILAS test mode by writing a 1 to Register 0x477, Bit 7. Then, enable the links. When the device recognizes 4 CGS characters on each lane, it

Read Register 0x473 to verify that initial lane synchronization has passed for all enabled link lanes. Program Register 0x300, Bit 2 = 0 to monitor the status of lanes on Link 0, and Register 0x300, Bit 2 = 1 to monitor the status of lanes on Link 1 for dual link mode.

JESD204B ERROR MONITORING

Disparity, Not in Table, and Unexpected Control Character Errors

Per Section 7.6 of the JESD204B specification, the AD9154 can detect disparity errors, not in table errors, and unexpected control character errors, and can optionally issue a sync request and reinitialize the link when errors occur.

Note that the disparity error counter counts all characters with invalid disparity, regardless of whether they are in the 8-bit/10-bit decoding table. This is a minor deviation from the JESD204B specification, which only counts disparity errors when they are in the 8-bit/10-bit decoding table.

Checking Error Counts

The error count can be checked for disparity errors, not in table errors, and unexpected control character errors. The error counts are on a per lane and per error type basis. Note that the lane select and counter select are programmed into Register 0x46B and the error count is read back from the same address. To check the error count, complete the following steps:

1. Select the desired link lane and error type of the counter to view. Write these to Register 0x46B according to Table 58. To select a link lane, first select a link (Register 0x300, Bit 2 = 0 to select Link 0 or Register 0x300, Bit 2 = 1 to select Link 1 [dual link only]). Note that, when using Link 1, Link Lane x refers to Logical Lane x + 4.
2. Read the error count from Register 0x46B. Note the maximum error count is equal to the error threshold set in Register 0x47C.

Table 58. Error Counters

Addr.	Bits	Variable	Description
0x46B	[6:4]	LaneSel	LaneSel = x to monitor the error count of Link Lane x. See the notes on link lane in Step 1 of the Checking Error Counts section.
	[1:0]	CntrSel	CntrSel = 0b00 for bad running disparity counter. CntrSel = 0b01 for not in table error counter. CntrSel = 0b10 for unexpected control character counter.

Check for Error Count Over Threshold

In addition to reading the error count per lane and error type as described in the Checking Error Counts section, the user can check a register to see if the error count for a given error type has reached a programmable threshold.

The same error threshold is used for the three error types: disparity, not in table, and unexpected control character. The error counters are on a per error type basis. To use this feature, complete the following steps:

1. Program the desired error count threshold into ERRORTHRES (Register 0x47C).
2. Read back the error status for each error type to see if the error count has reached the error threshold.
   Disparity errors are reported in Register 0x46D.
   Not in table errors are reported in Register 0x46E.
   Unexpected control character errors are reported in Register 0x46F.

Error Counter and IRQ Control

Write to Register 0x46D and Register 0x46F to reset or disable the error counts and to reset the IRQ for a given lane. Note that these are the same registers that are used to report error count over threshold (see the Check for Error Count Over Threshold section); thus, the readback is not the value that was written. For each error type,

1. Select the link lane to access. To select a link lane, first select a link (Register 0x300, Bit 2 = 0 to select Link 0, Register 0x300, Bit 2 = 1 to select Link 1 [dual link only]). Note that, when using Link 1, Link Lane x refers to Logical Lane x + 4.
2. Decide whether to reset the IRQ, disable the error count, and/or reset the error count for the given lane and error type.
3. Write the link lane and desired reset or disable action to Register 0x46D to Register 0x46F according to Table 59.

Table 59. Error Counter and IRQ Control: Disparity (Register 0x46D), Not In Table (Register 0x46E), Unexpected Control Character (Register 0x46F)

Bits	Variable	Description
7	RstIRQ	RstIRQ = 1 to reset IRQ for the lane selected in Bits[2:0].
6	Disable_ErrCnt	Disable_ErrCnt = 1 to disable the error count for the lane selected in Bits[2:0].
5	RstErrCntr	RsteErrCntr = 1 to reset the error count for the lane selected in Bits[2:0].
[2:0]	LaneAddr	LaneAddr = x to monitor the error count of Link Lane x. See the notes on link lane in Step 1 of the Checking Error Counts section.

Monitoring Errors via $\overline{\text{SYNCOUTx±}}$

When one or more disparity, not in table, or unexpected control character error occurs, the error is reported on the $\overline{\text{SYNCOUTx±}}$ pins as per Section 7.6 of the JESD204B specification. The JESD204B specification states that the $\overline{\text{SYNCOUTx±}}$ signal is asserted for exactly 2 frame periods when an error occurs. For the AD9154, the width of the $\overline{\text{SYNCOUTx±}}$ pulse can be programmed. The settings to achieve a $\overline{\text{SYNCOUTx±}}$ pulse of 2 frame clock cycles are given in Table 60.

Table 60. Setting $\overline{\text{SYNCOUTx±}}$ Error Pulse Duration

JESD204B Mode IDs	PClockFactor (Frames/PClock)	SYNCB_ERR_DUR (Register 0x312[5:4]) Setting[1]
0, 4, 9	4	0 (default)
1, 2, 5, 6, 10	2	1
3, 7	1	2

[1] These register settings assert the $\overline{\text{SYNCOUTx±}}$ signal for 2 frame clock cycles pulse widths.

Disparity, NIT, Unexpected Control Character IRQs

For disparity, not in table, and unexpected control character errors, error count over the threshold events are available as IRQ events. Enable these events by writing to Register 0x47A, Bits[7:5]. The IRQ event status can be read at the same address (Register 0x47A, Bits[7:5]) after the IRQs are enabled.

Errors Requiring Reinitializing

A link reinitialization automatically occurs when four invalid disparity characters are received as per Section 7.1 of the JESD specification. When a link reinitialization occurs, the resync request is 5 frames and 9 octets long.

The user can optionally reinitialize the link when the error count for disparity errors, not in table errors, or unexpected control characters reaches a programmable error threshold. The process to enable the reinitialization feature for certain error types is as follows:

1. Set THRESHOLD_MASK_EN (Register 0x477, Bit 3) = 1. Note that when this bit is set, unmasked errors do not saturate at either threshold or maximum value.
2. Enable the sync assertion mask for each type of error by writing to the SYNC_ASSERTION_MASK register (Register 0x47B, Bits[7:5]) according to Table 61.
3. Program the desired error counter threshold into ERRORTHRES (Register 0x47C).
4. For each error type enabled in the SYNC_ASSERTION_MASK register, if the error counter on any lane reaches the programmed threshold, $\overline{\text{SYNCOUTx±}}$ falls, issuing a sync request. Note that all error counts are reset when a link reinitialization occurs. The IRQ does not reset and must be reset manually.

Table 61. Sync Assertion Mask

Addr.	Bit No.	Bit Name	Description
0x47B	7	BADDIS_S	Set to 1 to assert $\overline{\text{SYNCOUTx±}}$ if the disparity error count reaches the threshold
	6	NIT_S	Set to 1 to assert $\overline{\text{SYNCOUTx±}}$ if the not in table error count reaches the threshold
	5	UCC_S	Set to 1 to assert $\overline{\text{SYNCOUTx±}}$ if the unexpected control character count reaches the threshold

CGS, Frame Sync, Checksum, and ILAS Monitoring

Register 0x470 to Register 0x473 can be monitored to verify that each stage of JESD204B link establishment has occurred. Program Register 0x300, Bit 2 = 0 to monitor the status of the lanes on Link 0, and Register 0x300, Bit 2 = 1 to monitor the status of the lanes on Link 1.

Bit x of CODEGRPSYNCFLAG (Register 0x470) is high if Link Lane x received at least 4 K28.5 characters and passed code group synchronization.

Bit x of FRAMESYNCFLAG (Register 0x471) is high if Link Lane x completed initial frame synchronization.

Bit x of GOODCHKSUMFLG (Register 0x472) is high if the checksum sent over the lane matches the sum of the JESD204B parameters sent over the lane during ILAS for Link Lane x. The parameters can be added either by summing the individual fields in registers or summing the packed register. If Register 0x300, Bit 6 = 0 (default), the calculated checksums are the lower 8 bits of the sum of the following fields: DID, BID, LID, SCR, L − 1, F − 1, K − 1, M − 1, N − 1, SUBCLASSV, NP − 1, JESDV, S − 1, and HD. If Register 0x300, Bit 6 = 1, the calculated checksums are the lower 8 bits of the sum of Register 0x400 to Register 0x40C and LID.

Bit x of INITIALLANESYNC (Register 0x473) is high if Link Lane x passed the initial lane alignment sequence.

CGS, Frame Sync, Checksum, and ILAS IRQs

Fail signals for CGS, frame sync, checksum, and ILAS are available as IRQ events. Enable them by writing to Register 0x47A, Bits[3:0]. The IRQ event status can be read at the same address (Register 0x47A, Bits[3:0]) after the IRQs are enabled. Write a 1 to Register 0x470, Bit 7 to reset the CGS IRQ. Write a 1 to Register 0x471 to reset the frame sync IRQ. Write a 1 to Register 0x472 to reset the checksum IRQ. Write a 1 to Register 0x473 to reset the ILAS IRQ.

Configuration Mismatch IRQ

The AD9154 has a configuration mismatch flag that is available as an IRQ event. Use Register 0x47B, Bit 3 to enable the mismatch flag (it is enabled by default), and then use Register 0x47B, Bit 4 to read back its status and reset the IRQ signal. See the Interrupt Request Operation section for more information.

The configuration mismatch event flag is high when the link configuration settings (in Register 0x450 to Register 0x45D) do not match the JESD204B transmitted settings (Register 0x400 to Register 0x40D). All these registers are paged per link (in Register 0x300).

Note that this function is different from the good checksum flags in Register 0x472. The good checksum flags ensure that the transmitted checksum matches a calculated checksum based on the transmitted settings. The configuration mismatch event ensures that the transmitted settings match the configured settings.

DIGITAL DATAPATH

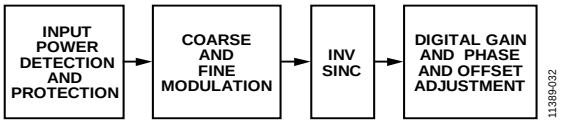


Figure 68. Block Diagram of the Digital Datapath

Figure 68 shows a block diagram of the signal processing digital datapath. The digital processing includes an input power detection block, three half-band interpolation filters, a quadrature modulator consisting of a fine resolution NCO modulator and $f_{DAC}/4$ and $f_{DAC}/8$ coarse modulator blocks, an inverse sinc filter, and gain, phase, offset, and group delay adjustment blocks.

The datapath is organized into two identical paths. Each path processes a pair of digital signals input from the JESD204B transport layer block. The digital signals are processed by a datapath and input to a pair of DAC cores. Interpolation modes process the pair of signals as independent data streams. The coarse and fine modulation block requires that a data stream to be upconverted be an I/Q pair of signals

DUAL PAGING

The digital datapath registers are paged to allow configuration of either DAC dual independently or both simultaneously. Table 62 shows how to use the dual paging register.

Table 62. Paging Modes

PAGEINDX Reg. 0x008[1:0]	Duals Paged	DACs Updated
1	A	DAC0 and DAC1
2	B	DAC2 and DAC3
3 (default)	A and B	DAC0, DAC1, DAC2, and DAC3

Several functions are paged by DAC dual, such as input data format, downstream protection, interpolation, modulation, inverse sinc, digital gain, phase offset, dc offset, group delay, IQ swap, datapath PRBS, LMFC sync, and NCO alignment.

DATA FORMAT

BINARY_FORMAT (Register 0x110, Bit 7), paged as described in the Dual Paging section) controls the expected input data format. By default it is 0, which means the input data must be in twos complement. It can also be set to 1, which means input data is in offset binary (0x0000 is negative full scale and 0xFFFF is positive full scale).

INTERPOLATION MODES

Interpolation increases the sampling rate of a digital signal and can be bypassed. The transmit path contains three half-band interpolation filters, which each provide a 2× increase in the output sampling rate and a low-pass function. Table 63 shows how to select each available interpolation mode, their usable bandwidths, and their maximum data rates. Note that

$$f_{DATA} = f_{DAC}/InterpolationFactor$$

The maximum values of f_{DATA} for interpolator bypass and the three interpolation factors are listed in Table 2 as adjusted DAC update rates; f_{DATA} is another name for the adjusted DAC update rate. Interpolation mode is paged as described in the Dual Paging section. Register 0x030, Bit 0 is high if an unsupported interpolation mode is selected.

Table 63. Interpolation Modes and Usable Bandwidth

Interpolation Mode	INTERPMODE Reg. 0x112[2:0]	Usable Bandwidth
1× (bypass)	0x00	0.5 x f_{DATA}
2×	0x01	0.4 × f_{DATA}
4×	0x03	0.4 × f_{DATA}
8×	0x04	0.4 × f_{DATA}

[1] The maximum speed for 1× interpolation is limited by the JESD204B interface.

Filter Performance

Interpolation modes increase the sampling rate of a digital signal by a factor of 2, 4, or 8. As part of the process, a digital low-pass filter is applied. The filter magnitude response for each interpolation mode is shown in Figure 69.

The usable bandwidth (as shown in Table 63) is defined as the frequency band over which the filters have a pass-band ripple of less than ±0.001 dB and an image rejection of greater than 85 dB.

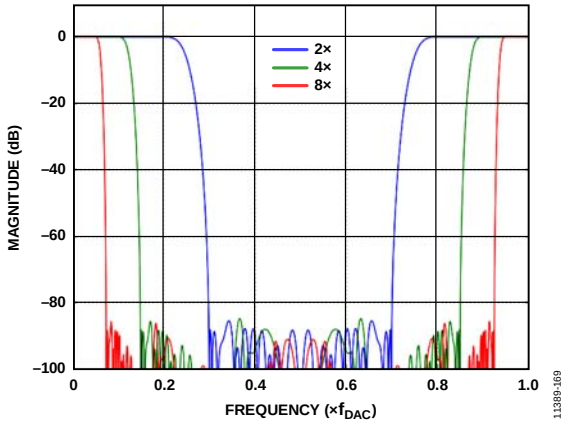


Figure 69. All Band Responses of Interpolation Filters

Filter Performance Beyond Specified Bandwidth

The usable pass band of the interpolation filter is specified as $0.4 \times f_{DATA}$. The filters can be used slightly beyond this ratio at the expense of increased pass-band ripple and decreased interpolation image rejection.

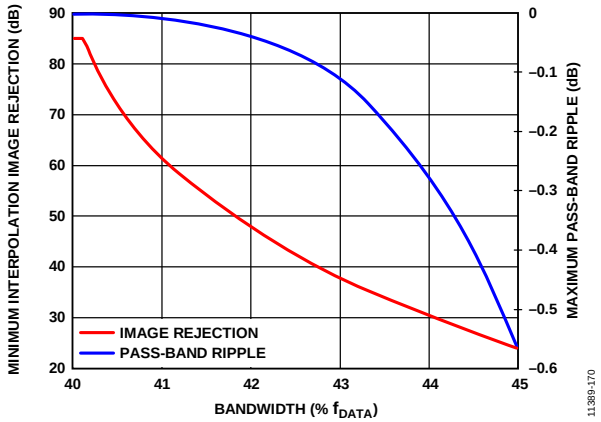


Figure 70. Interpolation Filter Performance Beyond Specified Bandwidth

Figure 70 shows the performance of the interpolation filters beyond $0.4 \times f_{DATA}$. Note that the ripple increases much slower than the image rejection decreases. This means that if the application can tolerate degraded image rejection from the interpolation filters, more bandwidth can be used.

DIGITAL MODULATION

The AD9154 includes modulation blocks that upconvert I/Q quadrature signal pairs to an IF frequency in the digital domain.

The coarse modulation modes ($f_{DAC}/4$ and $f_{DAC}/8$) upconvert an I/Q pair of digital signals to one of the selected IFs. The NCO fine modulation mode upconverts an I/Q signal pair to an IF frequency programmed into the NCO. Modulation mode is selected as shown in Table 64 and is paged as described in the Dual Paging section.

Table 64. Modulation Mode Selection

Modulation Mode	MODULATION_TYPE Register 0x111, Bits[3:2]
None	0b00
NCO Fine Modulation	0b01
Coarse – $f_{DAC}/4$	0b10
Coarse – $f_{DAC}/8$	0b11

NCO Fine Modulation

This modulation mode uses the NCO, a phase shifter, and a complex modulator to upconvert an I/Q digital signal pair to an IF frequency within the first Nyquist zone of the DAC cores. Figure 71 shows a block diagram of the NCO modulator. This allows output signals to be placed anywhere in the output spectrum with very fine frequency resolution. The NCO produces a quadrature carrier to translate the input signal to a new center frequency. A quadrature carrier is a pair of sinusoidal waveforms of the same frequency, offset 90° from each other.

The frequency of the quadrature carrier is set via an FTW. The quadrature carrier is mixed with the I and Q data and then summed into the I and Q datapaths, as shown in Figure 71.

$$-f_{DAC}/2 \le f_{CARRIER} < +f_{DAC}/2$$
$$FTW = (f_{CARRIER}/f_{DAC}) \times 2^{48}$$

where *FTW* is a 48-bit twos complement number.

The frequency tuning word is set as shown in Table 65 and paged as described in the Dual Paging section.

Table 65. NCO FTW Registers

Address	Value	Description
0x114	FTW[7:0]	8 LSBs of FTW
0x115	FTW[15:8]	Next 8 bits of FTW
0x116	FTW[23:16]	Next 8 bits of FTW
0x117	FTW[31:24]	Next 8 bits of FTW
0x118	FTW[39:32]	Next 8 bits of FTW
0x119	FTW[47:40]	8 MSBs of FTW

Unlike other registers, the FTW registers are not updated immediately upon writing. Instead, the FTW registers update on the rising edge of FTW_UPDATE_REQ (Register 0x113[0]). After an update request, FTW_UPDATE_ACK (Register 0x113[1]) must be high to acknowledge that the FTW has updated.

SEL_SIDEBAND (Register 0x111, Bit 1; paged as described in the Dual Paging section) is a convenience bit that can be set to use the negative modulation result. This is equivalent to flipping the sign of FTW.

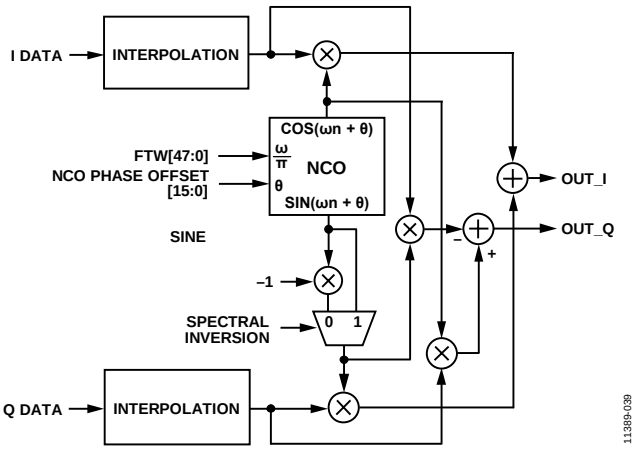


Figure 71. NCO Modulator Block Diagram

NCO Phase Offset

The NCO phase offset feature allows rotation of the I and Q phases. Unlike phase adjust, this feature moves the phases of both I and Q channels together. NCO phase offset can be used only when using NCO fine modulation.

$$-180° \le DegreesOffset < +180°$$
$$PhaseOffset = (DegreesOffset/180°) \times 2^{15}$$

where *PhaseOffset* is a 16-bit twos complement number.

The NCO phase offset is set as shown in Table 66 and paged as described in the Dual Paging section. Because this function is

part of the fine modulation block, phase offset is not updated immediately upon writing. Instead, it updates on the rising edge of FTW_ UPDATE_REQ (Register 0x113, Bit 0) along with the FTW.

Table 66. NCO Phase Offset Registers

Address	Value
0x11A	NCO_PHASE_OFFSET[7:0]
0x11B	NCO_PHASE_OFFSET[15:8]

INVERSE SINC

DACs have a sin(x)/x amplitude roll-off as a function frequency. This characteristic is shown in blue in Figure 72. The AD9154 provides a digital inverse sinc function to compensate for this roll-off over frequency. The filter is enabled by setting the INVSINC_ENABLE bit (Register 0x111, Bit 7, paged as described in the Dual Paging section). Inverse sinc is enabled by default.

Figure 72 shows the frequency response of sin(x)/x roll-off, the inverse sinc filter, and the composite response. The composite response has less than ±0.05 dB pass-band ripple up to a frequency of 0.4 × f_{DACCLK}. To provide the necessary peaking at the upper end of the pass band, the inverse sinc filter shown has an intrinsic insertion loss of about 3.8 dB; in many cases, this can be partially compensated as described in the Digital Gain section.

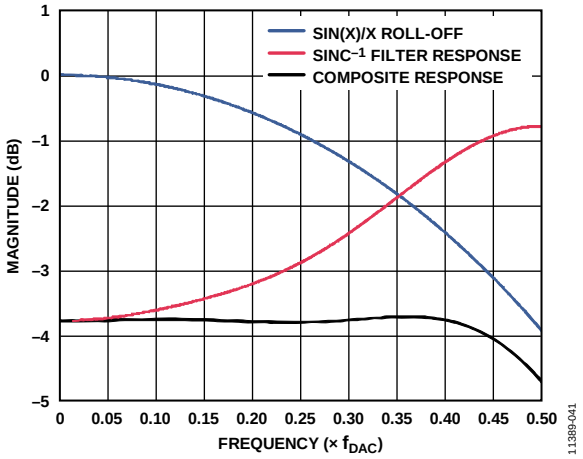


Figure 72. Responses of sin(x)/x Roll-Off, the Sinc^{-1} Filter, and the Composite of the Two Input Signal Power Detection and Protection

DIGITAL GAIN, PHASE ADJUST, DC OFFSET, AND GROUP DELAY

Digital gain, phase adjust, and dc offset (as described in the Digital Gain section, Phase Adjust section, and DC Offset section) allow compensation of imbalances in the I and Q paths due to analog mismatches between DAC I/Q outputs, quadrature modulator I/Q baseband inputs, and DAC/modulator interface I/Q paths. These imbalances can cause the two following issues:

- An unwanted sideband signal appears at the quadrature modulator output with significant energy. Cancel this signal using digital gain and phase adjust. Tuning the quadrature gain and phase adjust values can optimize complex image rejection in single sideband radios or can optimize the error vector magnitude (EVM) in zero IF (ZIF) architectures.
- The LO leakage at the output of a quadrature modulator following the AD9154 in a signal chain can be cancelled by adjusting the dc current output of each DAC driving modulator signal inputs.

Digital Gain

Digital gain is used to independently adjust the digital signal magnitude being fed into each DAC. The digital gain code can be left at its default value where it provides 0 dB of digital backoff (in other words, a gain of 1), or it can be programmed to provide larger digital backoff. Digital gain can be programmed to introduce an I/Q pair gain imbalance to help a quadrature modulator following the AD9154 in a signal chain cancel an unwanted SSB sideband. Digital gain is enabled by default and must not be disabled.

The amount of digital gain (GainCode) desired can be programmed in the registers shown in Table 67. The digital gain settings are described in the following equations:

$$0 \le Gain \le 4095/2048$$
$$-\infty \text{ dB} \le dBGain \le 6.018 \text{ dB}$$
$$Gain = GainCode \times (1/2048)$$
$$dBGain = 20 \times \log10(Gain)$$
$$GainCode = 2048 \times Gain = 2048 \times 10^{dBGain/20}$$

where *GainCode* is a 12-bit unsigned binary number.

The I/Q digital gain is set as shown in Table 67 and paged as described in the Dual Paging section.

Table 67. Digital Gain Registers

Addr.	Value	Description
0x111[5]	DIG_GAIN_ENABLE	Set to 1 to enable digital gain at reset
0x13C	GAINCODEI[7:0]	I DAC LSB gain code
0x13D	GAINCODEI[11:8]	I DAC MSB gain code
0x13E	GAINCODEQ[7:0]	Q DAC LSB gain code
0x13F	GAINCODEQ[11:8]	Q DAC MSB gain code

Phase Adjust

Ordinarily, the I and Q channels of each DAC pair have an angle of 90° between them. The phase adjust feature changes the angle between the I and Q channels, which balances the phase into a modulator.

$$-14 \le DegreesAdjust < 14$$
$$PhaseAdj = (DegreesAdjust/14) \times 2^{12}$$

where *PhaseAdj* is a 13-bit twos complement number.

The phase adjust is set as shown in Table 68 and paged as described in the Dual Paging section.

Table 68. I/Q Phase Adjustment Registers

Addr.	Value	Description
0x111[4]	PHASE_ADJ_ENABLE	Set to 1 to enable phase adjust
0x11C	PHASEADJ[7:0]	LSB phase adjust code
0x11D	PHASEADJ[12:8]	MSB phase adjust code

DC Offset

The dc offset feature is used to individually offset the data into the I or Q DACs. This feature is used to cancel LO leakage at the modulator output.

The offset is programmed individually for I and Q as a 16-bit twos complement number in LSBs, plus a 5-bit twos complement number in sixteenths of an LSB, as shown in Table 69. DC offset is paged as described in the Dual Paging section.

$-2^{15} \leq LSBsOffset < 2^{15}$

$-16 \leq SixteenthsOffset \leq 15$

Table 69. DC Offset Registers

Addr.	Value	Description
0x135[0]	DC_OFFSET_ON	Set to 1 to enable dc offset
0x136	LSBSOFFSETI[7:0]	I DAC LSB dc offset code
0x137	LSBSOFFSETI[15:8]	I DAC MSB dc offset code
0x138	LSBSOFFSETQ[7:0]	Q DAC LSB dc offset code
0x139	LSBSOFFSETQ[15:8]	Q DAC MSB dc offset code
0x13A[4:0]	SIXTEENTHSOFFSETI	I DAC sub-LSB dc offset code
0x13B[4:0]	SIXTEENTHSOFFSETQ	Q DAC sub-LSB dc offset code

Coarse Group Delay

Coarse group delay is a global adjustment of the DAC latency, and it is programmed to identically affect both DACs in an I/Q signal pair. The coarse group delay range is in +7/−8 steps. Each step is ½ DAC clock cycle. The default value of 0x8 sets the delay to zero. This is useful in applications where the user needs to tune the latency of the DAC path with some accuracy (for example, in DPD loop delay adjust).

Write the value to COARSE_GROUP_DLY (Register 0x014). This is paged as described in the Dual Paging section.

Group Delay Compensation

Group delay compensation provides separate delay tunability to either an I or Q channel within each dual digital signal pair. The user can delay either the I or Q output to align their quadrature. Table 70 shows the register settings used for group delay compensation. The group delay compensation bypass register is located at Register 0x046. The GROUPDELAYCOMP (Bits[7:0]) values are binary, and the default value of 0x00 is a delay compensation of zero. The difference between this mode and the phase adjust mode is that group delay compensation can correct for delay differences between the I and Q channels, while phase adjust cannot. Group delay compensation is paged as described in the Dual Paging section.

Table 70. Group Delay Compensation Registers

Addr.	Value	Description
0x046	GROUP DELAY COMP BYPASS	Set to 3 to bypass both I and Q compensation
0x044	GROUP DELAY COMP I [7:0]	±85 ps nominal range
0x045	GROUP DELAY COMP Q [7:0]	±85 ps nominal range

I TO Q SWAP

I_TO_Q (Register 0x111, Bit 0; paged as described in the Dual Paging section) is a convenience bit that can be set to send the I datapath to the Q DAC. Note that this swap occurs at the end of the datapath (after any modulation, digital gain, phase adjust, and phase offset). If using M = 1 DACs in DualLink mode (as described in the DAC Power-Down Setup section), set this bit to direct data to the DAC3 output.

NCO ALIGNMENT

The NCO alignment block phase aligns the NCO output from multiple converters. Two NCO alignment modes are supported by the AD9154. The first is a SYSREF± alignment mode that phase aligns the NCO outputs to the rising edge of a SYSREF± pulse. The second alignment mode is a data key alignment; when this mode is enabled, the AD9154 aligns the NCO outputs when a user specified data pattern arrives at the DAC input. Note that the NCO alignment is per dual, and is paged as described in the Dual Paging section.

SYSREF± NCO Alignment

As with the LMFC alignment, in Subclass 1, a SYSREF± pulse can be used to phase align the NCO outputs of multiple devices in a system and multiple channels on the same device. Note that in Subclass 0, this alignment mode can be used to align the NCO outputs within a device to an internal processing clock edge. No SYSREF± edge is needed in Subclass 0, but multichip alignment cannot be achieved. The steps to achieve a SYSREF NCO alignment are as follows:

1. Set NCOCLRMODE (Register 0x050, Bits[1:0]) = 0b01 for SYSREF NCO alignment mode.
2. Set NCOCLRARM to 1 (Register 0x050, Bit 7).
3. Perform an LMFC alignment to force the NCO phase align (see the Syncing LMFC Signals section). The phase alignment occurs on the next SYSREF± edge.
   Note that if in one shot sync mode, the LMFC alignment block must be armed by setting Register 0x03A, Bit 6 = 1. If in continuous mode or one shot then monitor mode, the LMFC align block does not need to be armed; the NCO align automatically trips on the next SYSREF± edge.
4. Check the alignment status. If NCO phase alignment was successful, NCOCLRPASS (Register 0x050, Bit 4) = 1. If phase alignment failed, NCOCLRFAIL (Register 0x050, Bit 3) = 1.

Data Key NCO Alignment

In addition to supporting the SYSREF± alignment mode, the AD9154 supports a mode where the NCO phase alignment occurs when a user-specified pattern is seen at the DAC input. The steps to achieve a data key NCO alignment are as follows:

1. Set NCOCLRMODE (Register 0x050, Bits[1:0]) = 0b10.
2. Write the expected 16-bit data key for the I and Q datapath into NCOKEYIx (Register 0x051 to Register 0x052) and NCOKEYQ (Register 0x053 to Register 0x054), respectively.
3. Set NCOCLRARM (Register 0x050, Bit 7) = 1.
4. Send the expected 16-bit I and Q data keys to the device to achieve NCO alignment.
5. Check the alignment status. If the expected data key was seen at the DAC input, then NCOCLRMTCH (Register 0x050, Bit 5) = 1. If NCO phase alignment was successful, NCOCLRPASS (Register 0x050, Bit 4) = 1. If phase alignment failed, NCO_ALIGN_FAIL (Register 0x050, Bit 3) = 1.

Multiple device NCO alignment can be achieved with the data key alignment mode. To achieve multichip NCO alignment, program the same expected data key on all devices, arm all devices, and then send the data key to all devices/channels at the same time.

NCO Alignment IRQ

An IRQ event showing whether the NCO align was tripped is available.

Use Register 0x021, Bit 4 to enable DAC Dual A (DAC0 and DAC1), and then use Register 0x025, Bit 4 to read back its status and reset the IRQ signal.

Use Register 0x022, Bit 4 to enable DAC Dual B (DAC2 and DAC3), and then use Register 0x026, Bit 4 to read back its status and reset the IRQ signal.

See the Interrupt Request Operation section for more information.

DOWNSTREAM PROTECTION

The AD9154 has several blocks designed to protect the power amplifier (PA) in its board level signal chain, as well as other downstream blocks. It consists of a power detection and protection (PDP) block, a blanking state machine (BSM), and a transmit enable state machine (Tx ENSM).

The PDP block monitors incoming data. If a moving average of the data power goes above a threshold, the PDP block provides a signal (PDP_PROTECT) that can be routed externally on the PDP OUT0 and PDP OUT1 pins.

The Tx ENSM is a simpler block that controls delay between TXENx and the Tx_PROTECT signal. The Tx_PROTECT signal is used as an input to the BSM and its inverse can optionally be routed externally. Optionally, the Tx ENSM can also power down its associated DAC dual.

The BSM gently ramps data entering the DAC and flushes the datapath. The BSM is activated by the Tx_PROTECT signal or automatically by the LMFC sync logic during a rotation. Digital gain must be enabled for proper function. Finally, some simple logic takes the outputs from each of those blocks and uses them to generate a desired PDP OUTx signal on an external pin. This signal can be used to enable/disable downstream components, such as a PA.

Power Detection and Protection

The input signal PDP block detects the average power of the DAC input signal and to prevent overrange signals from being passed to the next stage, which may potentially cause destructive breakdown on power sensitive devices, such as PAs. The protection function provides a signal (PDP_PROTECT) that can be routed externally to shut down a PA.

The PDP block uses a separate path with a shorter latency than the datapath to ensure that PDP_PROTECT gets triggered before the overrange signal reaches the analog DAC cores. The sum of the I^2 and Q^2 are calculated as a representation of the input signal power (only the top seven MSBs of data samples are used). The calculated sample power numbers are accumulated through a moving average filter whose output is the average of the input signal power in a certain number of samples. When the output of the averaging filter is larger than the threshold, the internal signal PDP_PROTECT goes high, which can optionally be configured to trigger a signal on the PDP OUTx pins. The PDP block is configured as shown in Table 71 and paged as described in the Dual Paging section.

The choice of PDP_AVG_TIME (Register 0x062) and PDP_THRESHOLD[12:0] (Register 0x060 to Register 0x061) for effective protection are application dependent. Experiment with real-world vectors to ensure proper configuration. The PDP_POWER[12:0] readback (Register 0x063 to Register 0x064) can help by storing the maximum power when a set threshold passes.

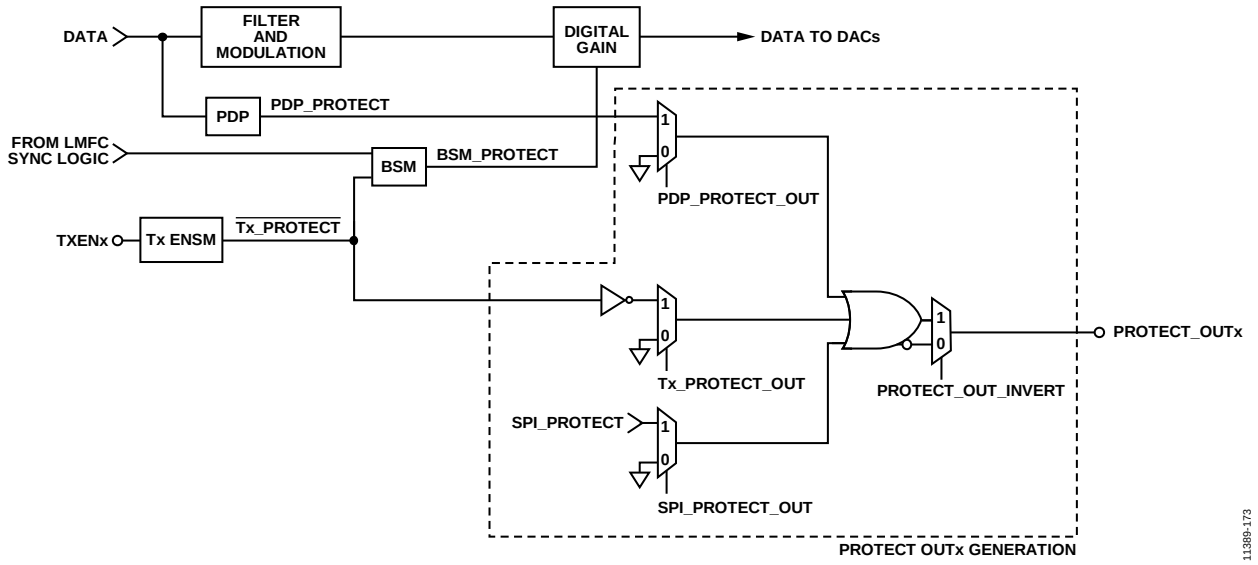


Figure 73. Downstream Protection Block Diagram

Table 71. PDP Registers

Addr.	Bit No.	Value	Description
0x060	[7:0]	PDP_THRESHOLD[7:0]	Power that triggers PDP_PROTECT. 8 LSBs.
0x061	[4:0]	PDP_THRESHOLD[12:8]	5 MSBs.
0x062	7	PDP_ENABLE	Set to 1 to enable PDP.
	[3:0]	PDP_AVG_TIME	Can be set from 0 to 10. Averages across $2^{(9 + PDP_AVG_TIME)}$, IQ sample pairs.
0x063	[7:0]	PDP_POWER[7:0]	If PDP_THRESHOLD is crossed, this reads back the maximum power seen. If not, this reads back the instantaneous power. 8 LSBs.
0x064	[4:0]	PDP_POWER[12:8]	5 MSBs.

Power Detection and Protection IRQ

The PDP_PROTECT signal is available as an IRQ event.

Use Register 0x021, Bit 7 to enable PDP_PROTECT for Dual A (DAC0 and DAC1), and then use Register 0x025, Bit 7 to read back its status and reset the IRQ signal.

Use Register 0x022, Bit 7 to enable PDP_PROTECT for Dual B (DAC2 and DAC3), and then use Register 0x026, Bit 7 to read back its status and reset the IRQ signal.

See the Interrupt Request Operation section for more information.

Transmit Enable State Machine

The Tx ENSM is a simple block that controls the delay between the TXENx signal and the $\overline{\text{TX_PROTECT}}$ signal. This signal is used as an input to the BSM and its inverse can be routed to an external pin (PDP_OUTx) to turn downstream components on or off as desired.

The TXENx signal can be used to power down their associated DAC duals. If DACA_MASK (Register 0x012, Bit 6) = 1, a falling edge of TXENx causes DAC Dual A (DAC0 and DAC1) to power down. If DACB_MASK (Register 0x012, Bit 7) = 1, a falling edge of TXENx causes DAC Dual B (DAC2 and DAC3) to power down. On a rising edge of TXENx, without DACA_MASK and DACB_MASK enabled, the output is valid after the BSM settles (see the Blanking State Machine (BSM) section). If the masks are enabled, an additional delay is imposed; the output is not valid until the BSM settles and the DACs fully power on (nominally an additional ~35 µs).

The Tx ENSM is configured as shown in Table 72 and is paged as described in the Dual Paging section.

Table 72. Tx ENSM Registers

Addr.	Bit No.	Value	Description
0x11F	[7:6]	PA_FALL	Number of fall counters to use (1 to 2).
	[5:4]	PA_RISE	Number of rise counters to use (0 to 2).
0x121	[7:0]	RISE_COUNT_0	Delay TX_PROTECT rise from TXENx rising edge by 32 × RISE_COUNT_0 DAC clock cycles.
0x122	[7:0]	RISE_COUNT_1	Delay TX_PROTECT rise from TXENx rising edge by 32 × RISE_COUNT_1 DAC clock cycles.
0x123	[7:0]	FALL_COUNT_0	Delay TX_PROTECT rise from TXENx rising edge by 32 × FALL_COUNT_0 DAC clock cycles. Must be at least 0x12.
0x124	[7:0]	FALL_COUNT_1	Delay TX_PROTECT rise from TXENx rising edge by 32 × FALL_COUNT_1 DAC clock cycles.

Blanking State Machine (BSM)

The BSM gently ramps data entering the DAC and flushes the datapath.

On a falling edge of $\overline{\text{TX_PROTECT}}$ (the TXENx signal delayed by the Tx ENSM), the datapath holds the latest data value and the digital gain gently ramps from its set value to 0. At the same time, the datapath is flushed with zeroes.

On a rising edge of $\overline{\text{TX_PROTECT}}$, the TXENx signal is delayed by the Tx ENSM; data is allowed to flow through the datapath again and the digital gain gently ramps the data from 0 up to the set digital gain.

Both of the above functions are also triggered automatically by the LMFC sync logic during a rotation to prevent glitching on the output.

Ramping

The step size to use when ramping gain to 0 or its assigned value can be controlled via the GAIN_RAMP_DOWN_STEPx registers (Register 0x142 and Register 0x143) and the GAIN_RAMP_UP_STEPx registers (Register 0x140 and Register 0x141). These registers are paged as described in the Dual Paging section.

The current BSM state can be read back as shown in Table 73.

Table 73. Blanking State Machine Ramping Readbacks

Address	Value	Description
0x147[7:6]	0b00	Data is being held at midscale.
	0b01	Ramping gain to 0. Data ramping to midscale.
	0b10	Ramping gain to assigned value. Data ramping to normal amplitude.
	0b11	Data at normal amplitude.

Blanking State Machine IRQ

Blanking completion is available as an IRQ event.

Use Register 0x021, Bit 5 to enable blanking completion for DAC Dual A (DAC0 and DAC1), and then use Register 0x025, Bit 5 to read back its status and reset the IRQ signal.

Use Register 0x022, Bit 5 to enable blanking completion for DAC Dual B (DAC2 and DAC3),and then use Register 0x026, Bit 5 to read back its status and reset the IRQ signal.

See the Interrupt Request Operation section for more information.

PDP OUTx Generation

Register 0x013 controls which signals are OR'ed into the external PDP OUTx signal. Register 0x11F, Bit 2 can be used to invert the PDP OUTx signal, By default, PDP OUTx is high when output is valid. Both of these registers are paged as described in the Dual Paging section.

Table 74. PDP OUTx Registers

Addr.	Bit No.	Description
0x013	6	1: PDP block triggers PDP_OUT
	5	1: Tx ENSM triggers PDP_OUT
	3	1: SPI_PROTECT triggers PDP_OUT
	2	Sets SPI_PROTECT
0x11F	2	Inverts PDP OUTx

DATAPATH PRBS

The datapath PRBS can be used to verify that the AD9154 datapath is receiving and correctly decoding data. The datapath PRBS verifies that the JESD204B parameters of the transmitter and receiver match, the lanes of the receiver are mapped appropriately, lanes have been appropriately inverted, if necessary, and in general that the start-up routine has been implemented correctly.

The datapath PRBS is paged as described in the Dual Paging section. To run the datapath PRBS test, complete the following steps:

1. Set up the device in the desired operating mode. See the Device Setup Guide section for details on setting up the device.
2. Send PRBS7 or PRBS15 data.
3. Write Register 0x14B, Bit 2 = 0 for PRBS7 or 1 for PRBS15.
4. Write Register 0x14B, Bit 1 and Bit 0 = 0b11 to enable and reset the PRBS test.
5. Write Register 0x14B, Bit 1 and Bit 0 = 0b01 to enable the PRBS test and release reset.
6. Wait 500 ms.
7. Check the status by checking the IRQ for DAC0 to DAC3 PRBS as described in the Datapath PRBS IRQ section.
8. If there are failures, set Register 0x008 = 0x01 to view the status of Dual A (DAC0/DAC1). Set Register 0x08 = 0x02 to view the status of Dual B (DAC2/DAC3).
9. Read Register 0x14B, Bit 7 and Bit 6. Bit 6 is 0 if the I DAC of the selected dual has any errors. Bit 7 is 0 if the Q DAC of the selected dual has any errors. This must match the IRQ.
10. Read Register 0x14C to read the error count for the I DAC of the selected dual. Read Register 0x14D to read the error count for the Q DAC of the selected dual.

Note that the PRBS processes 32 bits at a time, and compares the 32 new bits to the previous set of 32 bits. It detects (and reports) only 1 error in every group of 32 bits, so the error count partly depends on when the errors are seen. For example,

- Bits: 32 good, 31 good, 1 bad; 32 good (2 errors)
- Bits: 32 good, 22 good, 10 bad; 32 good (2 errors)
- Bits: 32 good, 31 good, 1 bad; 31 good, 1 bad; 32 good (3 errors)

Datapath PRBS IRQ

The PRBS fail signals for each DAC are available as IRQ events. Use Register 0x020, Bits[3:0] to enable the fail signals, and then use Register 0x024, Bits[3:0] to read back their statuses and reset the IRQ signals. See the Interrupt Request Operation section for more information.

DC TEST MODE

The AD9154 provides a dc test mode. When dc test mode is activated, the input to the digital data paths is set to a midscale DAC input dc level in place of data from the JESD204B transport layer. DC test mode is enabled by setting Register 0x520, Bit 1 and clearing Register 0x146, Bit 0. Register 0x146, Bit 0 must be set to 1 for all other modes of operation.

In dc test mode, the digital modulator can generate a sine wave at a fixed amplitude. Digital gain, dc offset, and phase adjustment can be applied to the sine wave on its way to each DAC core input.

INTERRUPT REQUEST OPERATION

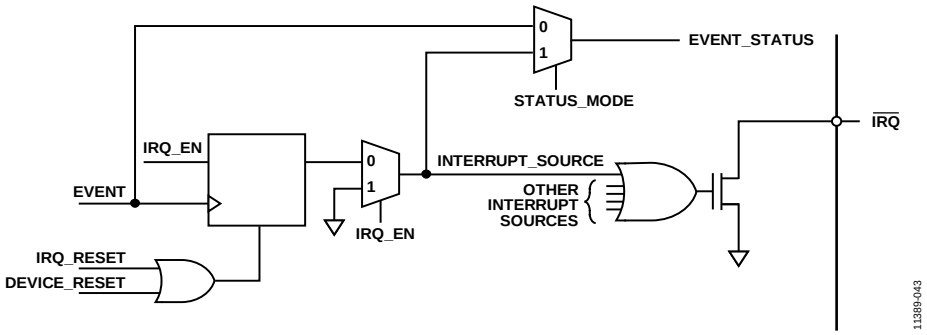


Figure 74. Simplified Schematic of IRQ Circuitry

The AD9154 provides an interrupt request output signal on Pin 60 (IRQ) that can be used to notify an external host processor of significant device events. On assertion of the interrupt, query the device to determine the precise event that occurred. The IRQ pin is an open-drain, active low output. Pull the IRQ pin high external to the device. This pin can be tied to the interrupt pins of other devices with open-drain outputs to wire; OR these pins together. Figure 74 shows a simplified block diagram of how the IRQ blocks works. If IRQ_EN is low, the INTERRUPT_SOURCE signal is set to 0. If IRQ_EN is high, any rising edge of EVENT causes the INTERRUPT_SOURCE signal to be set high. If any INTERRUPT_SOURCE signal is high, the IRQ pin is pulled low. INTERRUPT_SOURCE can be reset to 0 by either an IRQ_RESET signal or a DEVICE_RESET.

Depending on STATUS_MODE, the EVENT_STATUS bit reads back event or INTERRUPT_SOURCE. The AD9154 has several IRQ register blocks, which can monitor up to 75 events (depending on device configuration). Certain details vary by IRQ register block as described in Table 75. Table 76 shows which registers the IRQ_EN, IRQ_RESET, and STATUS_MODE signals in Figure 74 are coming from, as well as the address where EVENT_STATUS is read back.

Table 75. IRQ Register Block Details

Register Block	EVENT Reported	EVENT_STATUS
0x01F to 0x026	Per chip	INTERRUPT_SOURCE if IRQ is enabled, if not, it is EVENT
0x46D to 0x46F; 0x470 to 0x473; 0x47A	Per link and lane	INTERRUPT_SOURCE if IRQ is enabled, if not, 0
0x47B[4]	Per link	INTERRUPT_SOURCE if IRQ is enabled, if not, 0

INTERRUPT SERVICE ROUTINE

Interrupt request management starts by selecting the set of event flags that require host intervention or monitoring. Enable the events that require host action so that the host is notified when they occur. For events requiring host intervention upon IRQ activation, run the following routine to clear an interrupt request:

1. Read the status of the event flag bits that are being monitored.
2. Disable the interrupt by writing 0 to IRQ_EN.
3. Read the event source. For Register 0x01F to Register 0x026, EVENT_STATUS has a live readback. For other events, see their registers.
4. Perform any actions that may be required to clear the cause of the event. In many cases, no specific actions may be required.
5. Verify that the event source is functioning as expected.
6. Clear the interrupt by writing 1 to IRQ_RESET.
7. Enable the interrupt by writing 1 to IRQ_EN.

Table 76. IRQ Register Block Address of IRQ Signal Details

	Address of IRQ Signals			
Register Block	**IRQ_EN**	**IRQ_RESET**	**STATUS_MODE**	**EVENT_STATUS**
0x01F to 0x026	0x01F to 0x022; R/W per chip	0x023 to 0x026; W per chip	STATUS_MODE = IRQ_EN	0x023 to 0x26; R per chip
0x46D to 0x46F	0x47A; W per link	0x46D to 0x46F; W per link and lane	Not applicable, STATUS_MODE = 1	0x47A; R per link
0x470 to 0x473	0x47A; W per link	0x470 to 0x473; W per link	Not applicable, STATUS_MODE = 1	0x47A; R per link
0x47B[4]	0x47B[3]; R/W per link; 1 by default	0x47B[4]; W per link	Not applicable, STATUS_MODE = 1	0x47B[4]; R per link

DAC INPUT CLOCK CONFIGURATIONS

The AD9154 DAC sample clock or device clock (DACCLK) can be sourced directly through CLK± (Pin 2 and Pin 3) or by using on-chip clock multiplication with the same CLK± differential input serving as the reference. Clock multiplying employs the on-chip DAC PLL that accepts a reference clock operating at a submultiple of the desired DACCLK rate. The PLL then multiplies the reference clock up to the desired DACCLK frequency, which is then used to generate all the clocks within the AD9154.

DRIVING THE CLK± INPUTS

The CLK± differential input is shown in Figure 75. The on-chip clock receiver has a differential input impedance of 10 kΩ. CLK± are not terminated on chip; the inputs are self biased to a common-mode voltage of 600 mV. The inputs can be driven by differential PECL or LVDS drivers with ac coupling between the clock source and the receiver. A typical 100 Ω differential board level termination resistor is placed between the ac coupling capacitors and the CLK± pins.

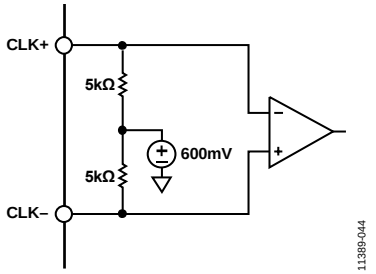


Figure 75. Clock Receiver Input Simplified Equivalent Circuit

DAC PLL FIXED REGISTER WRITES

To optimize the PLL across all operating conditions, the following SPI writes are recommended: 0x087 = 0x62, 0x088 = 0xC9, 0x089 = 0x0E, 0x08A = 0x12, 0x08D = 0x7B, 0x1B0 = 0x00, 0x1B5 = 0xC9, 0x1B9 = 0x24, 0x1BC = 0x0D, 0x1BE = 0x02, 0x1BF = 0x8E, 0x1C0 = 0x2A, 0x1C4 = 0x7E, and 0x1C5 = 0x06.

These writes properly set up the DAC PLL, including the loop filter and the charge pump.

Loop Filter

The RF PLL filter is fully integrated on-chip and is a standard passive third-order filter with five 4-bit programmable components (see Figure 76). The C1, C2, C3, R1, and R3 filter components are programmed in as listed in DAC PLL fixed register writes in the DAC PLL Fixed Register Writes section to Register 0x087, Register 0x088, and Register 0x089.

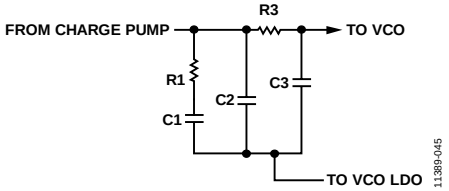


Figure 76. Loop Filter

Charge Pump

The charge pump current is 6-bit programmable variable with a range of 0.1 mA to 6.4 mA. It is programmed in Register 0x08A, Bits[5:0] as shown in the DAC PLL Fixed Register Writes section.

The charge pump is automatically calibrated the first time the DAC PLL is enabled. The charge pump calibration raises Bit 5 of Register 0x084 after it is complete and valid.

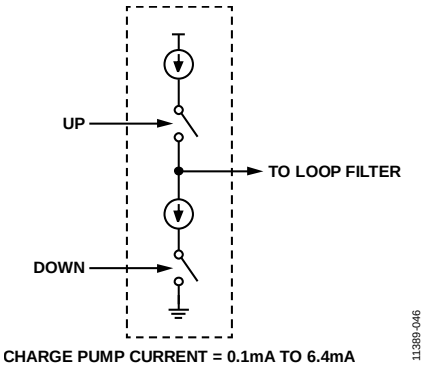


Figure 77. Charge Pump

CONDITION SPECIFIC REGISTER WRITES

Clock Multiplication Relationships

The on-chip PLL clock multiplier circuit can be used to generate the DAC sample rate clock from a lower frequency reference clock. The PLL is integrated on chip. The PLL VCO operates over a frequency range of 6 GHz to 12 GHz. The PLL configuration parameters must be programmed before the PLL is enabled. Step by step instructions on how to program the PLL can be found in the Starting the PLL section. A functional block diagram of the clock multiplier is shown in Figure 78.

When in use, the clock multiplication circuit generates the DAC sampling clock from the reference clock (REFCLK) input. The frequency of the REFCLK (CLK±) input is referred to as f_{REF}.

The REFCLK input is divided by the variable RefDivFactor. Select the RefDivFactor variable to ensure that the frequency into the phase frequency detector (PFD) block is between 35 MHz and 80 MHz. The valid values for RefDivFactor are 1, 2, 4, 8, 16, or 32. Each RefDivFactor maps to the appropriate REFDIVMODE register control according to Table 77. The REFDIVMODE register is programmed through Register 0x08C, Bits[2:0].

Table 77. Mapping of RefDivFactor to REFDIVMODE

DAC Reference Frequency Range (MHz)	Divide by (RefDivFactor)	REFDIVMODE Register 0x08C, Bits[2:0]
35 to 80	1	0
80 to 160	2	1
160 to 320	4	2
320 to 640	8	3
640 to 1000	16	4

Use the following equation to determine the RefDivFactor:

$$35\ \text{MHz} < \frac{f_{REF}}{RefDivFactor} < 80\ \text{MHz} \quad (1)$$

where:
RefDivFactor is the reference divider division ratio.
f_{REF} is the reference frequency on the CLK± input pins.

The BCount value is the divide ratio of the loop divider. It is set to divide the f_{DACCLK} to frequency match the f_{REF}/RefDivFactor. Select BCount so that the following equation is true:

$$\frac{f_{DACCLK}}{2 \times BCount} = \frac{f_{REF}}{RefDivFactor} \quad (2)$$

where:
BCount is the feedback loop divider ratio.
f_{DACCLK} is the DAC sample clock frequency.

The BCount value is programmed using Bits[7:0] of Register 0x085. It is programmable from 6 to 127.

The PFD compares f_{REF}/RefDivRate to f_{DAC}/(2 × BCount) and pulses the charge pump up or down to control the frequency of the VCO. The clock multiplication circuit operates such that the VCO outputs a frequency, f_{VCO}.

$$f_{VCO} = f_{DACCLK} \times LoDivFactor \quad (3)$$

and from Equation 2, the DAC sample clock frequency, f_{DACCLK}, is equal to

$$f_{DACCLK} = 2 \times BCount \times \frac{f_{REF}}{RefDivFact\ or} \quad (4)$$

The LODivFactor is chosen to keep f_{VCO} in the operating range between 6 GHz and 12 GHz. The valid values for LODivFactor are 4, 8, and 16. Each LODivFactor maps to a LODIVMODE value. The LODIVMODE (Register 0x08B[1:0]) is programmed as described in Table 78.

Table 78. DAC VCO Divider Selection

DAC Frequency Range (MHz)	Divide by (LODivFactor)	LODIVMODE Register 0x08B, Bits[1:0]
>1500	4	1
750 to 1500	8	2
420 to 750	16	3

Table 79 lists some common frequency examples for the RefDivFactor, LODivFactor, and BCount values that are needed to configure the PLL properly.

Table 79. Common Frequency Examples

Frequency (MHz)	f_{DACCLK} (MHz)	f_{VCO} (MHz)	RefDiv– Factor	LODiv– Factor	BCount
368.64	1474.56	11796.48	8	8	16
184.32	1474.56	11796.48	4	8	16
307.2	1228.88	9831.04	8	8	16
122.88	983.04	7864.35	2	8	8
61.44	983.04	7864.35	1	8	8
491.52	1966.08	7864.35	8	4	16
245.76	1966.08	7864.35	4	4	16

Table 79 includes different parameter sets based on f_{VCO}. The correct value to use is determined by the frequency into the phase frequency detector block of the PLL.

Temperature Tracking

When properly configured, the device automatically selects one of the 512 VCO bands. The PLL settings selected by the device ensure that the PLL remains locked over the full −40°C to +85°C operating temperature range of the device without further adjustment. The PLL remains locked over the full temperature range even if the temperature during initialization is at one of the temperature extremes.

To properly configure temperature tracking, follow the settings in the DAC PLL Fixed Register Writes section and the f_{vco} dependent SPI writes shown in Table 80.

Table 80. VCO Control Lookup Table Reference

VCO Frequency Range (GHz)	Register 0x1B4 Setting	Register 0x1B6 Setting	Register 0x1BB Setting
$f_{VCO} < 6.85$	0x60	0x49	0x15
$6.85 \le f_{VCO} < 8.72$	0x60	0x49	0x13
$8.72 \le f_{VCO} < 10.7$	0x60	0x4D	0x13
$f_{VCO} \ge 10.7$	0x78	0x4D	0x04

STARTING THE PLL

The programming sequence for the DAC PLL is as follows:

1. Use the equations in the Clock Multiplication Relationships section to find f_{VCO}, f_{REF}, BCount, REFDIVMODE, and LODIVMODE .
2. Program the registers in the DAC PLL Fixed Register Writes section.
3. Program LODIVMODE into Register 0x08B, Bits[1:0].
4. Program the BCount in Register 0x085, Bits[7:0].
5. Program REFDIVMODE in Register 0x08C, Bits[2:0].
6. Based on the f_{VCO} found in Step 1, write the temperature tracking registers as shown in Table 80.
7. Enable the DAC PLL synthesizer by setting Register 0x083, Bit 4 to 1.

Register 0x084, Bit 5 notifies the user that the DAC PLL calibration is completed and is valid.

Register 0x084, Bit 1 notifies the user that the PLL has locked.

Register 0x084, Bits[7:6] and Register 0x084, Bit 5 notify the user that the DAC PLL hit the upper or lower edge of its operating band, respectively. If either of these bits are high, recalibrate the DAC PLL by setting Register 0x083, Bit 7 to 0 and then 1.

DAC PLL IRQ

The DAC PLL lock and lost signals are available as IRQ events. Use Register 0x01F, Bit 5 and Bit 4 to enable these signals, and then use Register 0x023, Bit 5 and Bit 4 to read back their statuses and reset the IRQ signals. See the Interrupt Request Operation section.

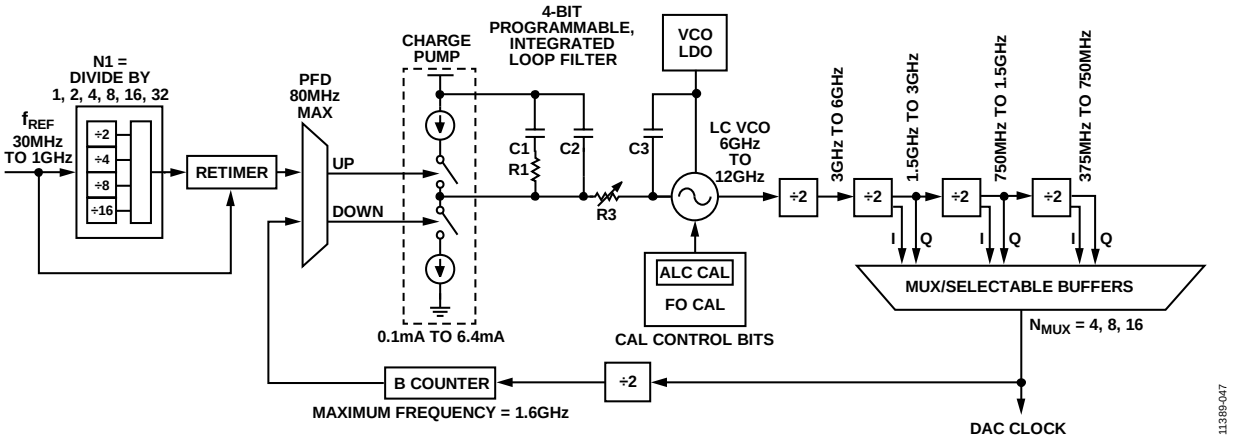


Figure 78. Device Clock PLL Block Diagram

ANALOG OUTPUTS

TRANSMIT DAC OPERATION

Figure 79 shows a simplified block diagram of the transmit path DAC cores. There are four DAC cores: DAC0 and DAC2 are designated I DACs; DAC1 and DAC3 are designated Q DACs. The DAC cores consist of a current switch array, digital control logic, and full-scale output current control. The DAC full-scale output current (I_{OUTFS}) is defined in Table 1. The output currents from the OUTx± pins are complementary, meaning that the sum of the two currents always equals the full-scale current of the DAC. OUTx± are current sinks. Current flows into the OUTx± ports. The digital input code to the DAC determines the differential current output.

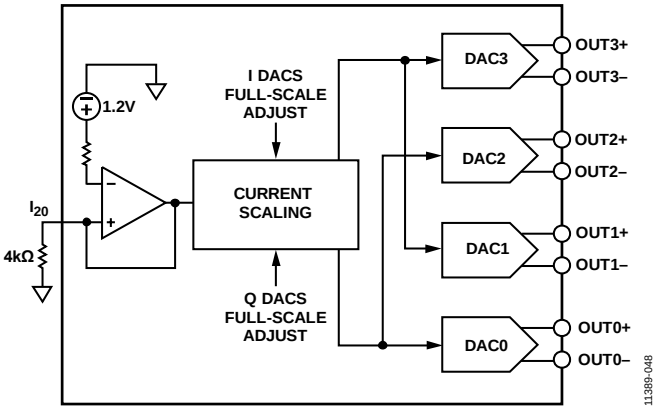


Figure 79. Simplified Block Diagram of the DAC Core

A 4 kΩ external resistor, R_{SET}, must be connected from the I120 pin to ground. This resistor, along with the reference control amplifier, sets up the correct internal bias currents for each DAC core.

The full-scale current equation, where the DAC gain is set for each I DAC core pair and each Q DAC core pair in Registers 0x040 through Register 0x043 is as follows:

$$I_{OUTFS} = \frac{V_{REF}}{R_{SET}} \times \left(13.33 + \left(\frac{1}{19.19} \times DAC\ gain \right) \right) \quad (5)$$

Figure 80 is a plot of I_{OUTFS} as a function of DAC_GAIN_Ix and DAC_GAIN_Qx

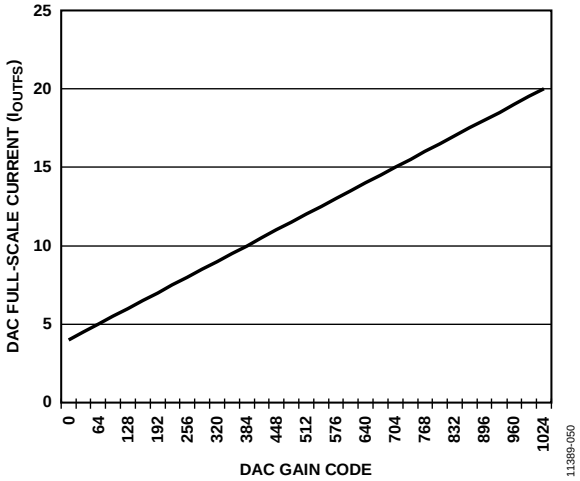


Figure 80. DAC Full-Scale Current (I_{OUTFS}) vs. DAC Gain Code

Transmit DAC Transfer Function

The output currents drawn by the OUTx+ and OUTx– pins are complementary, meaning that the sum of the two (positive plus negative) currents always equals the full-scale current of the DAC, I_{OUTFS}. The digital input code to a DAC determines the differential current output. The OUTx+ pins provide the maximum output current when all bits are high. The output currents vs. DACCODE for the DAC outputs are expressed as

$$I_{OUTP} = \left[\frac{DACCODE}{2^N} \right] \times I_{OUTFS} \quad (6)$$

$$I_{OUTN} = I_{OUTFS} - I_{OUTP} \quad (7)$$

where *DACCODE* = 0 to $2^N - 1$ and is the digital signal input to a DAC core consisting of a stream of 16 bit samples.

NORMAL AND MIX MODES OF OPERATION

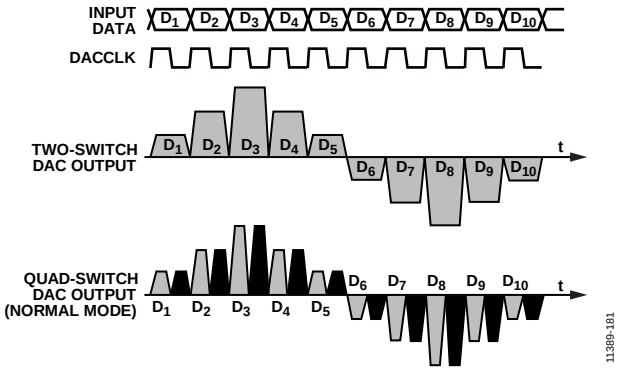


Figure 81. Two-Switch and Quad-Switch DAC Waveforms

The DAC cores have a quad-switch architecture. During each DACCLK cycle, one input sample is presented twice. Figure 81 shows the time domain DAC core output when operating in normal mode (default). In normal mode, the same output signal is presented twice during each DAC clock cycle. The DAC output mode is selected using Bit 0 of Register 0x04A.

Figure 82 depicts a time domain DAC output signal in mix mode. During each DACCLK cycle, the input sample is presented at the output on the rising edge and the inverse of the input sample is presented at the output on the falling edge of DACCLK.

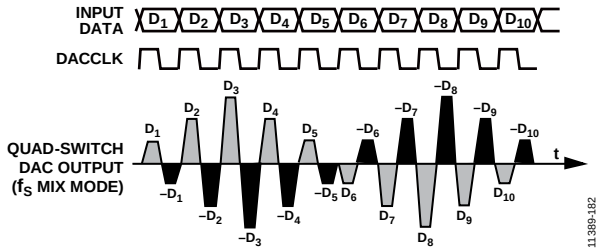


Figure 82. Mix Mode Waveform

Figure 83 is a depiction of the uncompensated DAC SINC roll-off for normal (or baseband) mode and for mix mode. In normal mode, the first Nyquist zone copy of the output signal has the highest amplitude. The output sampling images in the second and third Nyquist zones are attenuated. In MIX mode, the second and third Nyquist zone sampling images are emphasized, and the first Nyquist zone signal is attenuated.

This ability to change modes provides the user the flexibility to place a carrier anywhere in the first three Nyquist zones, depending on the operating mode selected. Switching between baseband and mix mode reshapes the sinc roll-off inherent at the DAC output.

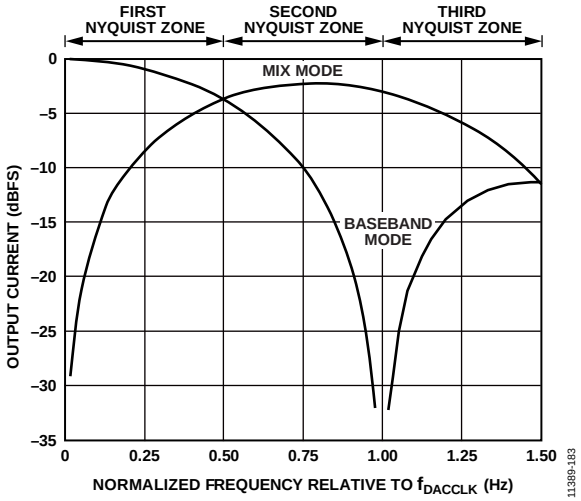


Figure 83. Sinc Roll-Off for Normal Mode and Mix-Mode Operation

TEMPERATURE SENSOR

The AD9154 has a band gap temperature sensor for monitoring junction temperature changes on the AD9154 die. The temperature must be calibrated against a known temperature to remove the device-to-device variation in the band gap circuit used to sense the temperature.

To monitor temperature change, the user must take a reading at a known ambient temperature for a single-point calibration of each AD9154 device.

$$Tx = T_{REF} + 7.3 \times (CODE_X - CODE_REF)/1000$$

where:
CODE_X is the DIE_TEMP readback code from Register 0x132 and Register 0x133 at the unknown temperature, *Tx*.
CODE_REF is the DIE_TEMP readback from the same addresses at the calibrated temperature, T_{REF}.

To use the temperature sensor, it must be enabled by setting Register 0x12F, Bit 0, to 1. The user must write a 1 to Register 0x134, Bit 0 before reading back the die temperature from Register 0x132 and Register 0x133.

EXAMPLE START-UP SEQUENCE

Table 81 through Table 90 show the register writes needed to set up the AD9154 with f_{DAC} = 1474.56 MHz, 2× interpolation, and the DAC PLL enabled with a 368.64 MHz reference clock. The JESD204B interface is configured in Mode 4, dual link mode, Subclass 1, and scrambling is enabled with all eight SERDES lanes running at 7.3728 Gbps, inputting twos complement formatted data. No remapping of lanes with the crossbar is performed in this example.

The sequence of steps to properly start up the AD9154 is as follows:

1. Set up the SPI interface, power up necessary circuit blocks, make required writes to the configuration register, and set up the DAC clocks (see Step 1: Start Up the DAC).
2. Set the digital features of the AD9154 (see Step 2: Digital Datapath).
3. Set up the JESD204B links (see Step 3: Transport Layer).
4. Set up the physical layer of the SERDES interface (see Step 4: Physical Layer).
5. Set up the data link layer of the SERDES interface. This procedure is for quick startup or debug only and does not guarantee deterministic latency (see Step 5: Data Link Layer).
6. Check for errors on Link 0 and Link 1 (see Step 6: Error Monitoring).

These steps are outlined in detail in the following sections, within tables that list the required register write and read commands.

STEP 1: START UP THE DAC

Power-Up and DAC Initialization

Table 81. Power-Up and DAC Initialization

Command	Address	Value	Description
W	0x000	0xBD	Soft reset
W	0x000	0x3C	Deassert reset, set 4-wire SPI
W	0x011	0x00	Enable reference, DAC channels, and master DAC
W	0x080	0x04	Power up all clocks with duty cycle correction on
W	0x081	0x00	Power up SYSREF receiver, disable hysteresis

Required Device Configurations

Table 82. Required Device Configuration

Command	Address	Value	Description
W	0x12D	0x8B	Digital datapath configuration
W	0x146	0x01	Digital datapath configuration
W	0x333	0x01	JESD interface configuration

Configure the DAC PLL

Table 83. Configure DAC PLL

Command	Address	Value	Description
W	0x087	0x62	Optimal DAC PLL loop filter settings
W	0x088	0xC9	Optimal DAC PLL loop filter settings
W	0x089	0x0E	Optimal DAC PLL loop filter settings
W	0x08A	0x12	Optimal DAC PLL CP settings
W	0x08D	0x7B	Optimal DAC LDO settings for DAC PLL
W	0x1B0	0x00	Power DAC PLL blocks when power machine disabled
W	0x1B5	0xC9	Optimal DAC PLL VCO settings
W	0x1B9	0x24	Optimal DAC PLL calibration options settings
W	0x1BC	0x0D	Optimal DAC PLL block control settings
W	0x1BE	0x02	Optimal DAC PLL VCO power control settings
W	0x1BF	0x8E	Optimal DAC PLL VCO calibration settings
W	0x1C0	0x2A	Optimal DAC PLL lock counter length setting
W	0x1C1	0x2A	Optimal DAC PLL CP setting
W	0x1C4	0x7E	Optimal DAC PLL varactor settings
W	0x1C5	0x06	Optimal DAC PLL VCO settings
W	0x08B	0x02	Set the VCO LO divider to 8 so that 6 GHz ≤ $f_{VCO} = f_{DACCLK} \times 2^{(LODivMode + 1)}$ ≤ 12 GHz
W	0x08C	0x03	Set the reference clock divider
W	0x085	0x10	Set the B counter to 16 to divide the DAC clock down to 2× the reference clock
W	0x1B6	0x4D	Write VCO Varactor settings from Table 80
W	0x1BB	0x04	Write VCO bias reference and TC from Table 80
W	0x1B4	0x78	Write VCO calibration offset from Table 80
W	0x1C5	0x06	Write VCO Varactor reference
W	0x083	0x10	Enable DAC PLL
R	0x084	0x01	Verify that Bit 1 reads back high for PLL locked

STEP 2: DIGITAL DATAPATH

Table 84. Digital Datapath

Command	Address	Value	Description
W	0x112	0x01	Set the interpolation to 2×
W	0x110	0x00	Set twos complement data format

STEP 3: TRANSPORT LAYER

Table 85. Link 0 Transport Layer

Command	Address	Value	Description
W	0x200	0x00	Power up the interface
W	0x201	0x00	Enable all lanes
W	0x300	0x08	Bit 3 = 1 for dual link, Bit 2 = 0 to access Link 0 registers
W	0x450	0x00	Set the device ID to match Tx (0x00 in this example)
W	0x451	0x00	Set the bank ID to match Tx (0x00 in this example)
W	0x452	0x00	Set the lane ID to match Tx (0x00 in this example)
W	0x453	0x83	Set descrambling and L = 4 (in n – 1 notation)
W	0x454	0x00	Set F = 1 (in n – 1 notation)
W	0x455	0x1F	Set K = 32 (in n – 1 notation)
W	0x456	0x01	Set M = 2 (in n – 1 notation)
W	0x457	0x0F	Set N = 16 (in n – 1 notation)
W	0x458	0x2F	Set Subclass 1 and NP = 16 (in n – 1 notation)
W	0x459	0x20	Set JESD 204B Version and S = 1 (in n – 1 notation)
W	0x45A	0x80	Set HD = 1
W	0x45D	0x45	Set checksum for Lane 0
W	0x46C	0x0F	Deskew Lane 0 to Lane3
W	0x476	0x01	Set F (not in n – 1 notation)
W	0x47D	0x0F	Enable Lane 0 to Lane 3

Table 86. Link 1 Transport Layer

Command	Address	Value	Description
W	0x300	0x0C	Bit 3 = 1 for dual link, Bit 2 = 1 to access registers for Link 1
W	0x450	0x00	Set the device ID to match Tx (0x00 in this example)
W	0x451	0x00	Set the bank ID to match Tx (0x00 in this example)
W	0x452	0x04	Set the lane ID to match Tx (0x04 in this example)
W	0x453	0x83	Set descrambling and L = 4 (in n – 1 notation)
W	0x454	0x00	Set F = 1 (in n – 1 notation)
W	0x455	0x1F	Set K = 32 (in n – 1 notation)
W	0x456	0x01	Set M = 2 (in n – 1 notation)
W	0x457	0x0F	Set N = 16 (in n – 1 notation)
W	0x458	0x2F	Set Subclass 1 and NP = 16 (in n – 1 notation)
W	0x459	0x20	Set JESD 204B and S = 1 (in n – 1 notation)
W	0x45A	0x80	Set HD
W	0x45D	0x45	Set checksum for Lane 0
W	0x46C	0x0F	Deskew Lane 4 to Lane 7
	0x476	0x01	Set F (not in n – 1 notation)
W	0x47D	0x0F	Enable Lane 4 to Lane 7

STEP 4: PHYSICAL LAYER

Table 87. Physical Layer

Command	Address	Value	Description
W	0x2A7	0x01	Autotune PHY setting
W	0x2AE	0x01	Autotune PHY setting
W	0x314	0x01	SERDES SPI configuration
W	0x230	0x28	Configure CDRs in half rate mode
W	0x206	0x00	Resets CDR logic
W	0x206	0x01	Release CDR logic reset
W	0x289	0x04	Configure PLL divider to 1 along with PLL required configuration
W	0x284	0x62	Optimal SERDES PLL loop filter
W	0x285	0xC9	Optimal SERDES PLL loop filter
W	0x286	0x0E	Optimal SERDES PLL loop filter
W	0x287	0x12	Optimal SERDES PLL charge pump
W	0x28A	0x7B	Optimal SERDES PLL VCO LDO
W	0x28B	0x00	Optimal SERDES PLL PD
W	0x290	0x89	Optimal SERDES PLL VCO
W	0x291	0x4C	Optimal SERDES PLL VCO
W	0x294	0x24	Optimal SERDES PLL charge pump
W	0x296	0x1B	Optimal SERDES PLL VCO
W	0x297	0x0D	Optimal SERDES PLL VCO
W	0x299	0x02	Optimal SERDES PLL PD
W	0x29A	0x8E	Optimal SERDES PLL VCO
W	0X29C	0x2A	Optimal SERDES PLL charge pump
W	0x29F	0x7E	Optimal SERDES PLL VCO
W	0x2A0	0x06	Configure SERDES PLL VCO
W	0x280	0x01	Enable SERDES PLL
R	0x281	0x01	Verify that Bit 0 reads back high for SERDES PLL lock
W	0x268	0x62	Set equalizer mode to low power

STEP 5: DATA LINK LAYER

Note that this procedure does not guarantee deterministic latency.

Table 88. Data Link Layer (Does Not Guarantee Deterministic Latency)

Command	Address	Value	Description
W	0x301	0x01	Set subclass = 1
W	0x304	0x00	Set the LMFC delay setting to 0
W	0x305	0x00	Set the LMFC delay setting to 0
W	0x306	0x0A	Set the LMFC receive buffer delay to 10
W	0x307	0x0A	Set the LMFC receive buffer delay to 10
W	0x03A	0x01	Set sync mode to one-shot sync
W	0x03A	0x81	Enable the sync machine
W	0x03A	0xC1	Arm the sync machine
SYSREF±			Ensure that at least one SYSREF± edge is sent to the device
W	0x300	0x0B	Bit 1 and Bit 0 = 1 to enable Link 0 and Link 1, Bit 2 = 0 to access Link 0

STEP 6: ERROR MONITORING

Link 0 Checks

Confirm that the registers in Table 89 read back as noted and system tasks are completed as described.

Table 89. Link 0 Checks

Command	Address	Value	Description
R	0x470	0x0F	Acknowledge that four consecutive K28.5 characters have been detected on Lane 0 to Lane 3.
$\overline{\text{SYNCOUT0}}$±			Confirm that $\overline{\text{SYNCOUT0}}$± is high.
SERDINx±			Apply ILAS and data to the SERDES input pins.
R	0x471	0x0F	Check for frame sync on all lanes.
R	0x472	0x0F	Check for good checksum.
R	0x473	0x0F	Check for ILAS.

Link 1 Checks

Confirm that the registers in Table 90 read back as noted and system tasks are completed as described.

Table 90. Link 1 Checks

Command	Address	Value	Description
W	0x300	0x0F	Bit 2 = 1 to access Link 1.
R	0x470	0x0F	Acknowledge that four consecutive K28.5 characters have been detected on Lane 4 to Lane 7.
$\overline{\text{SYNCOUT1}}$±			Confirm that $\overline{\text{SYNCOUT1}}$± is high.
SERDINx±			Apply ILAS and data to the SERDES input pins.
R	0x471	0x0F	Check for frame sync on all lanes.
R	0x472	0x0F	Check for good checksum.
R	0x473	0x0F	Check for ILAS.

BOARD LEVEL HARDWARE CONSIDERATIONS

POWER SUPPLY RECOMMENDATIONS

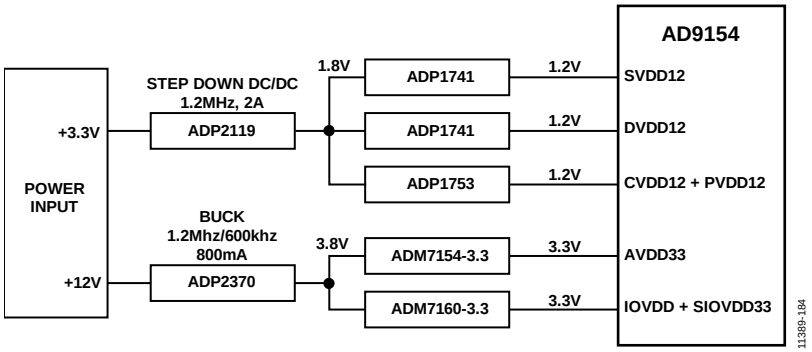


Figure 84. Power Supply Connections

Table 91. Power Supplies

Power Supply Domain	Voltage (V)	Circuitry
DVDD12[1]	1.2	Digital core
PVDD12[2]	1.2	DAC PLL
SVDD12[3]	1.2	JESD204B receiver interface
CVDD12[1]	1.2	DAC clocking
IOVDD	3.3	SPI interface
V_{TT}[4]	1.2	V_{TT}
SIOVDD33	3.3	Sync LVDS transmit
AVDD33	3.3	DAC

[1] This supply requires a 1.3 V supply when operating at maximum DAC sample rates. See Table 3 for details.
[2] This supply may be combined with CVDD12 on the same regulator with a separate supply filter network and sufficient bypass capacitors near the pins.
[3] This supply requires a 1.3 V supply when operating at maximum interface rates. See Table 4 for details.
[4] This supply is connected to SVDD12 and does not need separate circuitry.

The power supply domains are described in Table 91. The power supplies can be grouped into separate PCB domains as show in Figure 84. All the AD9154 supply domains must remain as noise free as possible. Optimal DAC output NSD and DAC output phase noise performance can be achieved using linear regulators that provide excellent power supply rejection. AVDD33, PVDD12, and CVDD12 are particularly sensitive to supply noise.

JESD204B SERIAL INTERFACE INPUTS (SERDIN0± TO SERDIN7±)

When considering the layout of the JESD204B serial interface transmission lines, there are many factors to consider to maintain optimal link performance. Among these factors are insertion loss, return loss, signal skew, and the topology of the differential traces.

Insertion Loss

The JESD204B specification limits the amount of insertion loss allowed in the transmission channel (see Figure 44). The AD9154 equalization circuitry allows significantly more loss in the channel than is required by the JESD204B specification. It is still important that the designer of the PCB minimize the amount of insertion loss by adhering to the following guidelines:

- Keep the differential traces short by placing the AD9154 as near to the transmitting logic device as possible and routing the trace as directly as possible between the devices.
- Route the differential pairs on a single plane using a solid ground plane as a reference.
- Use a PCB material with a low dielectric constant (<4) to minimize loss, if possible.

When choosing between stripline and microstrip techniques, consider the following: stripline has less loss (see Figure 45) and emits less EMI, but requires the use of vias that can add complexity to the task of controlling the impedance, whereas microstrip (see Figure 46) is easier to implement if the component placement and density allow routing on the top layer and eases the task of controlling the impedance.

If using the top layer of the PCB is problematic or the advantages of stripline are desirable, follow these recommendations:

- Minimize the number of vias.
- If possible, use blind vias to eliminate via stub effects and use micro vias to minimize via inductance.

- If using standard vias, use the maximum via length to minimize the stub size. For example, on an 8-layer board, use Layer 7 for the stripline pair (see Figure 85).
- For each via pair, place a pair of ground vias adjacent to them to minimize the impedance discontinuity (see Figure 85).

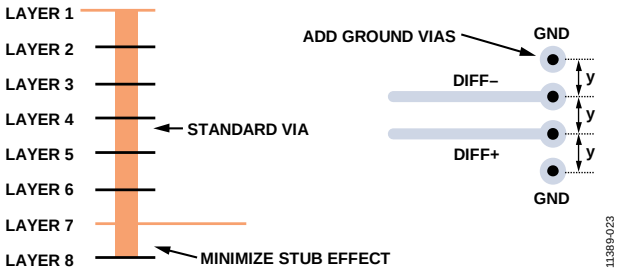


Figure 85. Minimizing Stub Effect and Adding Ground Vias for Differential Stripline Traces

Return Loss

The JESD204B specification limits the amount of return loss allowed in a converter device and a logic device, but does not specify return loss for the channel. However, every effort must be made to maintain a continuous impedance on the transmission line between the transmitting logic device and the AD9154. As mentioned in the Insertion Loss section, minimizing the use of vias, or eliminating them all together, reduces one of the primary sources for impedance mismatches on a transmission line. Maintain a solid reference beneath (for microstrip) or above and below (for stripline) the differential traces to ensure continuity in the impedance of the transmission line. If the stripline technique is used, follow the guidelines listed in the Insertion Loss section to minimize impedance mismatches and stub effects.

Another primary source for impedance mismatch is at either end of the transmission line, where care must be taken to match the impedance of the termination to that of the transmission line. The AD9154 handles this internally with a calibrated termination scheme for the receiving end of the line. See the Interface Power-Up and Input Termination section for details on this circuit and the calibration routine.

Signal Skew

There are many sources for signal skew, but the two sources to consider when laying out a PCB are interconnect skew within a single JESD204B link and skew between multiple JESD204B links. In each case, keeping the channel lengths matched to within 15 mm is adequate for operating the JESD204B link at speeds of up to 10.6 Gbps. Managing the interconnect skew within a single link is fairly straightforward. Managing multiple links across multiple devices is more complex. However, follow the 15 mm guideline for length matching.

Topology

Structure the differential SERDINx± pairs to achieve 50 Ω to ground for each half of the pair. Stripline vs. microstrip trade-offs are described in the Insertion Loss section. In either case, it is important to keep these transmission lines separated from potential noise sources such as high speed digital signals and noisy supplies. If using stripline differential traces, route them using a coplanar method, with both traces on the same layer. Although this does not offer more noise immunity than the broadside routing method (traces routed on adjacent layers), it is easier to route and manufacture so that the impedance continuity is maintained. An illustration of broadside vs. coplanar is shown in Figure 86.

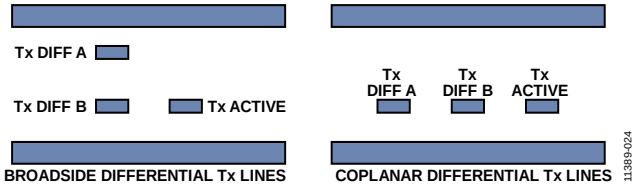


Figure 86. Broadside vs. Coplanar Differential Stripline Routing Techniques

When considering the trace width vs. copper weight and thickness, the speed of the interface must be considered. At multigigabit speeds, the skin effect of the conducting material confines the current flow to the surface. Maximize the surface area of the conductor by making the trace width made wider to reduce the losses. Additionally, loosely couple differential traces to accommodate the wider trace widths. This helps reduce the crosstalk and minimize the impedance mismatch when the traces must separate to accommodate components, vias, connectors, or other routing obstacles. Tightly coupled vs. loosely coupled differential traces are shown in Figure 87.

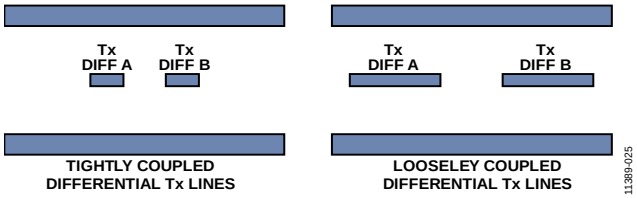


Figure 87. Tightly Coupled vs. Loosely Coupled Differential Traces

AC Coupling Capacitors

The AD9154 requires that the JESD204B input signals be ac-coupled to the source. These capacitors must be 100 nF and placed as close as possible to the transmitting logic device. To minimize the impedance mismatch at the pads, select the package size of the capacitor so that the pad size on the PCB matches the trace width as closely as possible.

SYNCOUTx±, SYSREF±, and CLK± Signals

The SYNCOUTx± and SYSREF± signals on the AD9154 are low speed LVDS differential signals. Use controlled impedance traces routed with 100 Ω differential impedance and 50 Ω to ground when routing these signals. As with the SERDIN0± to SERDIN7± data pairs, it is important to keep these signals separated from potential noise sources such as high speed digital signals and noisy supplies.

Separate the SYNCOUTx± signal from other noisy signals, because noise on the SYNCOUTx± might be interpreted as a request for K characters.

It is important to keep similar trace lengths for the CLK± and SYSREF± signals from the clock source to each of the devices on either end of the JESD204B links, see Figure 88. If using a clock chip that can tightly control the phase of CLK± and SYSREF±, the trace length matching requirements are greatly reduced.

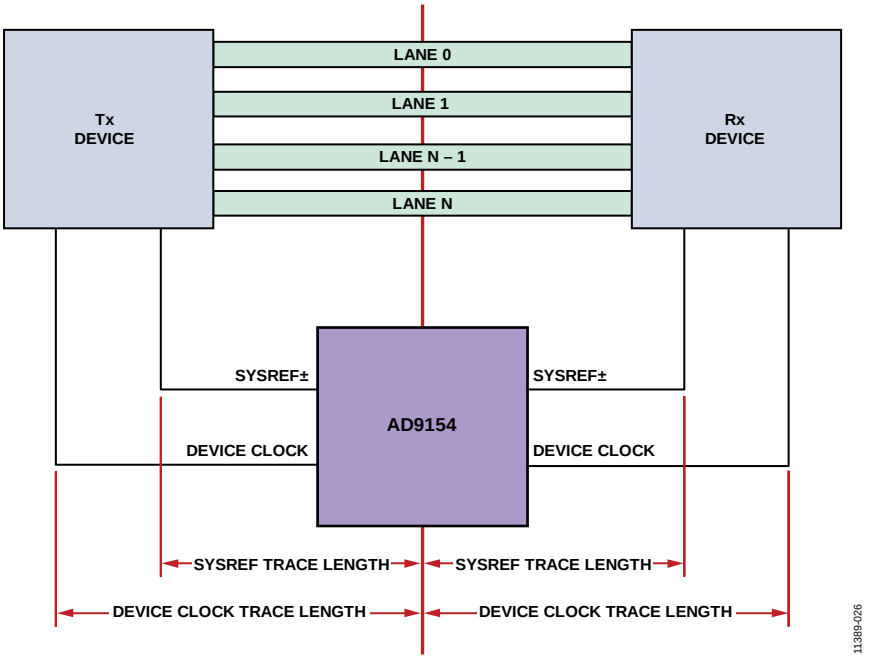


Figure 88. SYSREF± Signal and Device Clock Trace Length

REGISTER SUMMARY

Table 92. AD9154 Register Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x000	SPI_INTFCONFA	SOFTRESET_M	LSBFIRST_M	ADDRINC_M	SDOACTIVE_M	SDOACTIVE	ADDRINC	LSBFIRST	SOFTRESET	0x00	R/W
0x003	SPI_CHIPTYPE	CHIPTYPE								0x04	R
0x004	SPI_PRODIDL	PRODIDL								0x54	R
0x005	SPI_PRODIDH	PRODIDH								0x91	R
0x006	SPI_CHIPGRADE	PROD_GRADE				DEV_REVISION				0x89	R
0x008	DUAL_PAGE	RESERVED						PAGEINDX		0x03	R/W
0x011	PWRCNTRL0	PD_BG	PDDAC0	PDDAC1	PDDAC2	PDDAC3	RESERVED			0xF8	R/W
0x012	TXENMASK1	DACB_MASK	DACA_MASK	RESERVED						0x00	R/W
0x013	PWRCNTRL3	RESERVED	ENA_PA_CTRL_FROM_PAPROT_ERR	ENA_PA_CTRL_FROM_TXENSM	ENA_PA_CTRL_FROM_BLSM	ENA_PA_CTRL_FROM_SPI	SPI_PA_CTRL	ENA_SPI_TXEN	SPI_TXEN	0x20	R/W
0x014	COARSE_GROUP_DLY	RESERVED				COARSE_GROUP_DLY				0x88	R/W
0x01F	IRQ_ENABLE0	RESERVED		EN_DAC PLLLOST	EN_DAC PLLLOCK	EN_SER-PLLLOST	EN_SER-PLLLOCK	EN_LANE-FIFOERR	RESERVED	0x00	R/W
0x020	IRQ_ENABLE1	RESERVED				EN_PRBSQ1	EN_PRBSI1	EN_PRBSQ0	EN_PRBSI0	0x00	R/W
0x021	IRQ_ENABLE2	EN_PAERR0	RESERVED	EN_BLNKDONE0	EN_REFNCOCLR0	EN_REFLOCK0	EN_REFROTA0	EN_REFWLIM0	EN_REFTRIP0	0x00	R/W
0x022	IRQ_ENABLE3	EN_PAErr1	RESERVED	EN_BLNKDONE1	EN_REFNCOCLR1	EN_REFLOCK1	EN_REFROTA1	EN_REFWLIM1	EN_REFTRIP1	0x00	R/W
0x023	IRQ_STATUS0	RESERVED		IRQ_DAC-PLLLOST	IRQ_DAC-PLLLOCK	IRQ_SERPLLLOST	IRQ_SERPLLLOCK	IRQ_LANE FIFOERR	RESERVED	0x00	R
0x024	IRQ_STATUS1	RESERVED				IRQ_PRBSQ1	IRQ_PRBSI1	IRQ_PRBSQ0	IRQ_PRBSI0	0x00	R
0x025	IRQ_STATUS2	IRQ_PAErr0	RESERVED	IRQ_BLNKDONE0	IRQ_REFNCOCLR0	IRQ_REF-LOCK0	IRQ_REFROTA0	IRQ_REFWLIM0	IRQ_REFTRIP0	0x00	R
0x026	IRQ_STATUS3	IRQ_PAErr1	RESERVED	IRQ_BLNKDONE1	IRQ_REFNCOCLR1	IRQ_REFLOCK1	IRQ_REFROTA1	IRQ_REFWLIM1	IRQ_REFTRIP1	0x00	R
0x030	JESD_CHECKS	RESERVED		ERR_DLYOVER	ERR_WINLIMIT	ERR_JESDBAD	ERR_KUNSUPP	ERR_SUBCLASS	ERR_INTSUPP	0x00	R
0x034	SYNC_ERRWINDOW	RESERVED					ERRWINDOW			0x00	R/W
0x038	SYNC_LASTERR_L	LASTERROR_L								0x00	R
0x039	SYNC_LASTERR_H	LASTUNDER	LASTOVER	RESERVED					LAST ERROR_H	0x00	R
0x03A	SYNC_CONTROL	SYNCENABLE	SYNCARM	SYNCCLRSTKY	SYNCCLRLAST	SYNCMODE				0x00	R/W
0x03B	SYNC_STATUS	REFBUSY	RESERVED			REFLOCK	REFROTA	REFWLIM	REFTRIP	0x00	R
0x03C	SYNC_CURRERR_L	CURRERROR_L								0x00	R
0x03D	SYNC_CURRERR_H	CURRUNDER	CURROVER	RESERVED					CURR-ERROR_H	0x00	R
0x040	DAC_GAIN0_I	RESERVED						DAC_GAIN_I1		0x03	R/W
0x041	DAC_GAIN1_I	DAC_GAIN_I0								0xFF	R/W
0x042	DAC_GAIN0_Q	RESERVED						DAC_GAIN_Q1		0x03	R/W
0x043	DAC_GAIN1_Q	DAC_GAIN_Q0								0xFF	R/W
0x044	GROUPDELAY COMP_I	GROUP DELAY COMP I [7:0]								0x00	R/W
0x045	GROUPDELAY COMP_Q	GROUP DELAY COMP Q [7:0]								0x00	R/W
0x046	GROUPDELAY COMP_BYP	RESERVED						GROUP-COMP_BYPI	GROUP-COMP_BYPQ	0x03	R/W
0x04A	MIX_MODE	RESERVED							MIX_MODE	0x00	R/W
0x050	NCO_CLRMODE	NCOCLRARM	RESERVED	NCOCLRMTCH	NCOCLRPASS	NCOCLRFAIL	RESERVED	NCOCLRMODE		0x00	R/W
0x051	NCOKEY_ILSB	NCOKEYILSB								0x00	R/W
0x052	NCOKEY_IMSB	NCOKEYIMSB								0x00	R/W
0x053	NCOKEY_QLSB	NCOKEYQLSB								0x00	R/W

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x054	NCOKEY_QMSB	NCOKEYQMSB								0x00	R/W
0x060	PA_THRES0	PDP_THRESHOLD[7:0]								0x00	R/W
0x061	PA_THRES1	RESERVED			PDP_THRESHOLD[12:8]					0x00	R/W
0x062	PDP_AVG_TIME	PDP_ENABLE	PA_BUS_SWAP	RESERVED		PDP_AVG_TIME				0x00	R/W
0x063	PA_POWER0	PDP_POWER[7:0]								0x00	R
0x064	PA_POWER1	RESERVED		PDP_POWER[12:8]						0x00	R
0x080	CLKCFG0	PD_CLK01	PD_CLK23	PDCLOCKDIG	PD_PCLK	PDCLOCK-REC	DUTY_EN	RF_SYNC_EN	RF_CLKDIV_EN	0xFE	R/W
0x081	SYSREF_ACTRL0	RESERVED			PDSYSREF	HYS_ON	SYSREF_RISE	HYS_CNTRL1		0x10	R/W
0x082	SYSREF_ACTRL1	HYS_CNTRL0								0x00	R/W
0x083	DACPLLCNTRL	SYNTH_RECAL	RESERVED		ENABLE_SYNTH	RESERVED				0x00	R/W
0x084	DACPLLSTATUS	CP_OVERRANGE_H		CP_OVERRANGE_L	CP_CAL_VALID	VCO_CAL_PROGRESS	RESERVED	RFPLL_LOCK	RESERVED	0x00	R/W
0x085	DACINTEGER-WORD0	BCOUNT								0x06	R/W
0x087	DACLOOPFILT1	LF_C2_WORD				LF_C1_WORD				0x88	R/W
0x088	DACLOOPFILT2	LF_R1_WORD				LF_C3_WORD				0x88	R/W
0x089	DACLOOPFILT3	LF_BYPASS_R3	LF_BYPASS_R1	LF_BYPASS_C2	LF_BYPASS_C1	LF_R3_WORD				0x08	R/W
0x08A	DACCPCNTRL	RESERVED	VT_FORCE	CP_CURRENT						0x20	R/W
0x08B	DACLOGEN-CNTRL	RESERVED		LO_POWER_MODE		RESERVED		LODIVMODE		0x00	R/W
0x08C	DACLDOCNTRL1	LDO_REF_SEL	LDO_BYPASS_FILT	RESERVED			REFDIVMODE			0x00	R/W
0x08D	DACLDOCNTRL2	LDO_BYPASS	LDO_INRUSH		LDO_SEL			LDO_VDROP		0x2B	R/W
0x110	DATA_FORMAT	DATA_FMT	RESERVED							0x00	R/W
0x111	DATAPATH_CTRL	INVSINC_ENABLE	RESERVED	DIG_GAIN_ENABLE	PHASE_ADJ_ENABLE	MODULATION_TYPE		SEL_SIDEBAND	I_TO_Q	0xA0	R/W
0x112	INTERPMODE	RESERVED					INTERPMODE			0x01	R/W
0x113	NCO_FTW_UPDATE	RESERVED						FTW_UP-DATE_ACK	FTW_UP-DATE_REQ	0x00	R/W
0x114	FTW0	FTW0								0x00	R/W
0x115	FTW1	FTW1								0x00	R/W
0x116	FTW2	FTW2								0x00	R/W
0x117	FTW3	FTW3								0x00	R/W
0x118	FTW4	FTW4								0x00	R/W
0x119	FTW5	FTW5								0x10	R/W
0x11A	NCO_PHASE_OFFSET0	NCO_PHASE_OFFSET0								0x00	R/W
0x11B	NCO_PHASE_OFFSET1	NCO_PHASE_OFFSET1								0x00	R/W
0x11C	NCO_PHASE_ADJ0	PHASEADJ[7:0]								0x00	R/W
0x11D	NCO_PHASE_ADJ1	PHASEADJ[12:8]								0x00	R/W
0x11F	TXEN_SM_0	PA_FALL		PA_RISE		RESERVED	GP_PA_ON_INVERT	GP_PA_CTRL	TXEN_SM_EN	0x83	R/W
0x121	TXEN_SM_2	RISE_COUNT_0								0x0F	R/W
0x122	TXEN_SM_3	RISE_COUNT_1								0x00	R/W
0x123	TXEN_SM_4	FALL_COUNT_0								0xFF	R/W
0x124	TXEN_SM_5	FALL_COUNT_1								0xFF	R/W
0x12D	DEVICE_CONFIG_REG0	DEVICE_CONFIG_0								0x46	R/W
0x12F	DIE_TEMP_CTRL0	RESERVED							AUXADC_ENABLE	0x20	R/W
0x132	DIE_TEMP0	DIE_TEMP_LSB								0x00	R
0x133	DIE_TEMP1	DIE_TEMP_MSB								0x00	R

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x134	DIE_TEMP_UPDATE	RESERVED							DIE_TEMP_UPDATE	0x00	R/W
0x135	DC_OFFSET_CTRL	RESERVED							DC_OFFSET_ON	0x00	R/W
0x136	IPATH_DC_OFFSET_1PART0	IPATH_DC_OFFSET_1PART0								0x00	R/W
0x137	IPATH_DC_OFFSET_1PART1	IPATH_DC_OFFSET_1PART1								0x00	R/W
0x138	QPATH_DC_OFFSET_1PART0	QPATH_DC_OFFSET_1PART0								0x00	R/W
0x139	QPATH_DC_OFFSET_1PART1	QPATH_DC_OFFSET_1PART1								0x00	R/W
0x13A	IPATH_DC_OFFSET_2PART	RESERVED			IPATH_DC_OFFSET_2PART					0x00	R/W
0x13B	QPATH_DC_OFFSET_2PART	RESERVED			QPATH_DC_OFFSET_2PART					0x00	R/W
0x13C	IDAC_DIG_GAIN0	IDAC_DIG_GAIN0								0x00	R/W
0x13D	IDAC_DIG_GAIN1	RESERVED				IDAC_DIG_GAIN1				0x08	R/W
0x13E	QDAC_DIG_GAIN0	GAINCODEQ[7:0]								0x00	R/W
0x13F	QDAC_DIG_GAIN1	RESERVED				GAINCODEQ[11:8]				0x08	R/W
0x140	GAIN_RAMP_UP_STEP0	GAIN_RAMP_UP_STEP0								0x04	R/W
0x141	GAIN_RAMP_UP_STEP1	RESERVED				GAIN_RAMP_UP_STEP1				0x00	R/W
0x142	GAIN_RAMP_DOWN_STEP0	GAIN_RAMP_DOWN_STEP0								0x09	R/W
0x143	GAIN_RAMP_DOWN_STEP1	RESERVED				GAIN_RAMP_DOWN_STEP1				0x00	R/W
0x146	DEVICE_CONFIG_REG1	DEVICE_CONFIG1								0x00	R/W
0x147	BLSM_STAT	BE_ROTATE_REQ		RESERVED						0x00	R/W
0x14B	PRBS	PRBS_GOOD_Q	PRBS_GOOD_I	RESERVED			PRBS_MODE	PRBS_RESET	PRBS_EN	0x10	R/W
0x14C	PRBS_ERROR_I	PRBS_COUNT_I								0x00	R
0x14D	PRBS_ERROR_Q	PRBS_COUNT_Q								0x00	R
0x1B0	DACPLLT0	VCO_PD_IN	VCO_PD_PTAT	VCO_PD_ALC	SYNTH_PD	LDO_PD	RESERVED	LOGEN_PD	RESERVED	0xFA	R/W
0x1B1	DACPLLT1	RESERVED				PFD_DELAY		PFD_EDGE	RESERVED	0x04	R/W
0x1B2	DACPLLT2	EXT_ALC_WORD_EN	EXT_ALC_WORD							0x00	R/W
0x1B3	DACPLLT3	EXT_BAND1								0x00	W
0x1B4	DACPLLT4	BYP_LOAD_DELAY	VCO_CAL_OFFSET				RESERVED	EXT_BAND_EN	EXT_BAND2	0x78	R/W
0x1B5	DACPLLT5	INIT_ALC_VALUE				VCO_VAR				0x83	R/W
0x1B6	DACPLLT6	RESERVED	PORESETB_VCO	EXT_VCO_BITSEL		VCO_LVL_OUT				0x4A	R/W
0x1B7	DACPLLT7	LD_SYNTH	RESERVED	CP_IBLEED						0x00	R/W
0x1B8	DACPLLT8	RESERVED	COMP_OUT	CP_CAL_DONE	VCO_CAL_IN_PROG	CP_CALBITS				0x00	R
0x1B9	DACPLLT9	HALF_VCO_CAL_CLK	DITHER_MODE	MACHINE_ENABLE	CP_OFFSET_OFF	FORCE_CP_CALBITS	CAP_CAL_EN	CP_TEST		0x34	R/W
0X1BA	DACPLLTA	MACHINE_STATE				FCP_CALBITS				0x00	R/W
0x1BB	DACPLLTB	RESERVED			VCO_BIAS_TCF		VCO_BIAS_REF			0x0C	R/W
0x1BC	DACPLLTC	VCO_BYP_BIASR	RESERVED		VCO_COMP_BIASR	PRSC_HIGHR	LAST_ALC_EN	PRSC_BIAS_CTRL		0x00	R/W
0x1BD	DACPLLTD	RESERVED				VCO_CAL_REF_MON	VCO_CAL_REF_TCF			0x00	R/W
0x1BE	DACPLLTE	RESERVED				VCO_PDO_VR	VCO_PDO_VRTCF	VCO_PDO_CALTCF	VCO_PDO_VCOBUF	0x00	R/W
0x1BF	DACPLLTF	I_CAL_EN	I_ALC_WAIT_D			I_CAL_COUNT		FDBCK_DELAY		0x8D	R/W

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x1C0	DACPLLT10	RESERVED		USE_NEW_CAL	DOUBLE_F0_CAL_CNT	LOCKDETECT_COUNT		LOCK_MODE		0x2E	R/W
0x1C1	DACPLLT11	RESERVED	CP_LVL_DET_PD	CP_VL_LOW			CP_VL_HIGH			0x15	R/W
0x1C2	DACPLLT15	SDM_BP	SDM_PD	RESERVED		SDM_PROG				0x80	R/W
0x1C3	DACPLLT16	RESERVED	SDM_PROG3	SDM_PROG2	SDM_PROG1					0x00	R/W
0x1C4	DACPLLT17	RESERVED	VCO_VAR_REF_TCF			VCO_VAR_OFF				0x33	R/W
0x1C5	DACPLLT18	RESERVED				VCO_VAR_REF				0x08	R/W
0x200	MASTER_PD	RESERVED							SPI_PD_MASTER	0x01	R/W
0x201	PHY_PD	UNUSEDLANES								0x00	R/W
0x203	GENERIC_PD	RESERVED						SPI_SYNC1_PD	SPI_SYNC2_PD	0x00	R/W
0x206	CDR_RESET	RESERVED							SPI_CDR_RESETN	0x01	R/W
0x230	CDR_OPERATING_MODE_REG_0	RESERVED		HALFRATE	RESERVED			CDR_OVER-SAMP	RESERVED	0x28	R/W
0x268	EQ_BIAS_REG	EQ_POWER_MODE		RESERVED						0x62	R/W
0x280	SYNTH_ENABLE_CNTRL	RESERVED					SPI_RECAL_SYNTH	RESERVED	SPI_ENABLE_SYNTH	0x00	R/W
0x281	PLL_STATUS	RESERVED		SPI_CP_OVER_RANGE_HIGH_RB	SPI_CP_OVER_RANGE_LOW_RB	SPI_CP_CAL_VALID_RB	SPI_VCO_CAL_IN_PROGRESS_RB	SPI_CURRENTS_READY_RB	SPI_PLL_LOCK_RB	0x00	R
0x284	LOOP_FILTER_1	LOOP_FILTER_1								0x77	R/W
0x285	LOOP_FILTER_2	LOOP_FILTER_2								0x87	R/W
0x286	LOOP_FILTER_3	LOOP_FILTER_3								0x08	R/W
0x287	CP_CURRENT	RESERVED	SPI_SERDES_LOGEN_POWER_MODE	SPI_CP_CURRENT						0x3F	R/W
0x289	REF_CLK_DIVIDER_LDO	RESERVED				SPI_LDO_REF_SEL	SPI_LDO_BYPASS_FILT	SPI_CDR_OVERSAMP		0x04	R/W
0x28A	VCO_LDO	SPI_SERDES_LDO_CONFIG								0x2B	R/W
0x28B	PLL_PD_REG	RESERVED	SPI_VCO_PD	SPI_VCO_PD_PTAT	SPI_VCO_PD_ALC	SPI_SYN_PD	SPI_SERDES_LDO_PD	SPI_SERDES_LOGEN_PD_CORE		Ox7F	R/W
0x290	ALC_VARACTOR	SPI_INIT_ALC_VALUE				SPI_VCO_VARACTOR				0x83	R/W
0x291	VCO_OUTPUT	RESERVED				SPI_VCO_OUTPUT_LEVEL				0x49	R/W
0x294	CP_CONFIG	SPI_HALF_VCO_CAL_CLK	SPI_DITHER_MODE	SPI_ENABLE_MACHINE	SPI_CP_OFFSET_OFF	SPI_CP_FORCE_CALBITS	SPI_CP_CAL_EN	SPI_CP_TEST		0xB0	R/W
0x296	VCO_BIAS_1	RESERVED			SPI_VCO_BIAS_TCF		SPI_VCO_BIAS_REF			0x0C	R/W
0x297	VCO_BIAS_2	RESERVED		SPI_VCO_BYPASS_BIAS_DAC_R	SPI_VCO_COMP_BYPASS_BIASR	SPI_PRESCALE_BYPASS_R	SPI_LAST_ALC_EN	SPI_PRESCALE_BIAS		0x00	R/W
0x299	VCO_PD_OVERRIDES	RESERVED				SPI_VCO_PD_OVERRIDE_VAR_REF	SPI_VCO_PD_OVERRIDE_VAR_REF_TCF	SPI_VCO_PD_OVERRIDE_CAL_TCF	SPI_VCO_PD_OVERRIDE_VCOBUF	0x00	R/W
0x29A	VCO_CAL	SPI_VCO_CAL_EN	SPI_VCO_CAL_ALC_WAIT			SPI_VCO_CAL_COUNT		SPI_FB_CLOCK_ADV		0xFE	R/W
0x29C	CP_LEVEL_DETECT	RESERVED	SPI_CP_LEVEL_DET_PD	SPI_CP_LEVEL_THRESHOLD_LOW			SPI_CP_LEVEL_THRESHOLD_HIGH			0x17	R/W
0x29F	VCO_VARACTOR_CONTROL_0	RESERVED	SPI_VCO_VARACTOR_REF_TCF			SPI_VCO_VARACTOR_OFFSET				0x33	R/W
0x2A0	VCO_VARACTOR_CONTROL_1	RESERVED				SPI_VCO_VARACTOR_REF				0x08	R/W
0x2A7	TERM_BLK1_CTRLREG0	RESERVED							SPI_I_TUNE_R_CAL_TERMBLK1	0x00	R/W
0x2AE	TERM_BLK2_CTRLREG0	RESERVED							SPI_I_TUNE_R_CAL_TERMBLK2	0x00	R/W
0x300	GENERAL_JRX_CTRL_0	RESERVED	CHECKSUM_MODE	RESERVED		DUALLINK	CURRENT-LINK	ENLINKS		0x00	R/W
0x301	GENERAL_JRX_CTRL_1	RESERVED					SUBCLASSV_LOCAL			0x01	R/W

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x302	DYN_LINK_LATENCY_0	RESERVED			DYN_LINK_LATENCY_0					0x00	R/W
0x303	DYN_LINK_LATENCY_1	RESERVED			DYN_LINK_LATENCY_1					0x00	R/W
0x304	LMFC_DELAY_0	RESERVED			LMFCDEL0					0x00	R/W
0x305	LMFC_DELAY_1	RESERVED			LMFCDEL1					0x00	R/W
0x306	LMFCVAR0	RESERVED			LMFCVAR0					0x06	R/W
0x307	LMFCVAR1	RESERVED			LMFCVAR1					0x06	R/W
0x308	XBAR_LN_0_1	RESERVED		XBARVAL1			XBARVAL0			0x08	R/W
0x309	XBAR_LN_2_3	RESERVED		XBARVAL3			XBARVAL2			0x1A	R/W
0x30A	XBAR_LN_4_5	RESERVED		XBARVAL5			XBARVAL4			0x2C	R/W
0x30B	XBAR_LN_6_7	RESERVED		XBARVAL7			XBARVAL6			0x3E	R/W
0x30C	FIFO_STATUS_REG_0	LANE_FIFO_FULL								0x00	R
0x30D	FIFO_STATUS_REG_1	LANE_FIFO_EMPTY								0x00	R
0x312	SYNCB_GEN_1	RESERVED		SYNCB_ERR_DUR		RESERVED				0x00	R/W
0x314	SPI_SYNC_CTRL	RESERVED							SPI_SYNC_CLK_SEL	0x00	R/W
0x315	PHY_PRBS_TEST_EN	PHY_TEST_EN								0x00	R/W
0x316	PHY_PRBS_TEST_CTRL	RESERVED	PHY_SRC_ERR_CNT			PHY_PRBS_PAT_SEL		PHY_TEST_START	PHY_TEST_RESET	0x00	R/W
0x317	PHY_PRBS_TEST_THRESHOLD_LOBITS	PHY_PRBS_THRESHOLD_LOBITS								0x00	R/W
0x318	PHY_PRBS_TEST_THRESHOLD_MIDBITS	PHY_PRBS_THRESHOLD_MIDBITS								0x00	R/W
0x319	PHY_PRBS_TEST_THRESHOLD_HIBITS	PHY_PRBS_THRESHOLD_HIBITS								0x00	R/W
0x31A	PHY_PRBS_TEST_ERRCNT_LOBITS	PHY_PRBS_ERR_CNT_LOBITS								0x00	R
0x31B	PHY_PRBS_TEST_ERRCNT_MIDBITS	PHY_PRBS_ERR_CNT_MIDBITS								0x00	R
0x31C	PHY_PRBS_TEST_ERRCNT_HIBITS	PHY_PRBS_ERR_CNT_HIBITS								0x00	R
0x31D	PHY_PRBS_TEST_STATUS	PHY_PRBS_PASS								0xFF	R
0x32C	SHORT_TPL_TEST_0	RESERVED		SHORT_TPL_SP_SEL		SHORT_TPL_M_SEL		SHORT_TPL_TEST_RESET	SHORT_TPL_TEST_EN	0x00	R/W
0x32D	SHORT_TPL_TEST_1	SHORT_TPL_REF_SP_LSB								0x00	R/W
0x32E	SHORT_TPL_TEST_2	SHORT_TPL_REF_SP_MSB								0x00	R/W
0x32F	SHORT_TPL_TEST_3	RESERVED							SHORT_TPL_FAIL	0x00	R
0x333	DEVICE_CONFIG_REG2	RESERVED								0x00	R/W
0x334	JESD_BIT_INVERSE_CTRL	INVLANES								0x00	R/W
0x400	DID_REG	DID_RD								0x00	R
0x401	BID_REG	ADJCNT_RD				BID_RD				0x00	R
0x402	LID0_REG	RESERVED	ADJDIR_RD	PHADJ_RD	LID0_RD					0x00	R
0x403	SCR_L_REG	SCR_RD	RESERVED		L_RD					0x00	R
0x404	F_REG	F_RD								0x00	R
0x405	K_REG	RESERVED			K_RD					0x00	R
0x406	M_REG	M_RD								0x00	R
0x407	CS_N_REG	CS_RD		RESERVED	N_RD					0x00	R
0x408	NP_REG	SUBCLASSV_RD			NP_RD					0x00	R

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x409	S_REG	JESDV_RD			S_RD					0x00	R
0x40A	HD_CF_REG	HD_RD	RESERVED		CF_RD					0x00	R
0x40B	RES1_REG	RES1_RD								0x00	R
0x40C	RES2_REG	RES2_RD								0x00	R
0x40D	CHECKSUM_REG	LANE0CHECKSUM_RD								0x00	R
0x40E	COMPSUM0_REG	FCMP0_RD								0x00	R
0x412	LID1_REG	RESERVED			LID1_RD					0x00	R
0x415	CHECKSUM1_REG	FCHK1_RD								0x00	R
0x416	COMPSUM1_REG	FCMP1_RD								0x00	R
0x41A	LID2_REG	RESERVED			LID2_RD					0x00	R
0x41D	CHECKSUM2_REG	FCHK2_RD								0x00	R
0x41E	COMPSUM2_REG	FCMP2_RD								0x00	R
0x422	LID3_REG	RESERVED			LID3_RD					0x00	R
0x425	CHECKSUM3_REG	FCHK3_RD								0x00	R
0x426	COMPSUM3_REG	FCMP3_RD								0x00	R
0x42A	LID4_REG	RESERVED			LID4_RD					0x00	R
0x42D	CHECKSUM4_REG	FCHK4_RD								0x00	R
0x42E	COMPSUM4_REG	FCMP4_RD								0x00	R
0x432	LID5_REG	RESERVED			LID5_RD					0x00	R
0x435	CHECKSUM5_REG	FCHK5_RD								0x00	R
0x436	COMPSUM5_REG	FCMP5_RD								0x00	R
0x43A	LID6_REG	RESERVED			LID6_RD					0x00	R
0x43D	CHECKSUM6_REG	FCHK6_RD								0x00	R
0x43E	COMPSUM6_REG	FCMP6_RD								0x00	R
0x442	LID7_REG	RESERVED			LID7_RD					0x00	R
0x445	CHECKSUM7_REG	FCHK7_RD								0x00	R
0x446	COMPSUM7_REG	FCMP7_RD								0x00	R
0x450	ILS_DID	DID								0x00	R/W
0x451	ILS_BID	ADJCNT				BID				0x00	R/W
0x452	ILS_LID0	RESERVED	ADJDIR	PHADJ	LID0					0x00	R/W
0x453	ILS_SCR_L	SCR	RESERVED		L					0x83	R/W
0x454	ILS_F	F								0x00	R/W
0x455	ILS_K	RESERVED			K					0x1F	R/W
0x456	ILS_M	M								0x01	R
0x457	ILS_CS_N	CS		RESERVED	N					0x1F	R/W
0x458	ILS_NP	SUBCLASSV			NP					0x2F	R/W
0x459	ILS_S	JESDVER			S					0x20	R/W
0x45A	ILS_HD_CF	HD	RESERVED		CF					0x80	R/W
0x45D	ILS_CHECKSUM	LANE0CHECKSUM								0x45	R/W
0x46B	ERRCNTRMON	ERRCNTRMON								0x00	R/W
0x46C	LANEDESKEW	LANEDESKEW								0x0F	R/W
0x46D	BADDISPARITY	BADDISPARITY								0x00	R/W
0x46E	NITDISPARITY	NITDISPARITY								0x00	R/W
0x46F	UNEXPECTEDK-CHAR	UEKC								0x00	R/W
0x470	CODEGRPSYNC-FLG	CODEGRPSYNC								0x00	R/W
0x471	FRAMESYNCFLG	FRAMESYNC								0x00	R/W

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x472	GOODCHKSUM-FLG	GOODCHECKSUM								0x00	R/W
0x473	INITLANESYNC-FLG	INITIALLANESYNC								0x00	R/W
0x476	CTRLREG1	F_AGAIN								0x01	R/W
0x477	CTRLREG2	ILAS_MODE	RESERVED			THRESHOLD_ MASK_EN	RESERVED			0x00	R/W
0x478	KVAL	KSYNC								0x01	R/W
0x47A	IRQVECTOR	BADDIS_ MASK	NITD_MASK	UEKC_MASK	RESERVED	INITIALLANE-SYNC_MASK	BADCHECK-SUM_MASK	RESERVED	CODEGRP SYNC_ MASK	0x00	R/W
0x47B	SYNCASSERTION-MASK	BADDIS_S	NIT_S	UCC_S	CMM	CMM_ENABLE	RESERVED			0x08	R/W
0x47C	ERRORTHRES	ETH								0xFF	R/W
0x47D	LANEENABLE	LANE_ENA								0x0F	R/W
0x47E	RAMP_ENA	RESERVED							ENA_ RAMP_ CHECK	0x00	R/W
0x520	DIG_TEST0	RESERVED						DC_TEST_ MOD	RESERVED	0x1C	R/W
0x521	TEST_DC_ VALUEI0	TEST_DC_VALUEI0								0x00	R/W
0x522	TEST_DC_ VALUEI1	TEST_DC_VALUEI1								0x00	R/W
0x523	TEST_DC_ VALUEQ0	TEST_DC_VALUEQ0								0x00	R/W
0x524	TEST_DC_ VALUEQ1	TEST_DC_VALUEQ1								0x00	R/W

REGISTER DETAILS

Table 93. AD9154 Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x000	SPI_INTFCONFA	7	SOFTRESET_M		Soft Reset (Mirror).	0x0	R
		6	LSBFIRST_M		LSB First (Mirror).	0x0	R
		5	ADDRINC_M		Address Increment (Mirror).	0x0	R
		4	SDOACTIVE_M		SDO Active (Mirror).	0x0	R
		3	SDOACTIVE		SDO Active.	0x0	R/W
		2	ADDRINC		Address Increment. When set, causes incrementing streaming addresses; otherwise, descending addresses are generated.	0x0	R/W
				1	Streaming addresses are incremented.		
				0	Streaming addresses are decremented.		
		1	LSBFIRST		LSB First. When set, causes input and output data to be oriented LSB first. If this bit is clear, data is oriented MSB first.	0x0	R/W
				1	Shift LSB in first.		
				0	Shift MSB in first.		
		0	SOFTRESET		Soft Reset. Setting this bit initiates a reset. This bit is autoclearing after the soft reset is complete.	0x0	R/W
				1	Pulse the soft reset line.		
				0	Release soft reset.		
0x003	SPI_CHIPTYPE	[7:0]	CHIPTYPE		High Speed DAC.	0x4	R
0x004	SPI_PRODIDL	[7:0]	PRODIDL		Product ID Low.	0x54	R
0x005	SPI_PRODIDH	[7:0]	PRODIDH		Product ID High.	0x91	R
0x006	SPI_CHIP-GRADE	[7:4]	PROD_GRADE		Product Grade.	0x8	R
		[3:0]	DEV_REVISION		Device Revision.	0x9	R
0x008	DUAL_PAGE	[7:2]	RESERVED		Reserved.	0x0	R
		[1:0]	PAGEINDX		Page or Index Pointer.	0x3	R/W
				1	Select Link A.		
				2	Select Link B.		
				3	Select Link A and Link B.		
0x011	PWRCNTRL0	7	PD_BG		Reference Power-Down.	0x1	R/W
				0	Reference on.		
				1	Reference powered down. Overrides TXENx masked bit.		
		6	PDDAC0		PD I Channel DAC 0.	0x1	R/W
				0	Enable DAC0 I channel Dual0.		
				1	Power down DAC0 I channel Dual0. Overrides TXENx masked bit.		
		5	PDDAC1		PD Q Channel DAC 1.	0x1	R/W
				0	Enable Q channel DAC of Dual A.		
				1	Power Down Q channel DAC of Dual A. Overrides TXENx masked bit.		
		4	PDDAC2		PD I Channel DAC 2.	0x1	R/W
				0	Enable I channel DAC of Dual B.		
				1	Power Down I channel DAC of Dual B. Overrides TXENx masked bit.		
		3	PDDAC3		PD Q Channel DAC 3.	0x1	R/W
				0	Enable Q channel DAC of Dual B.		
				1	Powers down Q channel DAC of Dual B. Overrides TXENx masked bit.		
		[2:0]	RESERVED		Reserved.	0x0	R

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x012	TXENMASK1	7	DACB_MASK		Dual 23 DAC Power-Down Mask for TXEN1.	0x0	R/W
				0	Default power-down to control by power-down bit only.		
				1	If TXEN1 is low, DAC 2 and DAC 3 are powered down; otherwise state of individual power-downs.		
		6	DACA_MASK		Dual 01 DAC power-down mask for TXEN0.	0x0	R/W
				0	Default power-down to control by power-down bit only.		
				1	If TXEN0 is low, DAC 0 and DAC 1 are powered down; otherwise state of individual power-downs.		
		[5:0]	RESERVED		Reserved	0x0	R/W
0x013	PWRCNTRL3	7	RESERVED		Reserved.	0x0	R
		6	ENA_PA_CTRL_ FROM_PAPROT_ ERR		Control PA enable from PAProt block.	0x0	R/W
		5	ENA_PA_CTRL_ FROM_TXENSM		Control PA enable from TXEN state machine.	0x1	R/W
		4	ENA_PA_CTRL_ FROM_BLSM		Control PA enable from blanking state machine.	0x0	R/W
		3	ENA_PA_CTRL_ FROM_SPI		Control PA enable via SPI.	0x0	R/W
		2	SPI_PA_CTRL		PA on/off via SPI.	0x0	R/W
		1	ENA_SPI_TXEN		TXENx from SPI control.	0x0	R/W
		0	SPI_TXEN		SPI TXENx.	0x0	R/W
				1	TXENx SPI is high.		
				0	TXENx SPI is low.		
0x014	COARSE_ GROUP_DLY	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	COARSE_ GROUP_DLY		Coarse Group Delay. The range of the delay is −4 to +3 DAC clock periods and the resolution is 1/2 DAC clock period.	0x8	R/W
				0	minimum delay.		
				15	maximum delay.		
0x01F	IRQ_ENABLE0	[7:6]	RESERVED		Reserved.	0x0	R/W
		5	EN_DACPLLLOST		Enable DAC PLL Lost Detection. The DACPLLLOCK, when enabled, shows that the DAC (clock generation) PLL has dropped its lock state.	0x0	R/W
				1	Enable DAC PLL lost.		
		4	EN_DACPLLLOCK		Enable DAC PLL Lock Detection. The DACPLLLOCK, when enabled, shows that the DAC (clock generation) PLL has reached a lock state.	0x0	R/W
				1	Enable DAC PLL lock.		
		3	EN_SERPLLLOST		Enable SERDES PLL Lost Detection. The SERPLLLOCK, when enabled, shows that the SERDES (JESD204B interface) PLL has dropped its lock state.	0x0	R/W
				1	Enable SERDES PLL lost.		
		2	EN_SERPLLLOCK		Enable SERDES PLL Lock Detection. The SERPLLLOCK, when enabled, shows that the SERDES (JESD204B interface) PLL has reached a lock state.	0x0	R/W
				1	Enable SERDES PLL lock.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		1	EN_LANEFIFOERR		Enable Lane FIFO Error Detection. A lane FIFO error occurs when there is a full or empty condition on any of the FIFOs between the deserializer block and the core digital. An error on this FIFO requires a link disable and re-enable to remove. The STATUS of the Lane FIFOs can be found in Register 0x30C (FIFO full) and Register 0x30D (FIFO empty).	0x0	R/W
				1	Enable lane FIFO error.		
		0	RESERVED		Reserved	0x0	R/W
0x020	IRQ_ENABLE1	[7:4]	RESERVED		Reserved.	0x0	R
		3	EN_PRBSQ1		Enable PRBS Imaginary DAC Dual B interrupt.	0x0	R/W
				1	Enable PRBS Q1.		
		2	EN_PRBSI1		Enable PRBS real DAC Dual B interrupt.	0x0	R/W
				1	Enable PRBS I1.		
		1	EN_PRBSQ0		Enable PRBS Imaginary DAC Dual A interrupt.	0x0	R/W
				1	Enable PRBS Q0.		
		0	EN_PRBSI0		Enable PRBS real DAC Dual A interrupt.	0x0	R/W
				1	Enable PRBS I0.		
0x021	IRQ_ENABLE2	7	EN_PAERR0		Link A PA Error.	0x0	R/W
				1	Enable PA Error.		
		6	RESERVED		Reserved.	0x0	R/W
		5	EN_BLNKDONE0		Link A Blanking Done.	0x0	R/W
				1	Enable Link A blanking done.		
		4	EN_REFNCOCLR0		Link A NCO Clear Tripped.	0x0	R/W
				1	NCO clear tripped.		
		3	EN_REFLOCK0		Link A Alignment Locked.	0x0	R/W
				1	Enable ref locked interrupt.		
		2	EN_REFROTA0		Link A Alignment Rotate.	0x0	R/W
				1	Enable ref rotate interrupt.		
		1	EN_REFWLIM0		Link A Over/Under Threshold.	0x0	R/W
				1	Enable over/under limit interrupt.		
		0	EN_REFTRIP0		Link A Alignment Trip.	0x0	R/W
				1	Enable ref tripped interrupt.		
0x022	IRQ_ENABLE3	7	EN_PAERR1		Link B PA Error.	0x0	R/W
				1	Enable PA error.		
		6	RESERVED		Reserved.	0x0	R/W
		5	EN_BLNKDONE1		Link B Blanking Done.	0x0	R/W
				1	Enable Link B blanking done.		
		4	EN_REFNCOCLR1		Link B NCO Clear Tripped.	0x0	R/W
				1	NCO clear tripped.		
		3	EN_REFLOCK1		Link B Alignment Locked.	0x0	R/W
				1	Enable ref locked interrupt.		
		2	EN_REFROTA1		Link B Alignment Rotate.	0x0	R/W
				1	Enable ref rotate interrupt.		
		1	EN_REFWLIM1		Link B Over/Under Threshold.	0x0	R/W
				1	Enable over/under limit interrupt.		
		0	EN_REFTRIP1		Link B Alignment Trip.	0x0	R/W
				1	Enable ref tripped interrupt.		
0x023	IRQ_STATUS0	[7:6]	RESERVED		Reserved.	0x0	R
		5	IRQ_DACPLLLOST		DAC PLL Lost.	0x0	R
				1	DAC PLL lost.		
		4	IRQ_DACPLLLOCK		DAC PLL Lock.	0x0	R
				1	DAC PLL lock.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		3	IRQ_SERPLLLOST		SERDES PLL Lost.	0x0	R
				1	SERDES PLL lost.		
		2	IRQ_SERPLLLOCK		SERDES PLL Lock.	0x0	R
				1	SERDES PLL lock.		
		1	IRQ_LANEFIFOERR		Lane FIFO Error.	0x0	R
				1	Lane FIFO error.		
		0	RESERVED		Reserved	0x0	R
0x024	IRQ_STATUS1	[7:4]	RESERVED		Reserved.	0x0	R
		3	IRQ_PRBSQ1		PRBS Data Check Error DAC B Imaginary.	0x0	R
				1	Service PRBS Q1.		
		2	IRQ_PRBSI1		PRBS Data Check Error DAC B Real.	0x0	R
				1	Service PRBS I1.		
		1	IRQ_PRBSQ0		PRBS Data Check Error DAC A Imaginary.	0x0	R
				1	Service PRBS Q0.		
		0	IRQ_PRBSI0		PRBS Data Check Error DAC A Real.	0x0	R
				1	Service PRBS I0.		
0x025	IRQ_STATUS2	7	IRQ_PAERR0		Link A PA Error.	0x0	R
				1	Service Link A PA error.		
		6	RESERVED		Reserved.	0x0	R
		5	IRQ_BLNKDONE0		Link A Blanking Done.	0x0	R
				1	Link A blank done.		
		4	IRQ_REFNCOCLR0		Link A Alignment Underrange.	0x0	R
				1	NCO clear tripped.		
		3	IRQ_REFLOCK0		Link A BIST Done.	0x0	R
				1	Link A alignment locked.		
		2	IRQ_REFROTA0		Link A Alignment Trip.	0x0	R
				1	Rotate interrupt occurred.		
		1	IRQ_REFWLIM0		Link A Alignment Lock.	0x0	R
				1	Service over/under limit interrupt.		
		0	IRQ_REFTRIP0		Link A Alignment Rotate.	0x0	R
				1	Trip interrupt occurred.		
0x026	IRQ_STATUS3	7	IRQ_PAERR1		Link B PA Error.	0x0	R
				1	Service Link B PA error.		
		6	RESERVED		Reserved.	0x0	R
		5	IRQ_BLNKDONE1		Reserved	0x0	R
		4	IRQ_REFNCOCLR1		Link B Alignment Underrange.	0x0	R
				1	NCO clear tripped.		
		3	IRQ_REFLOCK1		Link B BIST Done.	0x0	R
				1	Link B alignment locked.		
		2	IRQ_REFROTA1		Link B Alignment Trip.	0x0	R
				1	Rotate interrupt occurred.		
		1	IRQ_REFWLIM1		Link B Alignment Lock.	0x0	R
				1	Service over/under limit interrupt.		
		0	IRQ_REFTRIP1		Link B Alignment Rotate.	0x0	R
				1	Ref trip.		
0x030	JESD_CHECKS	[7:6]	RESERVED		Reserved.	0x0	R
		5	ERR_DLYOVER		LMFC_Delay > JESD_K Parameter.	0x0	R
				1	LMFC_Delay > JESD_K.		
		4	ERR_WINLIMIT		Unsupported Window Limit.	0x0	R
				1	Unsupported window limit.		
		3	ERR_JESDBAD		Unsupported M/L/S/F Selection.	0x0	R
				1	This JESD combination is not supported.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		2	ERR_KUNSUPP		Unsupported K Values.	0x0	R
				1	K value unsupported.		
		1	ERR_SUBCLASS		Unsupported SUBCLASSV Value.	0x0	R
				1	Unsupported subclass value.		
		0	ERR_INTSUPP		Unsupported Interpolation Factor.	0x0	R
				1	Error with interpolation value.		
0x034	SYNC_ ERRWINDOW	[7:3]	RESERVED		Reserved.	0x0	R
		[2:0]	ERRWINDOW		Sync Error Window. Synchronization rotates the clock based on a difference in the sample of the current phase of the internal clocks and the programmed target based on the SYSREF± sample time. If SYSREF± cannot be guaranteed to always exist in the same period of the device clock associated with the target phase from SYSREF± to SYSREF± (ERRWINDOW = 0), then the user may choose to apply an error window to synchronization. The error window allows the SYSREF± sample phase to vary within the confines of the window without triggering a clock adjustment.	0x0	R/W
				0	Error window tolerance ±1/2.		
				1	Error window tolerance ±1.		
				2	Error window tolerance ±2.		
				3	Error window tolerance ±3.		
				4	Error window tolerance ±4.		
				5	Error window tolerance ±5.		
				6	Error window tolerance ±6.		
				7	Error window tolerance ±7.		
0x038	SYNC_ LASTERR_L	[7:0]	LASTERROR_L		Sync Last Error[7:0]. The value of SYNC_LASTERR_L and SYNC_LASTERR_H[0] for the readback SYNC_LASTERR. SYNC_LASTERR is a measure of the error between the SYSREF sample phase and the target value that caused the last clock adjustment. This value is sticky and does not update until a clock adjustment occurs. Clear this value using the SYNCCLRLAST bit. The value is in DAC clocks.	0x0	R
0x039	SYNC_ LASTERR_H	7	LASTUNDER		Sync Last Error Under Flag. This bit shows that the phase error between the SYSREF sample point and the target is below the error window limit.	0x0	R
				1	Current phase error over window tolerance.		
		6	LASTOVER		Sync Last Error Over Flag. This bit shows that the phase error between the SYSREF sample point and the target is above the error window limit.	0x0	R
				1	Last phase error under window tolerance.		
		[5:1]	RESERVED		Reserved.	0x0	R
		0	LASTERROR_H		Sync Last Error, Bit 8, and Flags.	0x0	R
0x03A	SYNC_ CONTROL	7	SYNCENABLE		Sync Logic Enable.	0x0	R/W
				1	Enable sync logic.		
				0	Disable sync logic.		
		6	SYNCARM		Sync Arming Strobe.	0x0	R/W
				1	Sync one-shot arming.		
		5	SYNCCLRSTKY		Sync Sticky Bit Clear.	0x0	R/W
				1	Clear sticky status bits REFROTA and REFTRIP.		
		4	SYNCCLRLAST		Sync Clear LAST.	0x0	R/W
				1	Clear the LAST errors.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[3:0]	SYNCMODE		Sync Mode.	0x0	R/W
				0	Reserved.		
				1	Sync one-shot mode.		
				2	Sync continuous mode.		
				5	Reserved.		
				6	Reserved.		
				8	Sync monitor only mode.		
				A	Sync one-shot then monitor.		
				9	Sync one-shot then monitor.		
				D	Reserved..		
				E	Reserved		
0x03B	SYNC_STATUS	7	REFBUSY		Sync Machine Busy.	0x0	R
				1	Sync logic SM is busy.		
		[6:4]	RESERVED		Reserved.	0x0	R
		3	REFLOCK		Sync Alignment Locked.	0x0	R
				1	Sync logic aligned within window.		
		2	REFROTA		Sync Rotated.	0x0	R
				1	Sync logic rotated with SYSREF± (sticky).		
		1	REFWLIM		Sync Alignment Limit Range.	0x0	R
				1	Phase error outside of specified window error threshold.		
		0	REFTRIP		Sync Tripped After Arming.	0x0	R
				1	Sync received SYSREF pulse (sticky).		
0x03C	SYNC_ CURRERR_L	[7:0]	CURRERROR_L		Sync Alignment Error. This register gives the user real time access of the SYSREF± to the internal clock counters. The value of SYNC_CURRERR = (SYNC_CURRERR_H[0],SYNC_CURRERR_L) is the difference between the SYSREF± position relative to the clock divider and the target position relative to the internal counter. This register monitors the phase of the internal clocks in monitor modes of operation. If an adjustment of the clocks is made on any given SYSREF±, the value of the phase error is placed into SYNC_LASTERR and SYNC_CURRERR is forced to 0.	0x0	R
0x03D	SYNC_ CURRERR_H	7	CURRUNDER		Sync Current Error Under Flag.	0x0	R
				1	Current phase error under window tolerance.		
		6	CURROVER		Sync Current Error Over Flag.	0x0	R
				1	Current phase error over window tolerance.		
		[5:1]	RESERVED		Reserved.	0x0	R
		0	CURRERROR_H		Sync Current Error[8].	0x0	R
0x040	DAC_GAIN0_I	[7:2]	RESERVED		Reserved.	0x0	R
		[1:0]	DAC_GAIN_I1		I DAC Current Scaling MSBs	0x3	R/W
0x041	DAC_GAIN1_I	[7:0]	DAC_GAIN_I0		I DAC Current Scaling LSBs.	0xFF	R/W
0x042	DAC_GAIN0_Q	[7:2]	RESERVED		Reserved.	0x0	R
		[1:0]	DAC_GAIN_Q1		Q DAC Current Scaling MSBs.	0x3	R/W
0x043	DAC_GAIN1_Q	[7:0]	DAC_GAIN_Q0		Q DAC current scaling LSBs.	0xFF	R/W
0x044	GROUPDELAY COMP_I	[7:0]	GROUP DELAY COMP I [7:0]		Group Delay Compensation Bits for I Channel. These bits set the group delay compensation for the I channel DAC.	0x0	R/W
0x045	GROUPDELAY COMP_Q	[7:0]	GROUP DELAY COMP Q [7:0]		Group Delay Compensation Bits for Q Channel. These bits set the group delay compensation for the Q channel DAC.	0x0	R/W
0x046	GROUPDELAY COMP_BYP	[7:2]	RESERVED		Reserved.	0x0	R

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		1	GROUPCOMP_ BYPI		Bypass the Q Channel Group Delay Compensation Circuitry.	0x1	R/W
		0	GROUPCOMP_ BYPQ		Bypass the I Channel Group Delay Compensation Circuitry.	0x1	R/W
0x04A	MIX_MODE	[7:1]	RESERVED		Reserved.	0x0	R
		0	MIX_MODE		Mix Mode Enable.	0x0	R/W
				0	Mix mode off.		
				1	Mix mode on.		
0x050	NCO_ CLRMODE	7	NCOCLRARM		Arm NCO Clear. Arms NCO clearing operation.	0x0	R/W
				1	Arm NCO clear logic.		
		6	RESERVED		Reserved.	0x0	R
		5	NCOCLRMTCH		NCO Clear Data Match.	0x0	R
				1	Key NCO clear data match.		
		4	NCOCLRPASS		NCO Clear Passed.	0x0	R
				1	NCO clear took effect.		
		3	NCOCLRFAIL		NCO Clear Failed.	0x0	R
				1	NCO reset during rotate.		
		2	RESERVED		Reserved.	0x0	R
		[1:0]	NCOCLRMODE		NCO Clear Mode.	0x0	R/W
				0	NCO clearing disabled.		
				2	NCO clear on data key.		
				1	NCO clear on SYSREF.		
0x051	NCOKEY_ILSB	[7:0]	NCOKEYILSB		NCO DataKey for I Channel LSB.	0x0	R/W
0x052	NCOKEY_IMSB	[7:0]	NCOKEYIMSB		NCO DataKey for I Channel MSB.	0x0	R/W
0x053	NCOKEY_QLSB	[7:0]	NCOKEYQLSB		NCO DataKey for Q Channel LSB.	0x0	R/W
0x054	NCOKEY_ QMSB	[7:0]	NCOKEYQMSB		NCO DataKey for Q Channel MSB.	0x0	R/W
0x060	PA_THRES0	[7:0]	PDP_THRESHOLD [7:0]		Average Power Threshold for Comparison.	0x0	R/W
0x061	PA_THRES1	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	PA_THRESHOLD_ MSB		Average Power Threshold for Comparison.	0x0	R/W
0x062	PDP_AVG_TIME	7	PDP_ENABLE	1	Enable Average Power Calculation and Error Detection	0x0	R/W
		6	PA_BUS_SWAP		Swap Channel A or Channel B Data Bus for Power Calculation.	0x0	R/W
		[5:4]	RESERVED		Reserved.	0x0	R
		[3:0]	PDP_AVG_TIME		Set Power Average Time.	0x0	R/W
0x063	PA_POWER0	[7:0]	PDP_POWER[7:0]		Average Power Bus = $I^2 + Q^2$ (I/Q Use 6 MSBs of Data Bus).	0x0	R
0x064	PA_POWER1	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	PDP_POWER[12:8]		Average Power Bus = $I^2 + Q^2$ (I/Q Use 6 MSBs of Data Bus).	0x0	R
0x080	CLKCFG0	7	PD_CLK01		Power-Down Clock for Dual A.	0x1	R/W
				0	Enable clock divider in Dual A.		
				1	Disable clock divider in Dual A.		
		6	PD_CLK23		Power-Down Clock for Dual B.	0x1	R/W
				0	Enable clock divider in Dual B.		
				1	Power-down clock divider in Dual B.		
		5	PDCLOCKDIG		Power-Down Clocks to All DACs.	0x1	R/W
				0	Enable clock for all DACs.		
				1	Power-down clock for all DACs.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		4	PD_PCLK		Power-Down Calibration Reference/SERDES PLL Clock.	0x1	R/W
				0	Enable clock to SERDES PLL/calibration logic.		
				1	Disable clock to SERDES PLL/calibration logic.		
		3	PDCLOCKREC		Power-Down Clock Receiver.	0x1	R/W
				0	Enable clock receiver analog buffer.		
				1	Power-down clock receiver analog buffer.		
		2	DUTY_EN		Enable Duty Cycle Control of Clock Receiver, Always = 1.	0x1	R/W
		1	RF_SYNC_EN		Enable SYSREF± timing for RF clock chain.	0x1	R/W
		0	RF_CLKDIV_EN		Enable RF Clock Divider. The RF clock divider divides the input clock by 2 and provides the result to the DAC for sampling.	0x0	R/W
				0	RF clock divider disabled.		
				1	RF clock divider enabled.		
0x081	SYSREF_ ACTRL0	[7:5]	RESERVED		Reserved.	0x0	R
		4	PDSYSREF		Power Down SYSREF± Buffer. This bit powers down the SYSREF± receiver. For Subclass 1 operation to work, this buffer must be enabled.	0x1	R/W
		3	HYS_ON		Hysteresis On. This bit enables the programmable hysteresis control for the SYSREF± receiver.	0x0	R/W
				0	Disable hysteresis in SYSREF± receiver.		
				1	Enable hysteresis in SYSREF± receiver.		
		2	SYSREF_RISE		Use SYSREF± Rising Edge.	0x0	R/W
				0	Use SYSREF± falling edge for alignment.		
				1	Use SYSREF± rising edge for alignment.		
		[1:0]	HYS_CNTRL1		MSBs of Hysteresis Control. Hysteresis control bits are control bits for the amount of hysteresis in the SYSREF± receiver. Each of the ten bits adds 10 mV of differential hysteresis to the receiver input. Two of the 10 bits are contained here. The other 8 bits are in HYS_CNTRL0.	0x0	R/W
0x082	SYSREF_ ACTRL1	[7:0]	HYS_CNTRL0		Low Bits of Hysteresis Control. Hysteresis control bits are control bits for the amount of hysteresis in the SYSREF± receiver. Each of the ten bits adds 10 mV of differential hysteresis to the receiver input. Eight of the 10 bits are contained here. The other 2 bits are in HYS_CNTRL1.	0x0	R/W
0x083	DACPLLCNTRL	7	SYNTH_RECAL		Recalibrate VCO Band. Set this bit to reinitialize the calibration of the VCO band in the DAC PLL. This bit does not power cycle the DAC PLL, nor does it recalibrate the charge pump. Set this bit after changing any setting associated with the PLL. Do not set this bit until after an initial PLL lock is achieved.	0x0	R/W
		[6:5]	RESERVED		Reserved.	0x0	R

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		4	ENABLE_SYNTH		Synthesizer Enable. The bit initiates the start-up sequence of the DAC PLL. The start-up sequence is as follows: 1. Enable the bias currents. 2. Enable DAC LDO. 3. Wait for LDO to settle. 4. Calibrate DAC PLL charge pump (The DAC charge pump will only calibrate upon the first setting of ENABLE_SYNTH). 5. Calibrate the band of the PLL. 6. Settle and lock.	0x0	R/W
				0	Disable synthesizer including all currents and calibration codes.		
				1	Power up synthesizer and initiate calibration sequence.		
		[3:0]	RESERVED		Reserved.	0x0	R
0x084	DACPLL-STATUS	7	CP_ OVERRANGE_H		Charge Pump High Overrange. This bit indicates that the charge pump voltage is too high and a recalibration must be applied.	0x0	R
				0	Control voltage not too high.		
				1	Control voltage too high.		
		6	CP_ OVERRANGE_L		Charge Pump Low Overrange. This bit indicates that the charge pump voltage is too low and a recalibration must be applied.	0x0	R
				0	Control voltage not too low.		
				1	Control VOLTAGE too low.		
		5	CP_CAL_VALID		Charge Pump Calibration Valid. This bit indicates that the charge pump has been successfully calibrated. The selection as to whether the charge pump needs to be calibrated upon startup can be found in Register 0x1B9.	0x0	R
				0	If CP_CAL_EN low, this stays low.		
				1	If CP_CAL_EN high (def), this happens when charge pump is calibrated.		
		4	VCO_CAL_ PROGRESS		VCO Calibration in Progress. This bit is high if the VCO calibration is currently occurring. If this bit is high for more than 1 sec there is something wrong with the VCO calibration.	0x0	R
				0	VCO not calibrating.		
				1	VCO calibrating.		
		[3:2]	RESERVED		Reserved.	0x0	R
		1	RFPLL_LOCK		PLL Lock bit. This bit is set high by the PLL once the PLL has achieved lock for the count set by LOCK_MODE bits in Register 0x1C0.	0x0	R
				1	PLL locked.		
				0	PLL unlocked.		
		0	RESERVED		Reserved.	0x0	R
0x085	DACINTEGER WORD0	[7:0]	BCOUNT		Bits[7:0] of the Integer Tuning Word. This bit controls the integer feedback divider for the DAC PLL. The frequency of the DAC clock can be determined by the following equations: $f_{DAC} = f_{REF}/(REFDIVMODE) \times 2 \times BCount$ $f_{VCO} = f_{REF}/(REFDIVMODE) \times 2 \times BCount \times LODivMode$ The minimum value is 6.	0x6	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x087	DACLOOPFILT1	[7:4]	LF_C2_WORD		C2 Control Word.	0x8	R/W
		[3:0]	LF_C1_WORD		C1 Control Word.	0x8	R/W
0x088	DACLOOPFILT2	[7:4]	LF_R1_WORD		R1 Control Word.	0x8	R/W
		[3:0]	LF_C3_WORD		C3 control Word.	0x8	R/W
0x089	DACLOOPFILT3	7	LF_BYPASS_R3		Bypass R3 Resistor.	0x0	R/W
				0	Enable R3 resistor programming start at 0.		
				1	Disable R3 resistor is LF_R3_WORD = 0.		
		6	LF_BYPASS_R1		Bypass R1 Resistor.	0x0	R/W
				0	Enable R1 resistor programming at 0.		
				1	Disable R1 if LF_R1_WORD = 0.		
		5	LF_BYPASS_C2		Bypass C2 Capacitor.	0x0	R/W
				0	Enable C2 capacitor programming at 0.		
				1	Disable C2 capacitor is LF_C2_WORD = 0.		
		4	LF_BYPASS_C1		Bypass C1 Capacitor.	0x0	R/W
				0	Enable C1 capacitor programming at 0.		
				1	Disable C1 capacitor if LF_C1_WORD = 0.		
		[3:0]	LF_R3_WORD		R3 Control Word.	0x8	R/W
0x08A	DACCPCNTRL	7	RESERVED		Reserved.	0x0	R
		6	VT_FORCE		VT Control Out.	0x0	R/W
				0	Control voltage not brought out for test.		
				1	Control voltage brought out for test.		
		[5:0]	CP_CURRENT		Charge Pump Current Control.	0x20	R/W
0x08B	DACLOGEN CNTRL	[7:6]	RESERVED		Reserved.	0x0	R
		[5:4]	LO_POWER_ MODE		Local Oscillator Generator (Logen) Power Mode.	0x0	R/W
				0	Full power—VCO, 8 GHz to 12 GHz.		
				1	Half power—VCO, 6 GHz to 8 GHz.		
				3	Off.		
		[3:2]	RESERVED		Reserved.	0x0	R
		[1:0]	LODIVMODE		Logen Division.	0x0	R/W
				0	Reserved.		
				1	Divide by 4—VCO to DAC clock.		
				2	Divide by 8—VCO to DAC clock.		
				3	Divide by 16—VCO to DAC clock.		
0x08C	DAC-LDOCNTRL1	7	LDO_REF_SEL		Reference Selection Bit.	0x0	R/W
				0	Generate reference from BG.		
				1	Generate reference from supply.		
		6	LDO_BYPASS_ FILT		Disable LDO Voltage Filter.	0x0	R/W
				0	Enable voltage filter to LDO input.		
				1	Disable voltage filter to LDO input.		
		[5:3]	RESERVED		Reserved.	0x0	R
		[2:0]	REFDIVMODE		Reference Clock Division Ratio.	0x0	R/W
				0	1×.		
				1	2×.		
				2	4×.		
				3	8×.		
				4	16×.		
				5	32×.		
				6	16×.		
				7	32×.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x08D	DAC-LDOCNTRL2	7	LDO_BYPASS		Bypass LDO Function.	0x0	R/W
				0	LDO operates normally.		
				1	LDO output shorted to VDD.		
		[6:5]	LDO_INRUSH		LDO Startup Speed Control.	0x1	R/W
		[4:2]	LDO_SEL		LDO Voltage and Power Setup.	0x2	R/W
				0	1.08 V low power.		
				1	1.08 V mid power.		
				2	1.08 V high power.		
				3	Not used.		
				4	1.02 V low power.		
				5	1.02 V mid power.		
				6	1.02 V high power.		
				7	Not used.		
		[1:0]	LDO_VDROP		LDO Passgate Control.	0x3	R/W
				0	One passgate used.		
				1	Two passgates used.		
				2	Three passgates used.		
				3	Four passgates used.		
0x110	DATA_FORMAT	7	BINARY_FMT		Binary or Twos Complementary Format on DATA Bus.	0x0	R/W
				0	Input data is twos compliment.		
				1	Input data is offset binary.		
		[6:0]	RESERVED		Reserved.	0x0	R
0x111	DATAPATH_CTRL	7	INVSINC_ENABLE	1	Enable Inverse Sinc Filter.	0x1	R/W
		6	RESERVED		Reserved.	0x0	R
		5	DIG_GAIN_ENABLE	1	Enable Digital Gain.	0x1	R/W
		4	PHASE_ADJ_ENABLE	1	Enable Phase Compensation.	0x0	R/W
		[3:2]	MODULATION_TYPE		Selects Type of Modulation Operation.	0x0	R/W
				0	No modulation.		
				1	Fine modulation (uses FTW).		
				2	$f_S/4$ modulation.		
				3	$f_S/8$ modulation.		
		1	SEL_SIDEBAND	1	Select Upper or Lower Sideband from Modulation Result.	0x0	R/W
		0	I_TO_Q	1	Send I Datapath into Q DAC.	0x0	R/W
0x112	INTERPMODE	[7:3]	RESERVED		Reserved.	0x0	R
		[2:0]	INTERPMODE		Interpolation Mode.	0x1	R/W
				0	1x (bypass).		
				1	2x mode.		
				3	4x mode.		
				4	8x mode.		
0x113	NCO_FTW_UPDATE	[7:2]	RESERVED		Reserved.	0x0	R
		1	FTW_UPDATE_ACK		Frequency Tuning Word Update Acknowledge.	0x0	R
		0	FTW_UPDATE_REQ		Frequency Tuning Word Update Request from SPI.	0x0	R/W
0x114	FTW0	[7:0]	FTW0		NCO Frequency Tuning Word, FTW[7:0].	0x0	R/W
0x115	FTW1	[7:0]	FTW1		NCO Frequency Tuning Word, FTW[15:8].	0x0	R/W
0x116	FTW2	[7:0]	FTW2		NCO Frequency Tuning Word, FTW[23:16].	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x117	FTW3	[7:0]	FTW3		NCO Frequency Tuning Word, FTW[31:24].	0x0	R/W
0x118	FTW4	[7:0]	FTW4		NCO Frequency Tuning Word, FTW[39:32].	0x0	R/W
0x119	FTW5	[7:0]	FTW5		NCO Frequency Tuning Word, FTW[47:40].	0x10	R/W
0x11A	NCO_PHASE_ OFFSET0	[7:0]	NCO_PHASE_ OFFSET0		NCO Phase Offset, NCO_PHASE_OFFSET[7:0].	0x0	R/W
0x11B	NCO_PHASE_ OFFSET1	[7:0]	NCO_PHASE_ OFFSET1		NCO Phase Offset, NCO_PHASE_OFFSET[15:8].	0x0	R/W
0x11C	NCO_ PHASEADJ[7:0]	[7:0]	PHASEADJ[7:0]		Phase Compensation Word, PHASE_ADJ[7:0].	0x0	R/W
0x11D	NCO_ PHASEADJ [12:8]	[7:0]	PHASEADJ[12:8]		Phase Compensation Word, PHASE_ADJ[12:8].	0x0	R/W
0x11F	TXEN_SM_0	[7:6]	PA_FALL		PA Fall Control.	0x2	R/W
		[5:4]	PA_RISE		PA Rises Control.	0x0	R/W
		3	RESERVED		Reserved.	0x0	R
		2	GP_PA_ON_ INVERT		External Modulator Polarity Invert.	0x0	R/W
		1	GP_PA_CTRL		External PA Control. Enabled by default to allow external mod control instead of sync signal through this pin.	0x1	R/W
		0	TXEN_SM_EN		Enable TXEN State Machine.	0x1	R/W
0x121	TXEN_SM_2	[7:0]	RISE_COUNT_0			0xF	R/W
0x122	TXEN_SM_3	[7:0]	RISE_COUNT_1			0x0	R/W
0x123	TXEN_SM_4	[7:0]	FALL_COUNT_0			0xFF	R/W
0x124	TXEN_SM_5	[7:0]	FALL_COUNT_1			0xFF	R/W
0x12D	DEVICE_ CONFIG_REG0	[7:0]	DEVICE_ CONFIG_0		Must Be Set to 0x8B for Proper Digital Datapath Configuration.	0x46	R/W
0x12F	DIE_TEMP_ CTRL0	[7:1]	RESERVED		Reserved.	0x10	R/W
		0	AUXADC_ ENABLE		1 = Enable AUXADC Block.	0x0	R/W
0x132	DIE_TEMP0	[7:0]	DIE_TEMP_LSB		AUXADC Readback Value Bits[7:0], LSB.	0x0	R
0x133	DIE_TEMP1	[7:0]	DIE_TEMP_MSB		AUXADC Readback Value Bits[15:8], MSB.	0x0	R
0x134	DIE_TEMP_ UPDATE	[7:1]	RESERVED		Reserved.	0x0	R
		0	DIE_TEMP_ UPDATE		Die Temperature Update. When updated, new temperature code is received.	0x0	R/W
0x135	DC_OFFSET_ CTRL	[7:1]	RESERVED		Reserved.	0x0	R
		0	DC_OFFSET_ON		1 = Enable DC Offset Module.	0x0	R/W
0x136	IPATH_DC_OFF-SET_1PART0	[7:0]	IPATH_DC_ OFFSET_1PART0		LSB of First Part of DC Offset Value for I Path.	0x0	R/W
0x137	IPATH_DC_OFF-SET_1PART1	[7:0]	IPATH_DC_ OFFSET_1PART1		MSB of First Part of DC Offset Value for I Path.	0x0	R/W
0x138	QPATH_DC_ OFFSET_ 1PART0	[7:0]	QPATH_DC_ OFFSET_1PART0		LSB of First Part of DC Offset Value for Q Path.	0x0	R/W
0x139	QPATH_DC_ OFFSET_ 1PART1	[7:0]	QPATH_DC_ OFFSET_1PART1		MSB of First Part of DC Offset Value for Q Path.	0x0	R/W
0x13A	IPATH_DC_ OFFSET_2PART	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	IPATH_DC_ OFFSET_2PART		Second Part Of DC Offset Value For I Path.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x13B	QPATH_DC_OFFSET_2PART	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	QPATH_DC_OFFSET_2PART		Second Part of DC Offset Value for Q Path.	0x0	R/W
0x13C	IDAC_DIG_GAIN0	[7:0]	IDAC_DIG_GAIN0		LSB of I DAC Digital Gain.	0x0	R/W
0x13D	IDAC_DIG_GAIN1	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	IDAC_DIG_GAIN1		MSB of I DAC Digital Gain.	0x8	R/W
0x13E	QDAC_DIG_GAIN0	[7:0]	QDAC_DIG_GAIN0		LSB of Q DAC Digital Gain.	0x0	R/W
0x13F	QDAC_DIG_GAIN1	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	QDAC_DIG_GAIN1		MSB of Q DAC Digital Gain.	0x8	R/W
0x140	GAIN_RAMP_UP_STEP0	[7:0]	GAIN_RAMP_UP_STEP0		LSB of Digital Gain Rises.	0x4	R/W
0x141	GAIN_RAMP_UP_STEP1	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	GAIN_RAMP_UP_STEP1		MSB of Digital Gain Rises.	0x0	R/W
0x142	GAIN_RAMP_DOWN_STEP0	[7:0]	GAIN_RAMP_DOWN_STEP0		LSB of Digital Gain Drops.	0x9	R/W
0x143	GAIN_RAMP_DOWN_STEP1	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	GAIN_RAMP_DOWN_STEP1		MSB of Digital Gain Drops.	0x0	R/W
0x146	DEVICE_CONFIG_REG1	[7:0]	DEVICE_CONFIG_1		Must be Set to 0x01 During Startup.	0x0	R/W
0x147	BLSM_STAT	[7:6]	BE_ROTATE_REQ		BE_ROTATE_REQ Forced Value.	0x0	R/W
		[5:0]	RESERVED		Reserved.	0x0	R/W
0x14B	PRBS	7	PRBS_GOOD_Q		Good Data Indicator Imaginary Channel.	0x0	R
				0	Incorrect sequence detected.		
				1	Correct PRBS sequence detected.		
		6	PRBS_GOOD_I		Good Data Indicator Real Channel.	0x0	R
				0	Incorrect sequence detected.		
				1	Correct PRBS sequence detected.		
		5	RESERVED		Reserved.	0x0	R
		[4:3]	RESERVED		Reserved.	0x1	R/W
		2	PRBS_MODE		Polynomial Select.	0x0	R/W
				0	7-bit: $x^7 + x^6 + 1$		
				1	15-bit: $x^{15} + x^{14} + 1$		
		1	PRBS_RESET		Reset Error Counters.	0x0	R/W
				0	Normal operation.		
				1	Reset counters.		
		0	PRBS_EN		Enable PRBS Checker.	0x0	R/W
				0	Disable.		
				1	Enable.		
0x14C	PRBS_ERROR_I	[7:0]	PRBS_COUNT_I		Error Count Value Real Channel.	0x0	R
0x14D	PRBS_ERROR_Q	[7:0]	PRBS_COUNT_Q		Error Count Value Imaginary Channel.	0x0	R

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1B0	DACPLLT0	7	VCO_PD_IN		VCO PD.	0x1	R/W
				0	If power machine disabled this powers up the VCO.		
				1	If power machine disabled this powers down the VCO.		
		6	VCO_PD_PTAT		PD ptat current gen VCO.	0x1	R/W
				1	If power machine disabled this powers down the VCO ptat gen.		
				0	If power machine disabled this powers up the VCO ptat gen.		
		5	VCO_PD_ALC		PD ALC Circuit in VCO.	0x1	R/W
				1	If power machine disabled this powers down the VCO ALC.		
				0	If power machine disabled this powers up the VCO ALC.		
		4	SYNTH_PD		PD Total Synthesizer/Reset Machine.	0x1	R/W
				0	If power machine disabled this powers up the synthesizer.		
				1	If power machine disabled this powers down the synthesizer.		
		3	LDO_PD		PD LDO.	0x1	R/W
				0	If power machine disabled this powers up the LDO.		
				1	If power machine disabled this powers down the LDO.		
		2	RESERVED		Reserved.	0x0	R
		1	LOGEN_PD		PD LO Generator.	0x1	R/W
				0	If power machine disabled this powers up the Prescaler/DAC clock gen.		
				1	If power machine disabled this powers down the Prescaler/DAC clock gen.		
		0	RESERVED		Reserved.	0x0	R
0x1B1	DACPLLT1	[7:4]	RESERVED		Reserved.	0x0	R
		[3:2]	PFD_DELAY		PFD Delay.	0x1	R/W
				0	Shortest delay.		
				1	Longer delay.		
				2	Longer delay still.		
				3	Longest delay.		
		1	PFD_EDGE		PFD Clock Edge.	0x0	R/W
				0	Reference rising edge.		
				1	Reference falling edge.		
		0	RESERVED		Reserved.	0x0	R
0x1B2	DACPLLT2	7	EXT_ALC_WORD_EN		Force ALC Word Externally.	0x0	R/W
				0	Norm operation auto ALC.		
				1	Manually set ALC.		
		[6:0]	EXT_ALC_WORD		External ALC Word.	0x0	W
0x1B3	DACPLLT3	[7:0]	EXT_BAND1		Bottom bit of VCO tuning band to be forced.	0x0	W
0x1B4	DACPLLT4	7	BYP_LOAD_DELAY		Bypass Load Delay.	0x0	R/W
		[6:3]	VCO_CAL_OFFSET		Starting Offset for VCO Calibration.	0xF	R/W
		2	RESERVED		Reserved.	0x0	R
		1	EXT_BAND_EN		FORCE VCO Tuning Band Externally.	0x0	R/W
				0	Normal autocal mode.		
				1	Manual for VCO band.		
		0	EXT_BAND2		External band MSB.	0x0	W
0x1B5	DACPLLT5	[7:4]	INIT_ALC_VALUE		Initial ALC Sweep Value.	0x8	R/W
		[3:0]	VCO_VAR		Varactor KVO Setting.	0x3	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1B6	DACPLLT6	7	RESERVED		Reserved.	0x0	R
		6	PORESETB_VCO		Reset for VCO Logic.	0x1	R/W
		[5:4]	EXT_VCO_BITSEL		External VCO Bitsel.	0x0	R/W
		[3:0]	VCO_LVL_OUT		VCO Amplitude Control.	0xA	R/W
0x1B7	DACPLLT7	7	LD_SYNTH		Manual Recalibration of Synthesizer.	0x0	R/W
				1	Enable circuitry to reduce the voltage of the cal offset target point.		
				0	Disable circuitry to reduce the voltage of the cal offset target point.		
		6	RESERVED		Reserved.	0x0	R
		[5:0]	CP_IBLEED		Charge Pump Offset.	0x0	R/W
0x1B8	DACPLLT8	7	RESERVED		Reserved.	0x0	R
		6	COMP_OUT		CP Calibration comparator output.	0x0	R
		5	CP_CAL_DONE		CP Calibration has completed.	0x0	R
		4	VCO_CAL_IN_PROG		VCO Calibration occurring.	0x0	R
		[3:0]	CP_CALBITS		Calibrated CP outcome.	0x0	R
0x1B9	DACPLLT9	7	HALF_VCO_CAL_CLK		Slow down VCO Calibration clock.	0x0	R/W
		6	DITHER_MODE		Dither Mode—Not used.	0x0	R/W
		5	MACHINE_ENABLE		PLL power mode machine enable.	0x1	R/W
		4	CP_OFFSET_OFF		Turn off CP offset.	0x1	R/W
		3	FORCE_CP_CALBITS		Force external CP cal code.	0x0	R/W
				0	CP Calibration auto—if device off.		
				1	CP Calibration manual—if device off.		
		2	CAP_CAL_EN		Enable CP Calibration.	0x1	R/W
				0	Disable charge pump calibration.		
				1	Enable charge pump calibration.		
		[1:0]	CP_TEST		CP Test Modes.	0x0	R/W
0x1BA	DACPLLTA	[7:4]	MACHINE_STATE		Power-Up Machine State.	0x0	R
		[3:0]	FCP_CALBITS		External CP Calibration Bits to Drive. These are the externally forced calibration bits for the charge pump in the PLL when the power-up machine is not in use. The power-up machine automatically calibrates the charge pump and stores the value in the device.	0x0	R/W
0x1BB	DACPLLTB	[7:5]	RESERVED		Reserved.	0x0	R
		[4:3]	VCO_BIAS_TCF		Temperature Coefficient for VCO bias.	0x1	R/W
		[2:0]	VCO_BIAS_REF		VCO Bias control.	0x4	R/W
0x1BC	DACPLLTC	7	VCO_BYP_BIASR		Bypass VCO bias Resistor.	0x0	R/W
		[6:5]	RESERVED		Reserved.	0x0	R/W
		4	VCO_COMP_BYP_BIASR		Bypass Resistor in VCO Comparator.	0x0	R/W
		3	PRSC_HIGHR		PRSC configuration.	0x0	R/W
		2	LAST_ALC_EN		Enable Last ALC.	0x0	R/W
		[1:0]	PRSC_BIAS_CTRL		PRSC bias Control.	0x0	R/W
0x1BD	DACPLLTD	[7:4]	RESERVED		Reserved.	0x0	R
		3	VCO_CAL_REF_MON		Sent control voltage to outside world.	0x0	R/W
		[2:0]	VCO_CAL_REF_TCF		Temperature Coefficient for Calibration reference.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1BE	DACPLLTE	[7:4]	RESERVED		Reserved.	0x0	R
		3	VCO_PDO_VR		Varactor Reference Power-down Override.	0x0	R/W
		2	VCO_PDO_VRTCF		Varactor Temperature Coefficient Power-Down	0x0	R/W
		1	VCO_PDO_ CALTCF		Calibration Temperature Coefficient Power-Down.	0x0	R/W
		0	VCO_PDO_ VCOBUF		VCO Buffer PD Override.	0x0	R/W
0x1BF	DACPLLTF	7	I_CAL_EN		VCO Band Calibration Enable.	0x1	R/W
		[6:4]	I_ALC_WAIT_D		VCO calibration wait for ALC cal from band change.	0x0	R/W
		[3:2]	I_CAL_COUNT		Calibration Count Length.	0x3	R/W
		[1:0]	FDBCK_DELAY		Feedback Clock Advance.	0x1	R/W
0x1C0	DACPLLT10	[7:6]	RESERVED		Reserved.	0x0	R
		5	USE_NEW_CAL		Use new calibrator.	0x1	R/W
				0	use old calibrator.		
				1	use new calibrator.		
		4	DOUBLE_F0_CAL_ CNT		Increase calibrator count by 2×—Old calibrator machine.	0x0	R/W
		[3:2]	LOCKDETECT_CO UNT		Counter length for Lock detector.	0x3	R/W
		[1:0]	LOCK_MODE		Lock Detector Mode.	0x2	R/W
0x1C1	DACPLLT11	7	RESERVED		Reserved.	0x0	R
		6	CP_LVL_DET_PD		Level detector power-down.	0x0	R/W
		[5:3]	CP_VL_LOW		Low Level detect voltage.	0x2	R/W
		[2:0]	CP_VL_HIGH		High Level detection point.	0x5	R/W
0x1C2	DACPLLT15	7	SDM_BP		Bypass Sigma Delta.	0x1	R/W
		6	SDM_PD		Power-Down SDM.	0x0	R/W
		[5:4]	RESERVED		Reserved.	0x0	R
		[3:0]	SDM_PROG		Program SDM.	0x0	R/W
0x1C3	DACPLLT16	7	RESERVED		Reserved.	0x0	R
		6	SDM_PROG3		SIF Clock.	0x0	R/W
		5	SDM_PROG2		SIF Preset Bar.	0x0	R/W
		[4:0]	SDM_PROG1		SIF Address.	0x0	R/W
0x1C4	DACPLLT17	7	RESERVED		Reserved.	0x0	R
		[6:4]	VCO_VAR_REF_ TCF		Varactor Reference Temperature Coefficient.	0x3	R/W
		[3:0]	VCO_VAR_OFF		Varactor Offset.	0x3	R/W
0x1C5	DACPLLT18	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	VCO_VAR_REF		VCO Varactor Reference.	0x8	R/W
0x200	MASTER_PD	[7:1]	RESERVED		Reserved.	0x0	R
		0	SPI_PD_MASTER		Power down the entire JESD204B Rx analog (all eight channels + bias).	0x1	R/W
0x201	PHY_PD	[7:0]	UNUSEDLANES		SPI override to power down the individual PHYs. Set Bit x to power down the corresponding SERDINx± PHY.	0x0	R/W
0x203	GENERIC_PD	[7:2]	RESERVED		Reserved.	0x0	R
		1	SPI_SYNC1_PD		Power down LVDS buffer for $\overline{\text{SYNCOUT0}}$±.	0x0	R/W
		0	SPI_SYNC2_PD		Power down LVDS buffer for $\overline{\text{SYNCOUT1}}$±.	0x0	R/W
0x206	CDR_RESET	[7:1]	RESERVED		Reserved.	0x0	R
		0	SPI_CDR_RESETN		Resets the digital control logic for all PHYs.	0x1	R/W
				0	CDR logic is reset.		
				1	CDR logic is operational.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x230	CDR_ OPERATING_ MODE_REG_0	[7:6]	RESERVED		Reserved.	0x0	R/W
		5	HALFRATE		Enables half rate CDR operation.	0x1	R/W
				0	Disables CDR half rate operation, data rate ≤6 Gbps.		
				1	Enables CDR half rate operation, data rate > 6 Gbps.		
		[4:2]	RESERVED		Reserved.	0x0	R/W
		1	CDR_OVERSAMP		Enables Oversampling of the Input Data. Set to 1 when 1.44 Gbps ≤ lane rate ≤ 2.88 Gbps.	0x0	R/W
		0	RESERVED		Reserved.	0x0	R/W
0x268	EQ_BIAS_REG	[7:6]	EQ_POWER_ MODE		Used to control the equalizer power/insertion loss capability.	0x1	R/W
				0	Normal Mode.		
				1	Low Power.		
		[5:0]	RESERVED		Reserved.	0x32	R/W
0x280	SYNTH_ ENABLE_ CNTRL	[7:3]	RESERVED		Reserved.	0x0	R
		2	SPI_RECAL_ SYNTH		Set this bit high to re-run all of the SERDES PLL calibration routines. Set this bit low again to allow for additional re-calibrations. Rising edge causes the calibration.	0x0	R/W
		1	RESERVED		Reserved.	0x0	R/W
		0	SPI_ENABLE_ SYNTH		Enable the SERDES PLL. Setting this bit turns on all currents and proceeds to calibrate the PLL. Make sure reference clock and division ratios are correct before enabling this bit.	0x0	R/W
0x281	PLL_STATUS	[7:6]	RESERVED		Reserved.	0x0	R
		5	SPI_CP_OVER_ RANGE_HIGH_RB		Applies if SPI_VCO_OUTPUT_LEVEL = 0. If set, the CP output is above CP Level Threshold High.	0x0	R
				0	Charge pump output is below CP_LEVEL_THRESHOLD_HIGH.		
				1	Charge pump output is above CP_LEVEL_THRESHOLD_HIGH.		
		4	SPI_CP_OVER_ RANGE_LOW_RB		Applies if SPI_VCO_OUTPUT_LEVEL = 0. If set, the CP output is below CP Level Threshold Low.	0x0	R
				0	Charge pump output is above CP_LEVEL_THRESHOLD_LOW.		
				1	Charge pump output is below CP_LEVEL_THRESHOLD_LOW.		
		3	SPI_CP_CAL_ VALID_RB		This bit tells the user if the charge pump cal has completed.	0x0	R
				0	Charge pump calibration is not valid.		
				1	Charge pump calibration is valid.		
		2	SPI_VCO_CAL_IN _PROGRESS_RB		This bit set indicates that a VCO calibration is running.	0x0	R
				0	VCO calibration is not running.		
				1	VCO calibration is running.		
		1	SPI_CURRENTS_ READY_RB			0x0	R
				0	PLL bias currents are not ready.		
				1	PLL bias currents are ready.		
		0	SPI_PLL_LOCK_ RB		If set, the synth locked in the number of clock cycles set by Lock Detect Count.	0x0	R
				0	PLL is not locked.		
				1	PLL is locked.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x284	LOOP_ FILTER_1	[7:4]	LOOP_FILTER_1		Loop filter configuration setting.	0x7	R/W
		[3:0]				0x7	R/W
0x285	LOOP_ FILTER_2	[7:4]	LOOP_FILTER_2		Loop filter configuration setting.	0x8	R/W
		[3:0]				0x7	R/W
0x286	LOOP_ FILTER_3	[7:4]	LOOP_FILTER_3		Loop filter configuration setting.	0x0	R/W
		[3:0]				0x8	R/W
0x287	CP_CURRENT	7	RESERVED		Reserved.	0x0	R
		6	SPI_SERDES_ LOGEN_POWER_ MODE			0x0	R/W
				0	Power Mode 0.		
				1	Power Mode 1.		
		[5:0]	SPI_CP_CURRENT		CP Current Setting.	0x3F	R/W
0x289	REF_CLK_ DIVIDER_LDO	[7:4]	RESERVED		Reserved.	0x0	R
		3	SPI_LDO_REF_ SEL		Selects LDO reference to be from the band gap or a voltage divider (VDD/2).	0x0	R/W
				0	Select band gap for reference.		
				1	Select voltage divider (VDD/2) for reference.		
		2	SPI_LDO_ BYPASS_FILT		Bypasses filter on LDO reference input.	0x1	R/W
				0	Filter enabled.		
				1	Filter bypassed.		
		[1:0]	SPI_CDR_ OVERSAMP		Enable oversampling of input data. The valid options are: 1×, 2×, and 4×. 1× works for Half Rate—6.25 Gbps to 12.5 Gbps. 1× works for Full Rate—3.125 Gbps to 6.25 Gbps. 2× works for Full Rate—1.625 Gbps to 3.125 Gbps (2× oversampling). 4× works for Full Rate—812.5 Mbps to 1.625 Gbps (4× oversampling).	0x0	R/W
					Oversampling set in Register 0x230.		
				0	No oversampling. Data rate > 6 Gbps.		
				1	Oversample by 2×. 3 Gbps < data rate ≤ 6 Gbps.		
				2	Oversample by 4×. 1.5 Gbps < data rate ≤ 3 Gbps.		
0x28A	VCO_LDO	[7:0]	SPI_SERDES_LDO _CONFIG		VCO LDO Setting.	0x2B	R/W
0x28B	PLL_PD_REG	7	RESERVED		Reserved.	0x0	R/W
		6	SPI_VCO_PD		VCO enable.	0x1	R/W
				0	VCO enabled.		
				1	VCO disabled.		
		5	SPI_VCO_PD_ PTAT			0x1	R/W
		4	SPI_VCO_PD_ALC			0x1	R/W
		3	SPI_SYN_PD			0x1	R/W
		2	SPI_SERDES_ LDO_PD		PD LDO.	0x1	R/W
				0	LDO enabled.		
				1	LDO disabled.		
		1	SPI_SERDES_ LOGEN_PD_ OUTBUF		PD divider buffer.	0x1	R/W
				0	Buffer enabled.		
				1	Buffer disabled.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		0	SPI_SERDES_LOGEN_PD_CORE		PD Logen Dividers.	0x1	R/W
				0	Dividers enabled.		
				1	Dividers disabled.		
0x290	ALC_VARACTOR	[7:4]	SPI_INIT_ALC_VALUE		ALC Value Setting.	0x8	R/W
		[3:0]	SPI_VCO_VARACTOR		VCO KV Setting.	0x3	R/W
0x291	VCO_OUTPUT	[7:4]	RESERVED		Reserved.	0x4	R/W
		[3:0]	SPI_VCO_OUTPUT_LEVEL		VCO output level setting.	0x9	R/W
0x294	CP_CONFIG	7	SPI_HALF_VCO_CAL_CLK			0x1	R/W
		6	SPI_DITHER_MODE			0x0	R/W
		5	SPI_ENABLE_MACHINE			0x1	R/W
		4	SPI_CP_OFFSET_OFF			0x1	R/W
		3	SPI_CP_FORCE_CALBITS			0x0	R/W
		2	SPI_CP_CAL_EN			0x0	R/W
		[1:0]	SPI_CP_TEST			0x0	R/W
0x296	VCO_BIAS_1	[7:5]	RESERVED		Reserved.	0x0	R/W
		[4:3]	SPI_VCO_BIAS_TCF			0x1	R/W
		[2:0]	SPI_VCO_BIAS_REF		CP Calibration Control.	0x4	R/W
0x297	VCO_BIAS_2	[7:6]	RESERVED		Reserved.	0x0	R
		5	SPI_VCO_BYPASS_BIAS_DAC_R			0x0	R/W
		4	SPI_VCO_COMP_BYPASS_BIASR			0x0	R/W
		3	SPI_PRESCALE_BYPASS_R			0x0	R/W
		2	SPI_LAST_ALC_EN			0x0	R/W
		[1:0]	SPI_PRESCALE_BIAS			0x0	R/W
0x299	VCO_PD_OVERRIDES	[7:4]	RESERVED			0x0	R/W
		3	SPI_VCO_PD_OVERRIDE_VAR_REF			0x0	R/W
		2	SPI_VCO_PD_OVERRIDE_VAR_REF_TCF			0x0	R/W
		1	SPI_VCO_PD_OVERRIDE_CAL_TCF			0x0	R/W
		0	SPI_VCO_PD_OVERRIDE_VCOBUF			0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x29A	VCO_CAL	7	SPI_VCO_CAL_EN			0x1	R/W
		[6:4]	SPI_VCO_CAL_ ALC_WAIT			0x7	R/W
		[3:2]	SPI_VCO_CAL_ COUNT			0x3	R/W
		[1:0]	SPI_FB_CLOCK_ ADV			0x2	R/W
0x29C	CP_LEVEL_ DETECT	7	RESERVED		Reserved.	0x0	R
		6	SPI_CP_LEVEL_ DET_PD			0x0	R/W
		[5:3]	SPI_CP_LEVEL_ THRESHOLD_LOW			0x2	R/W
		[2:0]	SPI_CP_LEVEL_ THRESHOLD_ HIGH			0x7	R/W
0x29F	VCO_ VARACTOR_ CONTROL_0	7	RESERVED			0x0	R
		[6:4]	SPI_VCO_VARAC-TOR_REF_TCF			0x3	R/W
		[3:0]	SPI_VCO_VARAC-TOR_OFFSET			0x3	R/W
0x2A0	VCO_ VARACTOR_ CONTROL_1	[7:4]	RESERVED			0x0	R
		[3:0]	SPI_VCO_ VARACTOR_REF			0x8	R/W
0x2A7	TERM_BLK1_ CTRLREG0	[7:1]	RESERVED		Reserved.	0x0	R
		0	SPI_I_TUNE_R_ CAL_TERMBLK1		Rising edge of this bit starts a termination calibration routine.	0x0	R/W
0x2AE	TERM_BLK2_ CTRLREG0	[7:1]	RESERVED		Reserved.	0x0	R
		0	SPI_I_TUNE_R_ CAL_TERMBLK2		Rising edge of this bit starts a termination calibration routine.	0x0	R/W
0x300	GENERAL_ JRX_CTRL_0	7	RESERVED		Reserved.	0x0	R
		6	CHECKSUMMODE		JESD204B link parameter checksum calculation method.	0x0	R/W
				0	checksum is the sum of fields.		
				1	checksum is the sum of octets.		
		[5:4]	RESERVED		Reserved	0x0	R/W
		3	DUALLINK		This register selects either single link or dual link mode.	0x0	R/W
				0	Single link mode.		
				1	Dual link mode.		
		2	CURRENTLINK		To select which QBD register map to work with.	0x0	R/W
				0	User access to QBD_0 registers.		
				1	User access to QBD_1 registers.		
		[1:0]	ENLINKS		Used to bring up JESD204B Rx digital when all link parameters are programmed and all clocks are ready Bit 0 applies to Link 0 while Bit 1 applies to Link 1. Link 1 is only available in dual link mode. Both links may be brought up separately or together.	0x0	R/W
0x301	GENERAL_ JRX_CTRL_1	[7:3]	RESERVED		Reserved.	0x0	R
		[2:0]	SUBCLASSV_ LOCAL		JESD204B Subclass	0x1	R/W
				0	Subclass 0		
				1	Subclass 1		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x302	DYN_LINK_ LATENCY_0	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	DYN_LINK_ LATENCY_0		Link 0 Dynamic Link Latency. Latency between current deframer LMFC and the global LMFC.	0x0	R
0x303	DYN_LINK_ LATENCY_1	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	DYN_LINK_ LATENCY_1		Link 1 Dynamic Link Latency. Latency between current deframer LMFC and the global LMFC.	0x0	R
0x304	LMFC_ DELAY_0	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LMFCDEL0		Delay in Frame clock cycles for global LMFC for Link 0.	0x0	R/W
0x305	LMFC_ DELAY_1	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LMFCDEL1		Delay in Frame clock cycles for global LMFC for Link 1.	0x0	R/W
0x306	LMFCVAR0	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LMFCVAR0		Location in Rx LMFC where JESD204B words are read out from buffer. This setting should not be more than 10.	0x6	R/W
0x307	LMFCVAR1	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LMFCVAR1		Location in Rx LMFC where JESD204B words are read out from buffer. This setting should not be more than 10.	0x6	R/W
0x308	XBAR_LN_0_1	[7:6]	RESERVED		Reserved.	0x0	R
		[5:3]	XBARVAL1		Logic Lane 1 Source. Selects a physical lane to be mapped onto Logical Lane 1. Data is from SERDINx±.	0x1	R/W
		[2:0]	XBARVAL0		Logic Lane 0 Source. Selects a physical lane to be mapped onto Logical Lane 0. Data is from SERDINx±.	0x0	R/W
0x309	XBAR_LN_2_3	[7:6]	RESERVED		Reserved.	0x0	R
		[5:3]	XBARVAL3		Logic Lane 3 Source. Selects a physical lane to be mapped onto Logical Lane 3. Data is from SERDINx±.	0x3	R/W
		[2:0]	XBARVAL2		Logic Lane 2 Source. Selects a physical lane to be mapped onto Logical Lane 2. Data is from SERDINx±.	0x2	R/W
0x30A	XBAR_LN_4_5	[7:6]	RESERVED		Reserved.	0x0	R
		[5:3]	XBARVAL5		Logic Lane 5 Source. Selects a physical lane to be mapped onto Logical Lane 5. Data is from SERDINx±.	0x5	R/W
		[2:0]	XBARVAL4		Logic Lane 4 Source. Selects a physical lane to be mapped onto Logical Lane 4. Data is from SERDINx±.	0x4	R/W
0x30B	XBAR_LN_6_7	[7:6]	RESERVED		Reserved.	0x0	R
		[5:3]	XBARVAL7		Logic Lane 7 Source. Selects a physical lane to be mapped onto Logical Lane 7. Data is from SERDINx±.	0x7	R/W
		[2:0]	XBARVAL6		Logic Lane 6 Source. Selects a physical lane to be mapped onto Logical Lane 6. Data is from SERDINx±.	0x6	R/W
0x30C	FIFO_ STATUS_ REG_0	[7:0]	LANE_FIFO_FULL		FIFO Full Flags for Each Logical Lane. A full FIFO indicates an error in the JESD204B configuration or with a system clock. If the FIFO for Lane x is full, Bit x in this register will be high.	0x0	R

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x30D	FIFO_STATUS_REG_1	[7:0]	LANE_FIFO_EMPTY		FIFO Empty Flags for Each Logical Lane. An empty FIFO indicates an error in the JESD204B configuration or with a system clock. If the FIFO for Lane x is empty, Bit x in this register will be high.	0x0	R
0x312	SYNCB_GEN_1	[7:6]	RESERVED		Reserved.	0x0	R/W
		[5:4]	SYNCB_ERR_DUR		Duration of $\overline{\text{SYNCOUTx±}}$ Low for Error. The duration applies to both $\overline{\text{SYNCOUT0}}$ and $\overline{\text{SYNCOUT1}}$. A sync error is asserted at the end of a multiframe whenever one or more disparity, not in table or unexpected control character errors are encountered.	0x0	R/W
				0	½ PCLK cycle.		
				1	1 PCLK cycle.		
				2	2 PCLK cycles.		
		[3:0]	RESERVED		Reserved.	0x0	R/W
0x314	SPI_SYNC_CTRL	[7:1]	RESERVED		Reserved.	0x0	R
		0	SPI_SYNC_CLK_SEL		SERDES SPI Configuration.	0x0	R/W
				0			
				1	Setting in PHY Layer setup.		
0x315	PHY_PRBS_TEST_EN	[7:0]	PHY_TEST_EN		Set Bit x to enable the PHY test for Lane x.	0x0	R/W
0x316	PHY_PRBS_TEST_CTRL	7	RESERVED		Reserved.	0x0	R
		[6:4]	PHY_SRC_ERR_CNT		Report Lane Error Count.	0x0	R/W
		[3:2]	PHY_PRBS_PAT_SEL		To select PRBS pattern for PHY BER test.	0x0	R/W
				0	PRBS7.		
				1	PRBS15.		
				2	PRBS31.		
				3	Not used.		
		1	PHY_TEST_START		To start and stop the PHY PRBS test.	0x0	R/W
				0	test not started.		
				1	test started.		
		0	PHY_TEST_RESET		Reset PHY PRBS test state machine, and error counters.	0x0	R/W
				0	not reset.		
				1	reset.		
0x317	PHY_PRBS_TEST_THRESHOLD_LOBITS	[7:0]	PHY_PRBS_THRESHOLD_LOBITS		Bits[7:0] of the 24-bit threshold value to set the error flag for PHY PRBS test.	0x0	R/W
0x318	PHY_PRBS_TEST_THRESHOLD_MIDBITS	[7:0]	PHY_PRBS_THRESHOLD_MIDBITS		Bits[15:8] of the 24-bit threshold value to set the error flag for PHY PRBS test.	0x0	R/W
0x319	PHY_PRBS_TEST_THRESHOLD_HIBITS	[7:0]	PHY_PRBS_THRESHOLD_HIBITS		Bits[23:16] of the 24-bit threshold value to set the error flag for PHY PRBS test.	0x0	R/W
0x31A	PHY_PRBS_TEST_ERRCNT_LOBITS	[7:0]	PHY_PRBS_ERR_CNT_LOBITS		Bits[7:0] of the 24-bit reported PHY BERT error count from selected lane.	0x0	R
0x31B	PHY_PRBS_TEST_ERRCNT_MIDBITS	[7:0]	PHY_PRBS_ERR_CNT_MIDBITS		Bits[15:8] of the 24-bit reported PHY BERT error count from selected lane.	0x0	R

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x31C	PHY_PRBS_TEST_ERRCNT_HIBITS	[7:0]	PHY_PRBS_ERR_CNT_HIBITS		Bits[23:16] of the 24-bit reported PHY BERT error count from selected lane.	0x0	R
0x31D	PHY_PRBS_TEST_STATUS	[7:0]	PHY_PRBS_PASS		Each bit is for the corresponding lane. Report PHY BERT pass/fail for each lane.	0xFF	R
0x32C	SHORT_TPL_TEST_0	[7:6]	RESERVED		Reserved.	0x0	R
		[5:4]	SHORT_TPL_SP_SEL		Short Transport Layer Sample Select. Select which sample to check from a specific DAC.	0x0	R/W
				0	Sample 0.		
				1	Sample 1.		
				2	Sample 2.		
				3	Sample 3.		
		[3:2]	SHORT_TPL_M_SEL		Short Transport Layer Test DAC Select. Select which DAC to check.	0x0	R/W
				0	DAC 0.		
				1	DAC 1.		
				2	DAC 2.		
				3	DAC 3.		
		1	SHORT_TPL_TEST_RESET		Short Transport Layer Test Reset. Resets the result of short transport layer test at SHORT_TPL_DIFF.	0x0	R/W
				0	Not reset.		
				1	Reset.		
		0	SHORT_TPL_TEST_EN		Short Transport Layer Test Enable. Enable short transport layer test.	0x0	R/W
				0	Disable.		
				1	Enable.		
0x32D	SHORT_TPL_TEST_1	[7:0]	SHORT_TPL_REF_SP_LSB		Short Transport Layer Reference Sample LSB. This is the lower 8 bits of expected DAC sample. It is used to compare with the received DAC sample at the output of JESD204B Rx.	0x0	R/W
0x32E	SHORT_TPL_TEST_2	[7:0]	SHORT_TPL_REF_SP_MSB		Short Transport Layer Test Reference Sample MSB. This is the upper 8 bits of expected DAC sample. It is used to compare with the received sample at JESD Rx output.	0x0	R/W
0x32F	SHORT_TPL_TEST_3	[7:1]	RESERVED		Reserved.	0x0	R
		0	SHORT_TPL_FAIL		Short Transport Layer Test Fail. This bit shows if the selected DAC sample matches the reference sample. If they match test pass; otherwise test fail.	0x0	R
				0	Test pass.		
				1	Test fail.		
0x333	DEVICE_CONFIG_REG2	[7:0]	RESERVED		Must be set to 0x1 for correct JESD204B receiver operation.	0x0	R/W
0x334	JESD_BIT_INVERSE_CTRL	[7:0]	INVLANES		Logic Lane Invert. Set Bit x high to invert the JESD204B deserialized data on Logical Lane x.	0x0	R/W
0x400	DID_REG	[7:0]	DID_RD		DID is the Device ID No. Link information received on Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
0x401	BID_REG	[7:4]	ADJCNT_RD		ADJCNT is the Adjustment Resolution to DAC LMFC. Link information received on Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
		[3:0]	BID_RD		BID is the Bank ID—Extension to DID. Link information received on Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x402	LID0_REG	7	RESERVED		Reserved.	0x0	R
		6	ADJDIR_RD		ADJDIR is the Direction to Adjust DAC LMFC. Link information received on Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
		5	PHADJ_RD		PHADJ is the Phase Adjustment Request to DAC. Link information received on Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
		[4:0]	LID0_RD		LID0 is the Lane Identification for Lane 0. Link information received on Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
0x403	SCR_L_REG	7	SCR_RD		SCR is the Tx Scrambling Status. Link information received on Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
				0	Scrambling is disabled.		
				1	Scrambling is enabled.		
		[6:5]	RESERVED		Reserved.	0x0	R
		[4:0]	L_RD		L is the Number of Lanes per Converter Device. Link information received on lane 0 as specified in section 8.3 of JESD204B.	0x0	R
				0	1 lane per converter device.		
				1	2 lanes per converter device.		
				3	4 lanes per converter device.		
0x404	F_REG	[7:0]	F_RD		F is the Number of Octets Per Frame. Settings of 1, 2, and 4 are valid. Link information received on Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
				0	1 octet per frame.		
				1	2 octets per frame.		
				3	4 octets per frame.		
0x405	K_REG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	K_RD		K is the Number of Frames per Multiframe. Settings of 16 or 32 are valid. Link information received on lane 0 as specified in section 8.3 of JESD204B. 01111 = 16. 11111 = 32.	0x0	R
0x406	M_REG	[7:0]	M_RD		M is the Number of Converters/Device. Link information received on Lane 0 as specified in Section 8.3 of JESD204B. Must be 1,2, or 4 to be compatible with AD9154	0x0	R
				0	1 converter per device.		
				1	2 converters per device.		
				3	4 converters per device.		
0x407	CS_N_REG	[7:6]	CS_RD		CS is the Number of Control Bits/Sample. Link information received on Lane 0 as specified in Section 8.3 of JESD204B. Must be 0 to be compatible with AD9154.	0x0	R
		5	RESERVED		Reserved.	0x0	R
		[4:0]	N_RD		N = converter resolution.	0x0	R
0x408	NP_REG	[7:5]	SUBCLASSV_RD		SUBCLASSV is the Device SubClass Version. Link information received on lane 0 as specified in section 8.3 of JESD204B.	0x0	R

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[4:0]	NP_RD		Np is the Total Number of Bits/Sample. Link information received on Lane 0 as specified in Section 8.3 of JESD204B. = 16 bits per sample.	0x0	R
0x409	S_REG	[7:5]	JESDV_RD		JESDV is the JESD204 Version. Link information received on lane 0 as specified in section 8.3 of JESD204B.	0x0	R
				0	JESD204A.		
				1	JESD204B.		
		[4:0]	S_RD		S is the Number of Samples/Converter per Frame Cycle. Link information received on lane 0 as specified in section 8.3 of JESD204B.	0x0	R
				0	One sample per converter per frame.		
				1	Two samples per converter per frame.		
0x40A	HD_CF_REG	7	HD_RD		HD is the High Density Format. Refer to Section 5.1.3 of JESD204B standard. Link information received on Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
				0	Low density mode.		
				1	High density mode.		
		[6:5]	RESERVED		Reserved.	0x0	R
		[4:0]	CF_RD		CF is the Number of Control Words per Frame Clock Period per Link. Link information received on Lane 0 as specified in Section 8.3 of JESD204B. Must be 0 to be compatible to the AD9154.	0x0	R
0x40B	RES1_REG	[7:0]	RES1_RD		Reserved Field 1. Link information received on Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
0x40C	RES2_REG	[7:0]	RES2_RD		Reserved Field 2. Link information received on Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
0x40D	CHECKSUM_REG	[7:0]	LANE0CHECKSUM_RD		Checksum for Lane 0. Link information received on Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
0x40E	COMPSUM0_REG	[7:0]	FCMP0_RD		Computed Checksum for Lane 0. The JESD204B Rx computes the checksum of the link information received on Lane 0 as specified in Section 8.3 of JESD204B. The computation method is set by the CHECKSUMMODE bit (Register 0x300[6]) and should match the likewise calculated checksum in Register 0x40D.	0x0	R
0x412	LID1_REG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LID1_RD		Lane Identification for Lane 1. Link information received on Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
0x415	CHECKSUM1_REG	[7:0]	FCHK1_RD		Checksum for Lane 1. Link information received on Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
0x416	COMPSUM1_REG	[7:0]	FCMP1_RD		Computed Checksum for Lane 1. See description for Register 0x40E.	0x0	R
0x41A	LID2_REG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LID2_RD		Lane Identification for Lane 2.	0x0	R

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x41D	CHECKSUM2_REG	[7:0]	FCHK2_RD		Checksum for Lane 2.	0x0	R
0x41E	COMPSUM2_REG	[7:0]	FCMP2_RD		Computed Checksum for Lane 2. See description for Register 0x40E.	0x0	R
0x422	LID3_REG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LID3_RD		Lane Identification for Lane 3.	0x0	R
0x425	CHECKSUM3_REG	[7:0]	FCHK3_RD		Checksum for Lane 3.	0x0	R
0x426	COMPSUM3_REG	[7:0]	FCMP3_RD		Computed Checksum for LANE 3 (see description for Register 0x40E).	0x0	R
0x42A	LID4_REG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LID4_RD		Lane Identification for Lane 4.	0x0	R
0x42D	CHECKSUM4_REG	[7:0]	FCHK4_RD		Checksum for Lane 4	0x0	R
0x42E	COMPSUM4_REG	[7:0]	FCMP4_RD		Computed Checksum for Lane 4 (see description for Register 0x40E).	0x0	R
0x432	LID5_REG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LID5_RD		Lane Identification for Lane 5.	0x0	R
0x435	CHECKSUM5_REG	[7:0]	FCHK5_RD		Checksum for Lane 5.	0x0	R
0x436	COMPSUM5_REG	[7:0]	FCMP5_RD		Computed Checksum for Lane 5 (see description for Register 0x40E).	0x0	R
0x43A	LID6_REG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LID6_RD		Lane Identification for Lane 6.	0x0	R
0x43D	CHECKSUM6_REG	[7:0]	FCHK6_RD		Checksum for Lane 6.	0x0	R
0x43E	COMPSUM6_REG	[7:0]	FCMP6_RD		Computed Checksum for Lane 6 (see description for Register 0x40E).	0x0	R
0x442	LID7_REG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LID7_RD		Lane Identification for Lane 7.	0x0	R
0x445	CHECKSUM7_REG	[7:0]	FCHK7_RD		Checksum for Lane 7.	0x0	R
0x446	COMPSUM7_REG	[7:0]	FCMP7_RD		Computed Checksum for Lane 7 (see description for Register 0x40E).	0x0	R
0x450	ILS_DID	[7:0]	DID		DID is the Device ID Number. Link information received on Lane 0 as specified in Section 8.3 of JESD204B. Must be set to value read in Register 0x400.	0x0	R/W
0x451	ILS_BID	[7:4]	ADJCNT		ADJCNT is the Adjustment Resolution to DAC LMFC. Link information received on Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R/W
		[3:0]	BID		BID is the Bank ID—Extension to DID. Link information received on Lane 0 as specified in Section 8.3 of JESD204B. Must be set to value read in Register 0x401[3:0].	0x0	R/W
0x452	ILS_LID0	7	RESERVED		Reserved.	0x0	R
		6	ADJDIR		ADJDIR is the Direction to Adjust DAC LMFC. Link information received on Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R/W
		5	PHADJ		PHADJ is the Phase Adjustment Request To DAC. Link information received on Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R/W
		[4:0]	LID0		LID0 is the Lane identification for Lane 0. Link information received on Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x453	ILS_SCR_L	7	SCR		SCR is the Rx Descrambling Enable.	0x1	R/W
				0	Is disabled.		
				1	Is enabled.		
		[6:5]	RESERVED		Reserved.	0x0	R
		[4:0]	L		L is the Number of Lanes Per Converter Device Settings of 2, 4, and 8 are valid for single single link mode. Settings of 1, 2, and 4 are valid for dual link mode.	0x3	R/W
				00000	1 lane.		
				00001	2 lanes.		
				00011	4 lanes.		
				00111	8 lanes.		
0x454	ILS_F	[7:0]	F		This value of F is not used to soft configure the QBD. The Register CTRLREG1 is used to soft configure the QBD.	0x0	R/W
0x455	ILS_K	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	K		K is the number of frames per multiframe. Settings of 16 or 32 are valid. Must be set to 32 when F = 4 (Register 0x476). 01111 = 16. 11111 = 32.	0x1F	R/W
0x456	ILS_M	[7:0]	M		M is the number of converters/device. Settings of 1, 2, and 4 are valid for single link mode. Settings of 1 and 2 are valid in dual link mode. Refer to Table 15 and Table 16.	0x1	R
				0	1 converter per device.		
				1	2 converters per device.		
				3	4 converters per device.		
0x457	ILS_CS_N	[7:6]	CS		CS is the number of control bits/sample. Must be set to 0. Control bits are not supported.	0x0	R/W
		5	RESERVED		Reserved.	0x0	R
		[4:0]	N		N = converter resolution. Must be set to 16 (0x0F).	0x1F	R/W
0x458	ILS_NP	[7:5]	SUBCLASSV		SUBCLASSV = device Subclass version. Must be set to 1 (3'b001).	0x1	R/W
		[4:0]	NP		Np = total no. of bits/sample. Must be set to 16 (0x0F). Refer to Table 15 and Table 16.	0xF	R/W
0x459	ILS_S	[7:5]	JESDVER		JESDV is the JESD204 version.	0x1	R/W
				0	JESD204A.		
				1	JESD204B .		
		[4:0]	S		S = no. of samples/converter per frame cycle. Settings of 1 and 2 are valid. Refer to Table 15 and Table 16. S = 00000 -> 1 Sample. S = 00001 -> 2 Samples.	0x0	R/W
0x45A	ILS_HD_CF	7	HD		HD is high density mode. Refer to section 5.1.3 of JESD204B standard.	0x1	R/W
				0	density mode.		
				1	density mode.		
		[6:5]	RESERVED		Reserved.	0x0	R
		[4:0]	CF		CF is the number of control words per frame clock period per link. Must be set to 0. Control bits are not supported.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x45D	ILS_CHECKSUM	[7:0]	LANE0-CHECKSUM		Checksum for Lane 0. The checksum for the values programmed into Register 0x450 to Register 0x45C must be calculated according to section 8.3 of the JESD204B spec and written here [SUM(Register 0x450 – Register 0x45C) % 256].	0x45	R/W
0x46B	ERRCNTRMON	7	RESERVED		Reserved.	0x0	R
		[6:4]	LANESEL		Lane Select for JESD204B Error Counter. Writing these bits selects the JESD lane to monitor the error type designated by the register write to CNTRSEL (Bits 1:0]) BADDISCNTR, NITCNTR and UEKCCNTR error counters in each lane are accessed via indirect addressing. To read a counter value, the LANESEL and CNTRSEL are first written, then the read back accesses the desired counter. 0 Selects Lane 0. 1 Selects Lane 1. 3 Selects Lane 2. 3 Selects Lane 3. 4 Selects Lane 4. 5 Selects Lane 5. 6 Selects Lane 6. 7 Selects Lane 7.	0x0	W
		[3:2]	RESERVED		Reserved.	0x0	R
		[7:0]	READERRORCNTR		Read JESD204B Error Counter. After selecting the lane and error counter by writing to LANESEL (Bits[6:4]) and CNTRSEL (1:0), the selected error counter is read back here.	0x0	R
		[1:0]	CNTRSEL		JESD204B Error Counter Select. Writing these bits allows the readback of the following JESD204B errors for the lane designated by the register write to LANESEL (Bits[6:4]). To read a counter value, the LANESEL and CNTRSEL are first written, then the read back access the desired counter. 0 BADDISCNTR: bad running disparity counter. 1 NITCNTR: not in table error counter. 2 UCCCNTR: Unexpected control character counter.	0x0	W
0x46C	LANEDESKEW	[7:0]	LANEDESKEW		Lane Deskew. Enabled on a per lane basis by writing 1 to the appropriate bit position: Bits[7:0] map to Lane 7 to Lane 0. Note that in dual link mode, only Bits[3:0] are used for each link. 1: Deskew enabled for Lane 0. 1: Deskew enabled for Lane 1. 1: Deskew enabled for Lane 2. 1: Deskew enabled for Lane 3. 1: Deskew enabled for Lane 4. 1: Deskew enabled for Lane 5. 1: Deskew enabled for Lane 6. 1: Deskew enabled for Lane 7.	0xF	R/W

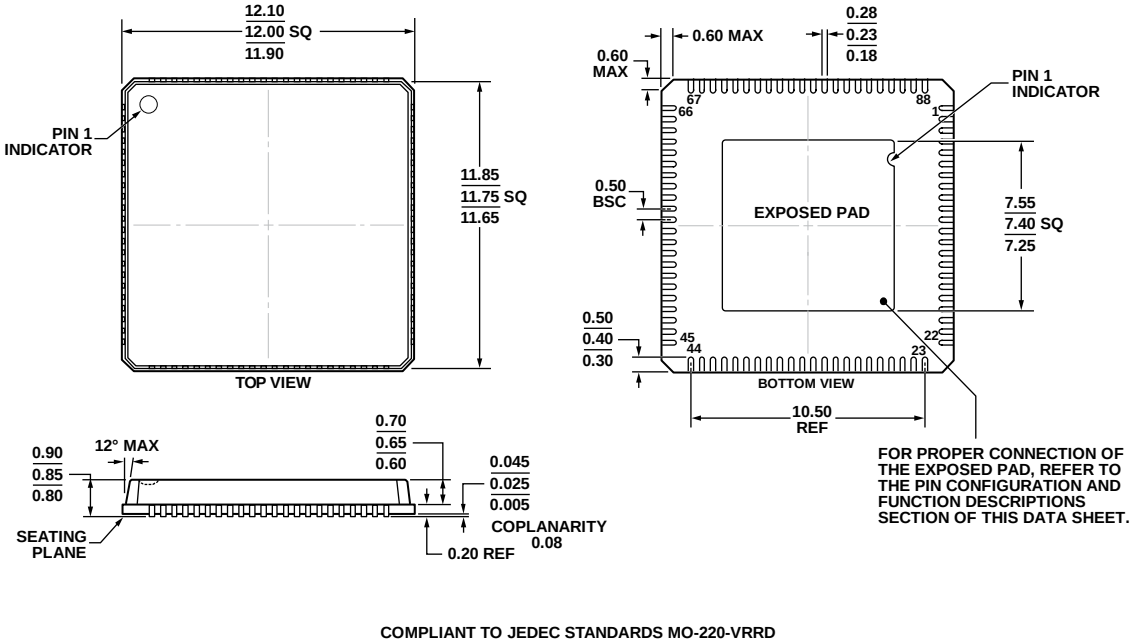
Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x46D	BADDISPARITY	7	RSTIRQ_DIS		Reset BADDIS IRQ counter for lane selected via Bits[2:0] by writing 1 to this bit.	0x0	W
		6	DISABLE_ERRCNT_DIS		Disable the BADDIS error counter for lane selected via Bits[2:0] by writing 1 to this bit.	0x0	W
		5	RSTERRCNTR_DIS		Reset BADDIS error counter for lane selected via Bits[2:0] by writing 1 to this bit.	0x0	W
		[4:3]	RESERVED		Reserved.	0x0	R
		[7:0]	BADDIS		Bad Disparity Character Error (BADDIS). Each bit corresponds to each lane. The error count can be accessed via Register 0x46B. Note that in dual link mode, only Bits[3:0] are used for each link. 1 BadDisparitycharacter error count has reached the threshold count of Register 0x7C for any lane with its corresponding bit set when reading this register. 0 Bad Disparity character error count has Not reached the threshold count.	0x0	R
		[2:0]	LANEADDR_DIS		Lane Address for functions described in Bits[7:5]	0x0	W
0x46E	NITDISPARITY	7	RSTIRQ_NIT		Reset IRQ for lane selected via Bits[2:0] by writing 1 to this bit.	0x0	W
		6	DISABLE_ERRCNT_NIT		Disable the error counter for lane selected via Bits[2:0] by writing 1 to this bit.	0x0	W
		5	RSTERRCNTR_NIT		Reset error counter for lane selected via Bits[2:0] by writing 1 to this bit.	0x0	W
		[4:3]	RESERVED		Reserved.	0x0	R
		[7:0]	NITD		Not In Table Disparity Character Error (NITD). Each bit corresponds to each lane. The error count can be accessed via Register 0x46B. Note that in dual link mode, only Bits[3:0] are used for each link.	0x0	R
		[2:0]	LANEADDR_NIT		Lane Address for functions described in Bits[7:5].	0x0	W
0x46F	UNEXPECTEDKCHAR	7	RSTIRQ_K		Reset IRQ for lane selected via Bits[2:0] by writing 1 to this bit.	0x0	W
		6	DISABLE_ERRCNT_K		Disable the error counter for lane selected via Bits[2:0] by writing 1 to this bit.	0x0	W
		5	RSTERRCNTR_K		Reset error counter for lane selected via Bits[2:0] by writing 1 to this bit.	0x0	W
		[4:3]	RESERVED		Reserved.	0x0	R
		[2:0]	LANEADDR_K		Lane Address for functions described in Bits[7:5].	0x0	W
0x470	CODEGRP-SYNCFLG	[7:0]	CODEGRPSYNC		Code Group Sync Flag (from each instantiated lane) Writing 1 to Bit 7 resets the IRQ. The associated IRQ flag is located in Register 0x470[0]. A loss of CODEGRPSYNC triggers Sync Request assertion. Refer to the SYSREF, SYNCOUT, and the Deterministic Latency section. 1 on Bit x of this register = synchronization was achieved on lane L. 0 on Bit x of this register = synchronization was lost on Lane x.	0x0	R/W
0x471	FRAMESYNC-FLG	[7:0]	FRAMESYNC		Frame Sync Flag (from each instantiated lane). This register indicates the live status for each lane. Writing 1 to Bit 7 resets the IRQ. A loss of Frame Sync automatically initiates a synchronization sequence.	0x0	R/W
0x472	GOODCHK-SUMFLG	[7:0]	GOOD-CHECKSUM		Good Check Sum flag (from each instantiated lane.) Writing 1 to Bit 7 resets the IRQ. The associated IRQ flag is located in Register 0x470[2].	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x473	INITLANE-SYNCFLG	[7:0]	INITIALLANESYNC		Initial Lane Sync Flag (from each instantiated lane). Writing 1 to Bit 7 resets the IRQ. The associated IRQ flag is located in Register 0x470[2]. Loss of synchronization is also reported on $\overline{\text{SYNCOUT}}$. Refer to the SYSREF, $\overline{\text{SYNCOUT}}$, and the Deterministic Latency section.	0x0	R/W
0x476	CTRLREG1	[7:0]	F_AGAIN		F is the number of octets per frame. Settings of 1, 2, and 4 are valid. Refer to Table 15 and Table 16.	0x1	R/W
0x477	CTRLREG2	7	ILAS_MODE		ILAS Test Mode. Defined in Section 5.3.3.8 of JESD204B specification.	0x0	R/W
				1	JESD204B receiver is constantly receiving ILAS frames.		
				0	Normal link operation.		
		[6:4]	RESERVED		Reserved.	0x0	R
		3	THRESHOLD_ MASK_EN		Threshold Mask Enable. Set this bit if using SYNC_ASSERTION_MASK (Register 0x47B[7:5]).	0x0	R/W
		[2:0]	RESERVED		Reserved.	0x0	R
0x478	KVAL	[7:0]	KSYNC		Number of 4 × K multiframes during ILAS. Sets the number of multiframes to send lane alignment sequence during the initial lane alignment. 1 = 4 × K multiframes.	0x1	R/W
0x47A	IRQVECTOR	7	BADDIS_FLAG		Bad Disparity Error Count.	0x0	R
				1	Bad disparity character count reached ERRORTHRESH (Register 0x47C) on at least one lane. Read Register 0x46D to determine which lanes are in error.		
		7	BADDIS_MASK		Bad Disparity Mask.	0x0	W
				1	If the bad disparity count reaches ERRORTHRESH on any lane, $\overline{\text{IRQ}}$ is pulled low.		
		6	NITD_MASK		Not in Table Mask.	0x0	W
				1	If the not in table character count reaches ERRORTHRESH on any lane, $\overline{\text{IRQ}}$ is pulled low.		
		6	NITD_FLAG		Not in Table Error Count.	0x0	R
				1	Not in table character count reached ERRORTHRESH (Register 0x47C) on at least one lane. Read Register 0x46E to determine which lanes are in error.		
		5	UEKC_FLAG		Unexpected Control Character Error Count.	0x0	R
				1	Unexpected control character count reached ERRORTHRESH (0x47C) on at least one lane. Read Register 0x46F to determine which lanes are in error.		
		5	UEKC_MASK		Unexpected Control Character Mask.	0x0	W
				1	If the unexpected control character count reaches ERRORTHRESH on any lane, $\overline{\text{IRQ}}$ is pulled low.		
		4	RESERVED		Reserved.	0x0	R
		3	INITIALLANESYNC _FLAG		Unexpected Control Character Error Count.	0x0	R
				1	Unexpected control character count reached ERRORTHRESH (Register 0x47C) on at least one lane. Read Register 0x46F to determine which lanes are in error.		
		3	INITIALLANESYNC _MASK		Initial Lane Sync Mask.	0x0	W
				1	If initial lane sync (Register 0x473) fails on any lane, $\overline{\text{IRQ}}$ is pulled low.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		2	BADCHECKSUM_MASK		Bad Checksum Mask.	0x0	W
				1	If there is a bad checksum (Register 0x472) on any lane, IRQ is pulled low.		
		2	BADCHECKSUM_FLAG		Bad Checksum Flag.	0x0	R
				1	Bad checksum on at least one lane. Read Register 0x472 to determine which lanes are in error.		
		1	RESERVED		Reserved.	0x0	R
		0	CODEGRPSYNC_FLAG	1	Code Group Sync Flag. Code group sync failed on at least one lane. Read Register 0x470 to determine which lanes are in error. Code group sync failed on at least one lane. Read Register 0x470 to determine which lanes are in error.	0x0	R
		0	CODEGRPSYNC_MASK	1	Code Group Sync Machine Mask. If code group sync (Register 0x470) fails on any lane, IRQ is pulled low.	0x0	W
0x47B	SYNCASSERTIONMASK	7	BADDIS_S		Bad Disparity Error on Sync.	0x0	R/W
				1	Asserts a sync request on SYNCOUTx± when the bad disparity character count reaches the threshold in Register 0x47C.		
		6	NIT_S		Not in table Error on Sync.	0x0	R/W
				1	Asserts a sync request on SYNCOUTx± when the not in table character count reaches the threshold in Register 0x47C.		
		5	UCC_S		Unexpected Control Character Error on Sync.	0x0	R/W
				1	Asserts a sync request on SYNCOUTx± when the unexpected control character count reaches the threshold in Register 0x47C.		
		4	CMM		Configuration Mismatch IRQ. If CMM_ENABLE is high, this bit latches on a rising edge and pull IRQ low. When latched, write a 1 to clear this bit. If CMM_ENABLE is low, this bit is non-functional.	0x0	R/W
				1	Link Lane 0 configuration registers (Register 0x450 to Register 0x45D) do not match the JESD204B transmit settings (Register 0x400 to Register 0x40D). Configuration Mismatch IRQ. If CMM_ENABLE is high, this bit latches on a rising edge and pull IRQ low. When latched, write a 1 to clear this bit. If CMM_ENABLE is low, this bit is non-functional.		
		3	CMM_ENABLE		Configuration Mismatch IRQ Enable.	0x1	R/W
				1	Enables IRQ generation if a configuration mismatch is detected.		
				0	Configuration mismatch IRQ disabled. Mismatch IRQ disabled.		
		[2:0]	RESERVED		Reserved.	0x0	R
0x47C	ERRORTHRES	[7:0]	ETH		Error Threshold. Bad disparity, not in table, and unexpected control character errors are counted and compared to the error threshold value. When the count reaches the threshold, either an IRQ is generated or the SYNCOUTx± signal is asserted per the mask register settings, or both. Function is performed in all lanes.	0xFF	R/W
0x47D	LANEENABLE	[7:0]	LANE_ENA		Lane Enable. Setting Bit x enables Link Lane x. This register must be programmed before receiving the code group pattern for proper operation.	0xF	R/W
0x47E	RAMP_ENA	[7:1]	RESERVED		Reserved.	0x0	R

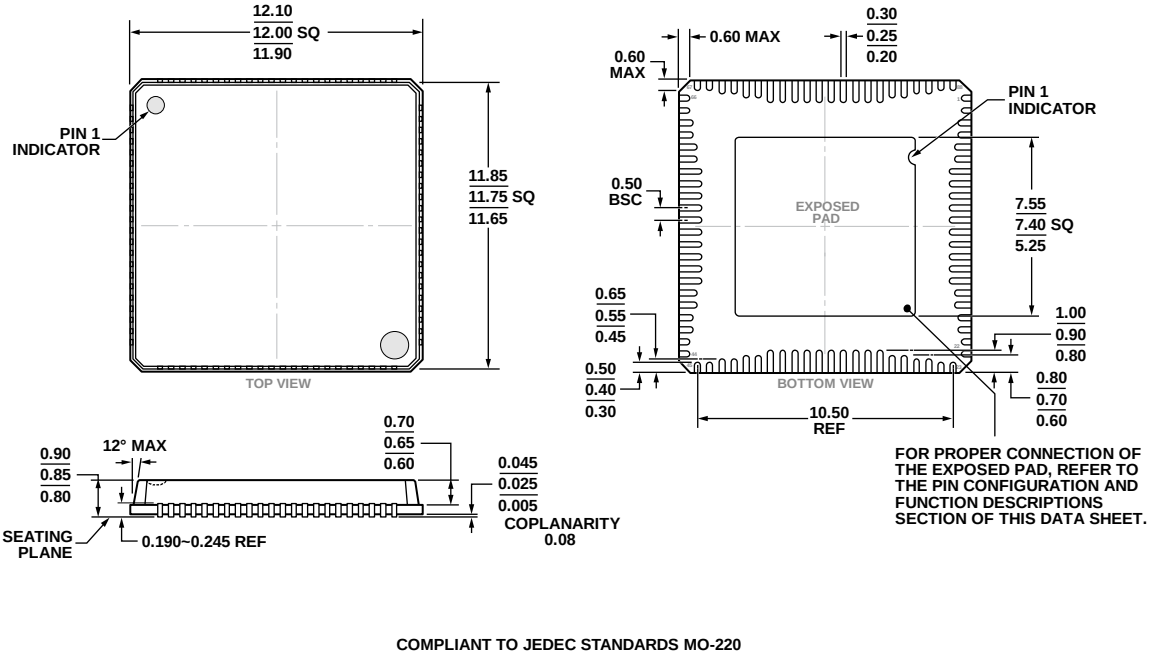
Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		0	ENA_RAMP_ CHECK		Enable Ramp Checking at the Beginning of ILAS.	0x0	R/W
				0	Disable ramp checking at beginning of ILAS; ILAS data need not be a ramp.		
				1	Enable ramp checking; ILAS data needs to be a ramp starting at 00-01-02; otherwise, the ramp ILAS fails and the device does not start up.		
0x520	DIG_TEST0	[7:2]	RESERVED		Reserved.	0x0	R
		1	DC_TEST_MOD		DC Test Mode Enable.	0x0	R/W
		0	RESERVED		Reserved.	0x0	R/W
0x521	TEST_DC_ VALUEI0	[7:0]	TEST_DC_ VALUEI0		DC value LSB of $f_S/8$ and decoder testing for I DAC.	0x0	R/W
0x522	TEST_DC_ VALUEI1	[7:0]	TEST_DC_ VALUEI1		DC value MSB of f_S /8 and decoder testing for I DAC.	0x0	R/W
0x523	TEST_DC_ VALUEQ0	[7:0]	TEST_DC_ VALUEQ0		DC value LSB of f_S /8 and decoder testing for Q DAC.	0x0	R/W
0x524	TEST_DC_ VALUEQ1	[7:0]	TEST_DC_ VALUEQ1		DC value MSB of f_S /8 and decoder testing for Q DAC.	0x0	R/W

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VRRD

Figure 89. 88-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
12 mm × 12 mm Body, Very Thin Quad
(CP-88-6)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220

Figure 90. 88-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
12 mm × 12 mm Body, Very Thin Quad
(CP-88-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9154BCPZ	−40°C to +85°C	88-Lead LFCSP_VQ	CP-88-6
AD9154BCPZRL	−40°C to +85°C	88-Lead LFCSP_VQ	CP-88-6
AD9154BCPAZ	−40°C to +85°C	88-Lead LFCSP_VQ (Variable Lead Length)	CP-88-9
AD9154BCPAZRL	−40°C to +85°C	88-Lead LFCSP_VQ (Variable Lead Length)	CP-88-9
AD9154-EBZ		DPG3 Evaluation Board	
AD9154-FMC-EBZ		FMC Evaluation Board	
AD9154-M6720-EBZ		DPG3 Evaluation Board with ADRF6720-27 Modulator	

[1] Z = RoHs Compliant Part.

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