STMicroelectronics

MB467
Airbag EVA Board

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User manual

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USER MANUAL

MB467
Airbag Eva Board

Introduction

The MB467 Airbag Eva Board is a complete demonstrator of an airbag system based on STMicroelectronics devices. The board implements a flexible and open design demonstrating the capability of the STMicroelectronics 16/32bit microcontrollers and safing devices for airbag applications.

The MB467 Airbag Eva Board mounts two safing devices with SQUIB drivers and satellite sensor interfaces L9654 and L9658 plus a safety power regulator L4998.

The board has opened connectivity to ST CPU boards, SQUIBs and to external power supply. A prototyping area allows users to do needed specific circuit.

Main components

- L9658, octal squib driver and quad sensor interface ASIC for safety application
- L9654, quad squib driver and dual sensor interface ASIC for safety application
- L4998, Safety Power Regulator
- Standardized CPU board connector providing access to off board I/O, PWM, SPI and power supply
- Connector for Squibs
- Connector for Satellites
- Connector for Hall Sensors

Features

- Support the ST30F7xx and ST10F3xx EVA boards
- Support for up to 6 satellites or 4 satellites and 2 Hall sensors, real or simulated
- Support for up to 12 Squibs, real or simulated
- Diagnostic testing and validation of safing functionality
  - SPI arming and deployment
  - Squibs and deployment drivers
  - Loss of ground and short circuit
  - Micro/satellites communication
- On board standard 100 mils prototyping area
- Main power supply 12V

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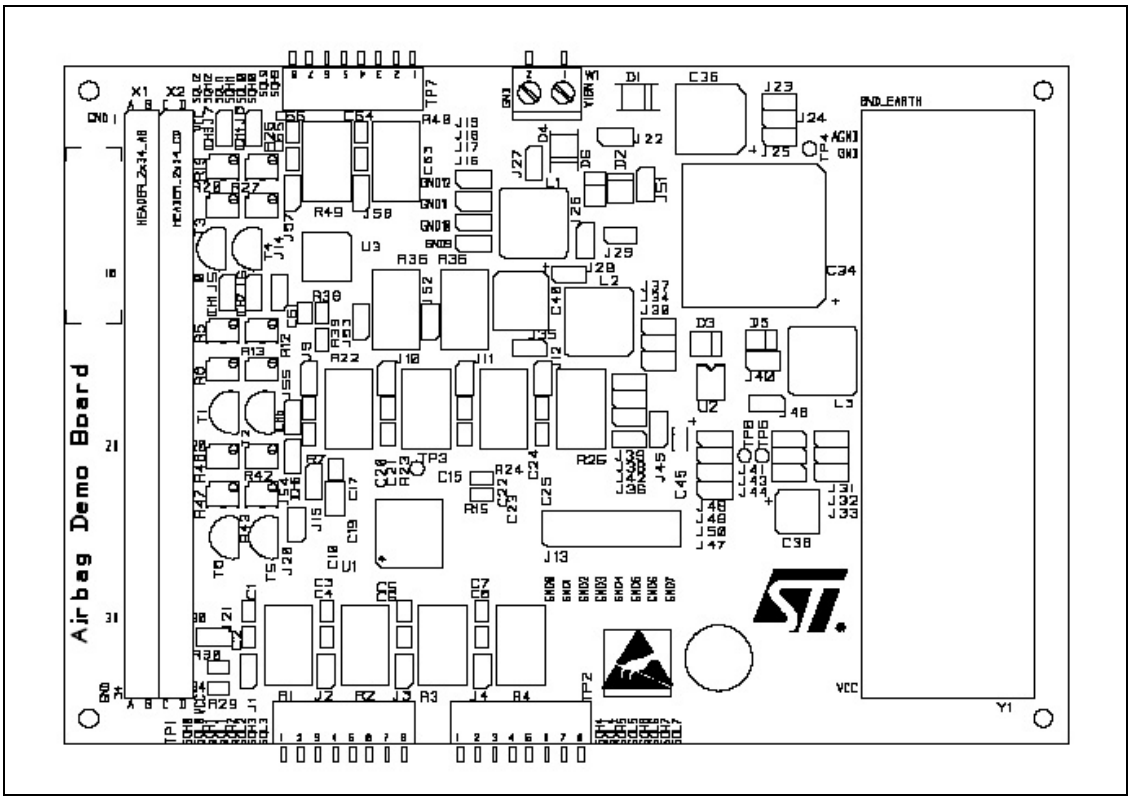
1 Introduction

The MB467 Airbag Eva Board is intended as a low cost development platform to demonstrate the capability of the L9658/L9654 safing and L4998 voltage regulator ASIC's. The board includes also a CPU board connector to interface with ST10/ST30 EVA board.

Main functionality includes deployment of airbags, switched-power sources to satellite sensors, diagnostic of sensing/deployment module and arming inputs.

Figure 1. The MB467 Airbag Eva Board



1.1 Features

General features of this board are:

- Complete airbag evaluation system
- Full compatibility with other microcontroller boards designed for the CPU board connector
- Full access to diagnostic functionality of the safing ASIC:
  - SPI arming and deployment
  - Squibs
  - Deployment drivers
  - Satellites communication

1.2 Devices

The MB467 Airbag Eva Board mounts the following devices:

- L9658 octal squib driver and quad sensor interface ASIC for safety application
  - 64-pin TQFP version
  - 8 deployment drivers
  - interface with 4 satellite sensors
  - support Manchester protocol for satellite sensors
  - supports for variable bit rate detection
  - SPI interface
  - Hall effect sensor support on satellite channels 3 and 4
- L9654 quad squib driver and dual sensor interface ASIC for safety application
  - 48-pin TQFP version
  - 4 deployment drivers
  - interface with 2 satellite sensor
  - support Manchester protocol for satellite sensor
  - supports for variable bit rate detection
  - SPI interface.
- L4998 Safety Power Regulator
  - boost regulator able of sourcing up to 90 mA
  - buck regulator operating in Continuous Conduction Mode able of sourcing up to 250mA output current
  - one 5.0 V linear regulator (Vcc) able of sourcing up to 200 mA output current
  - current limit and thermal shutdown protection

1.3 Board connections

The board provides the connections listed below:

- CPU board Connector to microcontroller I/O, PWM, SPI and power supply
- Connectors for 6 satellites or 4 satellites and 2 Hall sensors, real or simulated
- Connectors for 12 squibs, real or simulated
- On board standard 100 mils prototyping area
- Main power supply 12V

2 Before you start

This section describes operations needed before powering up the board.

Please, refer to *Chapter 4 on page 10* for detailed information on board configuration and jumper settings.

2.1 Jumper settings

For the location and (default) settings of the various jumpers, please refer as follows:

1. Close the jumper J51 to supply the board.
2. Close jumpers J48-J50 to supply V_{CC}.
3. Close jumpers J23-J25 to supply 35V V_{boost} to the board.
4. Close jumpers J31-J33, J40-J41 and J43-J44 to supply 8V V_{buck} to the board
5. Close the jumper J46 to supply a soft start function to SPR internal regulator (C_{slew}).
6. Close jumpers J22, J26-J30, J34-J35, J37-J39, J42 and J45. These jumpers are only for testing purpose and must always be closed.
7. Close the jumper J36 to pull up the $\overline{RST}$ signal at power on.
8. Close the jumper J14 to provide the clock signal to the Satellite/Deployment interface.
9. Connect satellites for L9658 to pin 1 of jumpers J5-J8. If you want to simulate them, close jumpers J5-J8 and provide the appropriate signals to the DICH1-DICH4 pins on the CPU board connector.
10. Connect satellites for L9654 to pin 1 of jumpers J54-J55. If you want to simulate them, close jumpers J54-J55 and provide the appropriate signals to the DICH5-DICH6 pins on the CPU board connector.
11. Close the jumper J15 to enable deployment on L9654.
12. Close the jumper J21 to enable deployment on L9658.
13. Close the jumper J20 to provide the clock signal to the Arming interface.
14. Close the jumpers J13, J16, J17, J18, J19 to enable the squibs.
15. Connect squibs to connectors TP1, TP2 and TP7. If you want to simulate squib loads instead of connecting them, close jumpers J1-J4, J9-J12, J52-J53 and J56-J57.

3 Using the board

3.1 How to exercise diagnostic functionality

3.1.1 Arming interface

Arming communication between micro and ASIC can be exercised by interrupting clock signal of the specific SPI. This can be done opening the jumper J20.

3.1.2 Squibs

This board support both real squibs or simulated loads. Real squib can be connected to TP1,TP2, TP7 plus the relative grounds J13, J16-J19. Loads can be simulated by closing jumpers J1-J4, J9-J12, J52-J53 and J56-J57.

3.1.3 Deployment drivers

The whole logic of the two ASIC can be exercised without firing the squib by keeping low the DEPEN signal of the relative ASIC. This can be done by opening the jumper J21 for L9658 or jumper J15 for L9654.

3.1.4 Satellites communications

Satellite and deployment communication between micro and ASIC can be exercised by interrupting clock signal of the specific SPI. This can be done opening the jumper J14.

4 Hardware

This chapter describes all the hardware modules of the board.

4.1 Overview

The MB467 Airbag Eva Board is a specific platform for airbag with SPI interface.

Figure 2. MB467 Airbag Eva Board layout block diagram

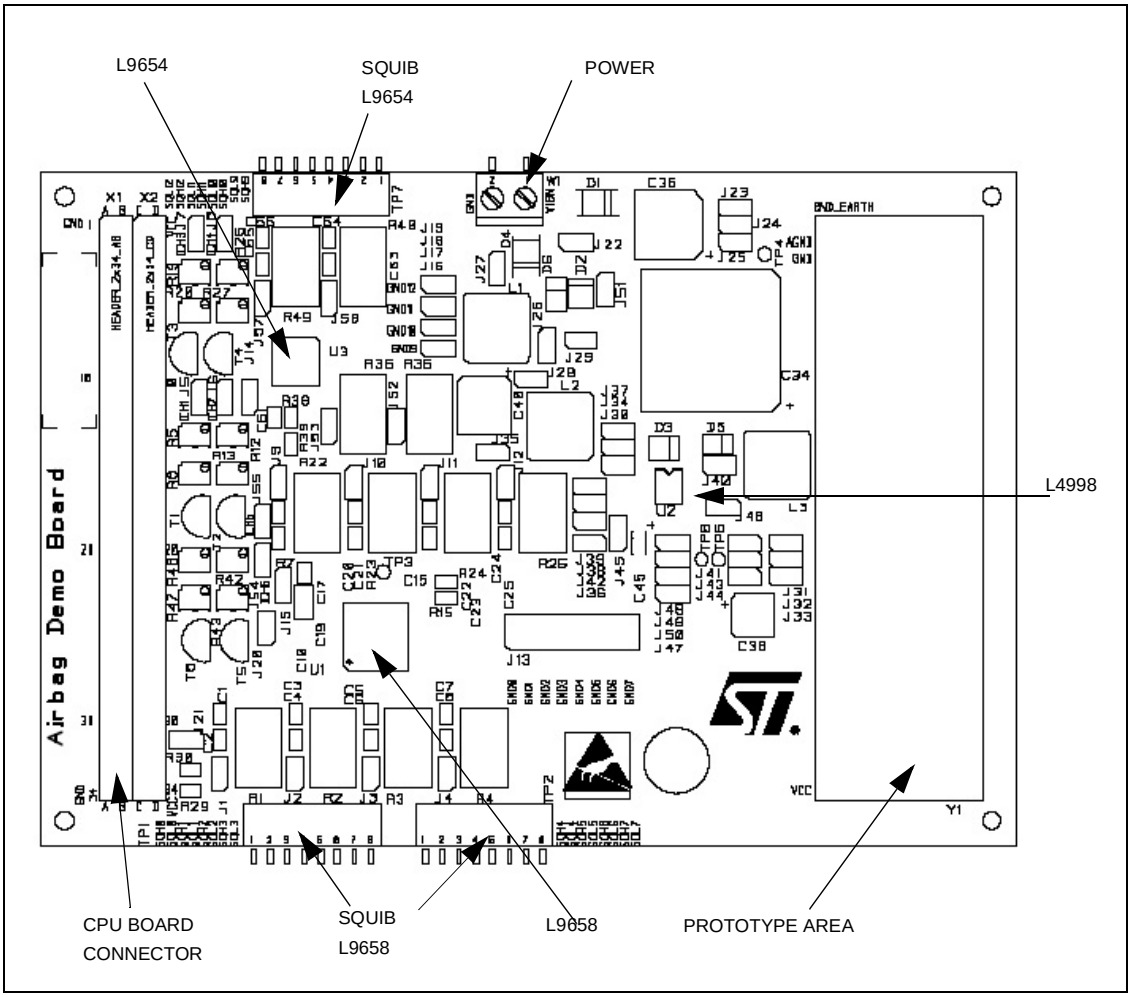
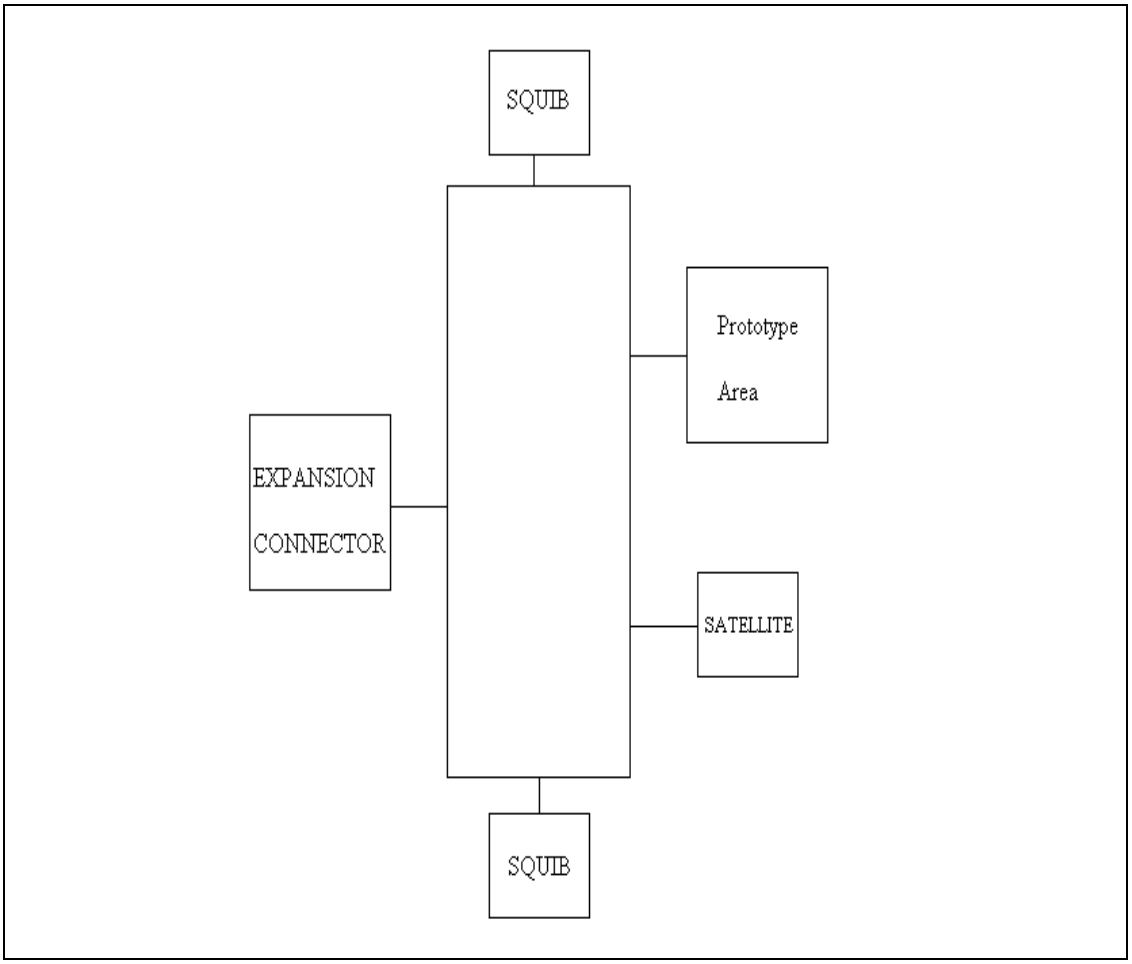


Figure 3. MB467 Airbag Eva Board system block diagram



4.2 L9658 octal squib driver and quad sensor interface ASIC

L9658 is intended to deploy up to 8 squibs and to interface up to 4 satellites. Two satellite interfaces can be used to interface Hall sensors. Squib drivers are sized to deploy 1.2A minimum for 2ms minimum during load dump and 1.75A minimum for 1ms minimum during load dump. Diagnostic of squib driver and squib resistance measurement is controlled by micro controller. Satellite interfaces support Manchester decoder with variable bit rate.

The main features set are described below:

- 8 deployment drivers sized to deliver 1.2A (min.) for 2ms (min.) and 1.75A(min) for 1ms(min).
- Independently controlled high-side and low-side MOS for diagnosis
- Analog output available for resistance
- Squib short to ground, short to battery and MOS diagnostic available on SPI register
- Capability to deploy the squib with 1.2A (min.) or 1.75A under 40V load-dump condition and the low side MOS is shorted to ground
- Capability to deploy the squib with 1.2A (min.) at 6.9V V_{RES} and 1.75A at 12V V_{RES}.
- Interface with 4 satellite sensors

- Programmable independent current trip points for each satellite channel
- Support Manchester protocol for satellite sensors
- Supports for variable bit rate detection
- Independent current limit and fault timer shutdown protection for each satellite output
- Short to ground and short to battery detection and reporting for each satellite channel
- 5.5MHz SPI interface
- Satellite message error detection
- Hall effect sensor support on satellite channels 3 and 4.
- Low voltage internal reset
- 2kV ESD capability on all pins
- Package: 64LD TQFP
- Technology: ST Proprietary BCD5 (0.65µm)

4.3 L9654 quad squib driver and dual sensor interface ASIC

L9654 is intended to deploy up to 4 squibs and to interface up to 2 satellites. Squib drivers are sized to deploy 1.2A minimum for 2ms minimum during load dump and 1.75A minimum for 1ms minimum during load dump. Diagnostic of squib driver and squib resistance measurement is controlled by micro controller. Satellite interfaces support Manchester decoder with variable bit rate.

The main features set are described below:

- 4 deployment drivers sized to deliver 1.2A (min.) for 2ms (min.) and 1.75A(min) for 1ms(min).
- Independently controlled high-side and low-side MOS for diagnosis
- Analog output available for resistance
- Squib short to ground, short to battery and MOS diagnostic available on SPI register
- Capability to deploy the squib with 1.2A (min.) or 1.75A under 40V load-dump condition and the low side MOS is shorted to ground
- Capability to deploy the squib with 1.2A (min.) at 6.9V V_{RES} and 1.75A at 12V V_{RES}.
- Interface with 2 satellite sensors
- Programmable independent current trip points for each satellite channel
- Support Manchester protocol for satellite sensors
- Supports for variable bit rate detection
- Independent current limit and fault timer shutdown protection for each satellite output
- Short to ground and short to battery detection and reporting for each satellite channel
- 5.5MHz SPI interface
- Satellite message error detection
- Low voltage internal reset
- 2kV ESD capability on all pins
- Package: 48LD TQFP
- Technology: ST Proprietary BCD5 (0.65µm)

4.4 L4998 Safety Power Regulator ASIC

The L4998 integrated circuit is intended for automotive applications.The main feature set is described below:

- Boost regulator able of sourcing up to 90mA output current
- Buck regulator operating in Continuous Conduction Mode able of sourcing up to 250 mA output current
- One 5.0V linear regulator (V_{CC}) able of sourcing up to 200mA output current
- Regulator soft-start control (C_{SLEW})
- Buck voltage out-of-regulation detection (BCKFLT)
- V_{CC} out-of-regulation detection with reset delay ($\overline{RST}$)
- Current-limit and thermal shutdown protection
- Package: PowerSSO14

4.5 Satellite/Sensor interface

The devices provide output current limited a 60 mA to drive up to six satellites or four satellites and two Hall sensors.
The L9658/L9654 will monitor the current flow from its output pin and “demodulate” the current to be decoded using Manchester protocol. Decoded satellite message is communicated to an external microprocessor via SPI.

4.5.1 Features

- Interface with 6 satellite sensors
- Programmable independent current trip points for each satellite channel
- Support Manchester protocol for satellite sensors
- Supports for variable bit rate detection
- Independent current limit and fault timer shutdown protection for each satellite output
- Short to ground and short to battery detection and reporting for each satellite channel
- 5.5MHz SPI interface
- Satellite message error detection
- Hall effect sensor support on satellite channels 3 and 4.

4.5.2 Functional description

Each output channel senses the current drawn by the remote satellite sensor; the circuit modulates the load current into logic voltage levels for post processing by a manchester decoder.

The L9658/L9654 decode satellite messages based on Manchester decoding, each of the six satellite channels have a Manchester decoder that can be enabled or disabled through a register.

Each output has a short circuit protection by independent current limit. When a short circuit occurs the output becomes current limited, a fault timer latch the output off and a fault condition bit is reported via SPI.That output returns to normal operation when it is re-enabled via SPI and

the current limit condition was removed, this fault condition does not interfere with the operation of any of the other output channels.

Channels 3 and 4 of the L9658 can by used to provide an analog feed back current as a 1/100th ratio of the sense current in this mode internal FIFO and decoder are bypassed. This will allow the IF3/V3 and IF4/V4 pins to be connected to a resistor to ground and provide an analog voltage equivalent to the sense current to be read by an A/D port. Otherwise the IF3/V3 and IF4/V4 pins can be configured as discrete output pins that provide logic level output voltage of the sensed current based on the internal current threshold set by the user through the CCR Register, which when used in conjunction with satellite sensors connected to channels 3 and 4 it can provide raw data out of the satellite message bypassing the internal decoder.

4.5.3 Satellite SPI interface

The board support up to 6 satellites (4 handled from L9658 and 2 from L9654).

The L9658/L9654 support two different communication protocols that are widely used by different automotive manufactures. One is based on the protocol used by Delphi satellite sensors and the other is a generic protocol that supports variable length messages based on BOSH, PAS3 and PAS4 protocols.

All decoded satellite messages are communicated to the external microcontroller via SPI. The MOSI input takes data from the master microprocessor while either CS_S1 (chip select of the L9658) or CS_S2 (chip select of the L9654) is asserted.The MISO reported the status of L9658/L9654 output channels. It is possible drive the two satellite interfaces (L9658/L9654) separately because there are two chip select, CS_S1 and CS_S2.

4.5.4 Board satellite functionality

Satellites can be connected directly to the ASIC's through pin 1 of jumpers J5-J8 and J54-J55.

Table 1. Satellite connector

Name	Figure	Description
J5 pin 1	*Figure 4*	L9658 satellite channel 1 (ICH1)
J6 pin 1	*Figure 4*	L9658 satellite channel 2 (ICH2)
J7 pin 1	*Figure 4*	L9658 satellite/sensor channel 3 (ICH3)
J8 pin 1	*Figure 4*	L9658 satellite/sensor channel 4 (ICH4)
J54 pin 1	*Figure 4*	L9654 satellite channel 1 (ICH1)
J55 pin 1	*Figure 4*	L9654 satellite channel 2 (ICH2)

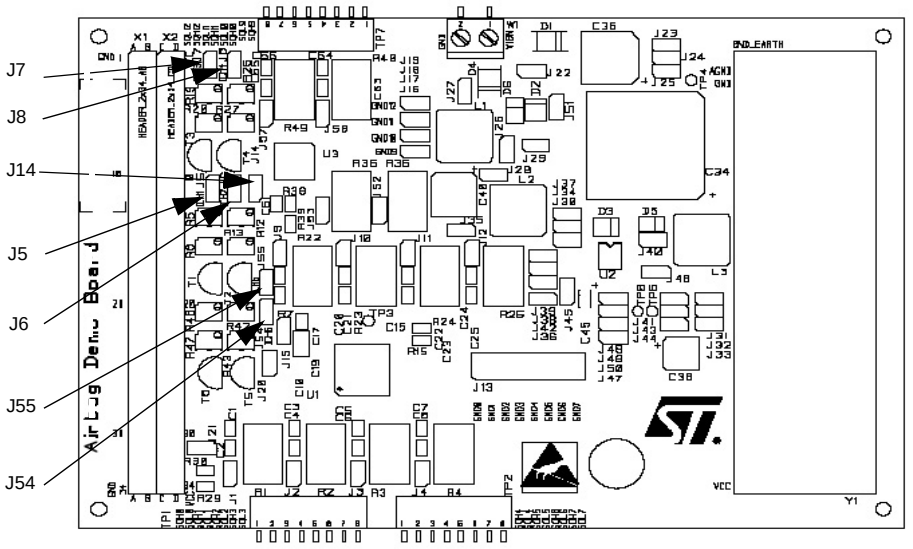
Diagnostic functionality of satellite communication can be tested using jumper J14. Opening this jumper interrupts the SCLK signal of the SPI used for satellite and deployment thus blocking any communication between the micro and the ASIC.

It is possible to simulate satellite signals by closing jumpers J5-J8 and J54-J55 and providing the appropriate signal to pins DICH1-DICH6 on the CPU board connector. You must drive the base of the BJT with a particular signal in order to generate the correct word to decode with manchester decoding and then to transmit via SPI. This dynamic digital signal shall be generated by using 2 PWM outputs provide on ST30F7xx board (or an ST10F27x board). This signal will be sent into the base of the BJT's to simulate the local acceleration values.

Table 2. Satellite jumpers

Name	Figure	Description
J14	*Figure 4*	Interrupt SPI communication for Satellite and Deployment
J5	*Figure 4*	Enable load simulation for L9658 satellite channel 1 through DICH1
J6	*Figure 4*	Enable load simulation for L9658 satellite channel 2 through DICH2
J7	*Figure 4*	Enable load simulation for L9658 satellite/sensor channel 3 through DICH3
J8	*Figure 4*	Enable load simulation for L9658 satellite/sensor channel 4 through DICH4
J54	*Figure 4*	Enable load simulation for L9654 satellite channel 1 through DICH5
J55	*Figure 4*	Enable load simulation for L9654 satellite channel 2 through DICH6

Figure 4. Satellite jumpers location



4.6 Arming interface

The arming interface is used as a fail-safe to prevent inadvertent airbag deployment. Along with deployment command, these signals provide redundancy. Pulse stretch timer is provided for each channel/loop. Either ARM signal or deployment command shall start the pulse stretch timer.

Arming interface has a dedicated 8-bit SPI interface. The devices can deploy a channel, only when the deployment enable is asserted and any of the following conditions are satisfied:

- the respective deployment command is sent during a valid pulse stretch timer, which initiated by ARM signal
- the respective SPI ARM command is sent during a valid pulse stretch timer, which initiate by deployment command.

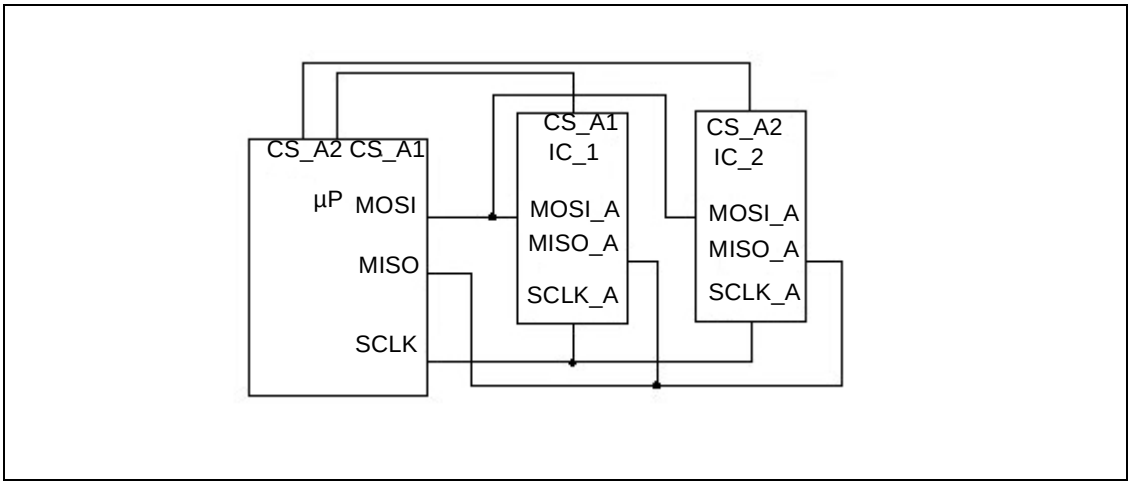
There are on board two different deployment enables for L9658 and L9654. When these pins are asserted, L9658/L9654 are able to turn on its high (SQH) and low side (SQL) drivers upon receiving a valid deployment command or a MOS diagnostic request. When a deployment is initiated, it cant be terminated, except during a reset event.

4.6.1 Arming SPI interface

L9654 and L9658 arming commands are based on 8bit SPI messages.

In a real airbag system, all the devices should be daisy-chained. Here, as this board has been designed for training purposes for each ASIC, ASIC's are connected on the same SPI and selected with different chip selects CS_A1 and CS_A2. You find the chips select on the CPU board connector at the position D30 and C27.

Figure 5. SPI configuration on Arming for eva board



The above figure is representing the SPI configuration for the system evaluation board where ASIC's are sharing a common SPI.

Diagnostic functionality of the arming interface can be tested using jumper J20. Opening this jumper interrupts the SCLK_A signal of the SPI used for arming thus blocking any communication between the micro and the ASIC.

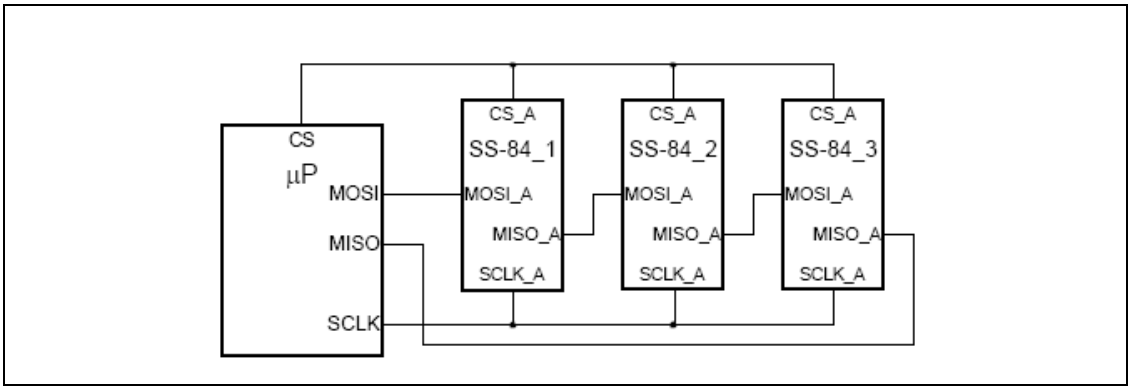
Table 3. Arming interface jumpers

Name	Figure	Description
J20	*Figure 7*	Interrupt SPI communication for Arming

Daisy chain configuration

Arming SPI interface shall support a daisy-chain configuration. In this configuration, the processor can send arming commands to multiple L9658 devices without having to use additional pins. The functioning is underline in the following figure:

Figure 6. Arming SPI daisy-chain configuration



In order to obtained daisy-chain configuration it's enough to connect the MOSI from microprocessor to MOSI_A of the ASIC, MISO_A to MOSI_A in fall and MOSI_A to the MISO of the microprocessor.

4.6.2 ASIC diagnostic functionality

Diagnostic on the L9658 can be performed by disabling deployment through the signal DEPEN. This signal is mapped to pin DEPEN1 of CPU board connector. DEPEN1 can also be manually forced low by opening the jumper J21.

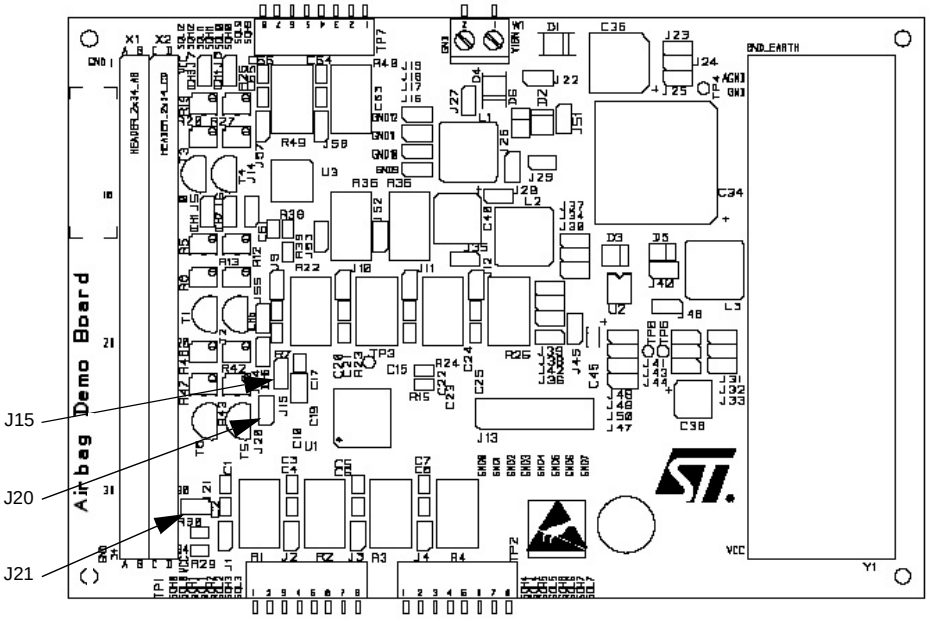
Diagnostic on the L9654 can be performed by disabling deployment through the signal DEPEN. This signal is mapped to pin DEPEN2 of CPU Board connector. DEPEN2 can also be manually forced low by opening the jumper J15.

L9658/L9654 are able to perform a short to battery, a short to ground, a resistance measurement and a MOS diagnostics on their deployment drivers. A short to ground and an open circuit conditions are distinguished using a resistance measurement. The diagnostic is performed when a valid SPI command is received.

Table 4. Deployment Enable jumpers

Name	Figure	Description
J21	*Figure 7*	Deployment enable for L9658
J15	*Figure 7*	Deployment enable for L9654

Figure 7. Arming jumpers location



4.7 Squib and deployment drivers

The on-chip deployment drivers are designed to deliver 1.2A (min.) at 6.9V VRES. Deployment current is be 1.2A (min.) for 2ms (min.). The high side driver can survives deployment with 1.47A, 40V at VRES and SQL is shorted to ground for 2.5ms. Minimum load resistance is 1.7 Ohm. At the end of a deployment, a deploy success flag is asserted via SPI. Each VRES and GND connection are used to accommodate 8 loops that can be deployed simultaneously. Upon receiving a valid deployment condition, the respective SQH and SQL drivers are turned on. SQH and SQL drivers are also turned on momentarily during a MOS diagnostic. Otherwise, SQH and SQL are inactive under any normal, fault, or transient conditions. Upon a successful deployment of the respective SQH and SQL drivers, a deploy command success flag is asserted via SPI.

4.7.1 Features

- 8 deployment drivers sized to deliver 1.2A (min.) for 2ms (min.) and 1.75A (min.) for 1ms (min.).
- Independently controlled high-side and low-side MOS for diagnosis.
- Analog output available for resistance.
- Squib short to ground, short to battery and MOS diagnostic available on SPI register.
- Capability to deploy the squib with 1.2A (min.) or 1.75A under 40V load-dump condition and the low side MOS is shorted to ground.
- Capability to deploy the squib with 1.2A (min.) at 6.9V VRES and 1.75A at 12V VRES.

4.7.2 Functional description

The Airbag Eva Board supports up to 12 squibs.

Upon receiving a valid deployment condition, the respective SQH and SQL drivers are turned on. SQH and SQL drivers are also turned on momentarily during a MOS diagnostic. Otherwise, SQH and SQL are inactive under any normal, fault, or transient conditions. Upon a successful deployment of the respective SQH and SQL drivers, a deploy command success flag is asserted via SPI. Only a valid deployment condition can turn on the respective SQH and SQL drivers.

4.7.3 Board functionality

Squib can be connected directly to the ASIC's through TP1, TP2 and TP7.

A loss of ground can be simulated by opening one of the jumpers insert in J13, J16, J17, J18, J19.When any of the grounds (GND0 – 7, GND9 - 12) are lost, no deployment can occur to the respective deployment channels. A loss of ground condition on one or several channels will not affect the operation of the remaining channels.

When a loss of ground condition occurs, the source of the low side MOS will be floating. In this case, no current will flow through the low side driver. This condition will be detected as a fault by a low side MOS diagnostic.

Table 5. Squib connectors

Name	Figure	Description
SQH0	*Figure 8*	High Side Driver Output for Channel 0 for L9658
SQH1	*Figure 8*	High Side Driver Output for Channel 1 for L9658
SQH2	*Figure 8*	High Side Driver Output for Channel 2 for L9658
SQH3	*Figure 8*	High Side Driver Output for Channel 3 for L9658
SQH4	*Figure 8*	High Side Driver Output for Channel 4 for L9658
SQH5	*Figure 8*	High Side Driver Output for Channel 5 for L9658
SQH6	*Figure 8*	High Side Driver Output for Channel 6 for L9658
SQH7	*Figure 8*	High Side Driver Output for Channel 7 for L9658
SQH9	*Figure 8*	High Side Driver Output for Channel 0 for L9654
SQH10	*Figure 8*	High Side Driver Output for Channel 1 for L9654
SQH11	*Figure 8*	High Side Driver Output for Channel 2 for L9654
SQH12	*Figure 8*	High Side Driver Output for Channel 3 for L9654
SQL0	*Figure 8*	Low Side Driver Output for Channel 0 for L9658
SQL1	*Figure 8*	Low Side Driver Output for Channel 1 for L9658
SQL2	*Figure 8*	Low Side Driver Output for Channel 2 for L9658
SQL3	*Figure 8*	Low Side Driver Output for Channel 3 for L9658
SQL4	*Figure 8*	Low Side Driver Output for Channel 4 for L9658
SQL5	*Figure 8*	Low Side Driver Output for Channel 5 for L9658
SQL6	*Figure 8*	Low Side Driver Output for Channel 6 for L9658

Name	Figure	Description
SQL7	*Figure 8*	Low Side Driver Output for Channel 7 for L9658
SQL9	*Figure 8*	Low Side Driver Output for Channel 0 for L9654
SQL10	*Figure 8*	Low Side Driver Output for Channel 1 for L9654
SQL11	*Figure 8*	Low Side Driver Output for Channel 2 for L9654
SQL12	*Figure 8*	Low Side Driver Output for Channel 3 for L9654
GND0	*Figure 8*	Power Ground for Loop Channel 0 for L9658
GND1	*Figure 8*	Power Ground for Loop Channel 1 for L9658
GND2	*Figure 8*	Power Ground for Loop Channel 2 for L9658
GND3	*Figure 8*	Power Ground for Loop Channel 3 for L9658
GND4	*Figure 8*	Power Ground for Loop Channel 4 for L9658
GND5	*Figure 8*	Power Ground for Loop Channel 5 for L9658
GND6	*Figure 8*	Power Ground for Loop Channel 6 for L9658
GND7	*Figure 8*	Power Ground for Loop Channel 7 for L9658
GND9	*Figure 8*	Power Ground for Loop Channel 0 for L9654
GND10	*Figure 8*	Power Ground for Loop Channel 1 for L9654
GND11	*Figure 8*	Power Ground for Loop Channel 2 for L9654
GND12	*Figure 8*	Power Ground for Loop Channel 3 for L9654

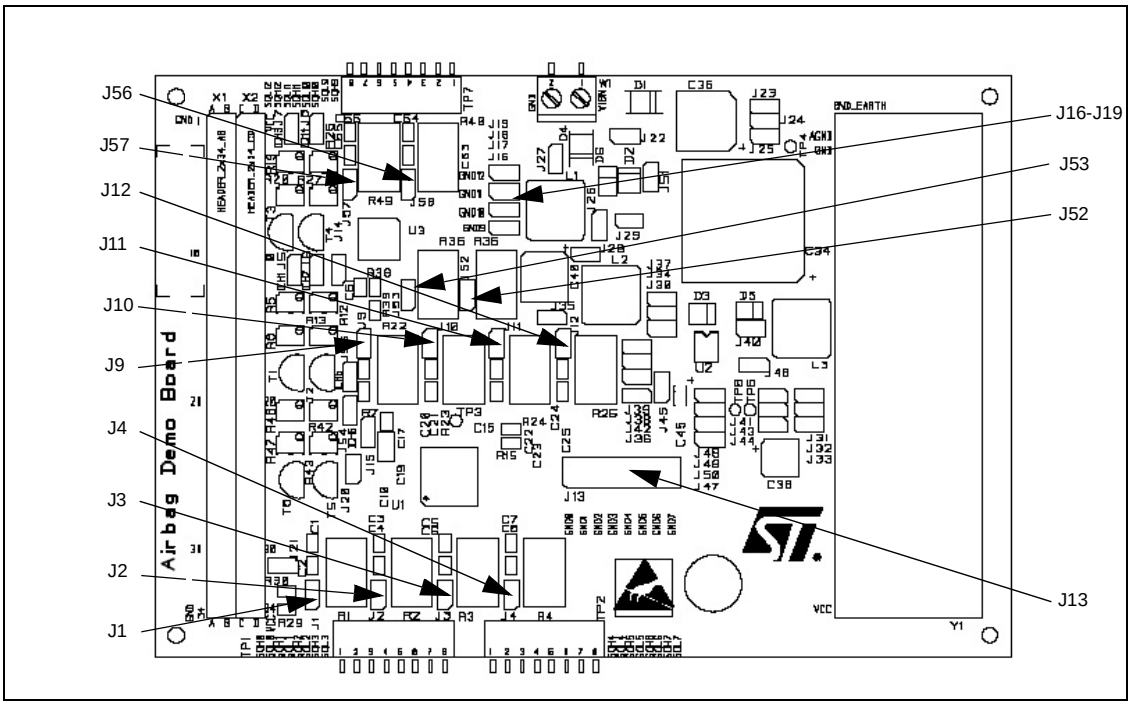
If no squibs are connected to the board, it is possible to simulate squib loads by closing the jumpers J1-J4, J9-J12 and J52-J53 and J56-J57.

Table 6. Squib dummy loads

Name	Figure	Description
J1	*Figure 8*	Driver Output for Channel 0 for L9658
J2	*Figure 8*	Driver Output for Channel 1 for L9658
J3	*Figure 8*	Driver Output for Channel 2 for L9658
J4	*Figure 8*	Driver Output for Channel 3 for L9658
J9	*Figure 8*	Driver Output for Channel 4 for L9658
J10	*Figure 8*	Driver Output for Channel 5 for L9658
J11	*Figure 8*	Driver Output for Channel 6 for L9658
J12	*Figure 8*	Driver Output for Channel 7 for L9658
J52	*Figure 8*	Driver Output for Channel 0 for L9654
J53	*Figure 8*	Driver Output for Channel 1 for L9654
J56	*Figure 8*	Driver Output for Channel 2 for L9654
J57	*Figure 8*	Driver Output for Channel 3 for L9654
J13	*Figure 8*	Power Ground for Loop Channel 0 - Channel 7 for L9658

Name	Figure	Description
J16	*Figure 8*	Power Ground for Loop Channel 0 for L9654
J17	*Figure 8*	Power Ground for Loop Channel 1 for L9654
J18	*Figure 8*	Power Ground for Loop Channel 2 for L9654
J19	*Figure 8*	Power Ground for Loop Channel 3 for L9654

Figure 8. Squib jumpers location



4.8 Power supply

The MB467 Airbag Eva Board is supplied using an external 12V supply.

All other required voltages (5V, 8V and 35V) are provided by the on-board Power Regulator. A connected microcontroller board can also be supplied via the V_{CC} pins available on the CPU board connector (5V, 200mA).

Power supply can be interrupted by opening jumper J51.

The 5V supply to L9654/L9658 and CPU board connector can be interrupted by opening jumpers J48-J50.

The 35V V_{boost} supply generated by the SPR to the board can be interrupted by opening jumpers J23, J24 and J25.

The 8V V_{buck} supply to L9654/9658 for satellite communications can be interrupted by opening jumpers J31-J33, J40-J41 and J43-J44.

A soft start function (C_{slew}) of V_{CC} linear regulator can be obtained by closing jumper J46. Closing J46 connect an external capacitor to the C_{slew} pin of the SPR producing a linear voltage ramp at the start-up. The SPR uses this linear voltage to limit the slew rate of the output.

Table 7. Power supply jumpers

Name	Figure	Description
J46	*Figure 9*	Soft start function (C_{slew})
J51	*Figure 9*	Power supply switch
J48-J50	*Figure 9*	V_{CC} partitioning
J23-J25	*Figure 9*	V_{boost} partitioning
J31-J33, J40-J41, J43-J44	*Figure 9*	V_{buck} partitioning

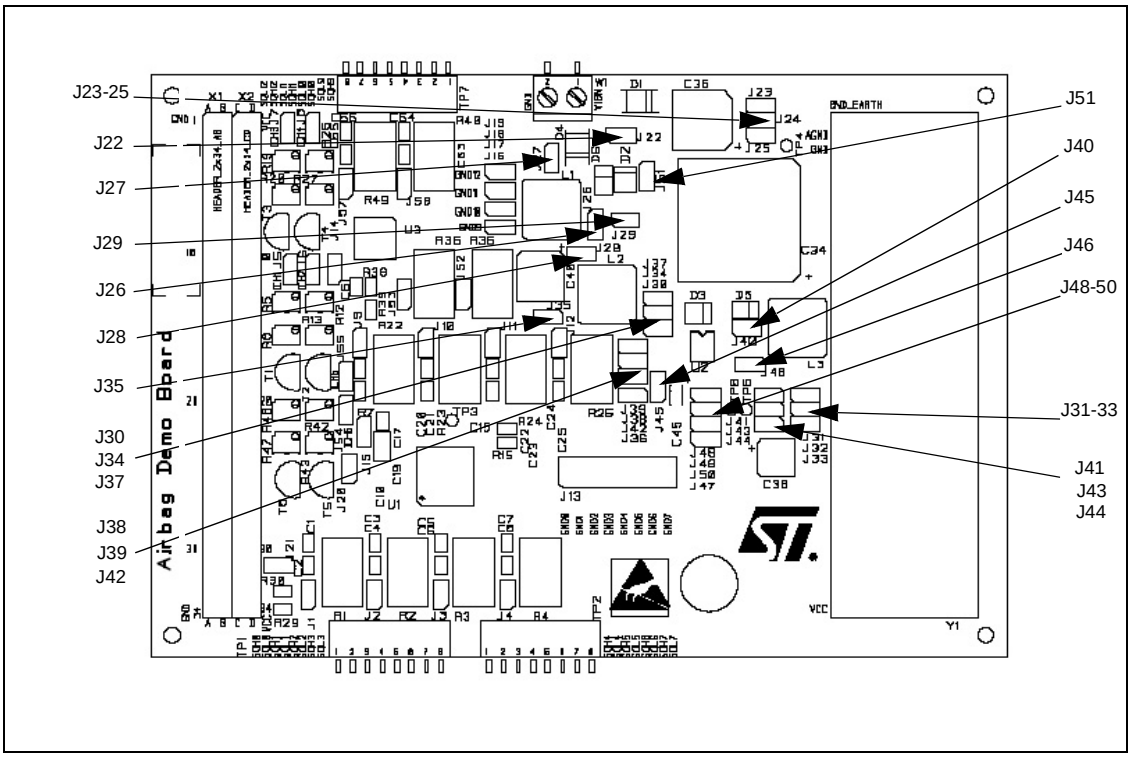
The following jumpers are available for testing purposes and must be closed:

- Power supply can be partitioned at different points by opening jumpers J22, J26-J29, J30, J34, J35, J37-J39 and J42.
- IREF signal to the SPR can be interrupted by opening jumper J45.

Table 8. Power supply jumpers (testing only)

Name	Figure	Description
J22, J26-J30, J34-J35, J37-J39, J42	*Figure 9*	V_{boost} partitioning for testing
J45	*Figure 9*	IREF partitioning

Figure 9. Power supply jumpers location



4.9 Reset

Power on reset is driven by the L4998 Safety Power Regulator (SPR). The SPR provides an output ($\overline{RST}$) to indicate the regulation status of VCC. The $\overline{RST}$ output is asserted low whenever VCC falls below its low voltage threshold or VCC rises above its over-voltage threshold.

The $\overline{RST}$ signal is connected to the $\overline{RESETB}$ pin of the two safing ASIC's and to the $\overline{RESETIN}$ pin of the CPU Board Connector. When this signal is asserted low, all components in the board and any connected microcontroller board will be reset.

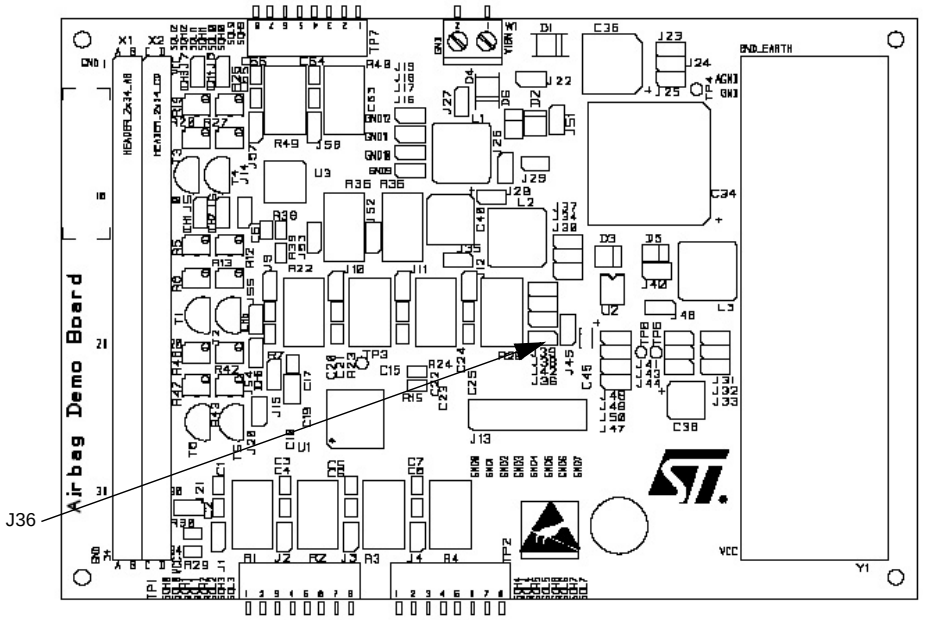
Please, note that during a deployment, the L9658/L9654 ignores but latches internally the reset signal. Only after the deployment is complete, the reset signal is asserted, any output operation interrupted and the ASIC internal registers reset to their default state.

$\overline{RESETB}$ signal of the two ASIC can be forced high (pull up), regardless of the $\overline{RST}$ signal coming from the SPR, through jumper J36.

Table 9. Reset jumper

Name	Figure	Description
J36	*Figure 10*	Force pull up of the $\overline{RESETB}$ signal

Figure 10. Reset jumper



4.10 CPU Board connector

The CPU board Connector allows interfacing this board to a ST30F7xx/ST10F3xx Eva Boards. Signals provided on the connector are listed in *Table 10. on page 24*.

Table 10. CPU Board connector pinout

Column	Row	Name	Description
A	12	$\overline{\text{RESETB}}$	Reset
A	16	MOSI	Satellite/Deployment: Data in
A	18	DICH3	Channel 3 Satellite/Sensor input simulation for L9658
A	22	DEPEN2	Deployment enable input for L9654
A	23	DICH5	Channel 1 Satellite input simulation for L9654
A	25	CS_S1	Chip select for Satellite Interface of L9658
A	26	IF3	Current Feedback for channel 3 Raw or Data output for channel 3 of the L9658
A	27	AOUT	Analog output for loop diagnostic for L9658
B	15	SCLK	Satellite/Deployment SPI: Clock
B	16	MISO	Satellite/Deployment SPI: Data Output
B	18	DICH4	Channel 4 Satellite/Sensor input simulation for L9658
B	23	DICH6	Channel 2 Satellite input simulation for L9654

Table 10. CPU Board connector pinout

Column	Row	Name	Description
B	25	CS_D1	Chip select for Deployment Driver of L9658
B	26	IF4	Current Feedback for channel 4 Raw or Data output for channel 4 of the L9658
B	27	AOUT2	Analog output for loop diagnostic for L9654
C	19	DICH1	Channel 1 Satellite input simulation for L9658
C	26	MOSI_A	Arming SPI: Data In
C	27	CS_A2	Chip select for Arming Interface of L9654
C	29	CS_D2	Chip select for Deployment Driver of L9654
C	30	DEPEN1	Deployment enable input for L9658
D	17	MSG2	Message waiting for L9654
D	18	BCKFLT	Buck fault output
D	19	DICH2	Channel 2 Satellite input simulation for L9658
D	25	SCLK_A	Arming SPI: Clock
D	26	MISO_A	Arming SPI: Data Out
D	27	CS_S2	Chip select for Satellite Interface of L9654
D	29	MSG	Message waiting for L9658
D	30	CS_A1	Chip select for Arming Interface of L9658

4.11 Prototyping area

A standard 100mils prototyping area is available for user's application.

4.12 Jumpers summary

Table 11. summarizes jumpers available on the MB467 Airbag Eva Board.

Table 11. Jumpers summary

Jumper	Name	Figure	Description
J1	SQUIB	*Figure 8*	Driver Output for Channel 0 for L9658
J2	SQUIB	*Figure 8*	Driver Output for Channel 1 for L9658
J3	SQUIB	*Figure 8*	Driver Output for Channel 2 for L9658
J4	SQUIB	*Figure 8*	Driver Output for Channel 3 for L9658
J5	SATELLITE	*Figure 4*	L9658 satellite channel 1: Open: real satellite (ICH1 on J5 pin 1) Closed: simulated satellite (load driven by DICH1)

Jumper	Name	Figure	Description
J6	SATELLITE	*Figure 4*	L9658 satellite channel 2: Open: real satellite (ICH2 on J6 pin 1) Closed: simulated satellite (load driven by DICH2)
J7	SATELLITE	*Figure 4*	L9658 satellite channel 3: Open: real satellite (ICH3 on J7 pin 1) Closed: simulated satellite (load driven by DICH3)
J8	SATELLITE	*Figure 4*	L9658 satellite channel 4: Open: real satellite (ICH4 on J8 pin 1) Closed: simulated satellite (load driven by DICH4)
J9	SQUIB	*Figure 8*	Driver Output for Channel 4 for L9658
J10	SQUIB	*Figure 8*	Driver Output for Channel 5 for L9658
J11	SQUIB	*Figure 8*	Driver Output for Channel 6 for L9658
J12	SQUIB	*Figure 8*	Driver Output for Channel 7 for L9658
J13	GND0-GND7	*Figure 8*	Power Ground for Loop Channel 0 - Channel 7 for L9658
J14	SCLK	*Figure 4*	Interrupt SPI communication for Satellite and Deployment
J15	DEPEN2	*Figure 7*	Deployment enable for L9654
J16	GND9	*Figure 8*	Power Ground for Loop Channel 0 for L9654
J17	GND10	*Figure 8*	Power Ground for Loop Channel 1 for L9654
J18	GND11	*Figure 8*	Power Ground for Loop Channel 2 for L9654
J19	GND12	*Figure 8*	Power Ground for Loop Channel 3 for L9654
J20	SCLK_A	*Figure 7*	Interrupt SPI communication for Arming
J21	DEPEN1	*Figure 7*	Deployment enable for L9658
J22	V_{boost}	*Figure 9*	V_{boost} partitioning for testing
J23-J25	V_{boost}	*Figure 9*	V_{boost} partitioning
J26-J30	V_{boost}	*Figure 9*	V_{boost} partitioning for testing
J31	V_{buck}	*Figure 9*	V_{buck} partitioning
J32	V_{buck}	*Figure 9*	V_{buck} partitioning
J33	V_{buck}	*Figure 9*	V_{buck} partitioning
J34-J35	V_{boost}	*Figure 9*	V_{boost} partitioning for testing
J36	$\overline{\text{RESETB}}$	*Figure 10*	Force pull up of the $\overline{\text{RESETB}}$ signal.
J37-J39	V_{boost}	*Figure 9*	V_{boost} partitioning for testing
J40	V_{buck}	*Figure 9*	V_{buck} partitioning
J41	V_{buck}	*Figure 9*	V_{buck} partitioning
J42	V_{boost}	*Figure 9*	V_{boost} partitioning for testing
J43	V_{buck}	*Figure 9*	V_{buck} partitioning
J44	V_{buck}	*Figure 9*	V_{buck} partitioning

Jumper	Name	Figure	Description
J45	IREF	*Figure 9*	IREF partitioning
J46	C_{SLEW}	*Figure 9*	Soft start function (C_{slew})
J48	Vcc	*Figure 9*	V_{CC} partitioning
J49	Vcc	*Figure 9*	V_{CC} partitioning
J50	Vcc	*Figure 9*	V_{CC} partitioning
J51	VIGN	*Figure 9*	Power supply switch
J52	SQUIB	*Figure 8*	Driver Output for Channel 0 for L9654
J53	SQUIB	*Figure 8*	Driver Output for Channel 1 for L9654
J54	SATELLITE	*Figure 4*	L9654 satellite channel 1: Open: real satellite (ICH5 on J54 pin 1) Closed: simulated satellite (load driven by DICH5)
J55	SATELLITE	*Figure 4*	L9654 satellite channel 2: Open: real satellite (ICH6 on J55 pin 1) Closed: simulated satellite (load driven by DICH6)
J56	SQUIB	*Figure 8*	Driver Output for Channel 3 for L9654
J57	SQUIB	*Figure 8*	Driver Output for Channel 4 for L9654

4.13 Connectors summary

Table 12. summarizes connectors available on the MB467 Airbag Eva Board.

Table 12. Connectors summary

Name	Figure	Description
SQH0	*Figure 8*	High Side Driver Output for Channel 0 for L9658
SQH1	*Figure 8*	High Side Driver Output for Channel 1 for L9658
SQH2	*Figure 8*	High Side Driver Output for Channel 2 for L9658
SQH3	*Figure 8*	High Side Driver Output for Channel 3 for L9658
SQH4	*Figure 8*	High Side Driver Output for Channel 4 for L9658
SQH5	*Figure 8*	High Side Driver Output for Channel 5 for L9658
SQH6	*Figure 8*	High Side Driver Output for Channel 6 for L9658
SQH7	*Figure 8*	High Side Driver Output for Channel 7 for L9658
SQH9	*Figure 8*	High Side Driver Output for Channel 0 for L9654
SQH10	*Figure 8*	High Side Driver Output for Channel 1 for L9654
SQH11	*Figure 8*	High Side Driver Output for Channel 2 for L9654
SQH12	*Figure 8*	High Side Driver Output for Channel 3 for L9654
SQL0	*Figure 8*	Low Side Driver Output for Channel 0 for L9658
SQL1	*Figure 8*	Low Side Driver Output for Channel 1 for L9658
SQL2	*Figure 8*	Low Side Driver Output for Channel 2 for L9658
SQL3	*Figure 8*	Low Side Driver Output for Channel 3 for L9658
SQL4	*Figure 8*	Low Side Driver Output for Channel 4 for L9658
SQL5	*Figure 8*	Low Side Driver Output for Channel 5 for L9658
SQL6	*Figure 8*	Low Side Driver Output for Channel 6 for L9658
SQL7	*Figure 8*	Low Side Driver Output for Channel 7 for L9658
SQL9	*Figure 8*	Low Side Driver Output for Channel 0 for L9654
SQL10	*Figure 8*	Low Side Driver Output for Channel 1 for L9654
SQL11	*Figure 8*	Low Side Driver Output for Channel 2 for L9654
SQL12	*Figure 8*	Low Side Driver Output for Channel 3 for L9654
GND0	*Figure 8*	Power Ground for Loop Channel 0 for L9658
GND1	*Figure 8*	Power Ground for Loop Channel 1 for L9658
GND2	*Figure 8*	Power Ground for Loop Channel 2 for L9658
GND3	*Figure 8*	Power Ground for Loop Channel 3 for L9658
GND4	*Figure 8*	Power Ground for Loop Channel 4 for L9658
GND5	*Figure 8*	Power Ground for Loop Channel 5 for L9658
GND6	*Figure 8*	Power Ground for Loop Channel 6 for L9658
GND7	*Figure 8*	Power Ground for Loop Channel 7 for L9658

Name	Figure	Description
GND9	*Figure 8*	Power Ground for Loop Channel 0 for L9654
GND10	*Figure 8*	Power Ground for Loop Channel 1 for L9654
GND11	*Figure 8*	Power Ground for Loop Channel 2 for L9654
GND12	*Figure 8*	Power Ground for Loop Channel 3 for L9654

5 Revision history

Date	Revision	Changes
18-Oct-2005	1	Initial release.

Appendix A Bill of materials

Table 13. Bill of materials

Item	Reference	Part
1	C1,C2,C3,C4,C5,C6,C7,C8,C11,C13,C17,C19,C20,C21,C22,C23,C24,C25,C26,C27,C28,C29,C30,C31,C32,C33,C44,C51,C54,C55,C56,C57,C59,C61,C63,C64,C65,C66,C67,C68,C69,C70	100nF
2	C9,C12,C14,C15,C16,C18,C60,C62	10pF
3	C10,C58	330pF
4	C34	3000 MF
5	C35,C39,C42,C43,C48	100nF
6	C36	100MF
7	C37	10MF
8	C38	220MF
9	C40	47MF
10	C41	4.7MF
11	C45	1MF
12	C46	220nF
13	C47	1nF
14	C49	470nF
15	C50	10nF
16	C52,C53	470pF
17	D1,D4	S2B
18	D2	SMBJ24A-TR
19	D3	MBRS1100T3
20	D5	ES1B
21	D6	SMAJ13A-TR
22	J1,J2,J3,J4,J5,J6,J7,J8,J9,J10,J11,J12,J14,J15,J16,J17,J18,J19,J20,J21,J22,J23,J24,J25,J26,J27,J28,J29,J30,J31,J32,J33,J34,J35,J36,J37,J38,J39,J40,J41,J42,J43,J44,J45,J46,J47,J48,J49,J50,J51,J52,J53,J54,J55,J56,J57	JUMPER_2
23	J1,J2,J3,J4,J5,J6,J7,J8,J9,J10,J11,J12,J14,J15,J16,J17,J18,J19,J20,J21,J22,J23,J24,J25,J26,J27,J28,J29,J30,J31,J32,J33,J34,J35,J36,J37,J38,J39,J40,J41,J42,J43,J44,J45,J46,J47,J48,J49,J50,J51,J52,J53,J54,J55,J56,J57, J13	JUMPER_2
24	J13	JUMPER_x8
25	L1	22uH
26	L2	100uH
27	L3	470uH

28	R1,R2,R3,R4,R22,R23,R24,R25,R35,R36,R48,R49	2
29	R5,R6,R12,R13,R19,R20,R26,R27,R42,R43,R46,R47	2K
30	R7,R11,R14,R17,R31,R37,R40,R41,R44	10K
31	R8,R18,R21,R28,R45,R50	4.7K
32	R9,R38	11.5K
33	R10,R39	1K
34	R15,R16	6.8K
35	R29,R30	0
36	R32	470
37	R33	12.4K
38	R34	100
39	TP1,TP2,TP7	Barr Screw
40	TP3,TP4,TP5,TP6	TP_CMS
41	T1,T2,T3,T4,T5,T6	2N4401
42	U1	L9658
43	U2	L4998
44	U3	L9654
45	W1	ED102
46	X1	Header 2x34 AB
47	X2	Header 2x34 CD

Appendix B Schematics

Figure 11. L4998 Safety Power Regulator

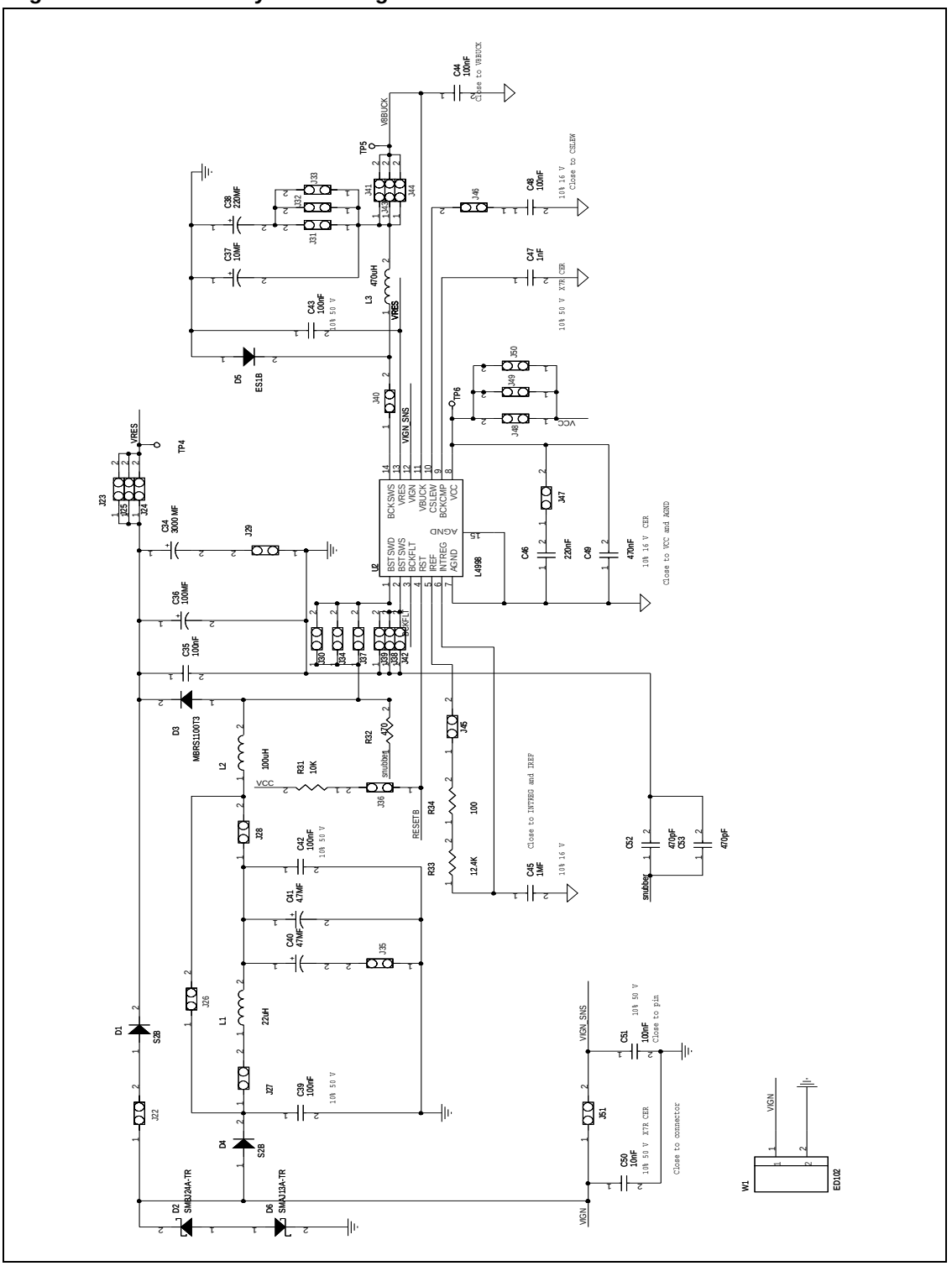


Figure 12. L9658 Octal Squib Driver and Quad Sensor Interfaces

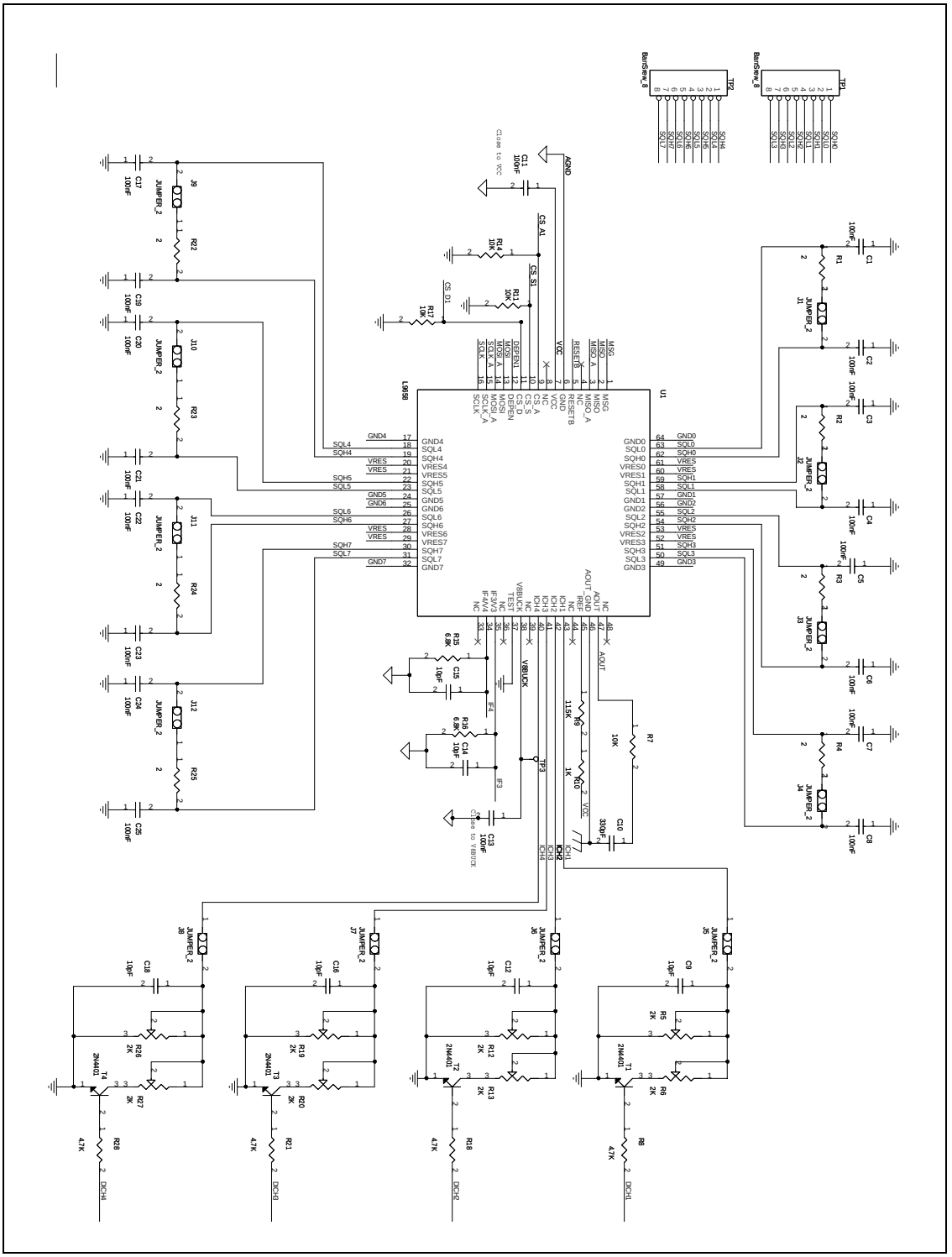


Figure 13. L9654 Quad Squib Driver and Dual Sensor Interfaces

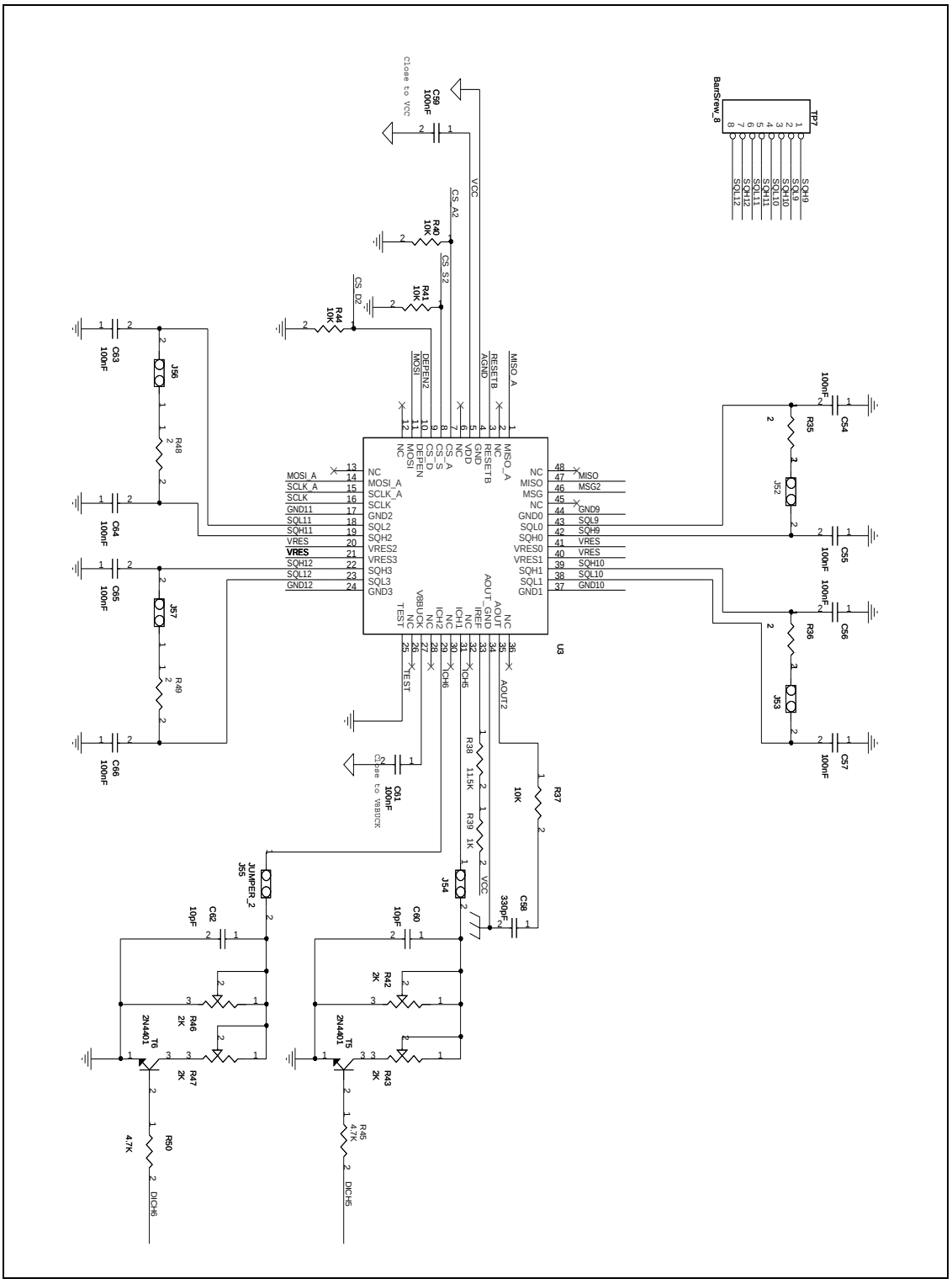
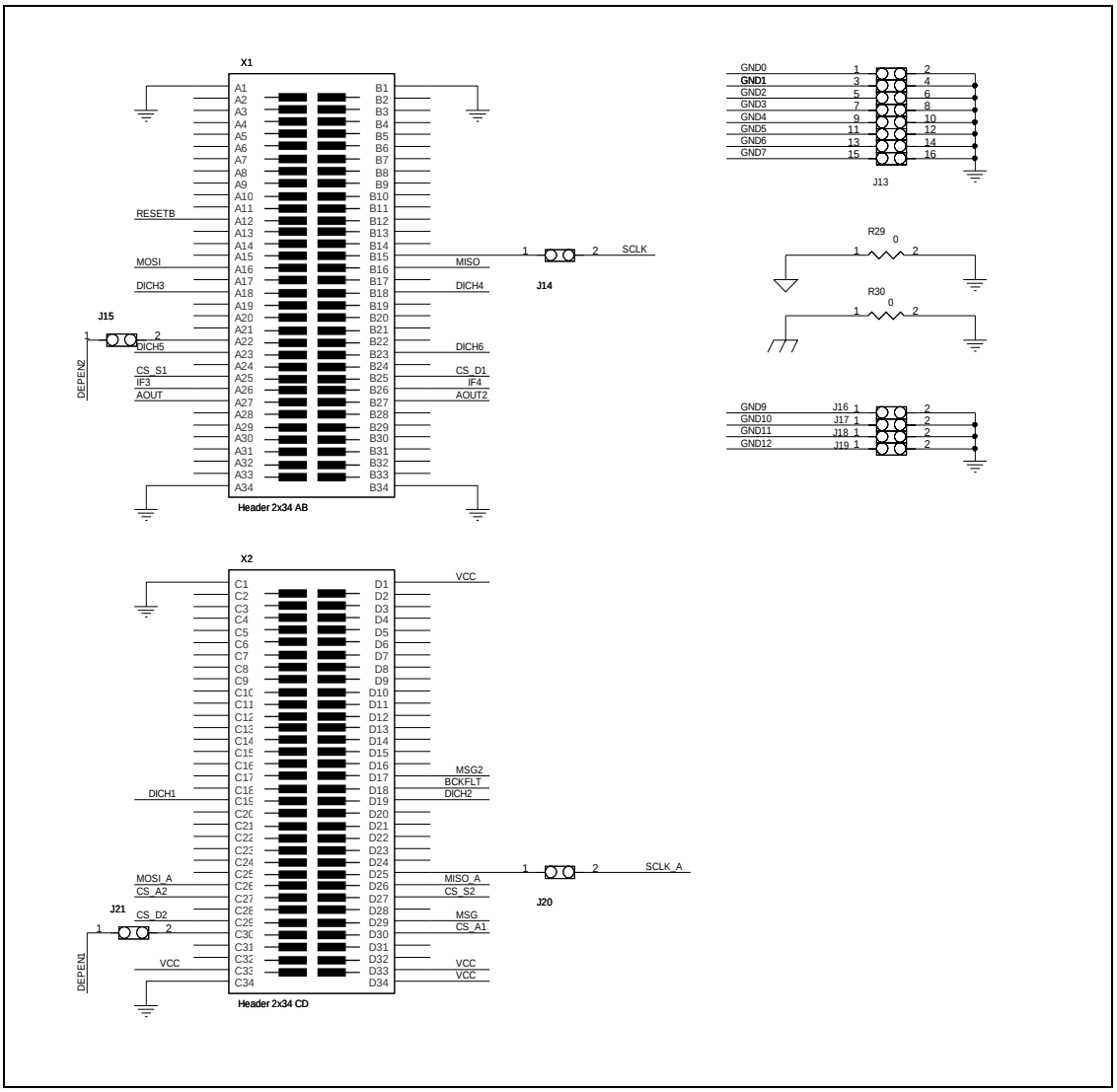


Figure 14. Connector to CPU board



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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9