

FEATURES

Output frequency range: 2300 MHz to 3000 MHz
Modulation bandwidth: >500 MHz (3 dB)
Output third-order intercept: 26 dBm @ 2500 MHz
1 dB output compression: 13.8 dBm @ 2500 MHz
Noise floor: -157.1 dBm/Hz @ 2500 MHz
Sideband suppression: -57 dBc @ 2500 MHz
Carrier feedthrough: -32 dBm @ 2500 MHz
Single supply: 4.75 V to 5.25 V
24-lead LFCSP

APPLICATIONS

WiMAX/broadband wireless access systems
Satellite modems

GENERAL DESCRIPTION

The [ADL5373](#) supports a frequency of operation from 2300 MHz to 3000 MHz and is a pin-compatible member of the fixed gain quadrature modulator (F-MOD) family designed for use from 300 MHz to 4000 MHz. The [ADL5373](#) provides excellent phase accuracy and amplitude balance enabling high performance intermediate frequency or direct radio frequency modulation for communications systems.

The [ADL5373](#) provides a >500 MHz, 3 dB baseband bandwidth, making it ideally suited for use in broadband zero IF or low IF-to-RF applications and in broadband digital predistortion transmitters.

FUNCTIONAL BLOCK DIAGRAM

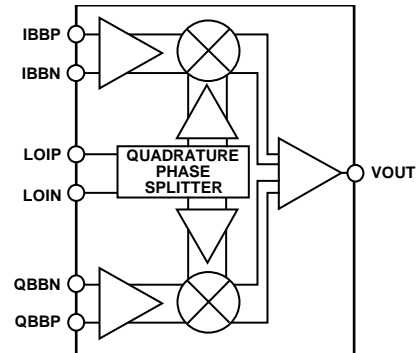


Figure 1.

The [ADL5373](#) accepts two differential baseband inputs that are mixed with a local oscillator (LO) to generate a single-ended output.

The [ADL5373](#) is fabricated using the Analog Devices, Inc. advanced silicon-germanium bipolar process. It is available in a 24-lead, exposed paddle, Pb-free LFCSP. Performance is specified over a -40°C to +85°C temperature range. A Pb-free evaluation board is available.

TABLE OF CONTENTS

| | | | |
|--|----|---|----|
| Features | 1 | RF Output..... | 12 |
| Applications..... | 1 | Optimization..... | 13 |
| Functional Block Diagram | 1 | Applications Information | 14 |
| General Description | 1 | DAC Modulator Interfacing | 14 |
| Revision History | 2 | Limiting the AC Swing | 14 |
| Specifications..... | 3 | Filtering..... | 14 |
| Absolute Maximum Ratings..... | 5 | Using the AD9779 Auxiliary DAC for Carrier Feedthrough Nulling | 15 |
| ESD Caution..... | 5 | WiMAX Operation | 15 |
| Pin Configuration and Function Descriptions..... | 6 | LO Generation Using PLLs | 16 |
| Typical Performance Characteristics | 7 | Transmit DAC Options | 16 |
| Theory of Operation | 11 | Modulator/Demodulator Options | 16 |
| Circuit Description..... | 11 | Evaluation Board | 17 |
| Basic Connections | 12 | Characterization Setup | 18 |
| Power Supply and Grounding..... | 12 | Outline Dimensions | 20 |
| Baseband Inputs..... | 12 | Ordering Guide | 20 |
| LO Input | 12 | | |

REVISION HISTORY

4/16—Rev. A to Rev. B

| | | | |
|--|----|---|----|
| Changes to Figure 2 and Table 3..... | 6 | Changes to Figure 3, Figure 4, and Figure 6 to Figure 8 | 7 |
| Changes to Figure 25..... | 12 | Changes to Figure 9 to Figure 14..... | 8 |
| Changes to LO Generation Using PLLs Section, Table 5, and Table 7 | 16 | Changes to Figure 15 to Figure 20..... | 9 |
| Changes to Figure 37..... | 17 | Changes to Figure 21 to Figure 23..... | 10 |
| Updated Outline Dimensions | 20 | Changes to Optimization Section and Figure 27 | 13 |
| Changes to Ordering Guide | 20 | Changes to Figure 35..... | 15 |
| | | Changes to WiMAX Operation Section and Figure 36..... | 16 |
| | | Changes to Evaluation Board Section..... | 17 |
| | | Changes to Characterization Setup Section..... | 18 |

2/08—Rev. 0 to Rev. A

| | |
|---|---|
| Changes to Features and General Description | 1 |
| Changes to Table 1..... | 3 |
| Changes to Table 2..... | 5 |

6/07—Revision 0: Initial Version

SPECIFICATIONS

$V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $LO = 0\text{ dBm}^1$, baseband I/Q amplitude = 1.4 V p-p differential sine waves in quadrature with a 500 mV dc bias, baseband I/Q frequency (f_{BB}) = 1 MHz, unless otherwise noted.

Table 1.

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|-----------------------------|---|-----|--------------|-----|------------|
| OPERATING FREQUENCY RANGE | Low frequency High frequency | | 2300 3000 | | MHz MHz |
| LO = 2300 MHz | | | | | |
| Output Power | $V_{IQ} = 1.4\text{ V}$ p-p differential | | 4.2 | | dBm |
| Output P1dB | | | 11.0 | | dBm |
| Carrier Feedthrough | | | -35 | | dBm |
| Sideband Suppression | | | -57 | | dBc |
| Quadrature Error | | | <0.2 | | Degrees |
| I/Q Amplitude Balance | | | 0.06 | | dB |
| Second Harmonic | $P_{OUT} - P(f_{LO} \pm (2 \times f_{BB}))$, $P_{OUT} = 4.6\text{ dBm}$ | | -58 | | dBc |
| Third Harmonic | $P_{OUT} - P(f_{LO} \pm (3 \times f_{BB}))$, $P_{OUT} = 4.6\text{ dBm}$ | | -49 | | dBc |
| Output IP2 | $f_{1BB} = 3.5\text{ MHz}$, $f_{2BB} = 4.5\text{ MHz}$, $P_{OUT} = -1.5\text{ dBm}$ per tone | | 56 | | dBm |
| Output IP3 | $f_{1BB} = 3.5\text{ MHz}$, $f_{2BB} = 4.5\text{ MHz}$, $P_{OUT} = -1.5\text{ dBm}$ per tone | | 25 | | dBm |
| WiMAX 802.16e | 10 MHz carrier bandwidth (1024 subcarriers), 64 QAM signal, 30 MHz carrier offset, $P_{OUT} = -10\text{ dBm}$, $P_{LO} = 0\text{ dBm}$ | | -158.6 | | dBm/Hz |
| LO = 2500 MHz | | | | | |
| Output Power | $V_{IQ} = 1.4\text{ V}$ p-p differential | | 7.1 | | dBm |
| Output P1dB | | | 13.8 | | dBm |
| Carrier Feedthrough | | | -32 | | dBm |
| Sideband Suppression | | | -57 | | dBc |
| Quadrature Error | | | 0.3 | | Degrees |
| I/Q Amplitude Balance | | | 0.06 | | dB |
| Second Harmonic | $P_{OUT} - P(f_{LO} \pm (2 \times f_{BB}))$, $P_{OUT} = 7.1\text{ dBm}$ | | -57 | | dBc |
| Third Harmonic | $P_{OUT} - P(f_{LO} \pm (3 \times f_{BB}))$, $P_{OUT} = 7.1\text{ dBm}$ | | -47 | | dBc |
| Output IP2 | $f_{1BB} = 3.5\text{ MHz}$, $f_{2BB} = 4.5\text{ MHz}$, $P_{OUT} = 1.1\text{ dBm}$ per tone | | 58 | | dBm |
| Output IP3 | $f_{1BB} = 3.5\text{ MHz}$, $f_{2BB} = 4.5\text{ MHz}$, $P_{OUT} = 1.1\text{ dBm}$ per tone | | 26 | | dBm |
| Noise Floor | I/Q inputs = 0 V differential with a 500 mV common-mode bias, 20 MHz carrier offset | | -157.1 | | dBm/Hz |
| WiMAX 802.16e | 10 MHz carrier bandwidth (1024 subcarriers), 64 QAM signal, 30 MHz carrier offset, $P_{OUT} = -10\text{ dBm}$, $P_{LO} = 0\text{ dBm}$ | | -157.4 | | dBm/Hz |
| LO = 2700 MHz | | | | | |
| Output Power | $V_{IQ} = 1.4\text{ V}$ p-p differential | | 7.7 | | dBm |
| Output P1dB | | | 13.8 | | dBm |
| Carrier Feedthrough | | | -33 | | dBm |
| Sideband Suppression | | | -54 | | dBc |
| Quadrature Error | | | <0.2 | | Degrees |
| I/Q Amplitude Balance | | | 0.07 | | dB |
| Second Harmonic | $P_{OUT} - P(f_{LO} \pm (2 \times f_{BB}))$, $P_{OUT} = 7.7\text{ dBm}$ | | -55 | | dBc |
| Third Harmonic | $P_{OUT} - P(f_{LO} \pm (3 \times f_{BB}))$, $P_{OUT} = 7.7\text{ dBm}$ | | -47 | | dBc |
| Output IP2 | $f_{1BB} = 3.5\text{ MHz}$, $f_{2BB} = 4.5\text{ MHz}$, $P_{OUT} = 1.6\text{ dBm}$ per tone | | 57 | | dBm |
| Output IP3 | $f_{1BB} = 3.5\text{ MHz}$, $f_{2BB} = 4.5\text{ MHz}$, $P_{OUT} = 1.6\text{ dBm}$ per tone | | 25 | | dBm |
| WiMAX 802.16e | 10 MHz carrier bandwidth (1024 subcarriers), 64 QAM signal, 30 MHz carrier offset, $P_{OUT} = -10\text{ dBm}$, $P_{LO} = 0\text{ dBm}$ | | -155.3 | | dBm/Hz |
| LO INPUTS | | | | | |
| LO Drive Level ¹ | Characterization performed at typical level | -6 | 0 | +6 | dBm |
| Input Return Loss | See Figure 9 for a plot of return loss vs. frequency | | -6 | | dB |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|------------------------------|---|------|---------|------|--------|
| BASEBAND INPUTS | Pin IBBP, Pin IBBN, Pin QBBP, Pin QBBN | | | | |
| I and Q Input Bias Level | | | 500 | | mV |
| Input Bias Current | Current sourcing from each baseband input with a bias of 500 mV dc ² | | 45 | | μA |
| Input Offset Current | | | 0.1 | | μA |
| Differential Input Impedance | f _{BB} = 1 MHz | | 40 1.5 | | kΩ pF |
| Bandwidth | LO = 2500 MHz, baseband input = 700 mV p-p sine wave on 500 mV dc | | | | |
| 0.1 dB | | | 70 | | MHz |
| 1 dB | | | 350 | | MHz |
| POWER SUPPLIES | Pin VPS1 and Pin VPS2 | | | | |
| Voltage | | 4.75 | | 5.25 | V |
| Supply Current | | | 174 | | mA |

¹ Driven through Johanson Technology balun (Model 2450BL15B050)

² See V-to-I Converter section for architecture information.

ABSOLUTE MAXIMUM RATINGS

Table 2.

| Parameter | Rating |
|--|-----------------|
| Supply Voltage VPSx | 5.5 V |
| IBBP, IBBN, QBBP, and QBBN | 0 V to 2 V |
| LOIP and LOIN | 13 dBm |
| Internal Power Dissipation | 1119 mW |
| θ_{JA} (Exposed Paddle Soldered Down) | 54°C/W |
| Maximum Junction Temperature | 150°C |
| Operating Temperature Range | -40°C to +85°C |
| Storage Temperature Range | -65°C to +150°C |

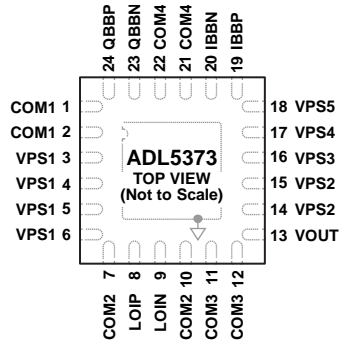
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
 1. EXPOSED PAD. CONNECT TO A GROUND PLANE VIA A LOW IMPEDANCE PATH.

06864-002

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---|------------------------------|--|
| 1, 2, 7, 10 to 12, 21, 22 3 to 6, 14 to 18 | COM1 to COM4 VPS1 to VPS5 | Input Common Pins. Connect to ground plane via a low impedance path. Positive Supply Voltage Pins. All pins should be connected to the same supply (V_s). To ensure adequate external bypassing, connect 0.1 μ F capacitors between each pin and ground. Adjacent power supply pins of the same name can share one capacitor (see Figure 25). |
| 8, 9 | LOIP, LOIN | 50 Ω Differential Local Oscillator Input. Internally dc-biased. Pins must be ac-coupled. See Figure 8 for LO input impedance. |
| 13 | VOUT | Device Output. Single-ended RF output. Pin should be ac-coupled to the load. The output is ground referenced. |
| 19, 20, 23, 24 | IBBP, IBBN, QBBN, QBBP | Differential In-Phase and Quadrature Baseband Inputs. These high impedance inputs must be dc-biased to 500 mV dc and must be driven from a low impedance source. Nominal characterized ac signal swing is 700 mV p-p on each pin. This results in a differential drive of 1.4 V p-p with a 500 mV dc bias. These inputs are not self-biased and must be externally biased. |
| | EPAD | Exposed Pad. Connect to a ground plane via a low impedance path. |

TYPICAL PERFORMANCE CHARACTERISTICS

$V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$, LO = 0 dBm, baseband I/Q amplitude = 1.4 V p-p differential sine waves in quadrature with a 500 mV dc bias, baseband I/Q frequency (f_{BB}) = 1 MHz, unless otherwise noted.

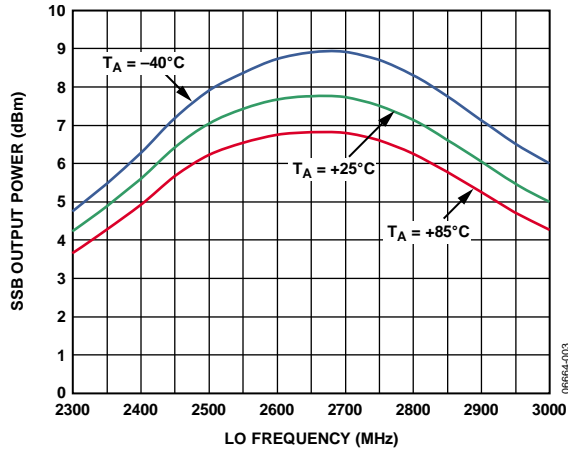


Figure 3. Single Sideband (SSB) Output Power (P_{out}) vs. LO Frequency (f_{LO}) and Temperature

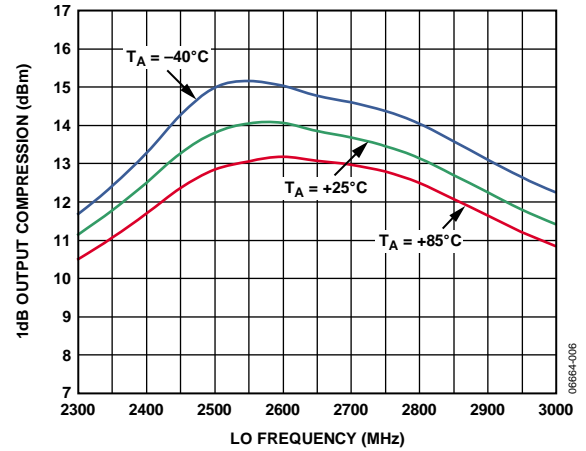


Figure 6. SSB Output P1dB Compression Point ($OP_{1\text{dB}}$) vs. f_{LO} and Temperature

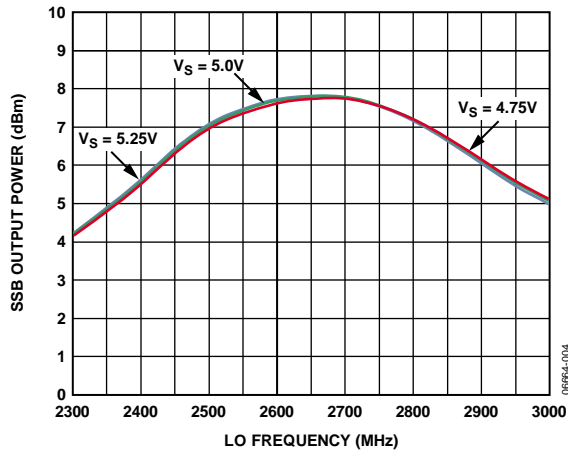


Figure 4. Single Sideband (SSB) Output Power (P_{out}) vs. f_{LO} and Supply

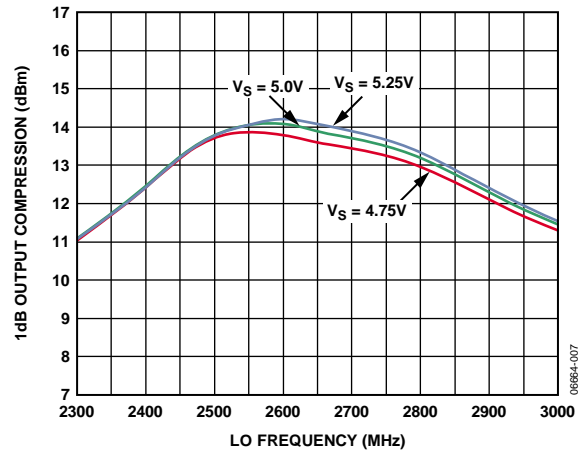


Figure 7. SSB Output P1dB Compression Point ($OP_{1\text{dB}}$) vs. f_{LO} and Supply

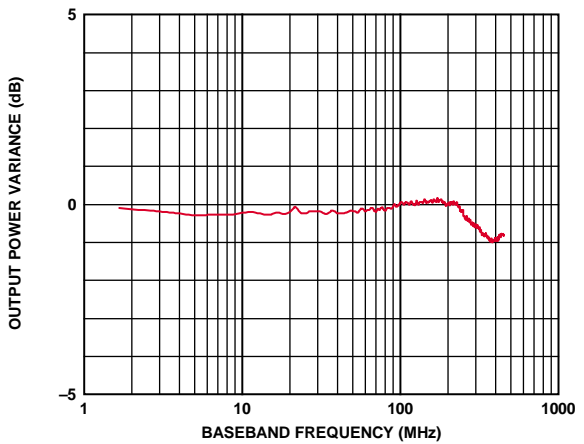


Figure 5. I and Q Input Bandwidth Normalized to Gain @ 1 MHz ($f_{\text{LO}} = 2500\text{ MHz}$)

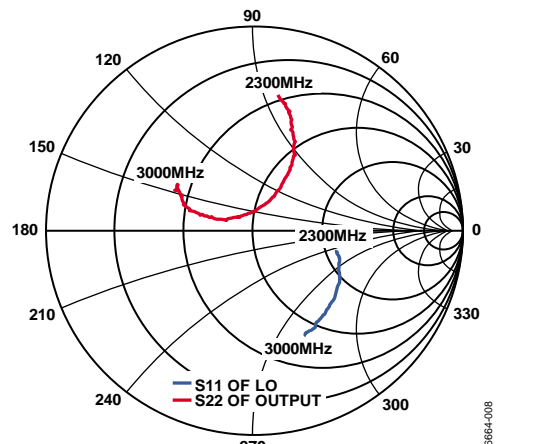


Figure 8. Smith Chart of LOIP (LOIN AC-Coupled to Ground) S11 and VOUT S22 (f_{LO} from 2300 MHz to 3000 MHz)

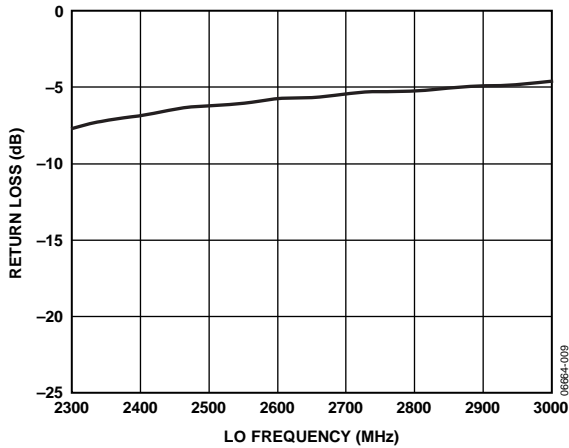


Figure 9. Return Loss (S11) of LOIP with LOIN AC-Coupled to Ground vs. f_{LO}

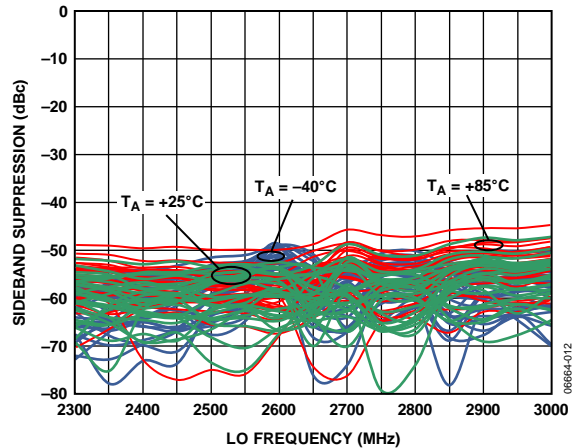


Figure 12. Sideband Suppression vs. f_{LO} and Temperature; Multiple Devices Shown

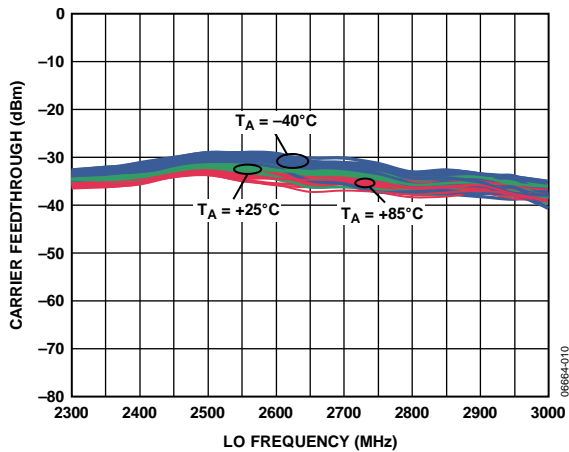


Figure 10. Carrier Feedthrough vs. f_{LO} and Temperature; Multiple Devices Shown

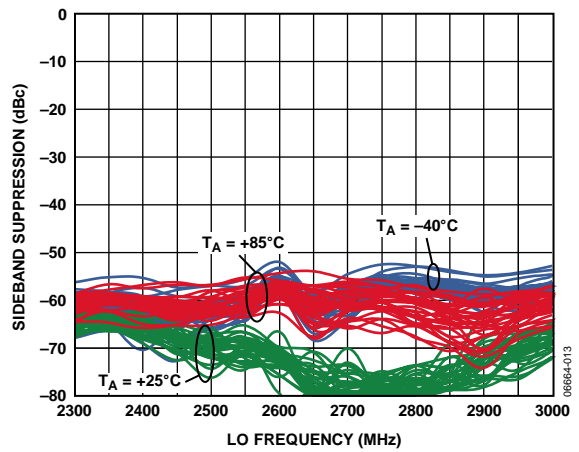


Figure 13. Sideband Suppression vs. f_{LO} and Temperature after Nulling at 25°C; Multiple Devices Shown

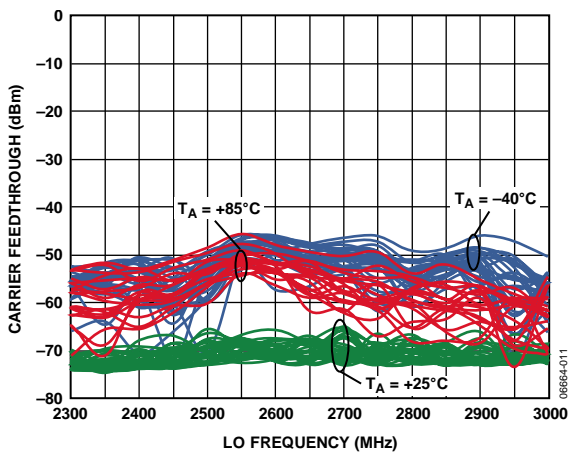


Figure 11. Carrier Feedthrough vs. f_{LO} and Temperature after Nulling at 25°C; Multiple Devices Shown

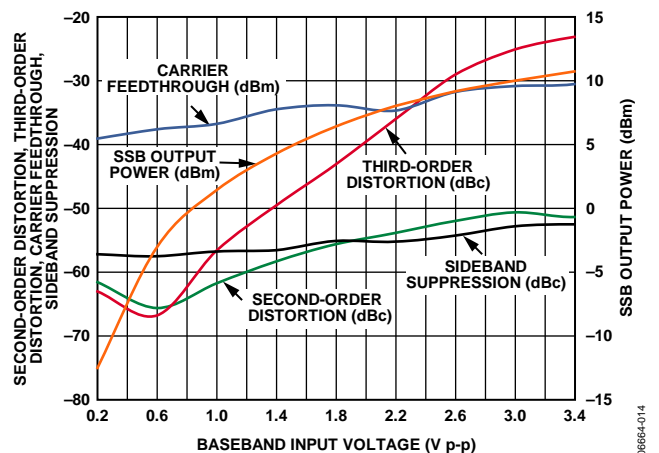


Figure 14. Second- and Third-Order Distortion, Carrier Feedthrough, Sideband Suppression, and SSB P_{OUT} vs. Baseband Differential Input Level ($f_{LO} = 2300$ MHz)

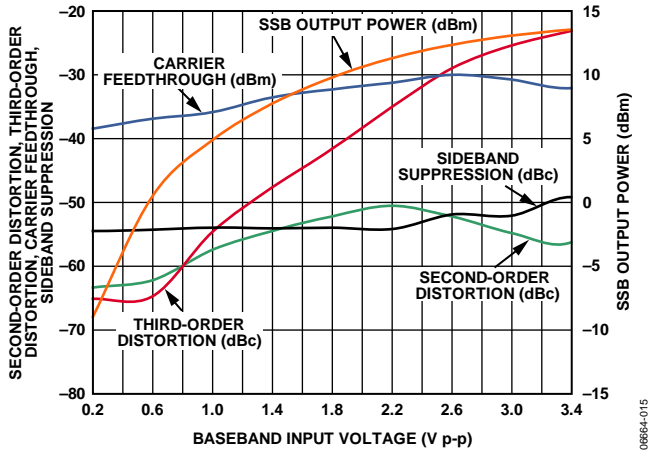


Figure 15. Second- and Third-Order Distortion, Carrier Feedthrough, Sideband Suppression, and SSB P_{OUT} vs. Baseband Differential Input Level ($f_{LO} = 2700$ MHz)

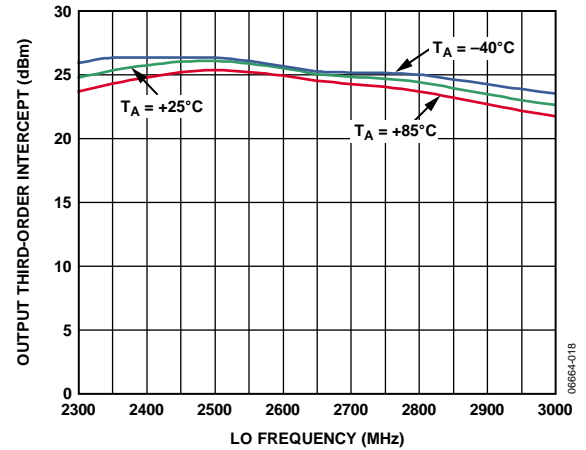


Figure 18. OIP3 vs. f_{LO} and Temperature

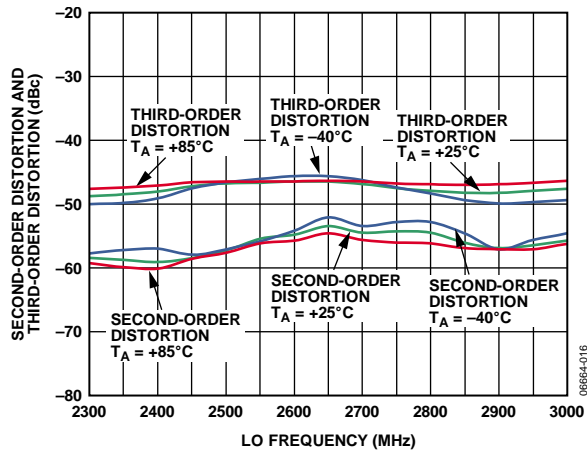


Figure 16. Second- and Third-Order Distortion vs. f_{LO} and Temperature (Baseband I/Q Amplitude = 1.4 V p-p Differential)

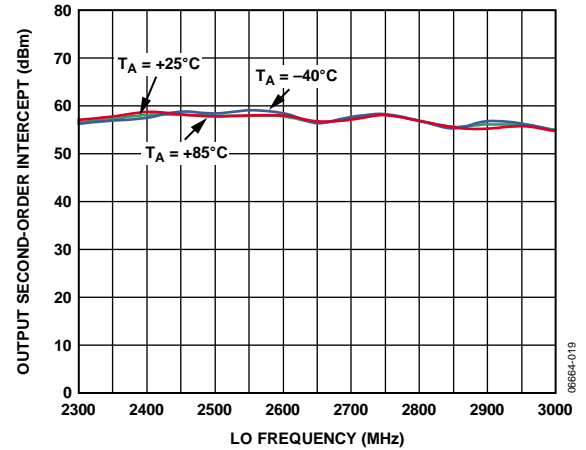


Figure 19. OIP2 vs. f_{LO} and Temperature

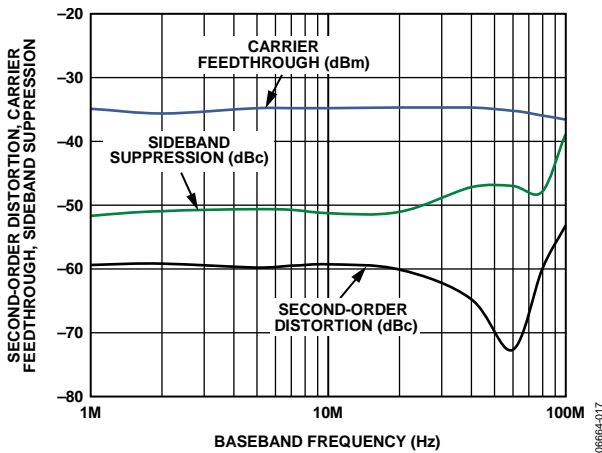


Figure 17. Second-Order Distortion, Carrier Feedthrough, and Sideband Suppression vs. f_{BB} ($f_{LO} = 2500$ MHz)

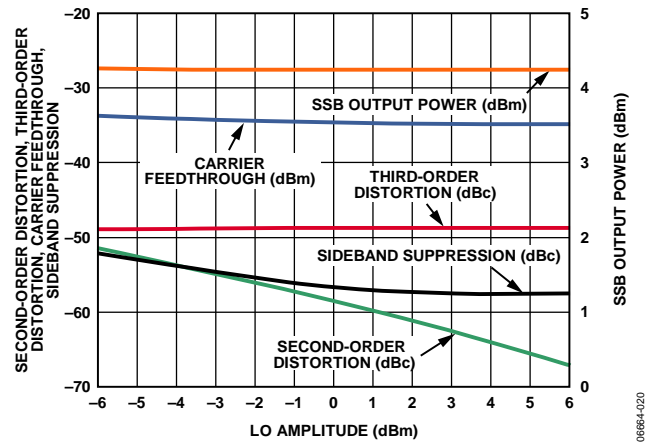


Figure 20. Second- and Third-Order Distortion, Carrier Feedthrough, Sideband Suppression, and SSB P_{OUT} vs. LO Amplitude ($f_{LO} = 2300$ MHz)

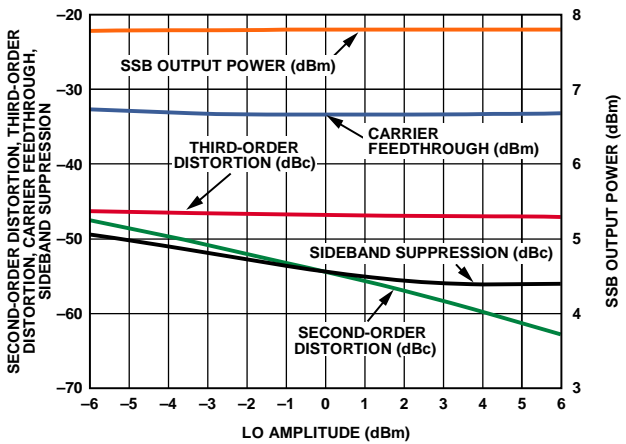


Figure 21. Second- and Third-Order Distortion, Carrier Feedthrough, Sideband Suppression, and SSB P_{OUT} vs. LO Amplitude ($f_{LO} = 2700$ MHz)

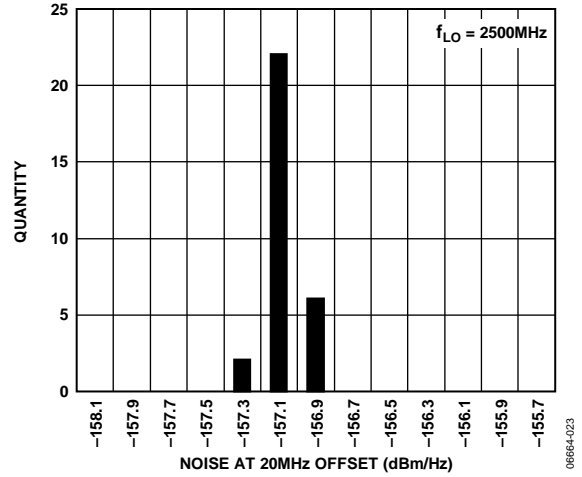


Figure 23. 20 MHz Offset Noise Floor Distribution at $f_{LO} = 2500$ MHz (I/Q Amplitude = 0 mV p-p with 500 mV dc Bias)

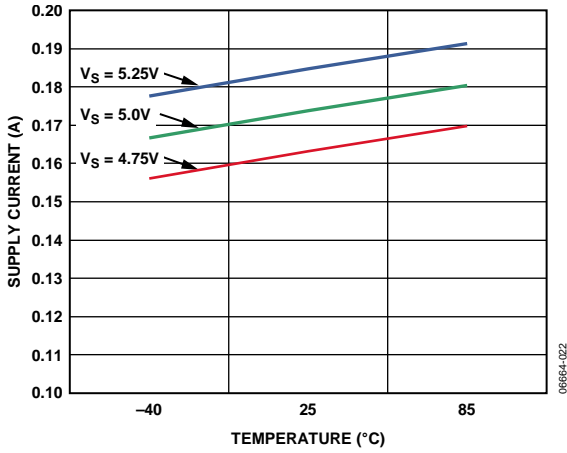


Figure 22. Power Supply Current vs. Temperature

THEORY OF OPERATION

CIRCUIT DESCRIPTION

Overview

The ADL5373 can be divided into five circuit blocks: the LO interface, the baseband voltage-to-current (V-to-I) converter, the mixers, the differential-to-single-ended (D-to-S) stage, and the bias circuit. A detailed block diagram of the device is shown in Figure 24.

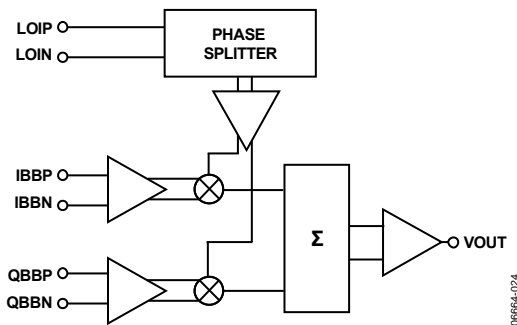


Figure 24. Block Diagram

The LO interface generates two LO signals in quadrature. These signals are used to drive the mixers. The I and Q baseband input signals are converted to currents by the V-to-I stages, which then drive the two mixers. The outputs of these mixers combine to feed the output balun, which provides a single-ended output. The bias cell generates reference currents for the V-to-I stage.

LO Interface

The LO interface consists of a polyphase quadrature splitter followed by a limiting amplifier. The LO input impedance is set by the polyphase. For optimal performance, the LO should be driven differentially. Each quadrature LO signal then passes through a limiting amplifier that provides the mixer with a limited drive signal.

V-to-I Converter

The differential baseband inputs (QBBP, QBBN, IBBN, and IBBP) consist of the bases of the PNP transistors, which present a high impedance. The voltages applied to these pins drive the V-to-I stage that converts baseband voltages into currents. The differential output currents of the V-to-I stages feed each of their respective Gilbert cell mixers. The dc common-mode voltage at the baseband inputs sets the currents in the two mixer cores. Varying the baseband common-mode voltage influences the current in the mixer and affects overall modulator performance. The recommended dc voltage for the baseband common-mode voltage is 500 mV dc.

Mixers

The ADL5373 has two double balanced mixers: one for the in-phase channel (I-channel) and one for the quadrature channel (Q-channel). Both mixers are based on the Gilbert cell design of four cross-connected transistors. The output currents from the two mixers sum together into a load. The signal developed across this load is used to drive the D-to-S stage.

D-to-S Stage

The output D-to-S stage consists of an on-chip balun that converts the differential signal to a single-ended signal. The balun presents high impedance to the output (VOUT); therefore, a matching network may be needed at the output for optimal power transfer.

Bias Circuit

An on-chip band gap reference circuit is used to generate a proportional-to-absolute temperature (PTAT) reference current for the V-to-I stage.

BASIC CONNECTIONS

Figure 25 shows the basic connections for the [ADL5373](#).

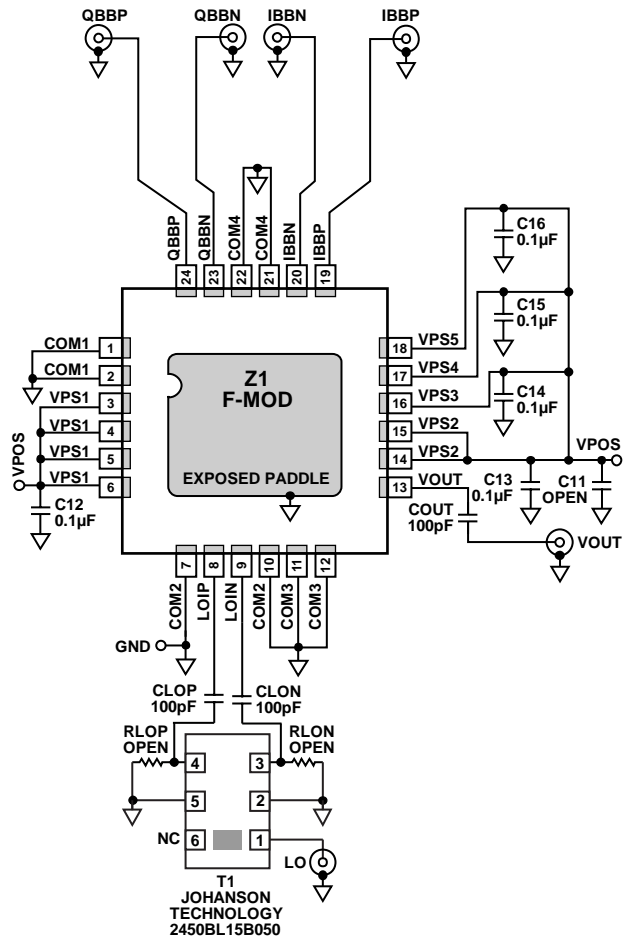


Figure 25. Basic Connections for the [ADL5373](#)

POWER SUPPLY AND GROUNDING

All the VPS pins must be connected to the same 5 V source. Adjacent pins of the same name can be tied together and decoupled with a 0.1 μF capacitor. Locate these capacitors as close as possible to the device. The power supply can range between 4.75 V and 5.25 V.

The COM1, COM2, COM3, and COM4 pins should be tied to the same ground plane through low impedance paths. Solder the exposed paddle on the underside of the package to a low thermal and electrical impedance ground plane. If the ground plane spans multiple layers on the circuit board, they should be stitched together with nine vias under the exposed paddle. Application Note [AN-772](#) describes the thermal and electrical grounding of the LFCSP in detail.

BASEBAND INPUTS

The baseband inputs QBBP, QBPN, IBPN, and IBBN must be driven from a differential source. Bias the nominal drive level of 1.4 V p-p differential (700 mV p-p on each pin) to a common-mode level of 500 mV dc.

The dc common-mode bias level for the baseband inputs can range from 400 mV to 600 mV. This results in a reduction in the usable input ac swing range. The nominal dc bias of 500 mV allows for the largest ac swing, limited on the bottom end by the [ADL5373](#) input range and on the top end by the output compliance range on most DACs from Analog Devices.

LO INPUT

The LO input should be driven differentially. The recommended balun for the [ADL5373](#) is the Johanson Technology model 2450BL15B050. The LO pins should be ac-coupled to the balun.

The nominal LO drive of 0 dBm can be increased to up to 6 dBm to realize an improvement in the noise performance of the modulator. If the LO source cannot provide the 0 dBm level, operation at a reduced power below 0 dBm is acceptable. Reduced LO drive results in slightly increased modulator noise. The effect of LO power on sideband suppression and carrier feedthrough is shown in Figure 20 and Figure 21.

RF OUTPUT

The RF output is available at the VOUT pin (Pin 13). The VOUT pin connects to an internal balun, which is capable of driving a 50 Ω load. For applications requiring 50 Ω output impedance, external matching is needed (see Figure 8 for S22 performance). The internal balun provides a low dc path to ground. In most situations, the VOUT pin should be ac-coupled to the load.

OPTIMIZATION

The carrier feedthrough and sideband suppression performance of the ADL5373 can be improved by using optimization techniques.

Carrier Feedthrough Nulling

Carrier feedthrough results from minute dc offsets that occur between each of the differential baseband inputs. In an ideal modulator, the quantities $(V_{IOPP} - V_{IOPN})$ and $(V_{QOPP} - V_{QOPN})$ are equal to zero, which results in no carrier feedthrough. In a real modulator, those two quantities are nonzero and, when mixed with the LO, they result in a finite amount of carrier feedthrough. The ADL5373 is designed to provide a minimal amount of carrier feedthrough. Should even lower carrier feedthrough levels be required, minor adjustments can be made to the $(V_{IOPP} - V_{IOPN})$ and $(V_{QOPP} - V_{QOPN})$ offsets. The I-channel offset is held constant while the Q-channel offset is varied until a minimum carrier feedthrough level is obtained. The Q-channel offset required to achieve this minimum is held constant, while the offset on the I-channel is adjusted until a new minimum is reached. Through two iterations of this process, the carrier feedthrough can be reduced to as low as the output noise. The ability to null is sometimes limited by the resolution of the offset adjustment. Figure 26 shows the relationship of carrier feedthrough vs. dc offset as null.

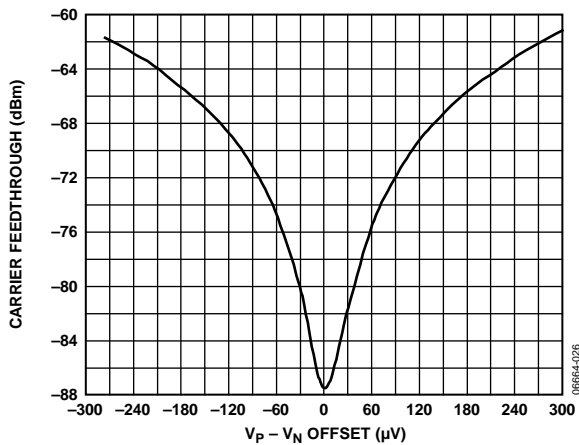


Figure 26. Carrier Feedthrough vs. DC Offset Voltage at 2500 MHz

Note that throughout the nulling process, the dc bias for the baseband inputs remains at 500 mV. When no offset is applied,

$$V_{IOPP} = V_{IOPN} = 500 \text{ mV, or}$$

$$V_{IOPP} - V_{IOPN} = V_{IOS} = 0 \text{ V}$$

When an offset of $+V_{IOS}$ is applied to the I-channel inputs,

$$V_{IOPP} = 500 \text{ mV} + V_{IOS}/2, \text{ and}$$

$$V_{IOPN} = 500 \text{ mV} - V_{IOS}/2, \text{ such that}$$

$$V_{IOPP} - V_{IOPN} = V_{IOS}$$

The same applies to the Q channel.

It is often desirable to perform a one-time carrier null calibration. This is usually performed at a single frequency. Figure 27 shows how carrier feedthrough varies with LO frequency over a range of ± 100 MHz on either side of a null at 2600 MHz.

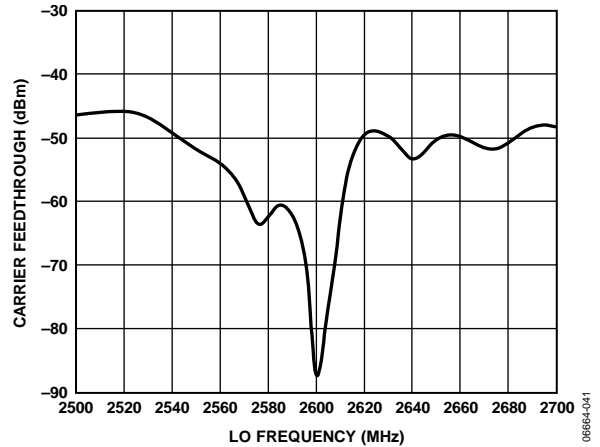


Figure 27. Carrier Feedthrough vs. Frequency After Nulling at 2600 MHz

Sideband Suppression Optimization

Sideband suppression results from relative gain and relative phase offsets between the I channel and Q channel and can be suppressed through adjustments to those two parameters. Figure 28 illustrates how sideband suppression is affected by the gain and phase imbalances.

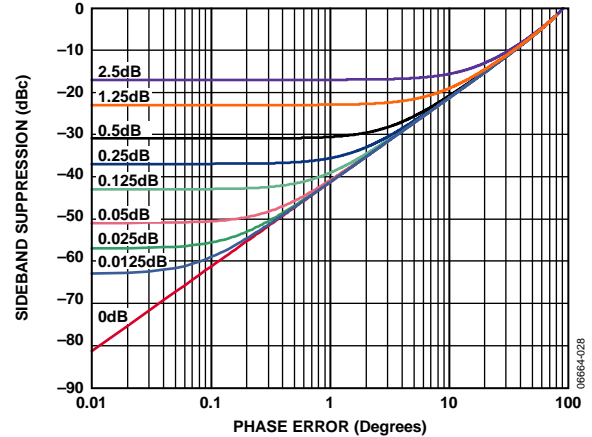


Figure 28. Sideband Suppression vs. Quadrature Phase Error for Various Quadrature Amplitude Offsets

Figure 28 underlines the fact that adjusting only one parameter improves the sideband suppression only to a point, unless the other parameter is also adjusted. For example, if the amplitude offset is 0.25 dB, improving the phase imbalance better than 1° does not yield any improvement in the sideband suppression. For optimum sideband suppression, an iterative adjustment between phase and amplitude is required.

The sideband suppression nulling can be performed either through adjusting the gain for each channel or through the modification of the phase and gain of the digital data coming from the digital signal processor.

APPLICATIONS INFORMATION

DAC MODULATOR INTERFACING

The **ADL5373** is designed to interface with minimal components to members of the Analog Devices family of DACs. These DACs feature an output current swing from 0 mA to 20 mA, and the interface described in this section can be used with any DAC that has a similar output.

Driving the **ADL5373** with a TxDAC®

An example of the interface using the **AD9779** TxDAC is shown in Figure 29. The baseband inputs of the **ADL5373** require a dc bias of 500 mV. The average output current on each of the outputs of the **AD9779** is 10 mA. Therefore, a single 50 Ω resistor to ground from each of the DAC outputs results in an average current of 10 mA flowing through each of the resistors, thus producing the desired 500 mV dc bias for the inputs to the **ADL5373**.

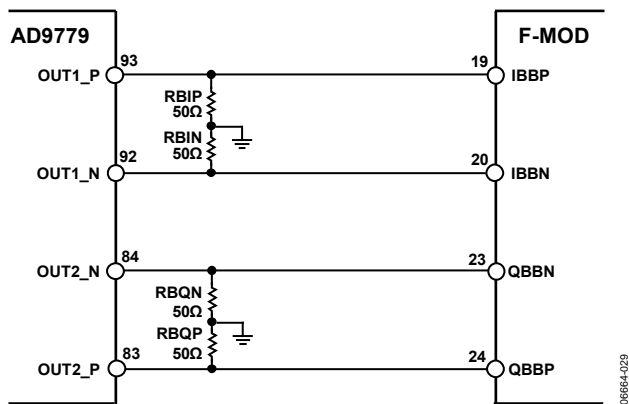


Figure 29. Interface Between the **AD9779** and **ADL5373** with 50 Ω Resistors to Ground to Establish the 500 mV DC Bias for the **ADL5373** Baseband Inputs

The **AD9779** output currents have a swing that ranges from 0 mA to 20 mA. With the 50 Ω resistors in place, the ac voltage swing going into the **ADL5373** baseband inputs ranges from 0 V to 1 V. A full-scale sine wave out of the **AD9779** can be described as a 1 V p-p single-ended (or 2 V p-p differential) sine wave with a 500 mV dc bias.

LIMITING THE AC SWING

There are situations in which it is desirable to reduce the ac voltage swing for a given DAC output current. This can be achieved through the addition of another resistor to the interface. This resistor is placed in the shunt between each side of the differential pair, as shown in Figure 30. It has the effect of reducing the ac swing without changing the dc bias already established by the 50 Ω resistors.

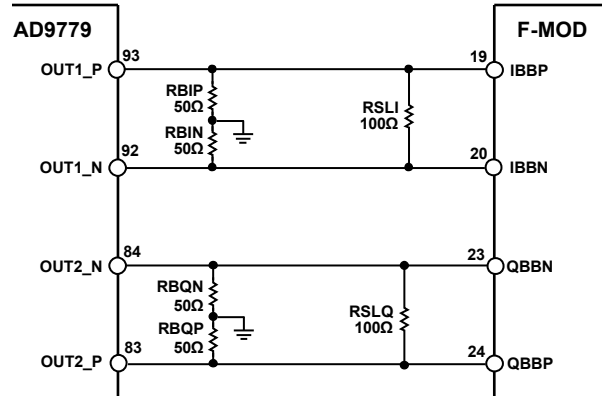


Figure 30. AC Voltage Swing Reduction Through the Introduction of a Shunt Resistor Between a Differential Pair

The value of this ac voltage swing limiting resistor is chosen based on the desired ac voltage swing. Figure 31 shows the relationship between the swing limiting resistor and the peak-to-peak ac swing that it produces when 50 Ω bias setting resistors are used.

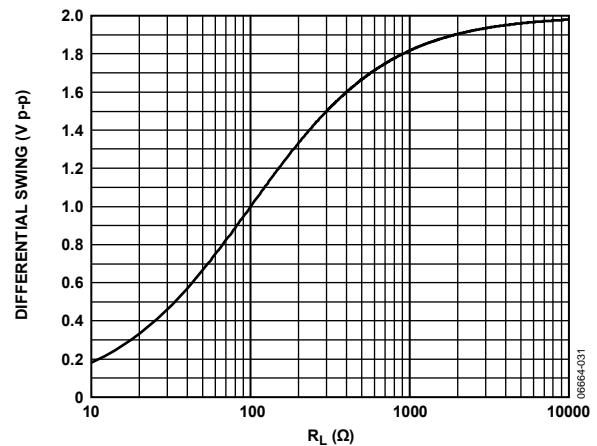


Figure 31. Relationship Between the AC Swing Limiting Resistor and the Peak-to-Peak Voltage Swing with 50 Ω Bias Setting Resistors

FILTERING

It is necessary to low-pass filter the DAC outputs to remove images when driving a modulator. The interface for setting up the biasing and ac swing that was described in the Limiting the AC Swing section lends itself well to the introduction of such a filter. The filter can be inserted between the dc bias setting resistors and the ac swing limiting resistor, which establishes the input and output impedances for the filter.

An example is shown in Figure 32 with a third-order, Bessel low-pass filter with a 3 dB frequency of 10 MHz. Matching input and output impedances makes the filter design easier, so the shunt resistor chosen is 100 Ω, producing an ac swing of 1 V p-p differential. The frequency response of this filter is shown in Figure 33.

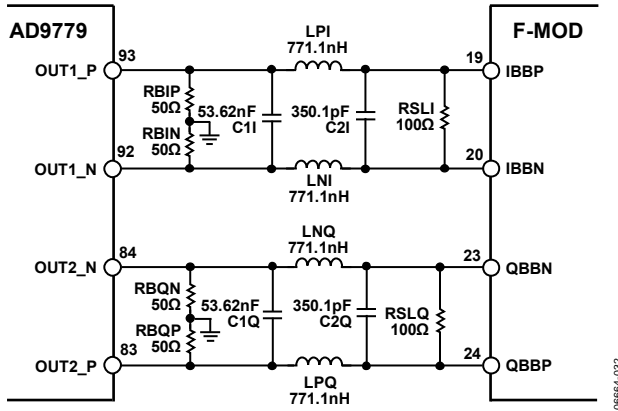


Figure 32. DAC Modulator Interface with 10 MHz Third-Order Bessel Filter

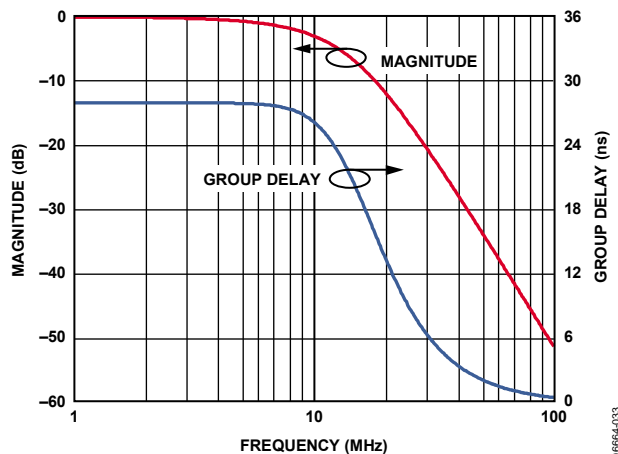


Figure 33. Frequency Response for DAC Modulator Interface with 10 MHz Third-Order Bessel Filter

USING THE AD9779 AUXILIARY DAC FOR CARRIER FEEDTHROUGH NULLING

The AD9779 features an auxiliary DAC that can be used to inject small currents into the differential outputs for each main DAC channel. This feature can be used to produce the small offset voltages necessary to null out the carrier feedthrough from the modulator. Figure 34 shows the interface required to use the auxiliary DACs, which adds four resistors to the interface.

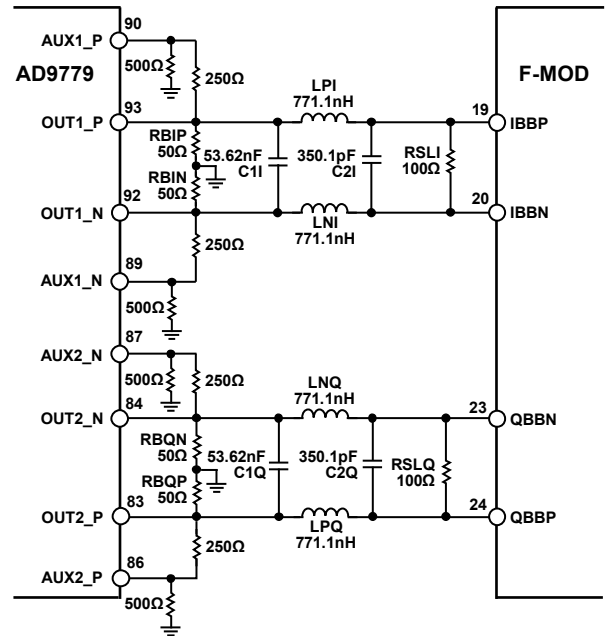


Figure 34. DAC Modulator Interface with Auxiliary DAC Resistors

WiMAX OPERATION

Figure 35 shows the first and second adjacent channel power ratios (10 MHz offset and 20 MHz offset), and the 30 MHz offset noise floor vs. output power for a 10 MHz 1024-OFDMA waveform at 2600 MHz.

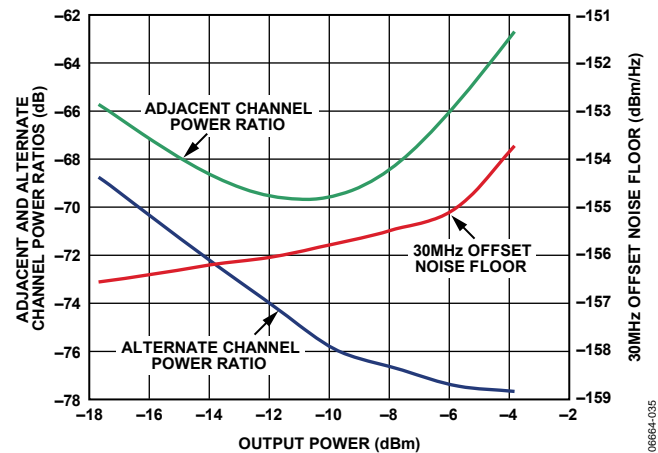


Figure 35. Adjacent and Alternate Channel Power Ratios and 30 MHz Offset Noise Floor vs. Channel Power for a 10 MHz 1024-OFDMA Waveform at 2600 MHz; LO Power = 0 dBm

Figure 35 illustrates that optimal performance is achieved when the output power from the modulator is -10 dBm or greater. The noise floor rises with increasing output power, but at less than half the rate at which ACPR degrades. Therefore, operating at powers greater than -10 dBm can improve the signal-to-noise ratio.

Figure 36 shows the error-vector magnitude (EVM) vs. output power for a 10 MHz, 1024-OFDMA waveform at 2600 MHz.

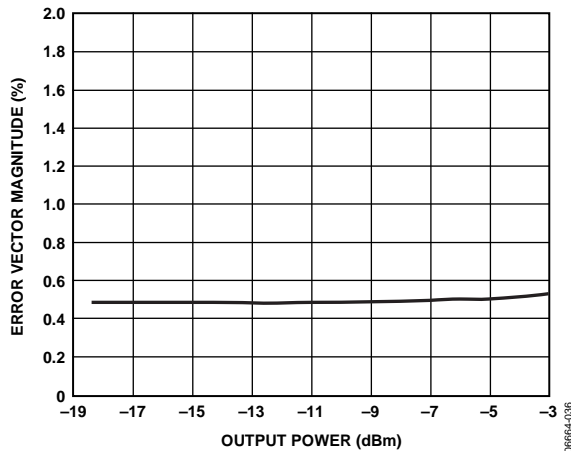


Figure 36. Error Vector Magnitude (EVM) vs. Output Power for 10 MHz, 1024-OFDMA Waveform at 2600 MHz; LO Power = 0 dBm

LO GENERATION USING PLLs

Analog Devices has a line of PLLs that can be used for generating the LO signal. Table 4 lists the PLLs together with their maximum frequency and phase noise performance.

Table 4. Analog Devices PLL Selection Table

| Part | Frequency f_{in} (MHz) | Phase Noise @ 1 kHz Offset and 200 kHz PFD (dBc/Hz) |
|---------|--------------------------|---|
| ADF4110 | 550 | -91 @ 540 MHz |
| ADF4111 | 1200 | -87 @ 900 MHz |
| ADF4112 | 3000 | -90 @ 900 MHz |
| ADF4113 | 4000 | -91 @ 900 MHz |
| ADF4116 | 550 | -89 @ 540 MHz |
| ADF4117 | 1200 | -87 @ 900 MHz |
| ADF4118 | 3000 | -90 @ 900 MHz |

The [ADF4360-0](#) through the [ADF4360-8](#) (see Table 5 for the full list of devices included in this range) comes as a family of chips, with nine operating frequency ranges. A device is chosen depending on the local oscillator frequency required. Although the use of the integrated synthesizer may come at the expense of slightly degraded noise performance from the [ADL5373](#), it can be a cheaper alternative to a separate PLL and VCO solution. Table 5 shows the options available.

Table 5. [ADF4360-0](#) to [ADF4360-8](#) Family Operating Frequencies

| Part | Output Frequency Range (MHz) |
|-----------|------------------------------|
| ADF4360-0 | 2400 to 2725 |
| ADF4360-1 | 2050 to 2450 |
| ADF4360-2 | 1850 to 2170 |
| ADF4360-3 | 1600 to 1950 |
| ADF4360-4 | 1450 to 1750 |
| ADF4360-5 | 1200 to 1400 |
| ADF4360-6 | 1050 to 1250 |
| ADF4360-7 | 350 to 1800 |
| ADF4360-8 | 65 to 400 |

TRANSMIT DAC OPTIONS

The [AD9779](#) recommended in the previous sections of this data sheet is not the only DAC that can be used to drive the [ADL5373](#). There are other appropriate DACs, depending on the level of performance required. Table 6 lists the dual TxDACs offered by Analog Devices.

Table 6. Dual TxDAC Selection Table

| Part | Resolution (Bits) | Update Rate (MSPS Minimum) |
|------------------------|-------------------|----------------------------|
| AD9709 | 8 | 125 |
| AD9761 | 10 | 40 |
| AD9763 | 10 | 125 |
| AD9765 | 12 | 125 |
| AD9767 | 14 | 125 |
| AD9773 | 12 | 160 |
| AD9775 | 14 | 160 |
| AD9777 | 16 | 160 |
| AD9776 | 12 | 1000 |
| AD9778 | 14 | 1000 |
| AD9779 | 16 | 1000 |

All DACs listed have nominal bias levels of 0.5 V and use the same simple DAC modulator interface that is shown in Figure 32.

MODULATOR/DEMODULATOR OPTIONS

Table 7 lists other Analog Devices modulators and demodulators.

Table 7. Modulator/Demodulator Options

| Part No. | Modulator/Demodulator | Frequency Range (MHz) | Comments |
|---------------------------------------|-----------------------|-----------------------|---|
| AD8345 | Modulator | 140 to 1000 | External quadrature |
| AD8346 | Modulator | 800 to 2500 | |
| AD8349 | Modulator | 700 to 2700 | |
| ADL5390 | Modulator | 20 to 2400 | |
| ADL5385 | Modulator | 30 to 2200 | |
| ADL5370 | Modulator | 300 to 1000 | |
| ADL5371 | Modulator | 500 to 1500 | Includes voltage variable attenuator and automatic gain control |
| ADL5372 | Modulator | 1500 to 2500 | |
| ADL5375-05/ADL5375-15 | Modulator | 400 to 6000 | |
| ADL5386 | Modulator | 50 to 2200 | |
| AD8347 | Demodulator | 800 to 2700 | |
| AD8348 | Demodulator | 50 to 1000 | |
| ADL5380 | Demodulator | 400 to 6000 | |
| ADL5382 | Demodulator | 700 to 2700 | |
| ADL5387 | Demodulator | 30 to 2000 | |
| AD8340 | Vector mod | 700 to 1000 | |
| AD8341 | Vector mod | 1500 to 2400 | |

CHARACTERIZATION SETUP

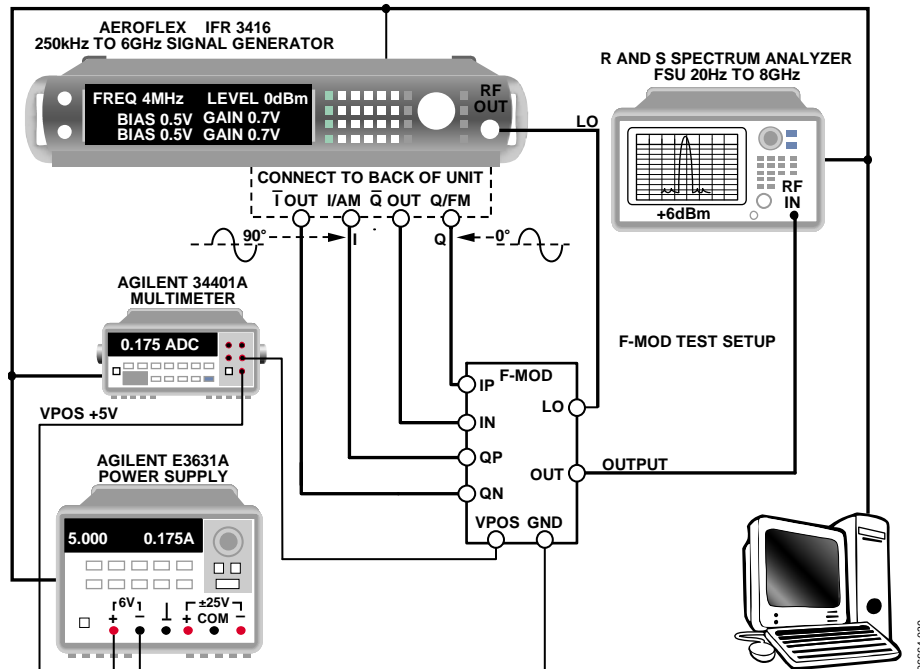


Figure 39. Characterization Bench Setup

The primary setup used to characterize the [ADL5373](#) is shown in Figure 39. This setup was used to evaluate the product as a single-sideband modulator. The Aeroflex signal generator supplied the LO and differential I and Q baseband signals to the device under test, DUT. The typical LO drive was 0 dBm. The I-channel is driven by a sine wave, and the Q-channel is driven by a cosine wave. The lower sideband is the single-sideband (SSB) output.

The majority of characterization for the [ADL5373](#) was performed using a 1 MHz sine wave signal with a 500 mV common-mode voltage applied to the baseband signals of the DUT. The baseband signal path was calibrated to ensure that the V_{IOS} and V_{QOS} offsets on the baseband inputs were minimized, as close as possible, to 0 V before connecting to the DUT.

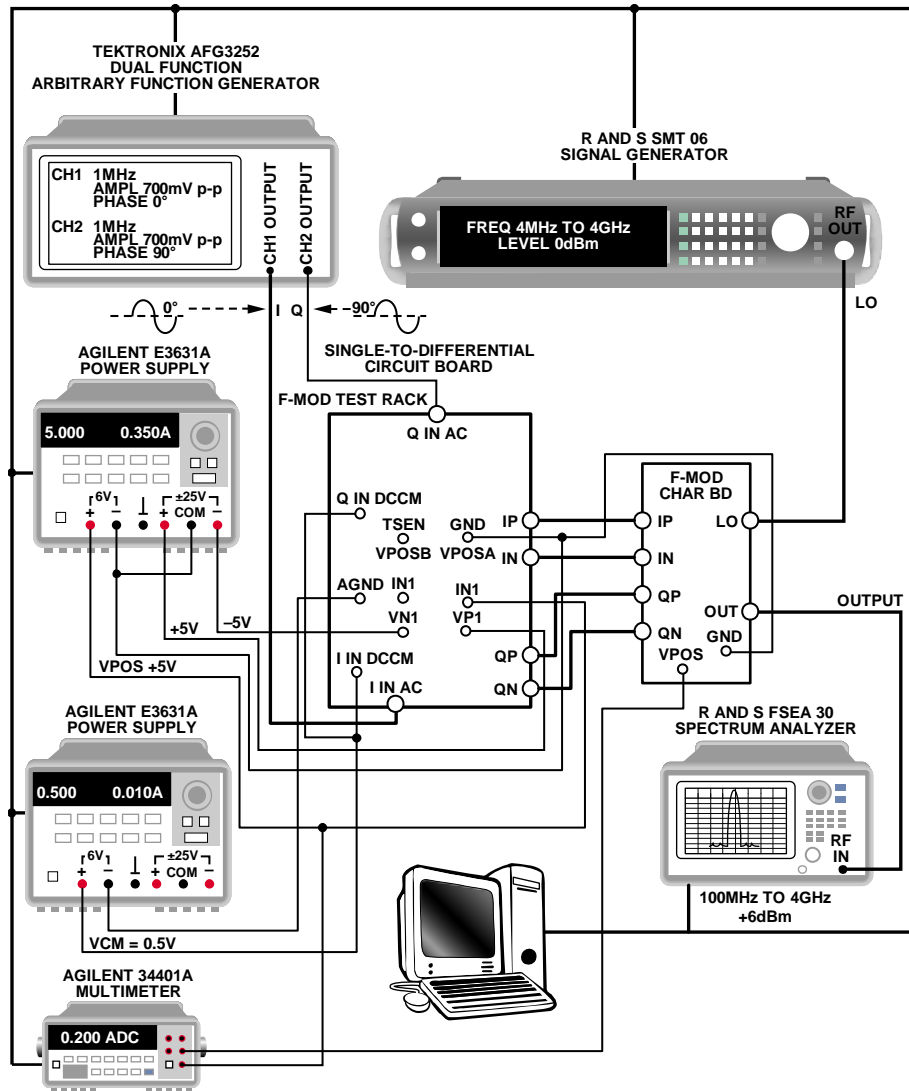


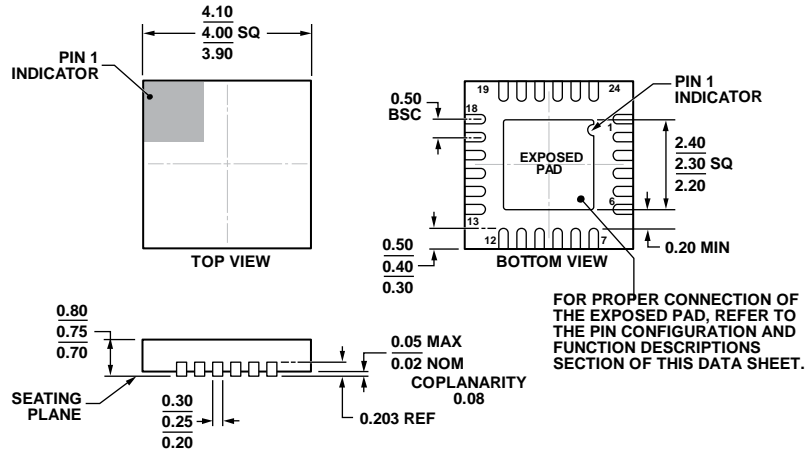
Figure 40. Setup for Baseband Frequency Sweep and Undesired Sideband Nulling

The setup used to evaluate baseband frequency sweep and undesired sideband nulling of the ADL5373 is shown in Figure 40. The interface board has circuitry that converts the single-ended I input and Q input from the arbitrary function generator to differential I and Q baseband signals with a dc bias of 500 mV.

Undesired sideband nulling was achieved through an iterative process of adjusting amplitude and phase on the Q-channel. See the Sideband Suppression Optimization section for detailed information on sideband nulling.

06664-040

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-8.

Figure 41. 24-Lead Lead Frame Chip Scale Package [LFCS]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-24-14)

Dimensions shown in millimeters

01-18-2015-A

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option | Ordering Quantity |
|--------------------|-------------------|--------------------------------|----------------|-------------------|
| ADL5373ACPZ-R7 | -40°C to +85°C | 24-Lead LFCS, 7" Tape and Reel | CP-24-14 | 1,500 |
| ADL5373ACPZ-WP | -40°C to +85°C | 24-Lead LFCS, Waffle Pack | CP-24-14 | 64 |
| ADL5373-EVALZ | | Evaluation Board | | |

¹ Z = RoHS Compliant Part.

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

moschip.ru_4

moschip.ru_6

moschip.ru_9