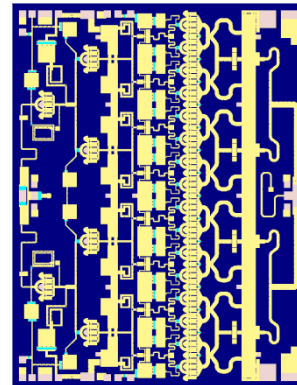


Applications

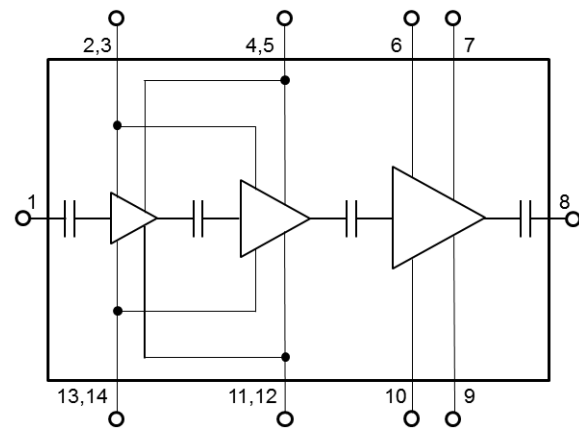
- Electronic Warfare
- Commercial and Military Radar

Product Features

- Frequency Range: 6 - 12 GHz
- Output Power: > 45 dBm ($P_{IN} = 23$ dBm)
- PAE: > 25 % ($P_{IN} = 23$ dBm)
- Large Signal Gain: > 22.0 dB
- $V_D = 20$ V, $I_{DQ} = 2.0$ A, $V_G = -2.4$ V typ.
- Chip Dimensions: 5.4 mm x 7.0 mm x 0.10 mm



Functional Block Diagram



General Description

TriQuint's TGA2590 is a wideband power amplifier fabricated on TriQuint's production 0.25um GaN on SiC process. The TGA2590 operates from 6 - 12GHz and provides greater than 30W of saturated output power with greater than 22 dB of large signal gain and greater than 25% power-added efficiency.

The TGA2590 is fully matched to 50Ω with DC blocking caps at both RF ports allowing for simple system integration. The broadband performance supports electronic warfare and radar across defense and commercial markets.

Lead-free and RoHS compliant.

Evaluation boards are available upon request.

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Pad Configuration

Pad No.	Symbol
1	RF In
2, 14	V_{G1}
3, 13	V_{G2}
4, 12	V_{D1}
5, 11	V_{D2}
6, 10	V_{G3}
7, 9	V_{D3}
8	RF Out

Ordering Information

Part	ECCN	Description
TGA2590	3A001.b.2.b	6-12 GHz 30W PA

Absolute Maximum Ratings

Parameter	Value
Drain Voltage (V_D)	40 V
Gate Voltage Range (V_G)	-8 to 0 V
Drain Current w/ RF Drive (I_{D_DRIVE})	8.0
Gate Current (I_G)	-20 to 60 mA
Power Dissipation (P_{DISS})	115 W
Input Power, CW, 50 Ω , 85 °C (P_{IN})	30 dBm
Input Power, CW, 6:1 VSWR, 85 °C (P_{IN})	27 dBm
Channel temperature (T_{CH})	275 °C
Mounting Temperature (30 Seconds maximum)	320 °C
Storage Temperature	-55 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value
Drain Voltage (V_D)	20 V
Drain Current (I_{DQ})	2.0 A
Drain Current w/ RF Drive (I_{D_DRIVE})	< 7.0 A
Gate Voltage (V_G), typ.	- 2.4 V
Input Power (P_{IN})	+17 to +25 dBm
Load VSWR	< 2.0:1

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: 25 °C, $V_D = 20$ V, $I_{DQ} = 2.0$ A, $V_G = -2.4$ V typ.

Parameter	Min	Typical	Max	Units
Operational Frequency Range	6.0		12.0	GHz
Output Power ($P_{IN} = 23$ dBm)		46.0		dBm
Power Added Efficiency ($P_{IN} = 23$ dBm)		32.5		%
Input Return Loss		13.0		dB
Output Return Loss		11.0		dB
Output Power Temperature Coefficient		-0.02		dBm/ °C
Input Power	17.0		25.0	dBm
Load VSWR			2.0:1	

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Thermal and Reliability Information

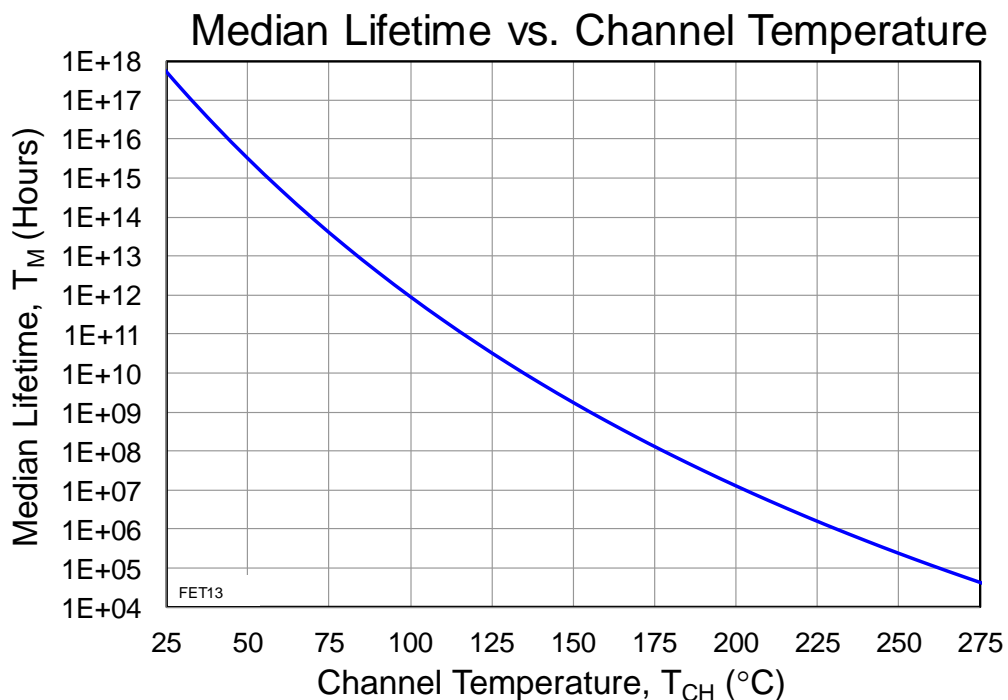
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) ⁽¹⁾	$T_{BASE} = 85^{\circ}C, V_D = 20V, I_{D_Drive} = 5.5 A,$ $P_{IN} = 23 dBm, P_{OUT} = 44 dBm, P_{DISS} =$ $85 W$	1.3	$^{\circ}C/W$
Channel Temperature (T_{CH})		201	$^{\circ}C$
Median Lifetime (T_M)		1.16E7	Hrs
Thermal Resistance (θ_{JC}) ⁽¹⁾	$T_{BASE} = 85^{\circ}C, V_D = 25V, I_{D_Drive} = 5.8 A,$ $P_{IN} = 23 dBm, P_{OUT} = 45.6 dBm, P_{DISS} =$ $109 W$	1.4	$^{\circ}C/W$
Channel Temperature (T_{CH})		237	$^{\circ}C$
Median Lifetime (T_M)		6.15E5	Hrs

Notes:

- MMIC soldered to 20 mil thick Cu-Mo carrier plate using 1.5 mil thick AuSn solder. Thermal resistance is determined from the channel to the back of the carrier plate (fixed 85 $^{\circ}C$ temp.).

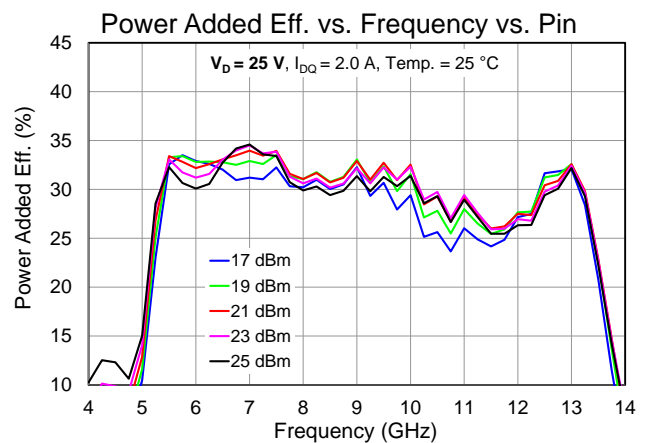
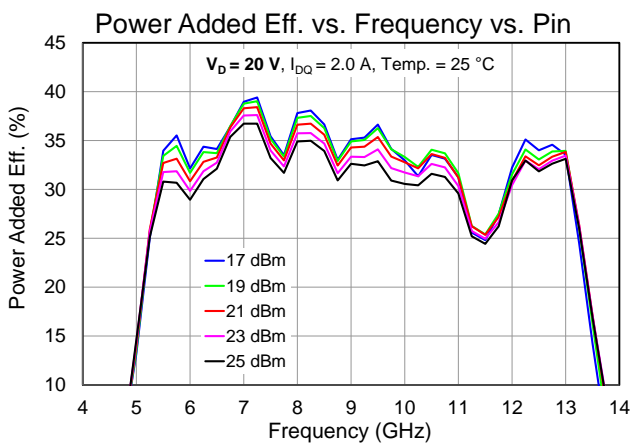
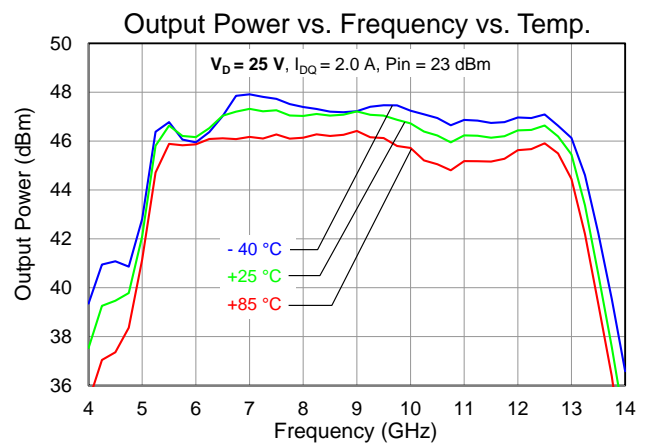
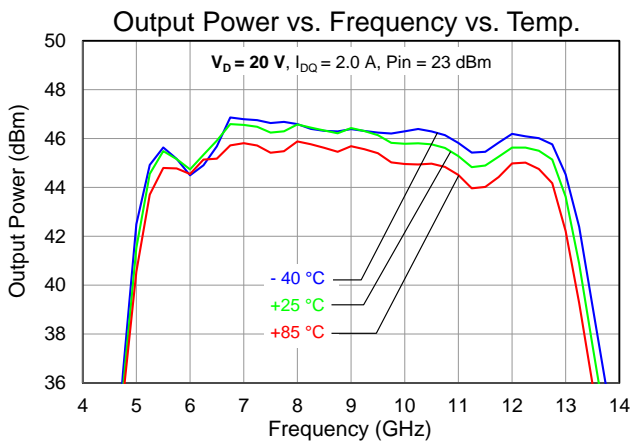
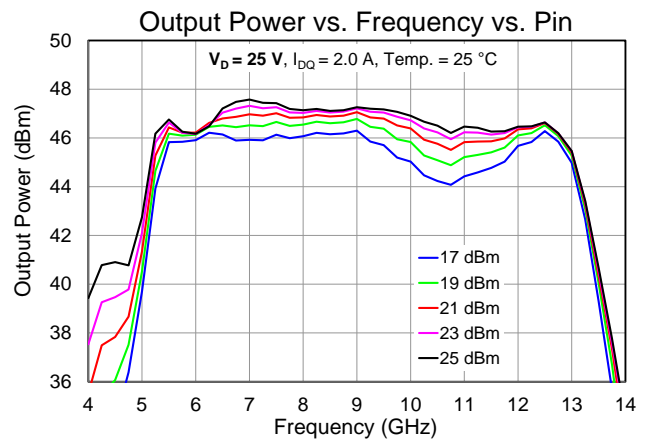
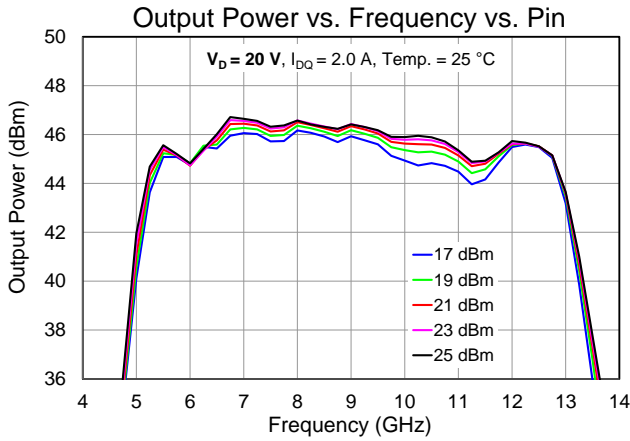
Median Lifetime

Test Conditions: 40 V; Failure Criteria = 10% reduction in I_{D_MAX}



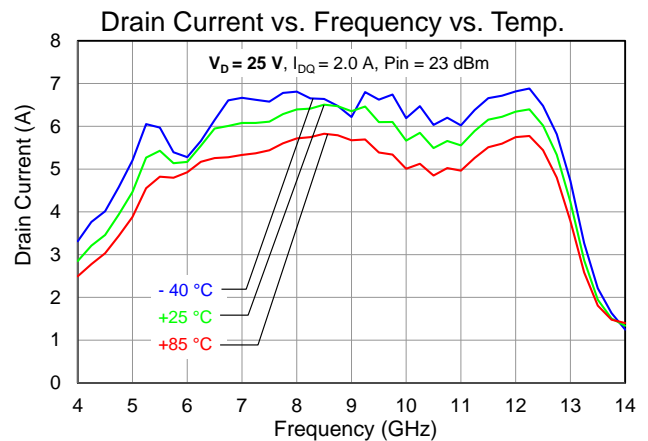
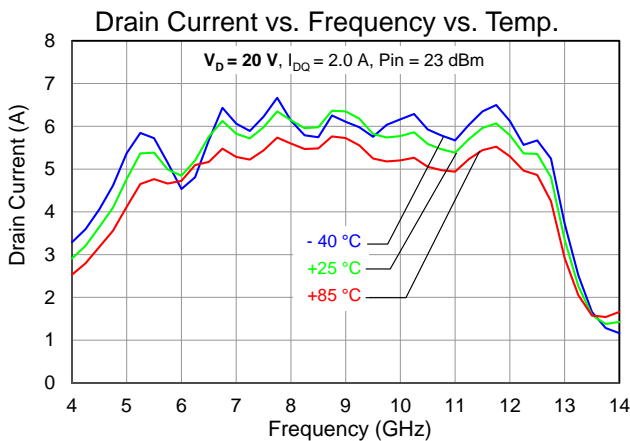
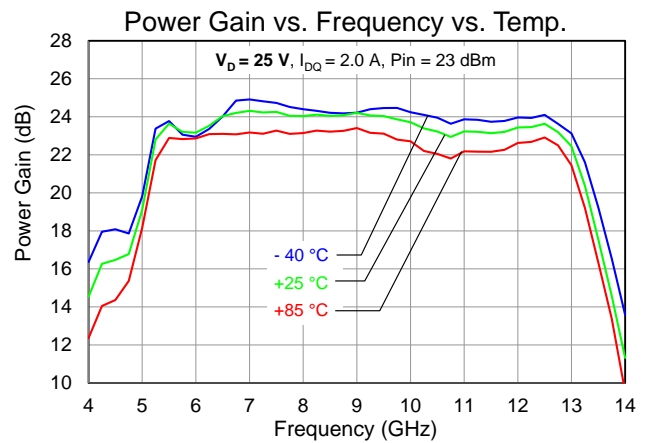
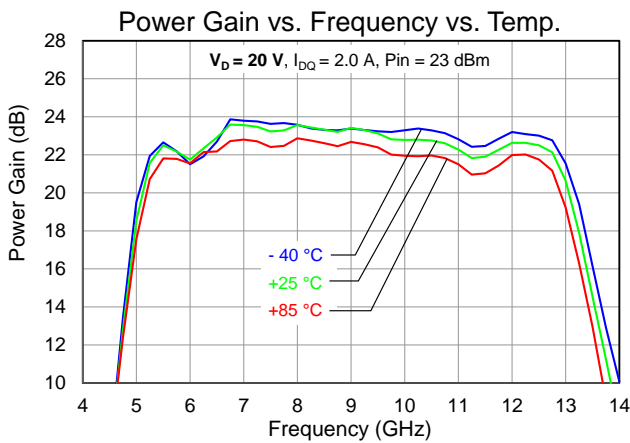
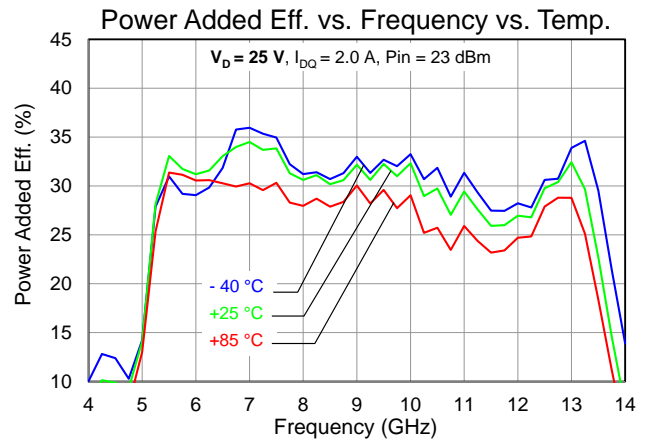
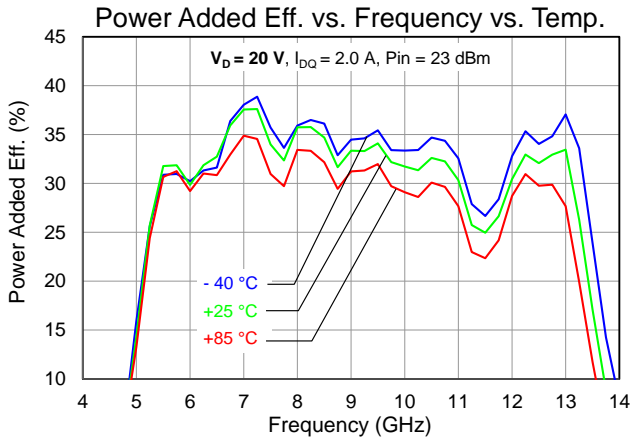
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Typical Performance



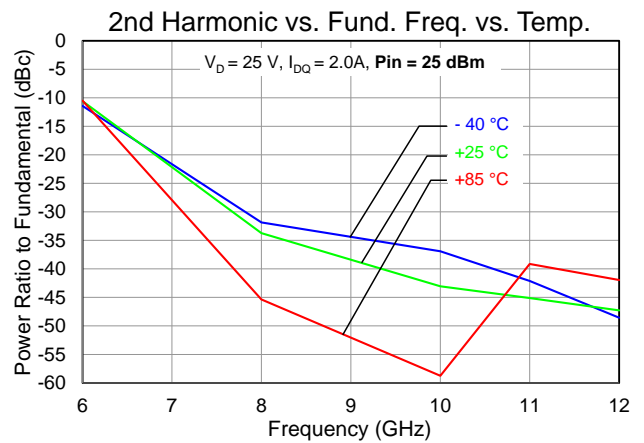
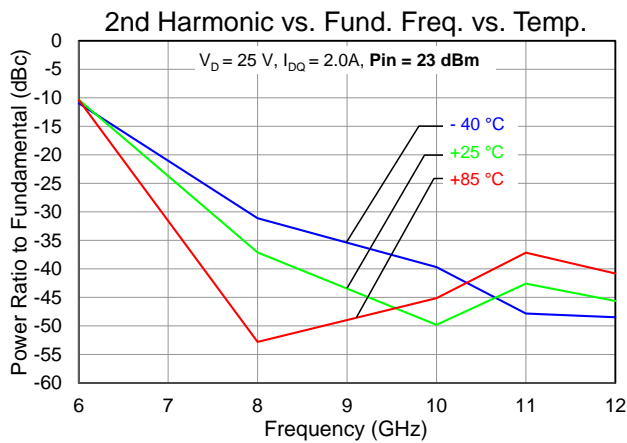
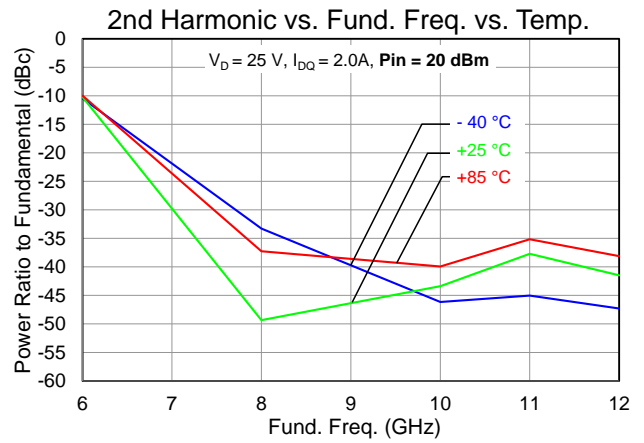
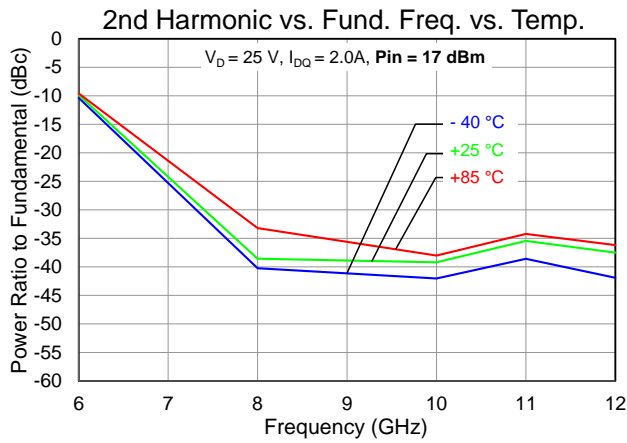
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Typical Performance



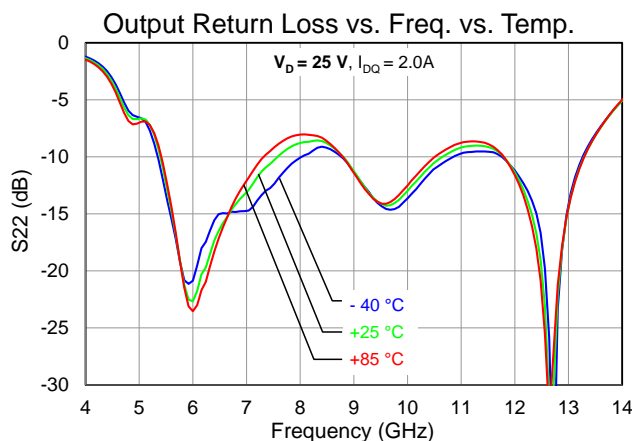
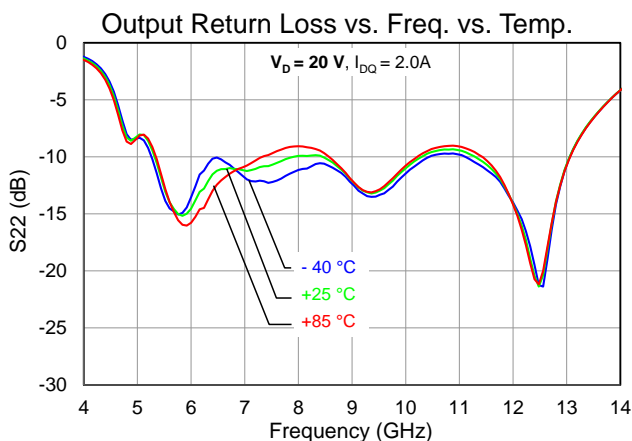
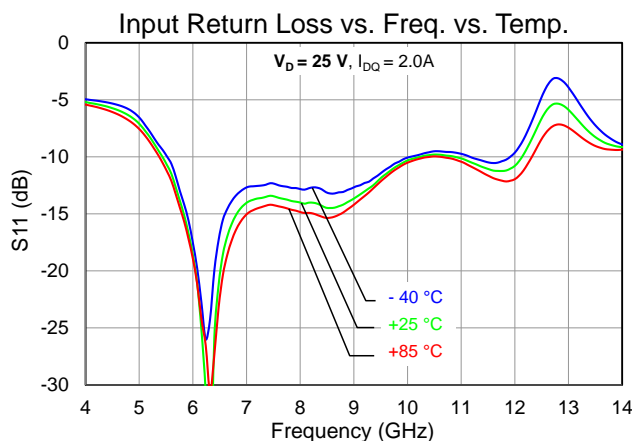
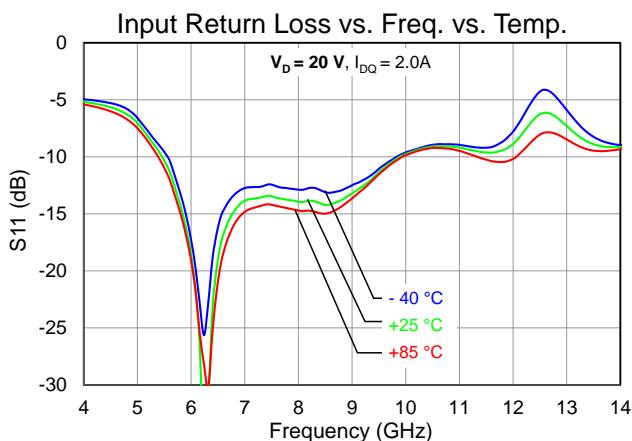
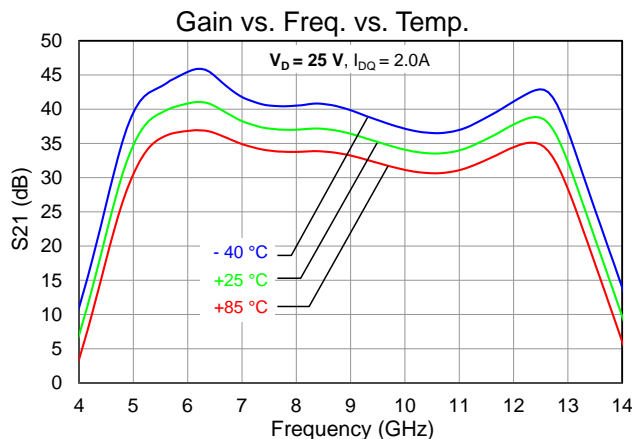
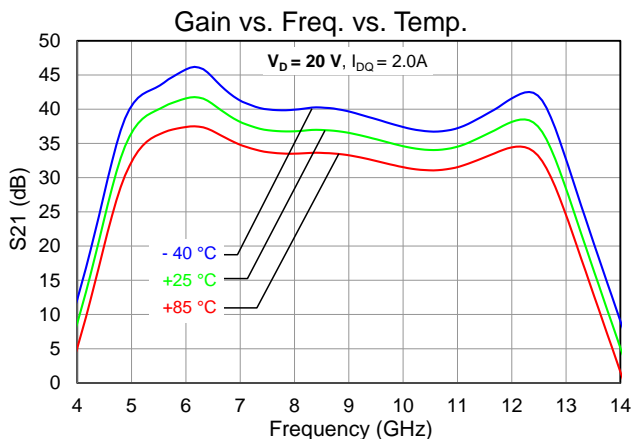
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Typical Performance



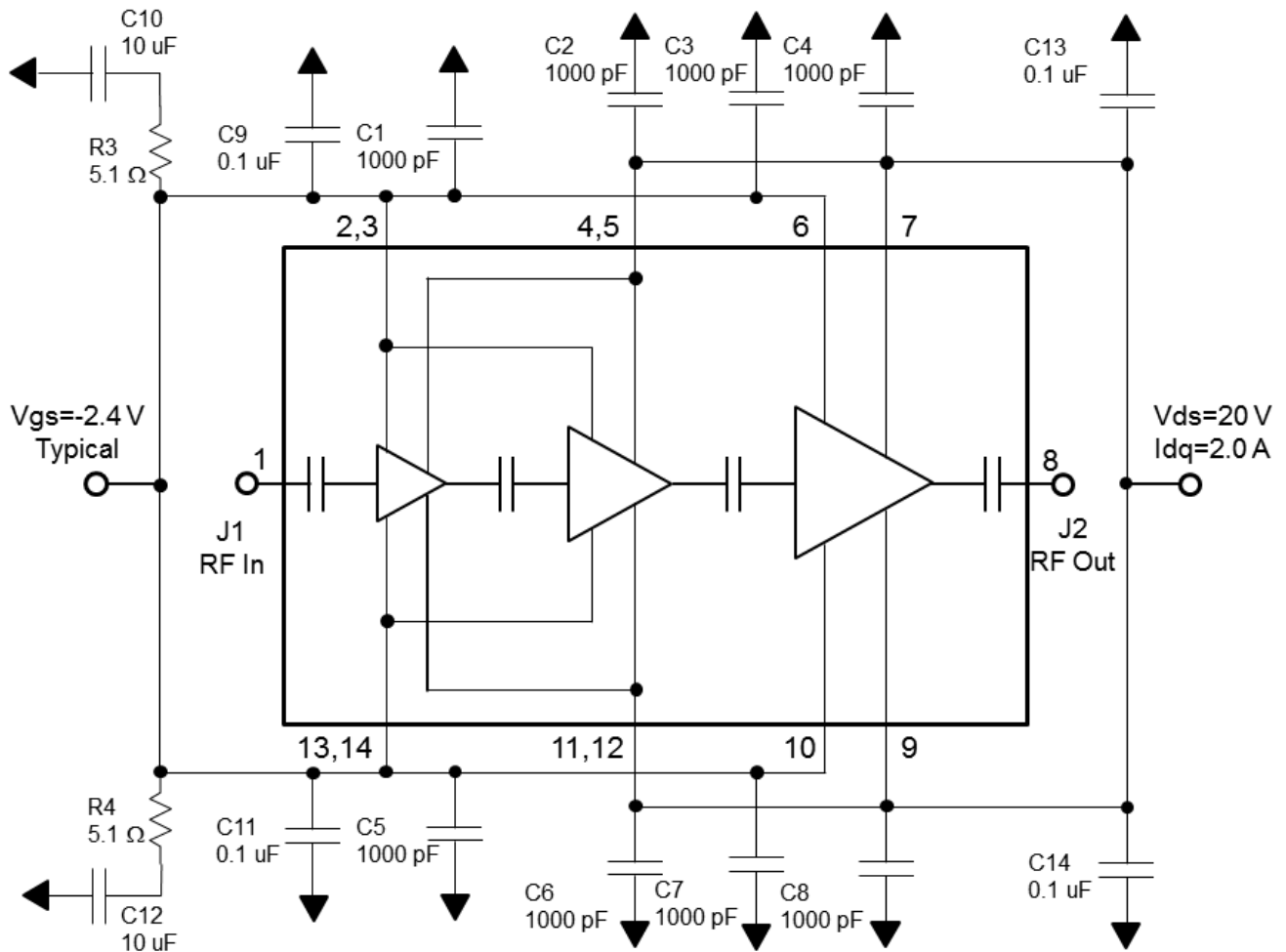
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Typical Performance



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Application Circuit



Bias-up Procedure

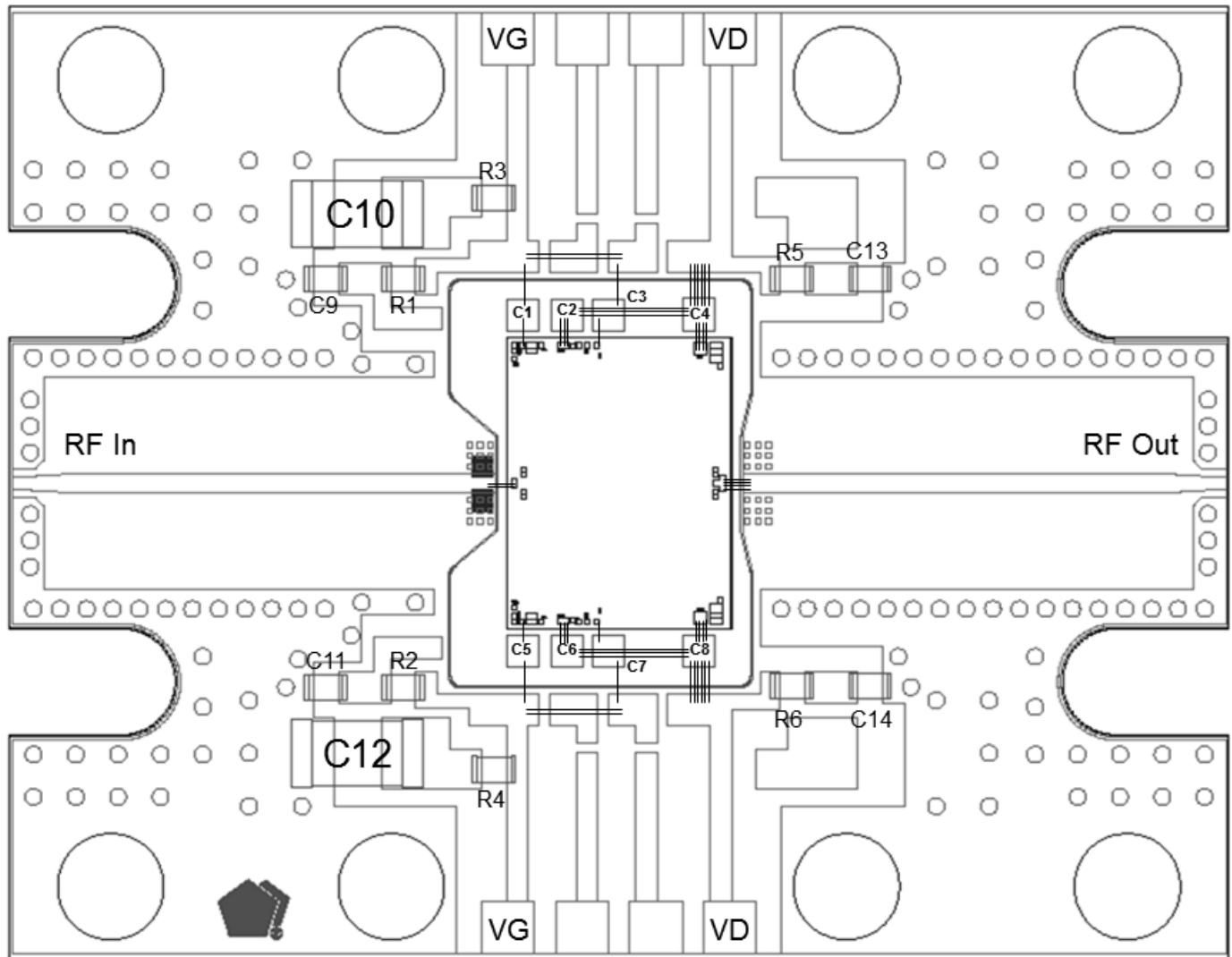
1. Set I_D limit to 8.0, I_G limit to 150mA
2. Set V_G to -5.0V
3. Set V_D +20V
4. Adjust V_G more positive until $I_{DQ} = 2.0$ A
5. Apply RF signal

Bias-down Procedure

1. Turn off RF signal
2. Reduce V_G to -5.0V. Ensure $I_{DQ} \sim 0$ mA
3. Set V_D to 0V
4. Turn off V_D supply
5. Turn off V_G supply

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Evaluation Board

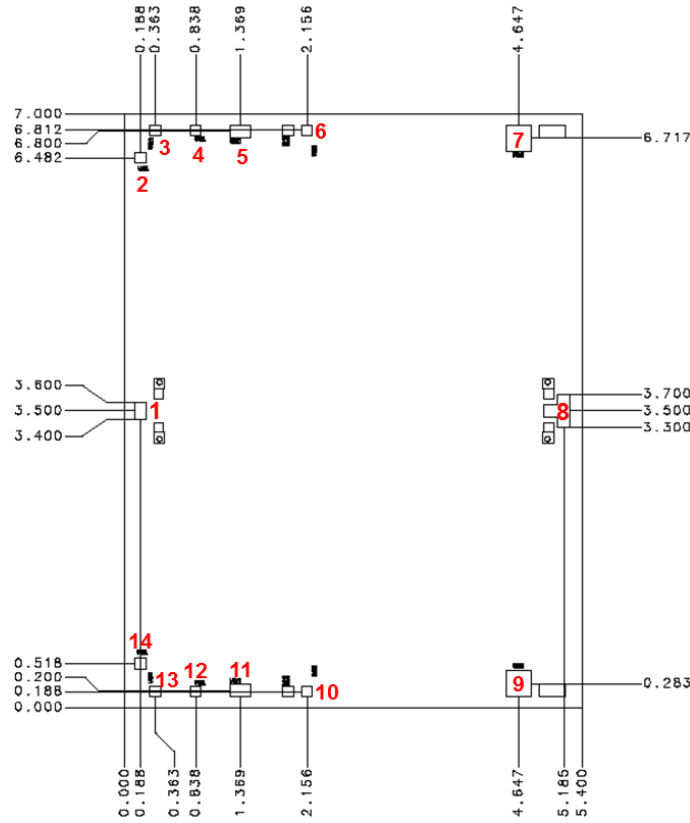


Bill of Materials

Ref. Designation	Value	Description	Manufacturer	Part Number
C1 – C8	1000 pF	SLC, 50V	Various	
C9, C11, C13, C14	0.1 uF	Cap, 0402, 50V, 10%, X7R	Various	
C10, C12	10 uF	Cap, 1206, 50V, 10%, X7R	Various	
R1, R2, R5, R6	0 Ω	Res, 0402	Various	
R3 – R4	5.1 Ω	Res, 0402	Various	

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Mechanical Drawing & Bond Pad Description



Unit: millimeters

Thickness: 0.10

Die x, y size tolerance: +/- 0.050

Chip edge to bond pad dimensions are shown to center of pad

Ground is backside of die

Bond Pad	Symbol	Description
1	RF In	Input; matched to 50 ohms; AC coupled.
2, 14	V_{G1}	Gate voltage, V_{G1} top and bottom. V_{G1} top (pad 2) internally connected to V_{G2} top (pad 3); V_{G1} bottom (pad 14) internally connected to V_{G2} bottom (pad 13).
3, 13	V_{G2}	Gate voltage, V_{G2} top and bottom. Bias network required; must be biased from both sides. V_{G1} top (pad 2) internally connected to V_{G2} top (pad 3); V_{G1} bottom (pad 14) internally connected to V_{G2} bottom (pad 13).
4, 12	V_{D1}	Drain voltage, V_{D1} top and bottom. Bias network required; must be biased from both sides.
5, 11	V_{D2}	Drain voltage, V_{D2} top and bottom. Bias network required; must be biased from both sides.
6, 10	V_{G3}	Gate voltage, V_{G3} top and bottom. Bias network required; must be biased from both sides.
7, 9	V_{D3}	Drain voltage, V_{D3} top and bottom. Bias network required; must be biased from both sides.
8	RF Out	Output; matched to 50 ohms; AC coupled.

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Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment (i.e. epoxy) can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300°C to 3-4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

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Product Compliance Information

ESD Sensitivity Ratings



Caution! ESD-Sensitive Device

ESD Rating: TBD
Value: TBD
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ECCN

US Department of State: 3A001.b.2.b

Solderability

Use only AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3-4 minutes, maximum.

RoHS-Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free

Contact Information

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