Ordering number : ENA2199

LE25U81AQE

ON Semiconductor®

http://onsemi.com

CMOS LSI

8M-bit (1024K x 8) Serial Flash Memory

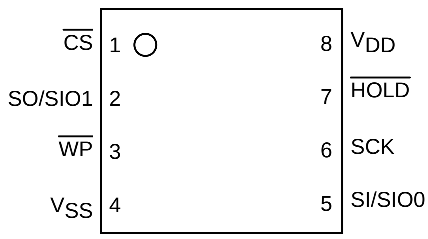
Overview

The LE25U81AQE is a SPI bus flash memory device with a 8M bit (1024K × 8-bit) configuration that adds a high performance Dual output and Dual I/O function. It uses a single 2.5V power supply. While making the most of the features inherent to a serial flash memory device, the LE25U81AQE is housed in an 8-pin ultra-miniature package. All these features make this device ideally suited to storing program in applications such as portable information devices, which are required to have increasingly more compact dimensions. The LE25U81AQE also has a small sector erase capability which makes the device ideal for storing parameters or data that have fewer rewrite cycles and conventional EEPROMs cannot handle due to insufficient capacity.

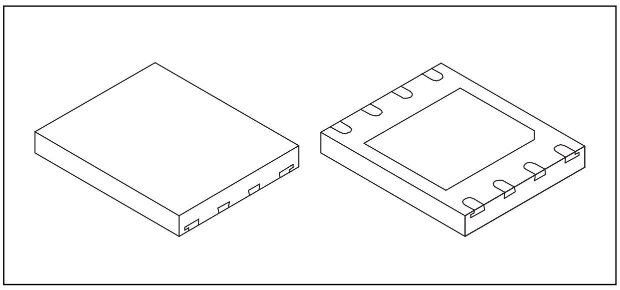
Features

- Read/write operations enabled by single 2.5V power supply : 2.3 to 2.7V supply voltage range
- Operating frequency : 40MHz
- Temperature range : –40 to +85°C
- Serial interface : SPI mode 0, mode 3 supported
- Sector size : 4K bytes/small sector, 64K bytes/sector
- Small sector erase, sector erase, chip erase functions
- Page program function (256 bytes / page)
- Block protect function
- Data retention period : 20 years
- Status functions : Ready/busy information, protect information
- Highly reliable read/write
  - Number of rewrite times: 100,000 times
  - Small sector erase time : 40ms (typ.), 150ms (max.)
  - Sector erase time : 80ms (typ.), 250ms (max.)
  - Chip erase time : 500ms (typ.), 6.0s (max.)
  - Page program time : 0.3ms/256 bytes (typ.), 0.5ms/256 bytes (max.)
- Package : VSON8T(6.0 × 5.0) CASE 509AG

Figure 1 Pin Assignments



Top view



VSON8T(6.0X5.0)

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ORDERING INFORMATION

See detailed ordering and shipping information on page 22 of this data sheet.

Figure 2 Block Diagram

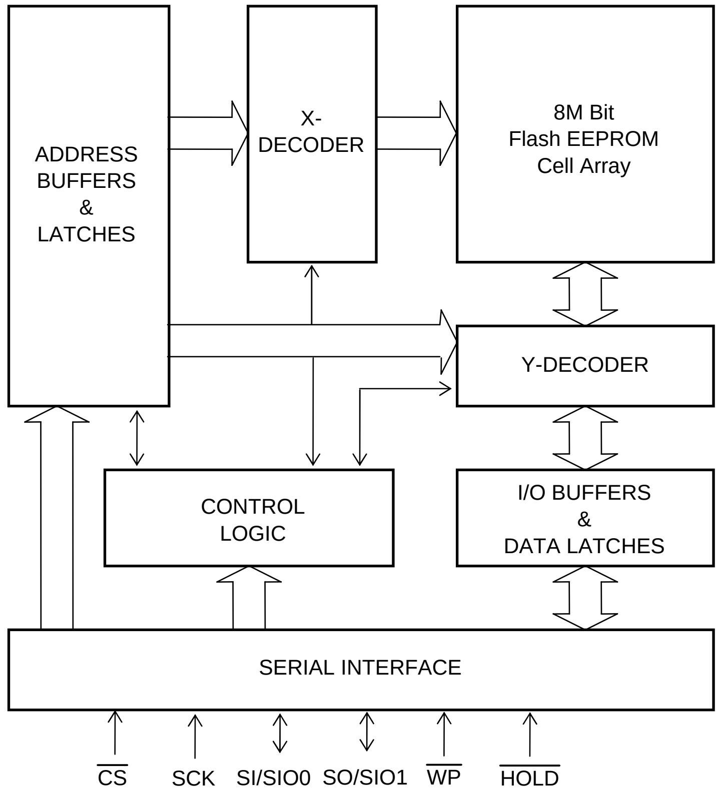


Table 1 Pin Description

Symbol	Pin Name	Description
SCK	Serial clock	This pin controls the data input/output timing. The input data and addresses are latched synchronized to the rising edge of the serial clock, and the data is output synchronized to the falling edge of the serial clock.
SI/SIO0	Serial data input / Serial data input output	The data and addresses are input from this pin, and latched internally synchronized to the rising edge of the serial clock. It changes into the output pin at Dual Output and it changes into the input output pin at Dual I/O.
SO/SIO1	Serial data input / Serial data input output	The data stored inside the device is output from this pin synchronized to the falling edge of the serial clock. It changes into the output pin at Dual Output and it changes into the input output pin at Dual I/O.
$\overline{CS}$	Chip select	The device becomes active when the logic level of this pin is low; it is deselected and placed in standby status when the logic level of the pin is high.
$\overline{WP}$	Write protect	The status register write protect (SRWP) takes effect when the logic level of this pin is low.
$\overline{HOLD}$	Hold	Serial communication is suspended when the logic level of this pin is low.
V_{DD}	Power supply	This pin supplies the 2.3 to 2.7V supply voltage.
V_{SS}	Ground	This pin supplies the 0V supply voltage.

Device Operation

The read, erase, program and other required functions of the device are executed through the command registers. The serial I/O corrugate is shown in Figure 3 and the command list is shown in Table 2. At the falling $\overline{CS}$ edge the device is selected, and serial input is enabled for the commands, addresses, etc. These inputs are normalized in 8 bit units and taken into the device interior in synchronization with the rising edge of SCK, which causes the device to execute operation according to the command that is input.
The LE25U81AQE supports both serial interface SPI mode 0 and SPI mode 3. At the falling $\overline{CS}$ edge, SPI mode 0 is automatically selected if the logic level of SCK is low, and SPI mode 3 is automatically selected if the logic level of SCK is high.

Figure 3 I/O waveforms

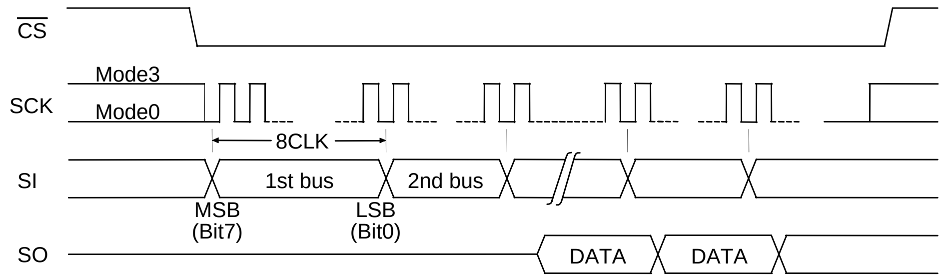


Table 2 Command Settings

Command	1st bus cycle	2nd bus cycle	3rd bus cycle	4th bus cycle	5th bus cycle	6th bus cycle	Nth bus cycle
Read	03h	A23-A16	A15-A8	A7-A0	RD *1	RD *1	RD *1
High Speed Read	0Bh	A23-A16	A15-A8	A7-A0	X	RD *1	RD *1
Dual Output Read	3Bh	A23-A16	A15-A8	A7-A0	Z	RD *1	RD *1
Dual I/O Read	BBh	A23-A8	A7-A0,X, Z	RD *1	RD *1	RD *1	RD *1
Small sector erase	20h / D7h	A23-A16	A15-A8	A7-A0			
Sector erase	D8h	A23-A16	A15-A8	A7-A0			
Chip erase	60h / C7h						
Page program	02h	A23-A16	A15-A8	A7-A0	PD *2	PD *2	PD *2
Write enable	06h						
Write disable	04h						
Power down	B9h						
Status register read	05h						
Status register write	01h	DATA					
JEDEC ID read	9Fh						
ID read	ABh	X	X	X			
power down	B9h						
Exit power down mode	ABh						

Explanatory notes for Table 2
"X" signifies "don't care" (that is to say, any value may be input).
The "h" following each code indicates that the number given is in hexadecimal notation.
Addresses A23 to A20 for all commands are "Don't care".
*1: "RD" stands for read data. *2: "PD" stands for page program data.

Table 3 Memory Organization

8M Bit

sector(64KB)	small sector(4KB)	address space(A23 to A0)	
15	255	0FF000h	0FFFFFh
	to		
	240	0F0000h	0F0FFFh
14 to 6	239	0EF000h	0EFFFFh
	To		
	96	060000h	060FFFh
5	95	05F000h	05FFFFh
	to		
	80	050000h	050FFFh
4	79	04F000h	04FFFFh
	to		
	64	040000h	040FFFh
3	63	03F000h	03FFFFh
	to		
	48	030000h	030FFFh
2	47	02F000h	02FFFFh
	to		
	32	020000h	020FFFh
1	31	01F000h	01FFFFh
	to		
	16	010000h	010FFFh
0	15	00F000h	00FFFFh
	to		
	2	002000h	002FFFh
	1	001000h	001FFFh
	0	000000h	000FFFh

Description of Commands and Their Operations

A detailed description of the functions and operations corresponding to each command is presented below.

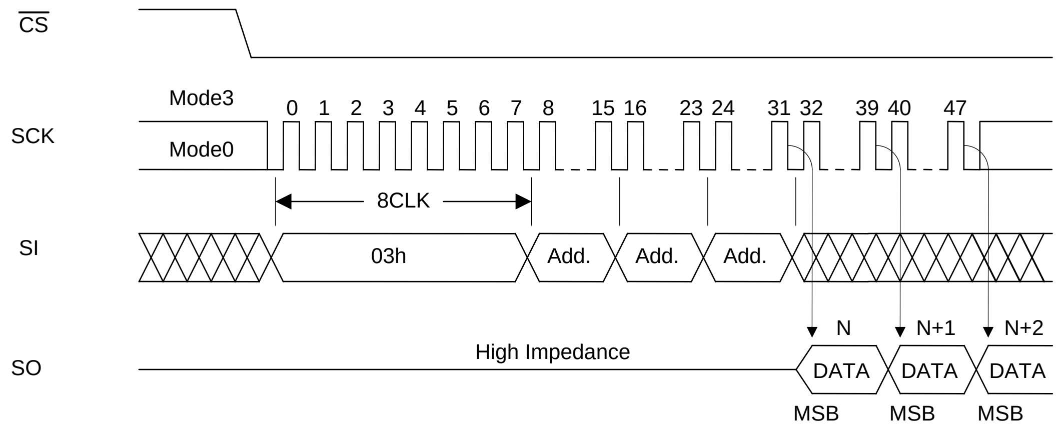
1. Standard SPI read

There are two read commands, the standard SPI read command and High-speed read command.

1-1. Read command

Consisting of the first through fourth bus cycles, the 4 bus cycle read command inputs the 24-bit addresses following (03h). The data is output from SO on the falling clock edge of fourth bus cycle bit 0 as a reference. "Figure 4-a Read" shows the timing waveforms.

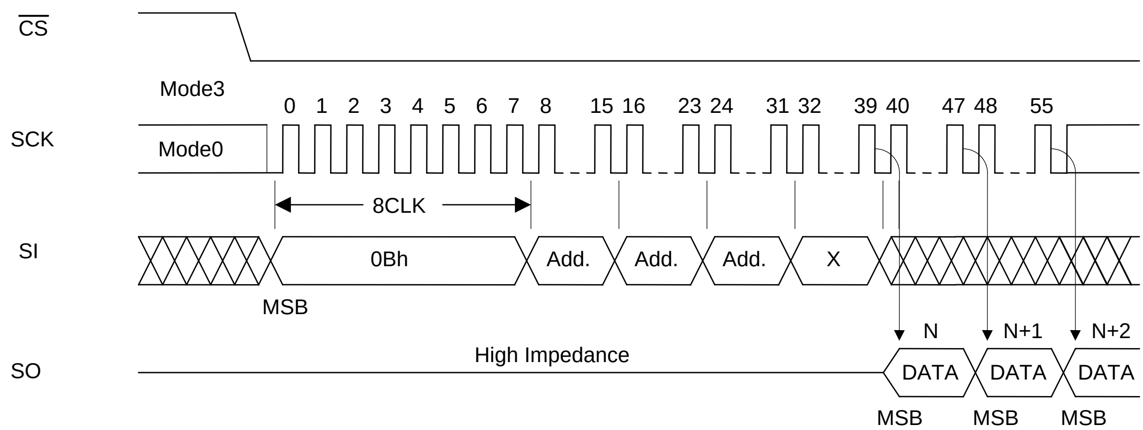
Figure 4-a Read



1-2. High-speed read command

Consisting of the first through fifth bus cycles, the High-speed read command inputs the 24-bit addresses and 8 dummy bits following (0Bh). The data is output from SO using the falling clock edge of fifth bus cycle bit 0 as a reference. "Figure 4-b High-speed Read" shows the timing waveforms.

Figure 4-b High-speed Read



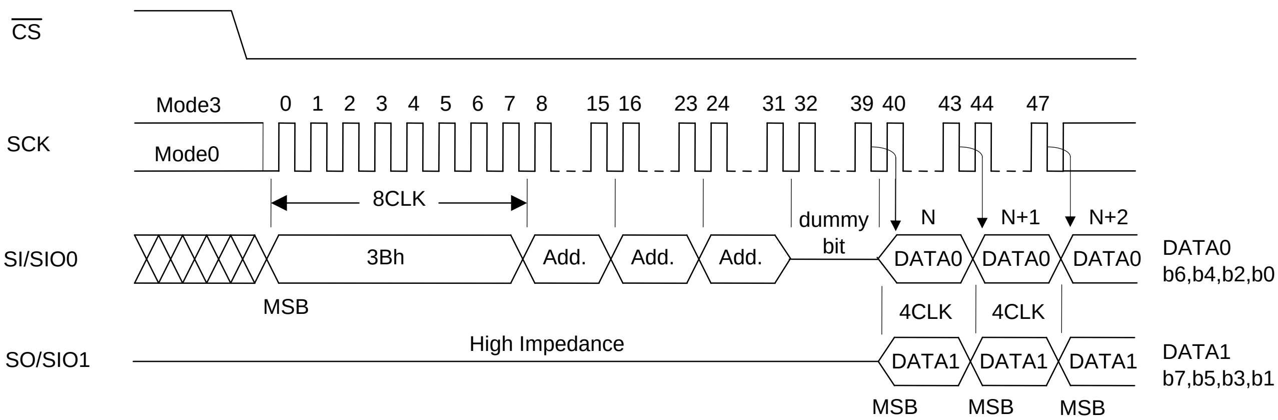
2. Dual read

There are two Dual read commands, the Dual Output read command and the Dual I/O read command. They achieve the twice speed-up from a High-speed read command.

2-1. Dual Output read command

The Dual Output read command changes SI/SIO0 into the output pin function in addition to SO/SIO1, makes the data output x2 bit and has achieved a high-speed output. Consisting of the first through fifth bus cycles, the Dual Output read command inputs the 24-bit addresses and 8 dummy bits following (3Bh). DATA1 (Bit7, BIt5, Bit3 and Bit1) is output from SI/SIO0 and DATA0 (Bit6, Bit4, Bit2 and Bit0) is output from SO/SIO1 on the falling clock edge of fifth bus cycle bit 0 as a reference. "Figure 5-a Dual Output read" shows the timing waveforms.

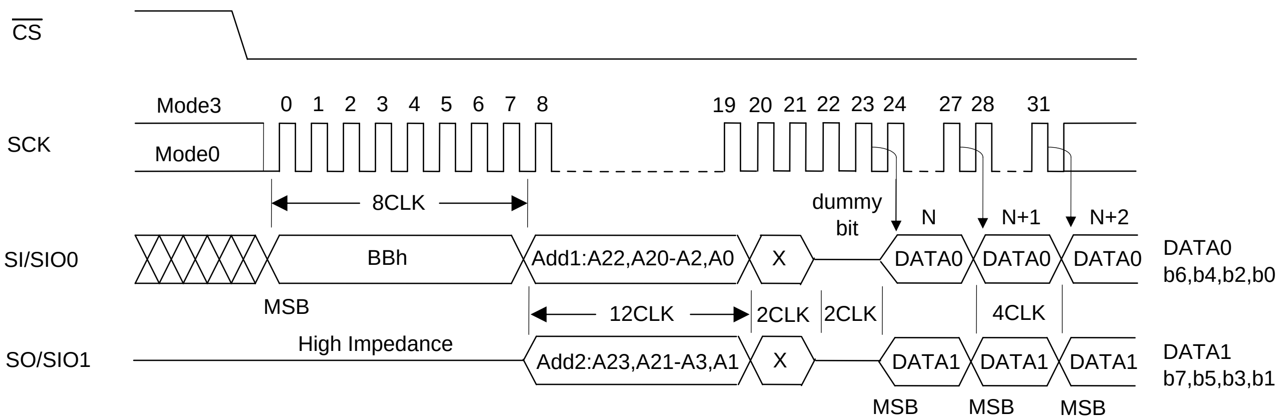
Figure 5-a Dual Output read



2-2. Dual I/O read command

The Dual I/O read command changes SI/SIO0 and SO/SIO1 into the input output pin function, makes the data input and output x2 bit and has achieved a high-speed output. Consisting of the first through third bus cycles, the Dual I/O read command inputs the 24-bit addresses and 4 dummy clocks following (BBh). The format of the address input and the dummy bit input is the x2 bit input. Add1 (A23, A21, -, A3 and A1) is input from S0/SIO1 and Add0 (A22, A20, -, A2 and A0) is input from SI/SIO0. 2CLK of the latter half of the dummy clock is in the state of high impedance, the controller can switch I/O for this period. DATA1 (Bit7, BIt5, Bit3 and Bit1) is output from SI/SIO0 and DATA0 (Bit6, Bit4, Bit2 and Bit0) is output from SO/SIO1 on the falling clock edge of third bus cycle bit 0 as a reference. "Figure 5-b Dual I/O Read" shows the timing waveforms.

Figure 5-b Dual I/O Read



When SCK is input continuously after the read command has been input and the data in the designated addresses has been output, the address is automatically incremented inside the device while SCK is being input, and the corresponding data is output in sequence. If the SCK input is continued after the internal address arrives at the highest address (FFFFFh), the internal address returns to the lowest address (00000h), and data output is continued. By setting the logic level of CS to high, the device is deselected, and the read cycle ends. While the device is deselected, the output pin SO is in a high-impedance state.

3. Status Registers

The status registers hold the operating and setting statuses inside the device, and this information can be read (Status Register read) and the protect information can be rewritten (Status Register write). There are 8 bits in total, and "Table 4 Status registers" gives the significance of each bit.

Table 4 Status Registers

Bit	Name	Logic	Function	Power-on Time Information
Bit0	$\overline{\text{RDY}}$	0	Ready	0
		1	Erase/Program	
Bit1	WEN	0	Write disabled	0
		1	Write enabled	
Bit2	BP0	0	Block protect information Protecting area switch	Nonvolatile information
		1		
Bit3	BP1	0		Nonvolatile information
		1		
Bit4	BP2	0		Nonvolatile information
		1		
Bit5	TB	0	Block protect Upper side/Lower side switch	Nonvolatile information
		1		
Bit6	CMP	0	Block protect Reverse switch	Nonvolatile information
		1		
Bit7	SRWP	0	Status register write enabled	Nonvolatile information
		1	Status register write disabled	

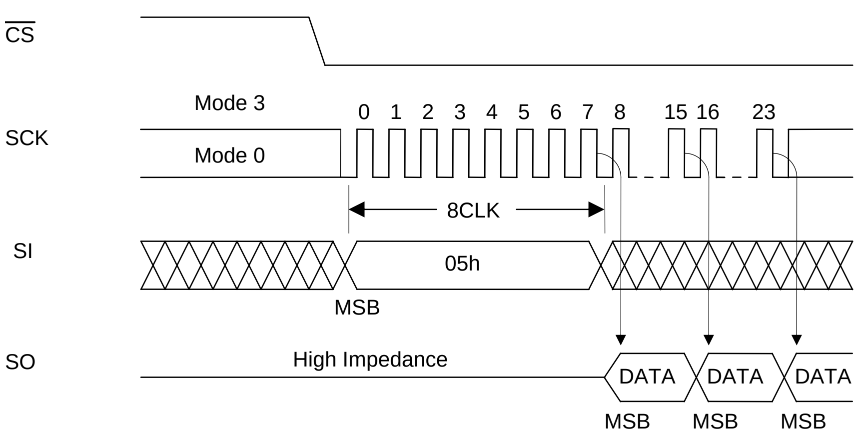
3-1. Status register read

The contents of the status registers can be read using the status register read command. This command can be executed even during the following operations.

- Small sector erase, sector erase, chip erase
- Page program
- Status register write

"Figure 6 Status Register Read" shows the timing waveforms of status register read. Consisting only of the first bus cycle, the status register command outputs the contents of the status registers synchronized to the falling edge of the clock (SCK) with which the eighth bit of (05h) has been input. In terms of the output sequence, SRWP (bit 7) is the first to be output, and each time one clock is input, all the other bits up to $\overline{\text{RDY}}$ (bit 0) are output in sequence, synchronized to the falling clock edge. If the clock input is continued after $\overline{\text{RDY}}$ (bit 0) has been output, the data is output by returning to the bit (SRWP) that was first output, after which the output is repeated for as long as the clock input is continued. The data can be read by the status register read command at any time (even during a program or erase cycle).

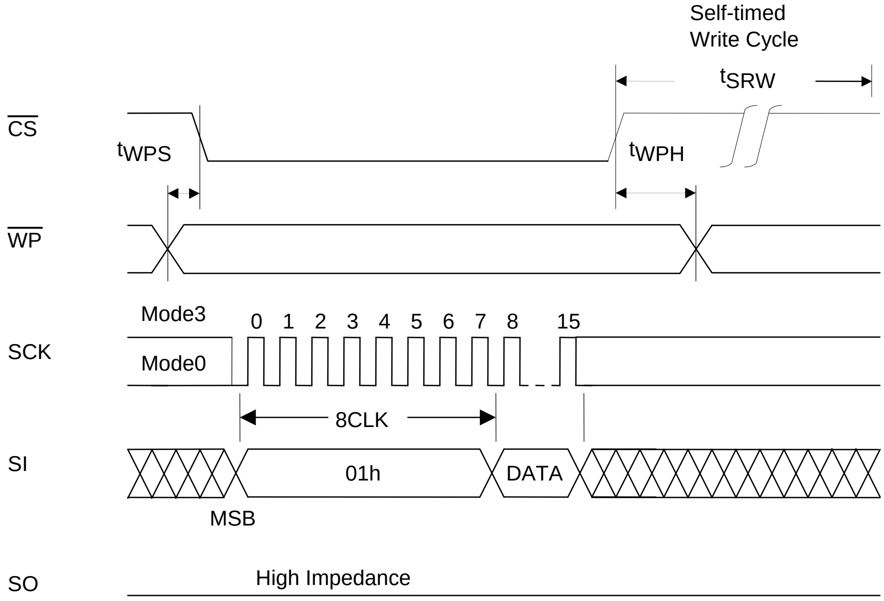
Figure 6 Status Register Read



3-2. Status register write

The information in status registers BP0, BP1, BP2, TB, CMP and SRWP can be rewritten using the status register write command. $\overline{\text{RDY}}$ and WEN are read-only bits and cannot be rewritten. The information in bits BP0, BP1, BP2, TB, CMP and SRWP is stored in the non-volatile memory, and when it is written in these bits, the contents are retained even at power-down. "Figure 7 Status Register Write" shows the timing waveforms of status register write, and Figure 20 shows a status register write flowchart. Consisting of the first and second bus cycles, the status register write command initiates the internal write operation at the rising $\overline{\text{CS}}$ edge after the data has been input following (01h). Erase and program are performed automatically inside the device by status register write so that erasing or other processing is unnecessary before executing the command. By the operation of this command, the information in bits BP0, BP1, BP2, TB, CMP and SRWP can be rewritten. Since bits $\overline{\text{RDY}}$ (bit 0) and WEN (bit 1) of the status register cannot be written, no problem will arise if an attempt is made to set them to any value when rewriting the status register. Status register write ends can be detected by $\overline{\text{RDY}}$ of status register read. To initiate status register write, the logic level of the $\overline{\text{WP}}$ pin must be set high and status register WEN must be set to "1".

Figure 7 Status Register Write



3-3. Contents of each status register

$\overline{\text{RDY}}$ (Bit 0)

The $\overline{\text{RDY}}$ register is for detecting the write (program, erase and status register write) end. When it is "1", the device is in a busy state, and when it is "0", it means that write is completed.

WEN (bit 1)

The WEN register is for detecting whether the device can perform write operations. If it is set to "0", the device will not perform the write operation even if the write command is input. If it is set to "1", the device can perform write operations in any area that is not block-protected.
WEN can be controlled using the write enable and write disable commands. By inputting the write enable command (06h), WEN can be set to "1"; by inputting the write disable command (04h), it can be set to "0." In the following states, WEN is automatically set to "0" in order to protect against unintentional writing.

- At power-on
- Upon completion of small sector erase, sector erase or chip erase
- Upon completion of page program
- Upon completion of status register write

* If a write operation has not been performed inside the LE25U81AQE because, for instance, the command input for any of the write operations (small sector erase, sector erase, chip erase, page program, or status register write) has failed or a write operation has been performed for a protected address, WEN will retain the status established prior to the issue of the command concerned. Furthermore, its state will not be changed by a read operation.

BP0, BP1, BP2, TB, CMP (Bits 2, 3, 4, 5, 6)

Block protect BP0, BP1, BP2, TB and CMP are status register bits that can be rewritten, and the memory space to be protected can be set depending on these bits. For the setting conditions, refer to "Table 5 Protect level setting conditions".
BP0, BP1, and BP2 are used to select the protected area, TB to allocate the protected area to the higher-order address area or lower-order address area and CMP to reverse the protected area.

Table 5 Protect Level Setting Conditions

Protect Level	Status Register Bits					Protected Area
	CMP	TB	BP2	BP1	BP0	
0 (Whole area unprotected)	X	X	0	0	0	None
T1 (Upper side 1/16 protected)	0	0	0	0	1	0FFFFFh to 0F0000h
T2 (Upper side 1/8 protected)	0	0	0	1	0	0FFFFFh to 0E0000h
T3 (Upper side 1/4 protected)	0	0	0	1	1	0FFFFFh to 0C0000h
T4 (Upper side 1/2 protected)	0	0	1	0	0	0FFFFFh to 080000h
B1 (Lower side 1/16 protected)	0	1	0	0	1	00FFFFh to 000000h
B2 (Lower side 1/8 protected)	0	1	0	1	0	01FFFFh to 000000h
B3 (Lower side 1/4 protected)	0	1	0	1	1	03FFFFh to 000000h
B4 (Lower side 1/2 protected)	0	1	1	0	0	07FFFFh to 000000h
B7 (Lower side 15/16 protected)	1	0	0	0	1	0EFFFFh to 000000h
B6 (Lower side 7/8 protected)	1	0	0	1	0	0DFFFFh to 000000h
B5 (Lower side 3/4 protected)	1	0	0	1	1	0BFFFFh to 000000h
B4 (Lower side 1/2 protected)	1	0	1	0	0	07FFFFh to 000000h
T7 (Upper side 15/16 protected)	1	1	0	0	1	0FFFFFh to 010000h
T6 (Upper side 7/8 protected)	1	1	0	1	0	0FFFFFh to 020000h
T5 (Upper side 3/4 protected)	1	1	0	1	1	0FFFFFh to 040000h
T4 (Upper side 1/2 protected)	1	1	1	0	0	0FFFFFh to 080000h
5 (Whole area protected)	X	X	1	0	1	0FFFFFh to 000000h
5 (Whole area protected)	X	X	1	1	X	0FFFFFh to 000000h

* Chip erase is enabled only when the protect level is 0.

SRWP (bit 7)

Status register write protect SRWP is the bit for protecting the status registers, and its information can be rewritten. When SRWP is "1" and the logic level of the $\overline{WP}$ pin is low, the status register write command is ignored, and status registers BP0, BP1, BP2, TB, CMP and SRWP are protected. When the logic level of the $\overline{WP}$ pin is high, the status registers are not protected regardless of the SRWP state. The SRWP setting conditions are shown in "Table 6 SRWP setting conditions".

Table 6 SRWP Setting Conditions

$\overline{WP}$ Pin	SRWP	Status Register Protect State
0	0	Unprotected
	1	Protected
1	0	Unprotected
	1	Unprotected

4. Write Enable

Before performing any of the operations listed below, the device must be placed in the write enable state. Operation is the same as for setting status register WEN to "1", and the state is enabled by inputting the write enable command. "Figure 8 Write Enable" shows the timing waveforms when the write enable operation is performed. The write enable command consists only of the first bus cycle, and it is initiated by inputting (06h).

- Small sector erase, sector erase, chip erase
- Page program
- Status register write

5. Write Disable

The write disable command sets status register WEN to "0" to prohibit unintentional writing. "Figure 9 Write Disable" shows the timing waveforms. The write disable command consists only of the first bus cycle, and it is initiated by inputting (04h). The write disable state (WEN "0") is exited by setting WEN to "1" using the write enable command (06h).

Figure 8 Write Enable

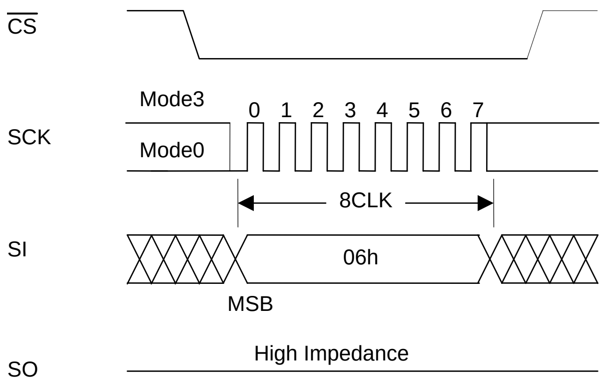
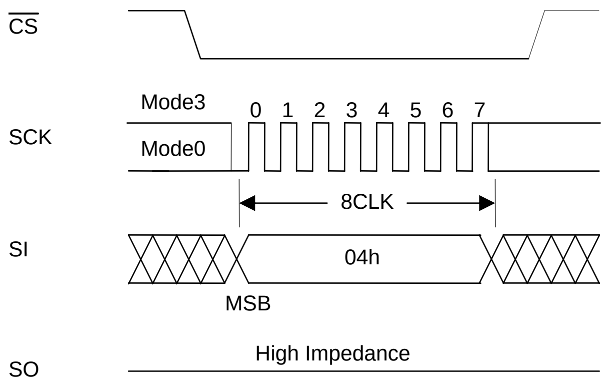


Figure 9 Write Disable



6. Power-down

The power-down command sets all the commands, with the exception of the silicon ID read command and the command to exit from power-down, to the acceptance prohibited state (power-down). "Figure 10 Power-down" shows the timing waveforms. The power-down command consists only of the first bus cycle, and it is initiated by inputting (B9h). However, a power-down command issued during an internal write operation will be ignored. The power-down state is exited using the power-down exit command (power-down is exited also when one bus cycle or more of the silicon ID read command (ABh) has been input). "Figure 11 Exiting from Power-down" shows the timing waveforms of the power-down exit command.

Figure 10 Power-down

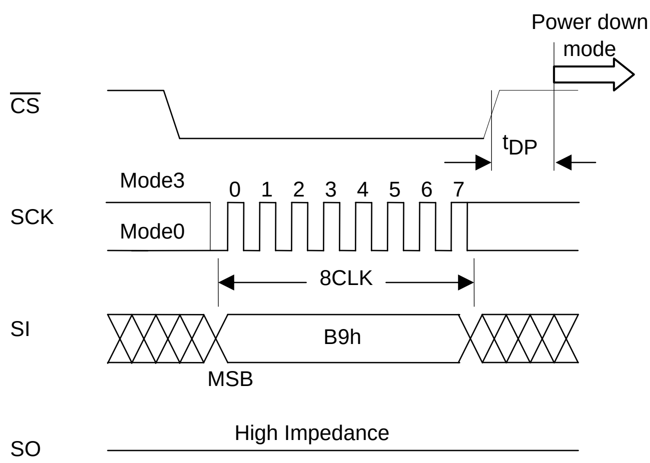
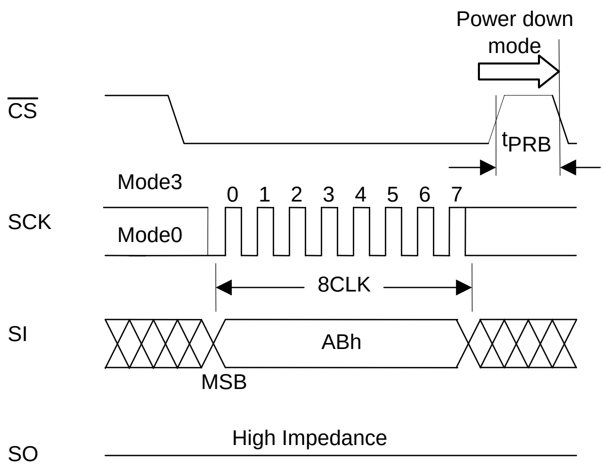


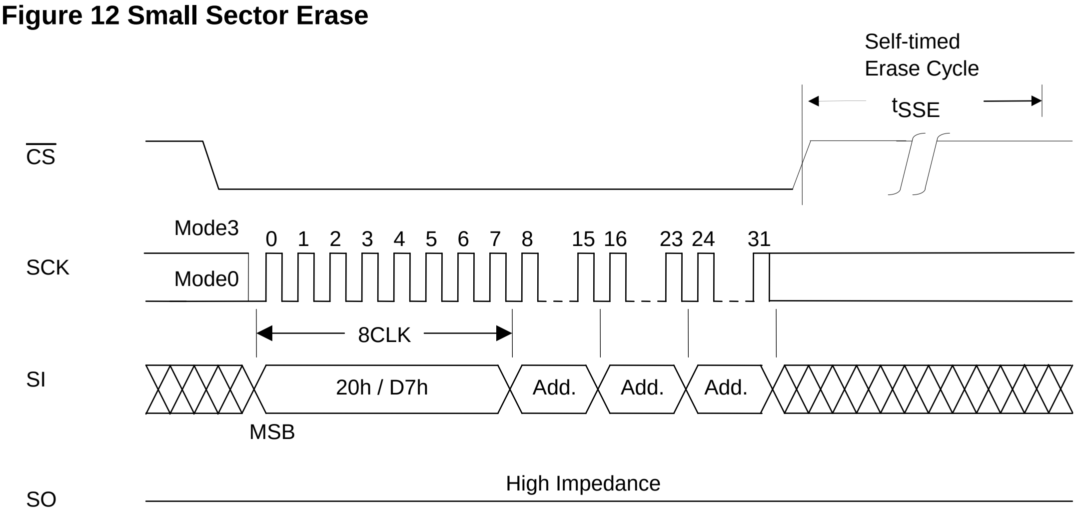
Figure 11 Exiting from Power-down



7. Small Sector Erase

Small sector erase is an operation that sets the memory cell data in any small sector to "1". A small sector consists of 4Kbytes. "Figure 12 Small Sector Erase" shows the timing waveforms, and Figure 21 shows a small sector erase flowchart. The small sector erase command consists of the first through fourth bus cycles, and it is initiated by inputting the 24-bit addresses following (20h) or (D7h). Addresses A19 to A12 are valid, and Addresses A23 to A20 are "don't care". After the command has been input, the internal erase operation starts from the rising $\overline{\text{CS}}$ edge, and it ends automatically by the control exercised by the internal timer. Erase end can also be detected using status register $\overline{\text{RDY}}$.

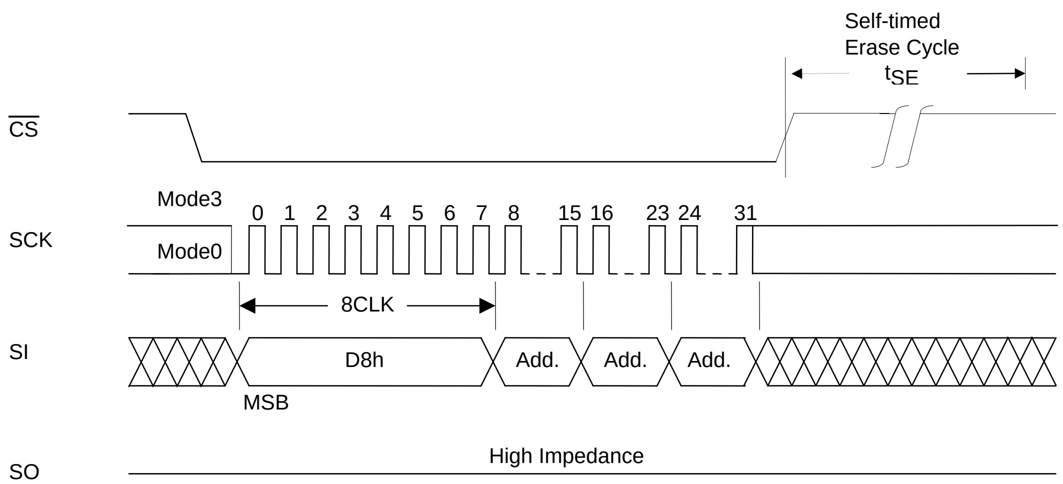
Figure 12 Small Sector Erase



8. Sector Erase

Sector erase is an operation that sets the memory cell data in any sector to "1". A sector consists of 64Kbytes. "Figure 13 Sector Erase" shows the timing waveforms, and Figure 21 shows a sector erase flowchart. The sector erase command consists of the first through fourth bus cycles, and it is initiated by inputting the 24-bit addresses following (D8h). Addresses A19 to A16 are valid, and Addresses A23 to A20 are "don't care". After the command has been input, the internal erase operation starts from the rising $\overline{\text{CS}}$ edge, and it ends automatically by the control exercised by the internal timer. Erase end can also be detected using status register $\overline{\text{RDY}}$.

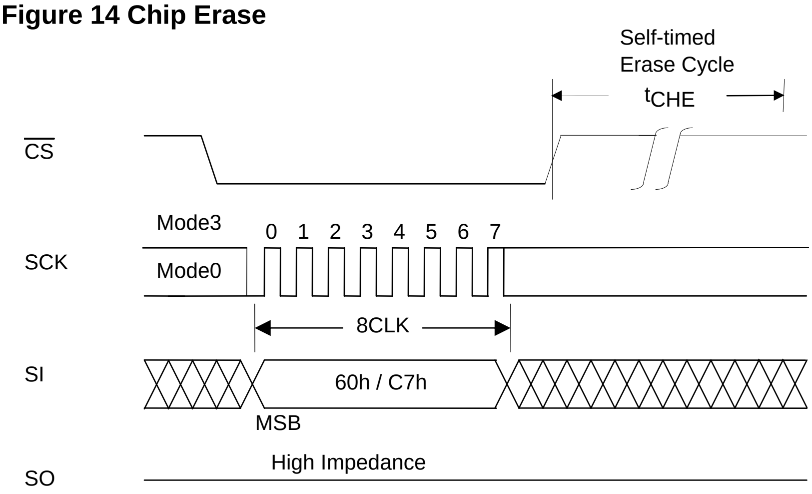
Figure 13 Sector Erase



9. Chip Erase

Chip erase is an operation that sets the memory cell data in all the sectors to "1". "Figure 14 Chip Erase" shows the timing waveforms, and Figure 21 shows a chip erase flowchart. The chip erase command consists only of the first bus cycle, and it is initiated by inputting (60h) or (C7h). After the command has been input, the internal erase operation starts from the rising $\overline{CS}$ edge, and it ends automatically by the control exercised by the internal timer. Erase end can also be detected using status register $\overline{RDY}$.

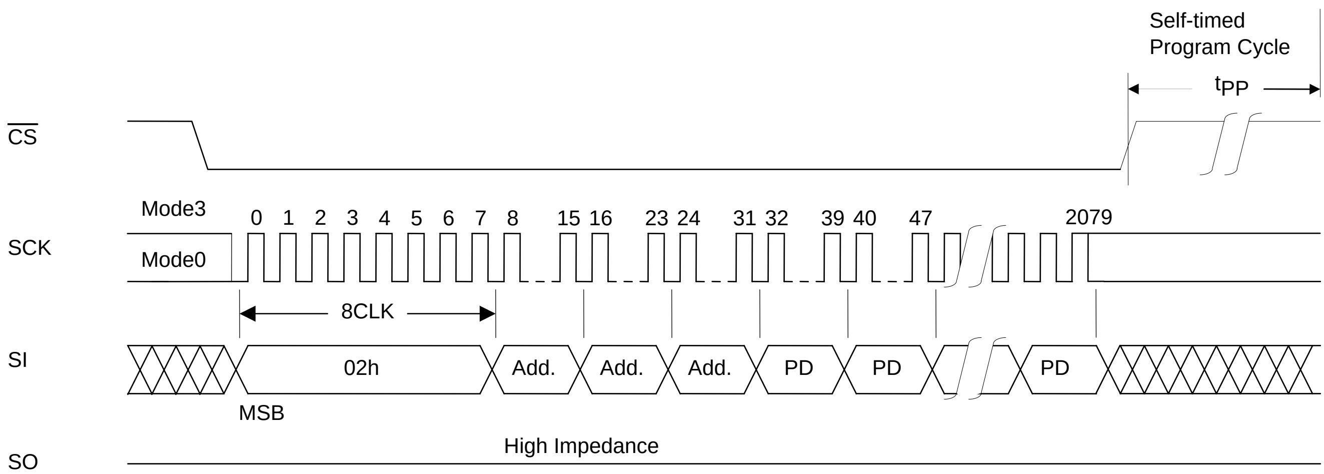
Figure 14 Chip Erase



10. Page Program

Page program is an operation that programs any number of bytes from 1 to 256 bytes within the same sector page (page addresses: A19 to A8). Before initiating page program, the data on the page concerned must be erased using small sector erase, sector erase, or chip erase. "Figure 15 Page Program" shows the page program timing waveforms, and Figure 22 shows a page program flowchart. After the falling $\overline{CS}$, edge, the command (02H) is input followed by the 24-bit addresses. Addresses A19 to A0 are valid. The program data is then loaded at each rising clock edge until the rising $\overline{CS}$ edge, and data loading is continued until the rising $\overline{CS}$ edge. If the data loaded has exceeded 256 bytes, the 256 bytes loaded last are programmed. The program data must be loaded in 1-byte increments, and the program operation is not performed at the rising $\overline{CS}$ edge occurring at any other timing.

Figure 15 Page Program



11. ID Read

ID read is an operation that reads the manufacturer code and device ID information. The silicon ID read command is not accepted during writing. There are two methods of reading the silicon ID, each of which is assigned a device ID. In the first method, the read command sequence consists only of the first bus cycle in which (9Fh) is input. In the subsequent bus cycles, the manufacturer code 62h which is assigned by JEDEC, 2-byte device ID code (memory type, memory capacity), and reserved code are output sequentially. The 4-byte code is output repeatedly as long as clock inputs are present, "Table 7-1 JEDEC ID codes table" lists the silicon ID codes and "Figure 16-a JEDEC ID read" shows the JEDEC ID read timing waveforms.

The second method involves inputting the ID read command. This command consists of the first through fourth bus cycles, and the one bite silicon ID can be read when 24 dummy bits are input after (ABh). "Table 7-2 ID codes table" lists the silicon ID codes and "Figure 16-b ID read" shows the ID read timing waveforms.

If the SCK input persists after a device code is read, that device code continues to be output. The data output is transmitted starting at the falling edge of the clock for bit 0 in the fourth bus cycle and the silicon ID read sequence is finished by setting $\overline{CS}$ high.

Table 7-1 JEDEC ID read

		Output code
Manufacturer code		62h
2 byte device ID	Memory type	06h
	Memory capacity code	14h(8M Bit)
Device code	1	00h

Table 7-2 ID read

	Output Code
1 byte device ID	27h (LE25U81AQE)

Figure 16-a Silicon ID Read 1

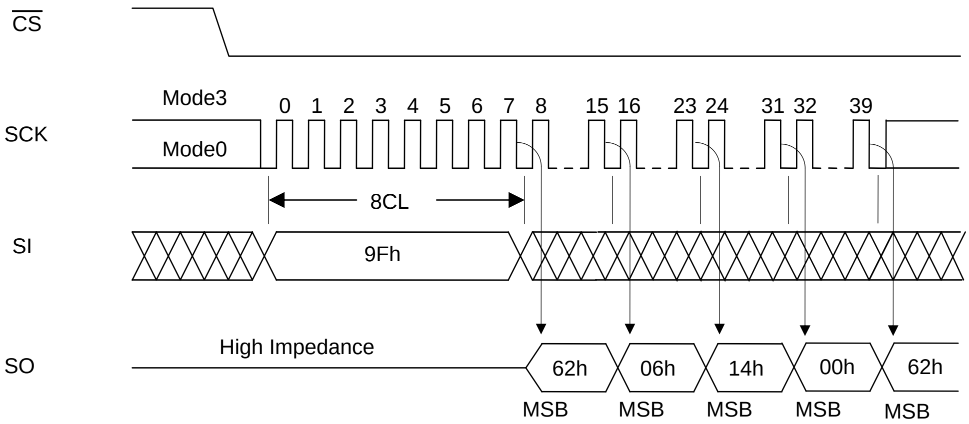
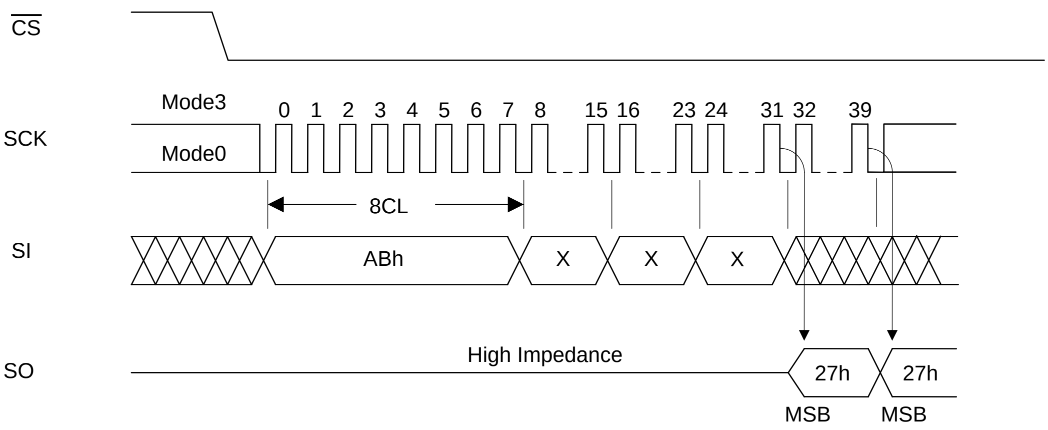


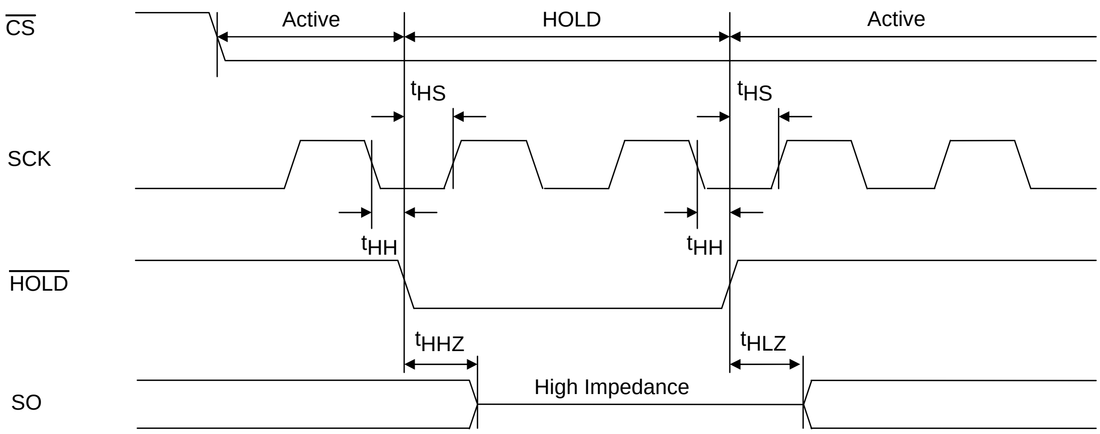
Figure 16-b Silicon ID Read 2



12. Hold Function

Using the $\overline{HOLD}$ pin, the hold function suspends serial communication (it places it in the hold status). "Figure 17 $\overline{HOLD}$" shows the timing waveforms. The device is placed in the hold status at the falling $\overline{HOLD}$ edge while the logic level of SCK is low, and it exits from the hold status at the rising $\overline{HOLD}$ edge. When the logic level of SCK is high, $\overline{HOLD}$ must not rise or fall. The hold function takes effect when the logic level of $\overline{CS}$ is low, the hold status is exited and serial communication is reset at the rising $\overline{CS}$ edge. In the hold status, the SO output is in the high-impedance state, and SI and SCK are "don't care".

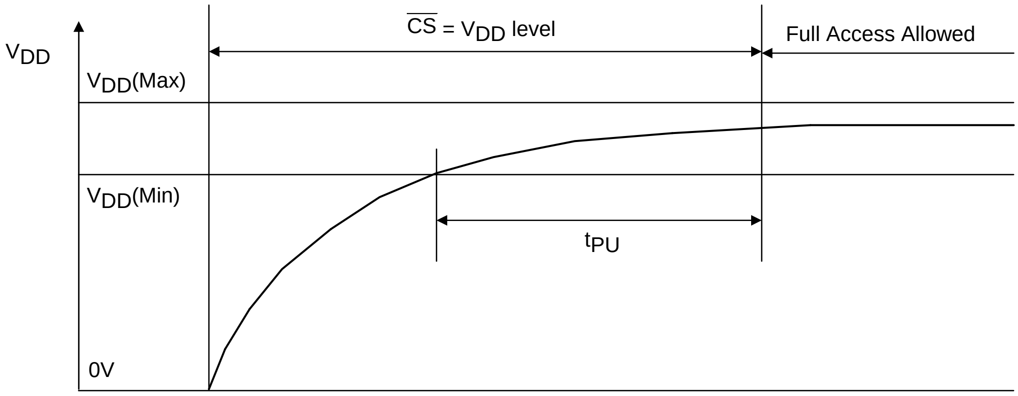
Figure 17 $\overline{HOLD}$



13. Power-on

In order to protect against unintentional writing, $\overline{CS}$ must be within at V_{DD}-0.3 to V_{DD}+0.3 on power-on. After power-on, the supply voltage has stabilized at VDD min. or higher, waits for t_{PU} before inputting the command to start a device operation. The device is in the standby state and not in the power-down state after power is turned on. To put the device into the power-down state, it is necessary to enter a power-down command.

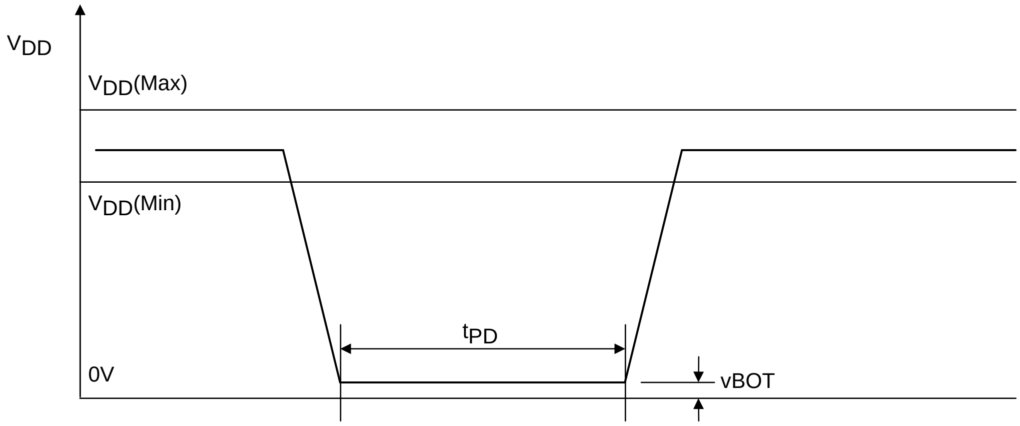
Figure 18 Power-on Timing



14. Hardware Data Protection

LE25U81AQE incorporates a power-on reset function. The following conditions must be met in order to ensure that the power reset circuit will operate stably.
No guarantees are given for data in the event of an instantaneous power failure occurring during the writing period.

Figure 19 Power-down Timing



Power-on timing

Parameter	Symbol	spec		unit
		min	max	
power-on to operation time	t_{PU}	500		µs
power-down time	t_{PD}	10		ms
power-down voltage	v_{BOT}		0.2	V

15. Software Data Protection

The LE25U81AQE eliminates the possibility of unintentional operations by not recognizing commands under the following conditions.

- When a write command is input and the rising $\overline{CS}$ edge timing is not in a bus cycle (8 CLK units of SCK)
- When the page program data is not in 1-byte increments
- When the status register write command is input for 2 bus cycles or more

16. Decoupling Capacitor

A 0.1µF ceramic capacitor must be provided to each device and connected between V_{DD} and V_{SS} in order to ensure that the device will operate stably.

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	unit
Maximum supply voltage		With respect to V_{SS}	-0.5 to +4.6	V
DC voltage (all pins)		With respect to V_{SS}	-0.5 to V_{DD}+0.5	V
Storage temperature	Tstg		-55 to +150	°C

Operating Conditions

Parameter	Symbol	Conditions	Ratings	unit
Operating supply voltage	VDD		2.3 to 2.7	V
Operating ambient temperature	Topr		-40 to +85	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable DC Operating Conditions

Parameter	Symbol	Conditions			Ratings min	Ratings typ	Ratings max	unit
Read mode operating current	I_{CCR}	SCK=0.1V_{DD}/0.9V_{DD}, $\overline{HOLD}$=$\overline{WP}$=0.9V_{DD}, SO=open	Single	30MHz			6	mA
			Single	40MHz			8	mA
			Dual	40MHz			10	mA
Write mode operating current (erase+page program)	I_{CCW}	t_{SSE}= t_{SE}= t_{CHE}=typ.,t_{PP}=max					40	mA
CMOS standby current	I_{SB}	$\overline{CS}$=V_{DD}, $\overline{HOLD}$=$\overline{WP}$=V_{DD}, SI=V_{SS}/V_{DD}, SO=open,					50	μA
Power-down standby current	I_{DSB}	$\overline{CS}$=V_{DD}, $\overline{HOLD}$=$\overline{WP}$=V_{DD}, SI=V_{SS}/V_{DD}, SO=open,					10	μA
Input leakage current	I_{LI}						2	μA
Output leakage current	I_{LO}						2	μA
Input low voltage	V_{IL}				-0.3		0.3V_{DD}	V
Input high voltage	V_{IH}				0.7V_{DD}		V_{DD}+0.3	V
Output low voltage	V_{OL}	I_{OL}=100μA, V_{DD}=V_{DD} min					0.2	V
		I_{OL}=1.6mA, V_{DD}=V_{DD} min					0.4	V
Output high voltage	V_{OH}	I_{OH}=-100μA, V_{DD}=V_{DD} min			V_{DD}-0.2			V

Data hold, Rewriting frequency -0.2

Parameter	condition	min	max	unit
Rewriting frequency	Program/Erase	100,000		times/ Sector
	Status resister write	1,000		times/ Sector
Data hold		20		year

Pin Capacitance at Ta=25°C, f=1MHz

Parameter	Symbol	Conditions	Ratings max	unit
Output pin capacitance	C_{SO}	V_{SO}=0V	12	pF
Input pin Capacitance	C_{IN}	V_{IN}=0V	6	pF

Note: These parameter values do not represent the results of measurements undertaken for all devices but rather values for some of the sampled devices.

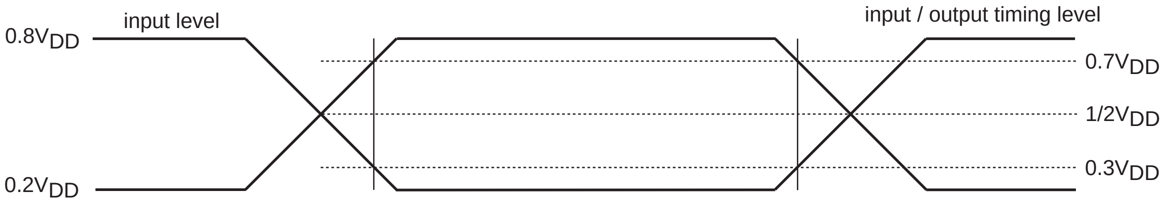
AC Characteristics

Parameter		Symbol	Ratings min	Ratings typ	Ratings max	unit
Clock frequency	Read instruction (03h)	f_{CLK}			30	MHz
	All instruction except for read (03h)				40	MHz
Input signal rising/falling time		t_{RF}	0.1			V/ns
SCK logic high level pulse width	30MHz	t_{CLHI}	14			ns
	40MHz		11.5			ns
SCK logic low level pulse width	30MHz	t_{CLLO}	14			ns
	40MHz		11.5			ns
$\overline{CS}$ setup time		t_{CSS}	10			ns
Data setup time		t_{DS}	5			ns
Data hold time		t_{DH}	4			ns
$\overline{CS}$ hold time		t_{CSH}	10			ns
$\overline{CS}$ wait pulse width		t_{CPH}	25			ns
Output high impedance time from $\overline{CS}$		t_{CHZ}			15	ns
Output data time from SCK		t_V		8	9	ns
Output data hold time		t_{HO}	1			ns
$\overline{HOLD}$ setup time		t_{HS}	5			ns
$\overline{HOLD}$ hold time		t_{HH}	5			ns
Output low impedance time from $\overline{HOLD}$		t_{HLZ}			12	ns
Output high impedance time from $\overline{HOLD}$		t_{HHZ}			9	ns
$\overline{WP}$ setup time		t_{WPS}	20			ns
$\overline{WP}$ hold time		t_{WPH}	20			ns
Write status register time		t_{SRW}		8	10	ms
Page programming cycle time	256Byte	t_{PP}		0.3	0.5	ms
	nByte			0.15+ n*0.15/256	0.20+ n*0.30/256	ms
Small sector erase cycle time		t_{SSE}		0.04	0.15	s
Sector erase cycle time		t_{SE}		0.08	0.25	s
Chip erase cycle time		t_{CHE}		0.5	6.0	s
Power-down time		t_{DP}			5	μs
Power-down recovery time		t_{PRB}			500	μs
Output low impedance time from SCK		t_{CLZ}	0			ns

AC Test Conditions

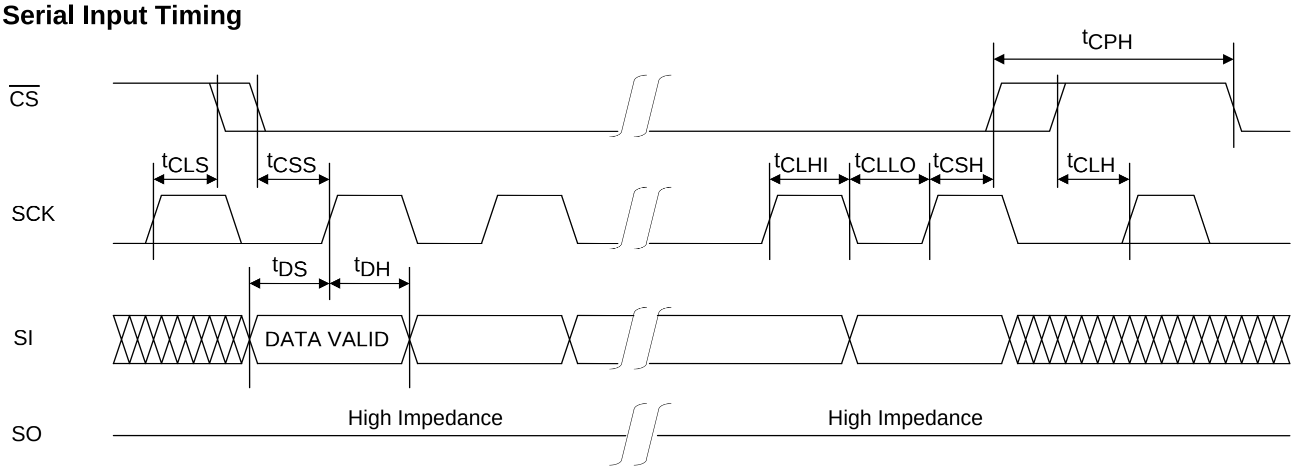
Input pulse level ··········· $0.2V_{DD}$ to $0.8V_{DD}$
Input rising/falling time ·· 5ns
Input timing level ········· $0.3V_{DD}$, $0.7V_{DD}$
Output timing level ······· $1/2 \times V_{DD}$
Output load ················ 15pF

Note: As the test conditions for "typ", the measurements are conducted using 2.5V for V_{DD} at room temperature.

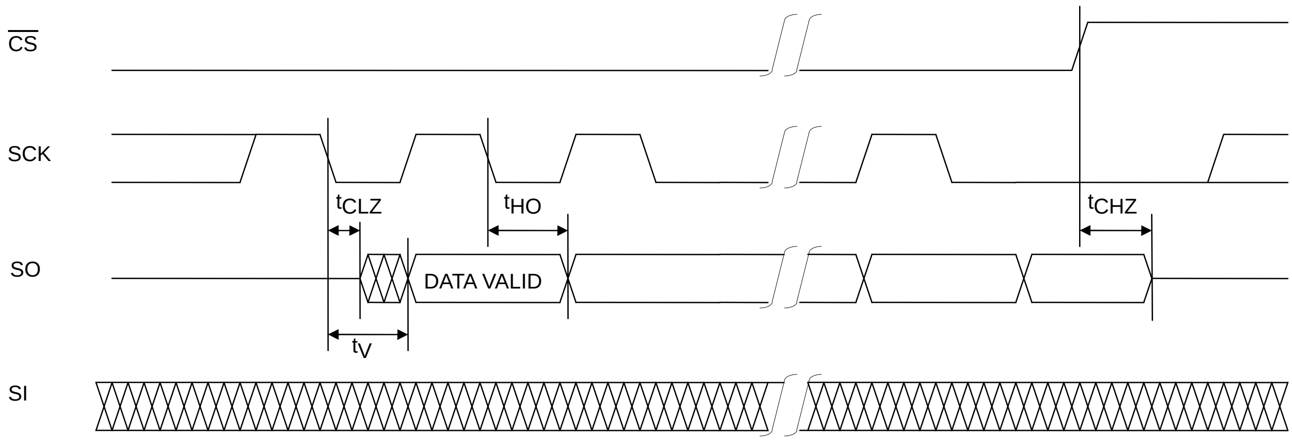


Timing waveforms

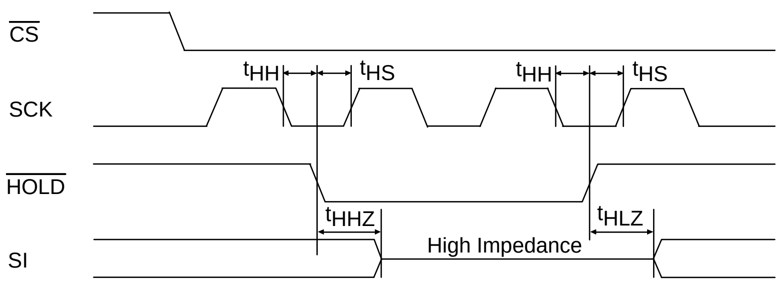
Serial Input Timing



Serial Output Timing



Hold Timing



Status resistor write Timing

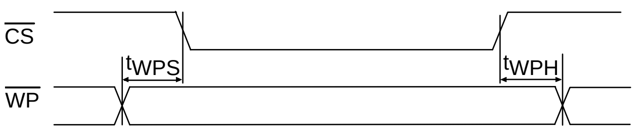
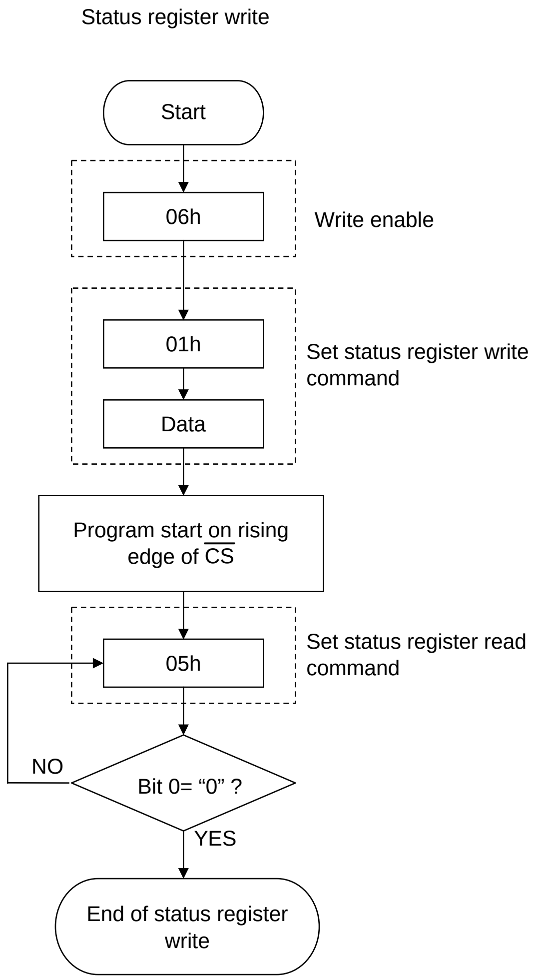
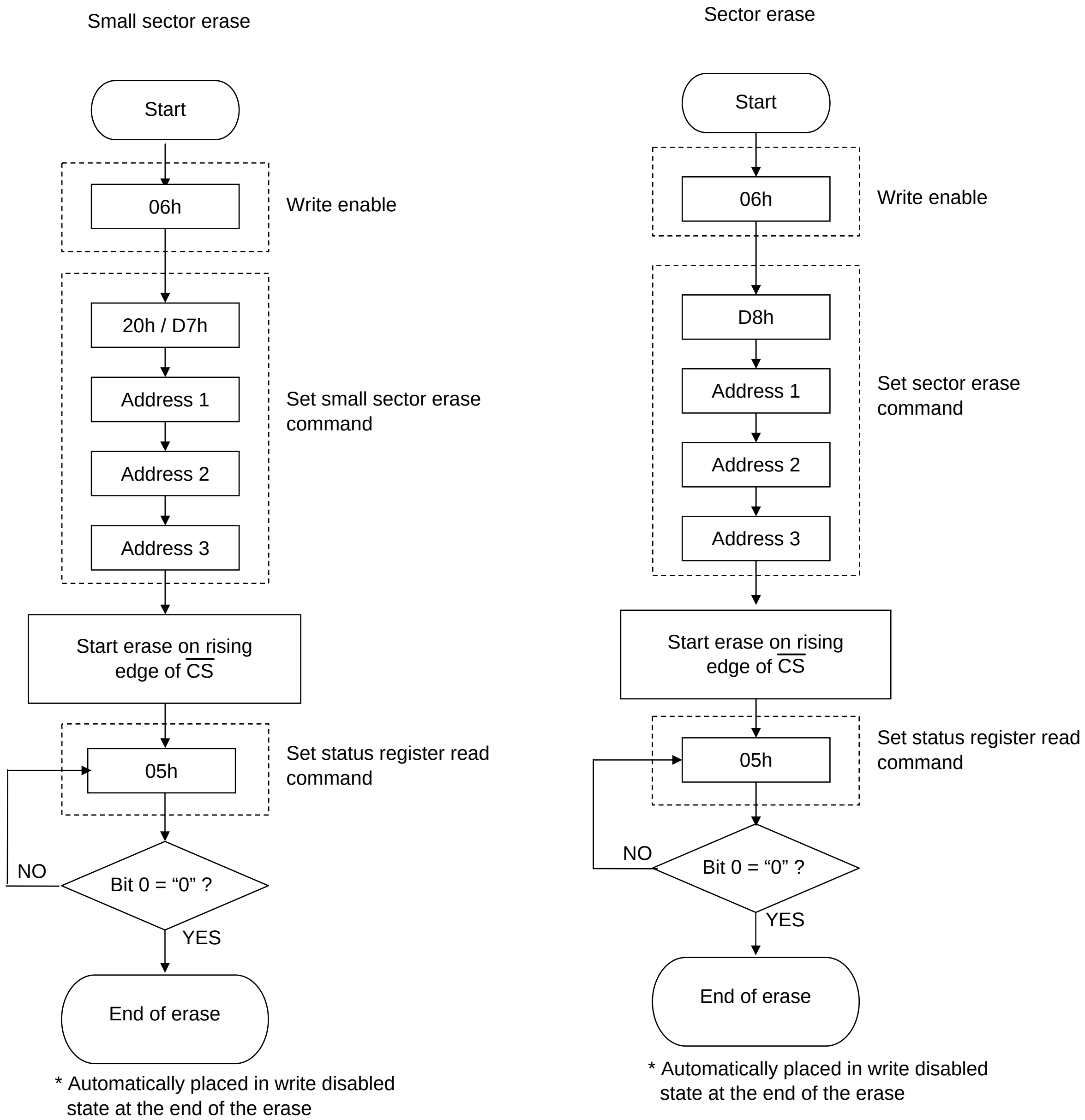


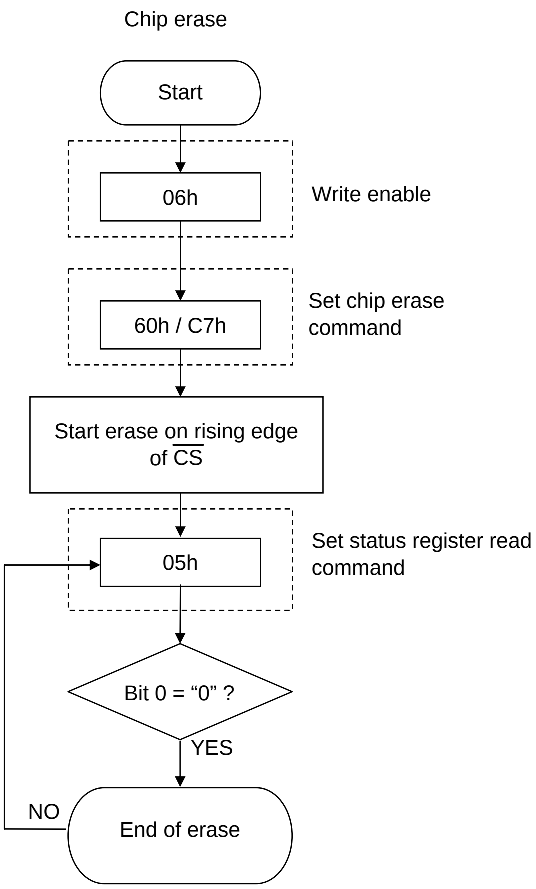
Figure 20 Status Register Write Flowchart



* Automatically placed in write disabled state at the end of the status register write

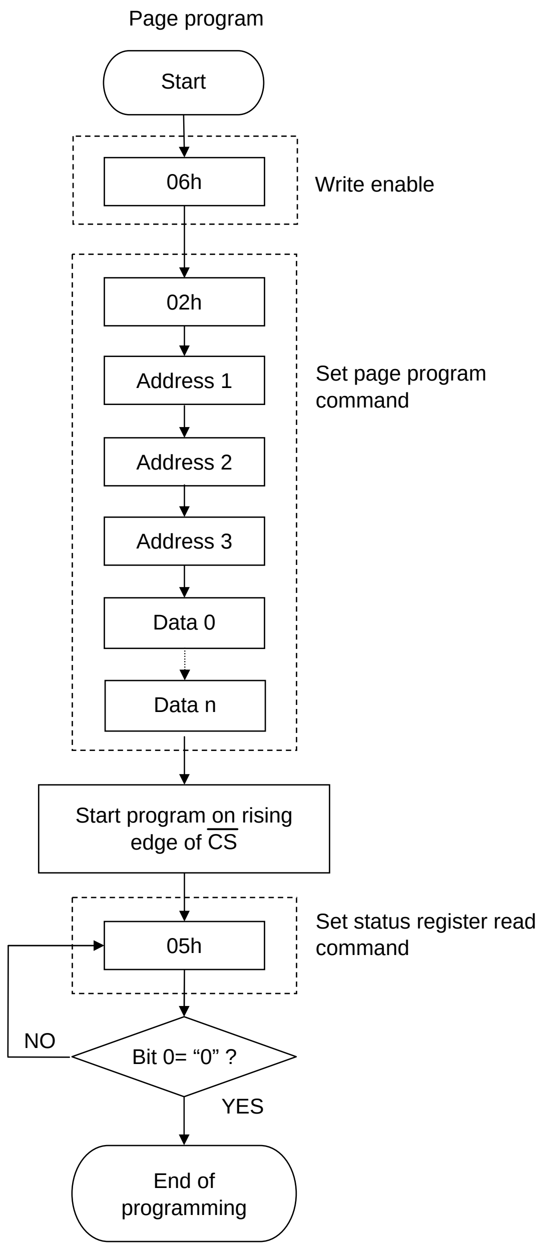
Figure 21 Erase Flowcharts





* Automatically placed in write disabled state at the end of the erase

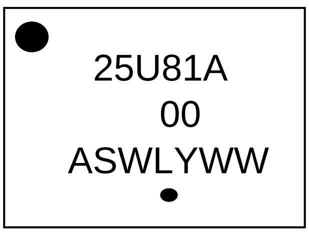
Figure 22 Page Program Flowchart



* Automatically placed in write disabled state at the end of the programming operation.

Figure 23 Making Diagrams

1Pin Index mark



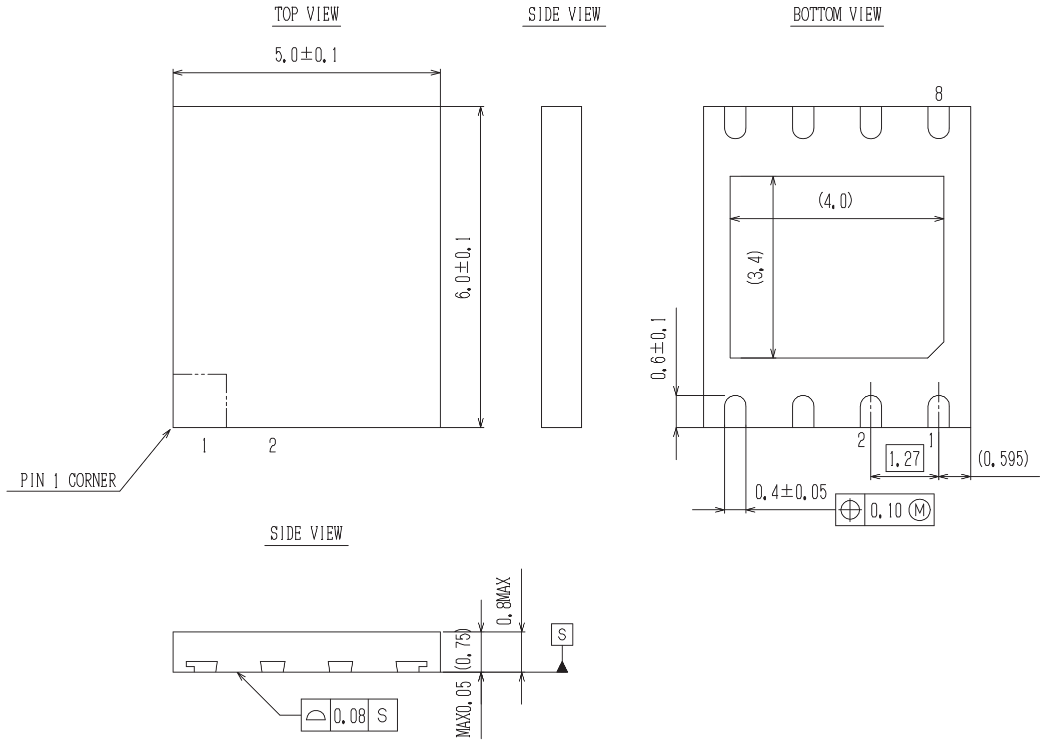
25U81	**=Specific Device Code**
00	**=Blank data**
AS	**=Assembly Location**
WL	**=Wafer Lot Traceability**
YWW	**=DATE CODE (One Digits Year and Work Week)**
●	**=Pb-Free Package**

VSON8T 6x5

Package Dimensions

unit : mm

VDFN8 5x6, 1.27P / VSON8T (6x5)
CASE 509AG
ISSUE O



ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LE25U81AQETXG	VSON8T(6.0X5.0) (Pb-Free / Halogen Free)	2000 / Tape & Real

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

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