

# MC74HC165A

## 8-Bit Serial or Parallel-Input/ Serial-Output Shift Register

### High-Performance Silicon-Gate CMOS

The MC74HC165A is identical in pinout to the LS165. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device is an 8-bit shift register with complementary outputs from the last stage. Data may be loaded into the register either in parallel or in serial form. When the Serial Shift/Parallel Load input is low, the data is loaded asynchronously in parallel. When the Serial Shift/Parallel Load input is high, the data is loaded serially on the rising edge of either Clock or Clock Inhibit (see the Function Table).

The 2-input NOR clock may be used either by combining two independent clock sources or by designating one of the clock inputs to act as a clock inhibit.

#### Features

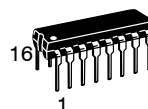
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 286 FETs or 71.5 Equivalent Gates
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable



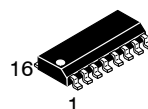
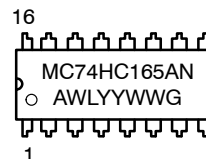
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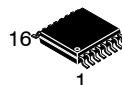
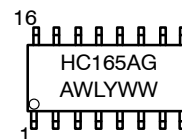
#### MARKING DIAGRAMS



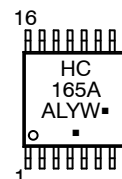
PDIP-16  
N SUFFIX  
CASE 648



SOIC-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



A = Assembly Location  
L, WL = Wafer Lot  
Y, YY = Year  
W, WW = Work Week  
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# MC74HC165A

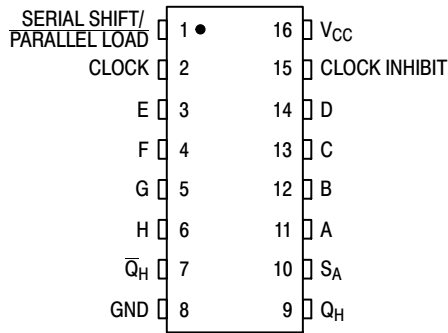


Figure 1. Pin Assignment

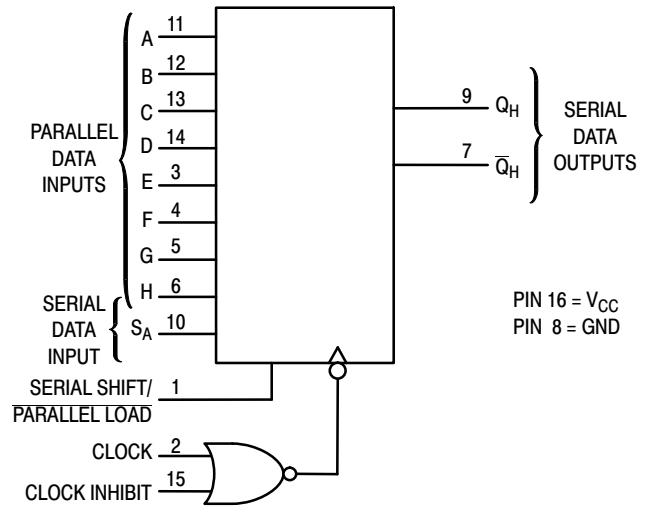


Figure 2. Logic Diagram

## FUNCTION TABLE

Inputs					Internal Stages		Output	Operation
Serial Shift/ Parallel Load	Clock	Clock Inhibit	S <sub>A</sub>	A - H	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>H</sub>	
L	X	X	X	a ... h	a	b	h	Asynchronous Parallel Load
H	↗	L	L	X	L	Q <sub>An</sub>	Q <sub>Gn</sub>	Serial Shift via Clock
H	↗	L	H	X	H	Q <sub>An</sub>	Q <sub>Gn</sub>	
H	L	↗	L	X	L	Q <sub>An</sub>	Q <sub>Gn</sub>	Serial Shift via Clock Inhibit
H	L	↗	H	X	H	Q <sub>An</sub>	Q <sub>Gn</sub>	
H	X	H	X	X	No Change			Inhibited Clock
H	H	X	X	X	No Change			
H	L	L	X	X	No Change			No Clock

X = don't care      Q<sub>An</sub> - Q<sub>Gn</sub> = Data shifted from the preceding stage

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC74HC165ANG	PDIP-16 (Pb-Free)	500 Units / Rail
MC74HC165ADG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74HC165ADR2G	SOIC-16 (Pb-Free)	2500 Units / Reel
MC74HC165ADTR2G	TSSOP-16 (Pb-Free)	2500 Units / Reel
NLV74HC165ADR2G*	SOIC-16 (Pb-Free)	2500 Units / Reel
NLV74HC165ADTR2G*	TSSOP-16 (Pb-Free)	2500 Units / Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

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## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit	
$V_{CC}$	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V	
$V_{in}$	DC Input Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V	
$V_{out}$	DC Output Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V	
$I_{in}$	DC Input Current, per Pin	$\pm 20$	mA	
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA	
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA	
$P_D$	Power Dissipation in Still Air	Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
$T_{stg}$	Storage Temperature	- 65 to + 150	°C	
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	260	°C	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

†Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C  
SOIC Package: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V	
$T_A$	Operating Temperature, All Package Types	- 55	+ 125	°C	
$t_r, t_f$	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0\text{ V}$ $V_{CC} = 3.0\text{ V}$ $V_{CC} = 4.5\text{ V}$ $V_{CC} = 6.0\text{ V}$	0 0 0 0	1000 600 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	$V_{CC}$ V	Guaranteed Limit			Unit	
				- 55 to 25°C	≤ 85°C	≤ 125°C		
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = 0.1\text{ V}$ or $V_{CC} - 0.1\text{ V}$ $ I_{out}  \leq 20\ \mu\text{A}$	2.0	1.5	1.5	1.5	V	
			3.0	2.1	2.1	2.1		
			4.5	3.15	3.15	3.15		
			6.0	4.2	4.2	4.2		
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = 0.1\text{ V}$ or $V_{CC} - 0.1\text{ V}$ $ I_{out}  \leq 20\ \mu\text{A}$	2.0	0.5	0.5	0.5	V	
			3.0	0.9	0.9	0.9		
			4.5	1.35	1.35	1.35		
			6.0	1.80	1.80	1.80		
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 20\ \mu\text{A}$	2.0	1.9	1.9	1.9	V	
			4.5	4.4	4.4	4.4		
			6.0	5.9	5.9	5.9		
		$V_{in} = V_{IH}$ or $V_{IL}$	$ I_{out}  \leq 2.4\text{ mA}$	3.0	2.48	2.34	2.20	V
			$ I_{out}  \leq 4.0\text{ mA}$	4.5	3.98	3.84	3.70	
			$ I_{out}  \leq 5.2\text{ mA}$	6.0	5.48	5.34	5.20	

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## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				- 55 to 25 °C	≤ 85 °C	≤ 125 °C	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 2.4 mA  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	3.0	0.26	0.33	0.40	
			4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	4	40	160	μA

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			- 55 to 25 °C	≤ 85 °C	≤ 125 °C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 8)	2.0	6	4.8	4	MHz
		3.0	18	17	15	
		4.5	30	24	20	
		6.0	35	28	24	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock (or Clock Inhibit) to Q <sub>H</sub> or $\bar{Q}_H$ (Figures 1 and 8)	2.0	150	190	225	ns
		3.0	52	63	65	
		4.5	30	38	45	
		6.0	26	33	38	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Serial Shift/Parallel Load to Q <sub>H</sub> or $\bar{Q}_H$ (Figures 2 and 8)	2.0	175	220	265	ns
		3.0	58	70	72	
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input H to Q <sub>H</sub> or $\bar{Q}_H$ (Figures 3 and 8)	2.0	150	190	225	ns
		3.0	52	63	65	
		4.5	30	38	45	
		6.0	26	33	38	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 8)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	-	10	10	10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Per Package)*	Typical @ 25 °C, V <sub>CC</sub> = 5.0 V			pF	
		40				

\* Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>.

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## TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
t <sub>su</sub>	Minimum Setup Time, Parallel Data Inputs to Serial Shift/Parallel Load (Figure 4)	2.0	75	95	110	ns
		3.0	30	40	55	
		4.5	15	19	22	
		6.0	13	16	19	
t <sub>su</sub>	Minimum Setup Time, Input SA to Clock (or Clock Inhibit) (Figure 5)	2.0	75	95	110	ns
		3.0	30	40	55	
		4.5	15	19	22	
		6.0	13	16	19	
t <sub>su</sub>	Minimum Setup Time, Serial Shift/Parallel Load to Clock (or Clock Inhibit) (Figure 6)	2.0	75	95	110	ns
		3.0	30	40	55	
		4.5	15	19	22	
		6.0	13	16	19	
t <sub>su</sub>	Minimum Setup Time, Clock to Clock Inhibit (Figure 7)	2.0	75	95	110	ns
		3.0	30	40	55	
		4.5	15	19	22	
		6.0	13	16	19	
t <sub>h</sub>	Minimum Hold Time, Serial Shift/Parallel Load to Parallel Data Inputs (Figure 4)	2.0	5	5	5	ns
		3.0	5	5	5	
		4.5	5	5	5	
		6.0	5	5	5	
t <sub>h</sub>	Minimum Hold Time, Clock (or Clock Inhibit) to Input SA (Figure 5)	2.0	5	5	5	ns
		3.0	5	5	5	
		4.5	5	5	5	
		6.0	5	5	5	
t <sub>h</sub>	Minimum Hold Time, Clock (or Clock Inhibit) to Serial Shift/Parallel Load (Figure 6)	2.0	5	5	5	ns
		3.0	5	5	5	
		4.5	5	5	5	
		6.0	5	5	5	
t <sub>rec</sub>	Minimum Recovery Time, Clock to Clock Inhibit (Figure 7)	2.0	75	95	110	ns
		3.0	30	40	55	
		4.5	15	19	22	
		6.0	13	16	19	
t <sub>w</sub>	Minimum Pulse Width, Clock (or Clock Inhibit) (Figure 1)	2.0	70	90	100	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	16	19	
t <sub>w</sub>	Minimum Pulse width, Serial Shift/Parallel Load (Figure 2)	2.0	70	90	100	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	16	19	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		3.0	800	800	800	
		4.5	500	500	500	
		6.0	400	400	400	

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## PIN DESCRIPTIONS

### INPUTS

#### **A, B, C, D, E, F, G, H (Pins 11, 12, 13, 14, 3, 4, 5, 6)**

Parallel Data inputs. Data on these inputs are asynchronously entered in parallel into the internal flip-flops when the Serial Shift/Parallel Load input is low.

#### **SA (Pin 10)**

Serial Data input. When the Serial Shift/Parallel Load input is high, data on this pin is serially entered into the first stage of the shift register with the rising edge of the Clock.

### CONTROL INPUTS

#### **Serial Shift/Parallel Load (Pin 1)**

Data-entry control input. When a high level is applied to this pin, data at the Serial Data input (SA) are shifted into the register with the rising edge of the Clock. When a low level

is applied to this pin, data at the Parallel Data inputs are asynchronously loaded into each of the eight internal stages.

#### **Clock, Clock Inhibit (Pins 2, 15)**

Clock inputs. These two clock inputs function identically. Either may be used as an active-high clock inhibit. However, to avoid double clocking, the inhibit input should go high only while the clock input is high.

The shift register is completely static, allowing Clock rates down to DC in a continuous or intermittent mode.

### OUTPUTS

#### **Q<sub>H</sub>, $\bar{Q}_H$ (Pins 9, 7)**

Complementary Shift Register outputs. These pins are the noninverted and inverted outputs of the eighth stage of the shift register.

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## SWITCHING WAVEFORMS

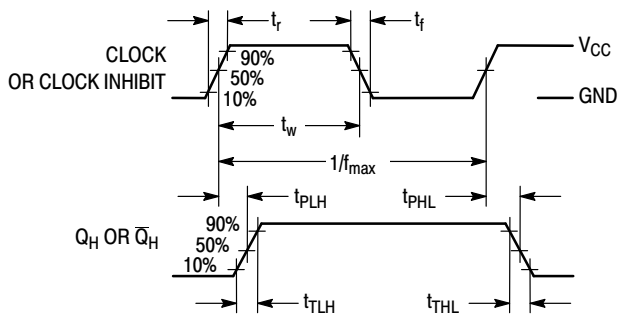


Figure 3. Serial-Shift Mode

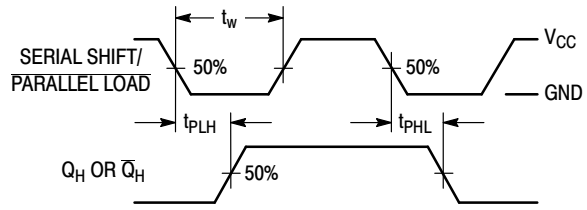


Figure 4. Parallel-Load Mode

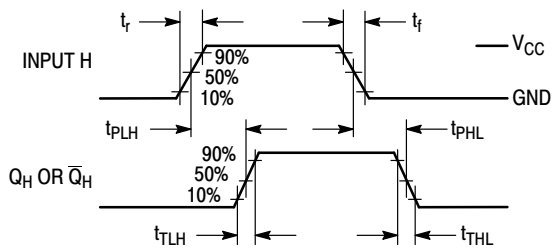


Figure 5. Parallel-Load Mode

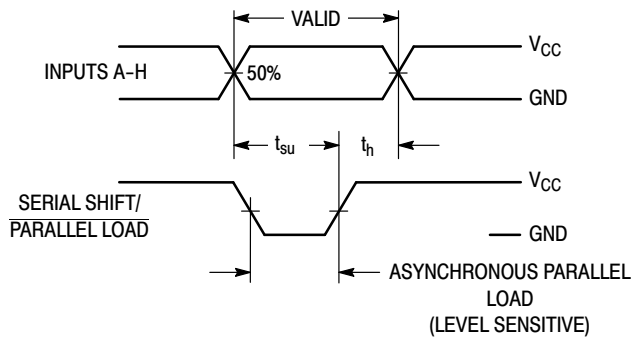


Figure 6. Parallel-Load Mode

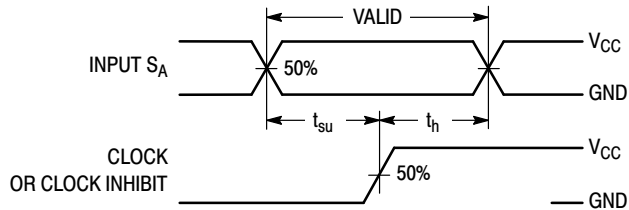


Figure 7. Serial-Shift Mode

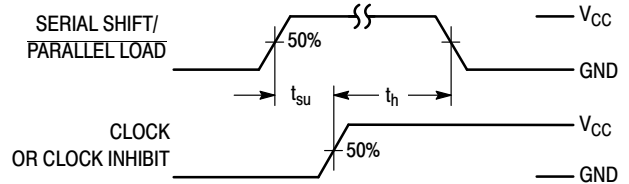


Figure 8. Serial-Shift Mode

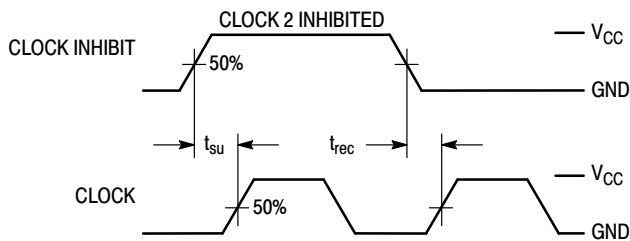
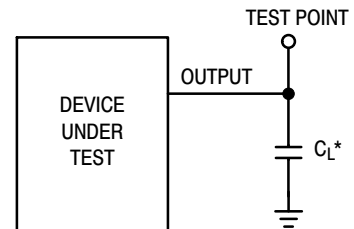


Figure 9. Serial-Shift, Clock-Inhibit Mode

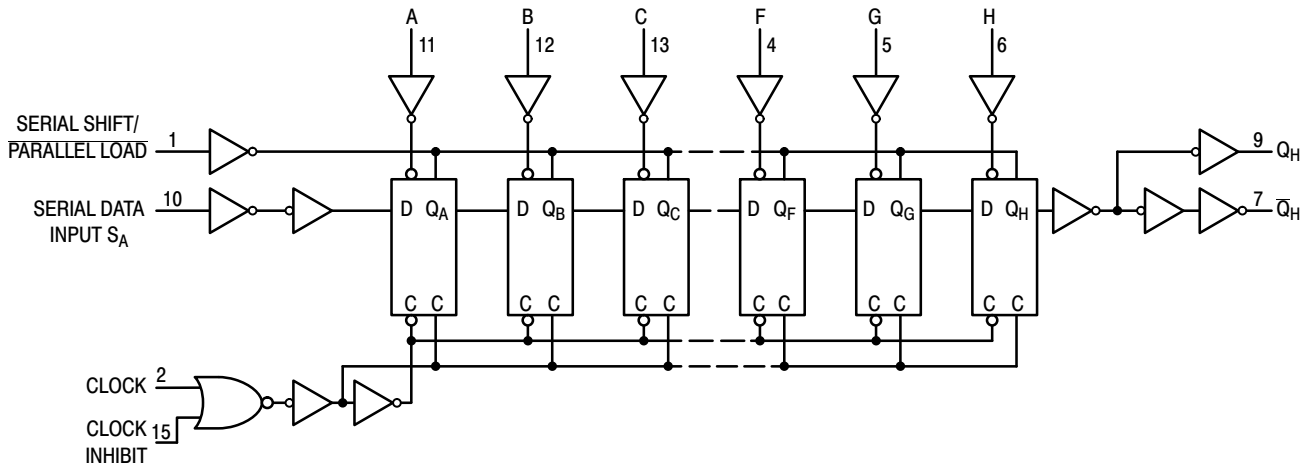


\*Includes all probe and jig capacitance

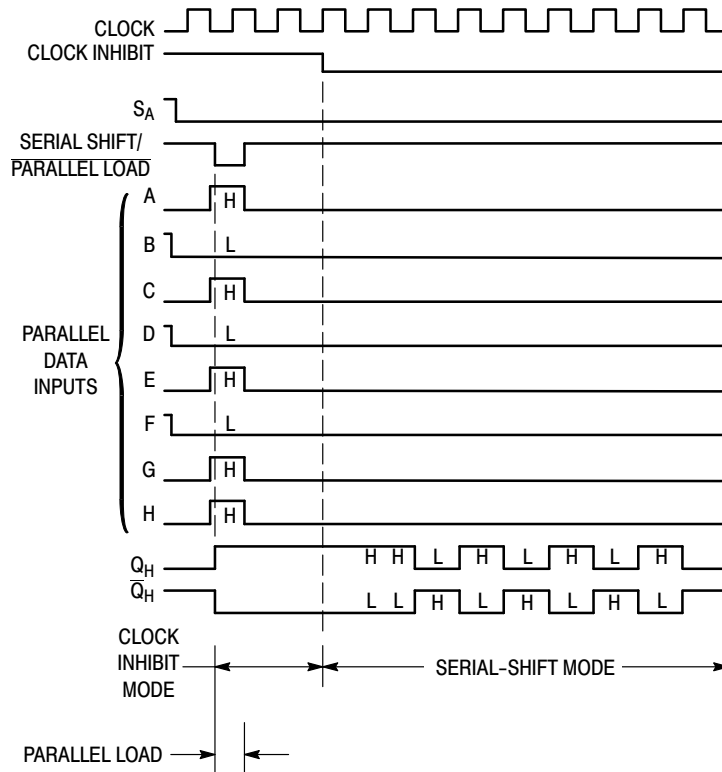
Figure 10. Test Circuit

# MC74HC165A

## EXPANDED LOGIC DIAGRAM



## TIMING DIAGRAM

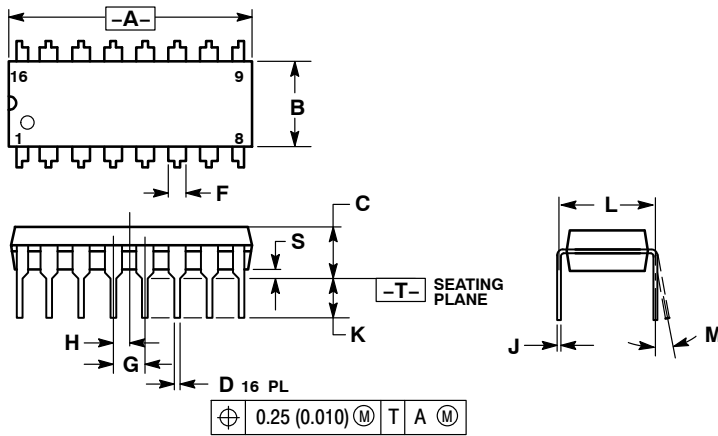




# MC74HC165A

## PACKAGE DIMENSIONS

PDIP-16  
CASE 648-08  
ISSUE T



NOTES:

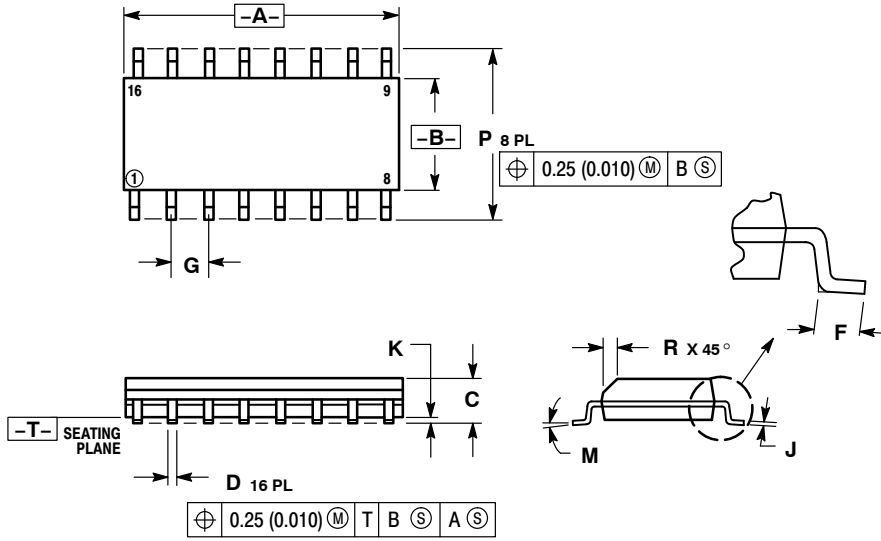
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

# MC74HC165A

## PACKAGE DIMENSIONS

SOIC-16  
CASE 751B-05  
ISSUE K

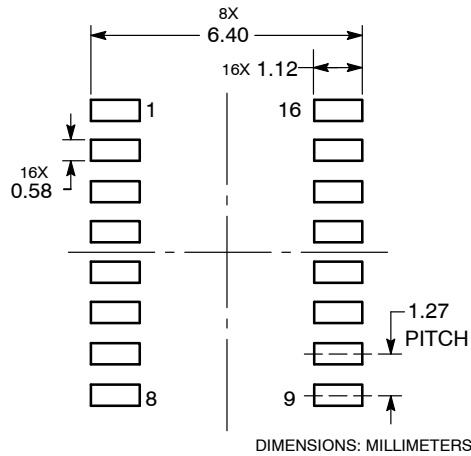


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

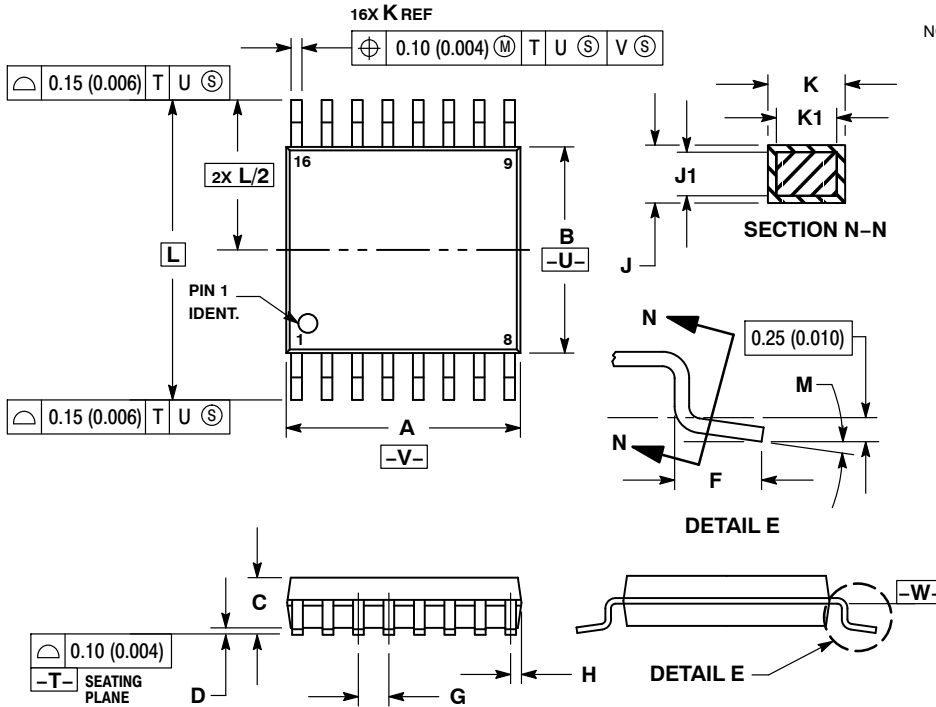
### SOLDERING FOOTPRINT



# MC74HC165A

## PACKAGE DIMENSIONS

TSSOP-16  
CASE 948F  
ISSUE B

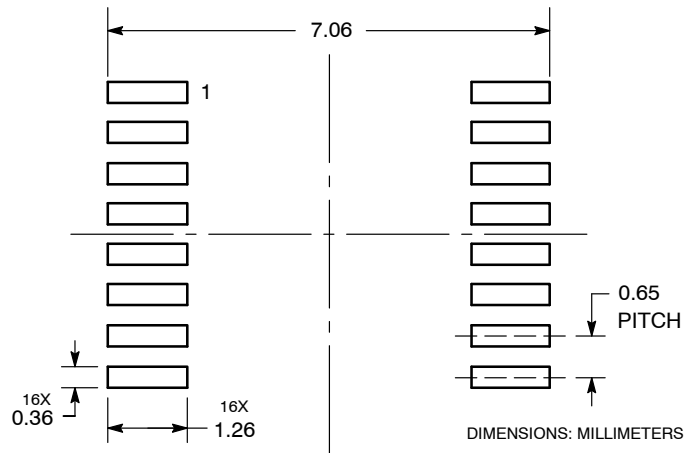


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

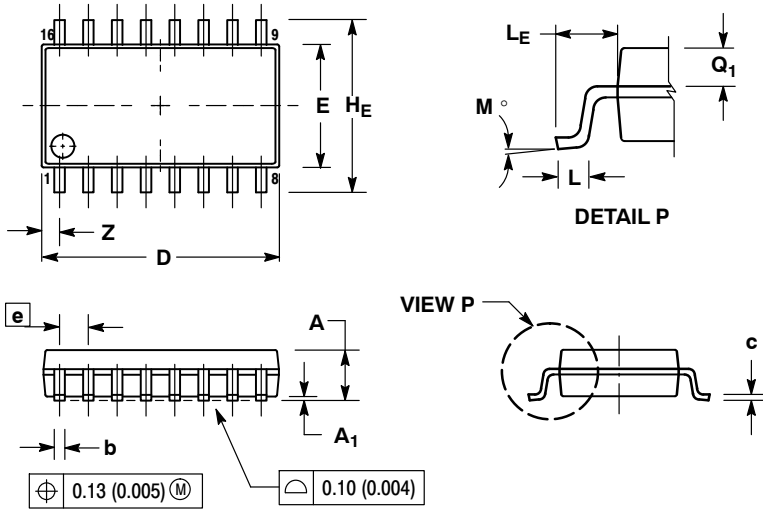
### SOLDERING FOOTPRINT



# MC74HC165A

## PACKAGE DIMENSIONS

SOEIAJ-16  
CASE 966  
ISSUE A



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H <sub>E</sub>	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L <sub>E</sub>	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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