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EClamp2384K
ESD/EMI Protection
for Color LCD Interfaces

PROTECTION PRODUCTS - EMIClamp™

Description

The EClamp™2384K is a low pass filter array with integrated TVS diodes. It is designed to suppress un-wanted EMI/RFI signals and provide electrostatic discharge (ESD) protection in portable electronic equipment. This state-of-the-art device utilizes solid-state silicon-avalanche technology for superior clamping performance and DC electrical characteristics. It has been optimized for **protection of color LCD panels** in cellular phones and other portable electronics.

The device consists of four identical circuits comprised of TVS diodes for ESD protection, and a resistor - capacitor network for EMI/RFI filtering. A series resistor value of 200Ω and a capacitance value of 12pF are used to achieve 30dB minimum attenuation from 800MHz to 2.7GHz. The TVS diodes provide effective suppression of ESD voltages in excess of ±15kV (air discharge) and ±8kV (contact discharge) per IEC 61000-4-2, level 4.

The EClamp2384K is in a 8-pin, RoHS/WEEE compliant, SLP1713P8 package. It measures 1.7 x 1.3 x 0.50mm. The leads are spaced at a pitch of 0.4mm and are finished with lead-free NiPdAu. The small package makes it ideal for use in portable electronics such as cell phones, digital still cameras, and PDAs.

Features

◆ Bidirectional EMI/RFI filter with integrated TVS for ESD protection
◆ ESD protection to **IEC 61000-4-2 (ESD) Level 4, ±15kV (air), ±8kV (contact)**
◆ Filter performance: 30dB minimum attenuation 800MHz to 2.7GHz
◆ TVS working voltage: 5V
◆ Resistor: 200Ω +/− 15%
◆ Typical Capacitance: 12pF (VR = 2.5V)
◆ Protection and filtering for four lines
◆ Solid-state technology

Mechanical Characteristics

◆ SLP1713P8 8-pin package
◆ RoHS/WEEE Compliant
◆ Nominal Dimensions: 1.7 x 1.3 x 0.50 mm
◆ Lead Pitch: 0.40mm
◆ Lead finish: NiPdAu
◆ Marking: Marking Code
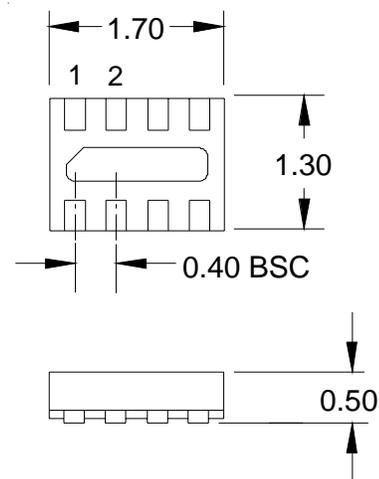◆ Packaging: Tape and Reel per EIA 481

Applications

◆ Color LCD Protection
◆ Cell Phone CCD Camera Lines
◆ Clamshell Cell Phones

Circuit Diagram (Each Line)
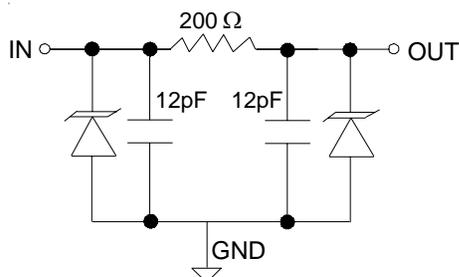
Device Schematic (4X)

Package Configuration

8 Pin SLP package (Bottom Side View)
Nominal Dimensions in mm

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Maximum Ratings

Rating	Symbol	Value	Units
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	+/- 17 +/- 12	kV
Junction Temperature	T_J	125	^{o}C
Operating Temperature	T_{op}	-40 to +85	^{o}C
Storage Temperature	T_{STG}	-55 to +150	^{o}C

Electrical Characteristics (T = 25°C)

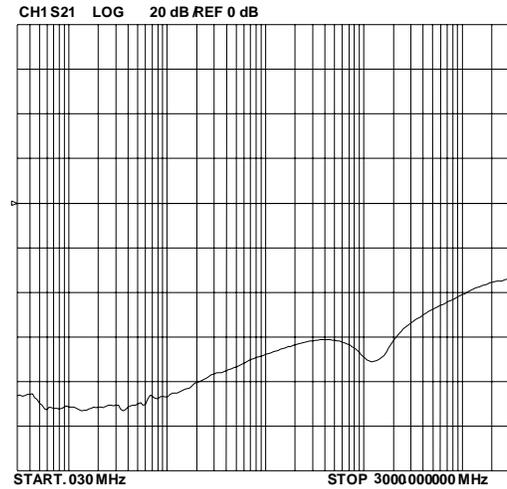| Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
TVS Reverse Stand-Off Voltage	V_{RWM}				5	V
TVS Reverse Breakdown Voltage	V_{BR}	I_t = 1mA	6	8	10	V
TVS Reverse Leakage Current	I_R	V_{RWM} = 3.0V			0.5	µA
Total Series Resistance	R	Each Line	170	200	230	Ohms
Capacitance	C_1, C_2	Each Line V_R = 2.5V, f = 1MHz	10	12	15	pF
Total Capacitance	C_{in}	Input to Gnd, Each Line V_R = 2.5V, f = 1MHz	20	24	30	pF

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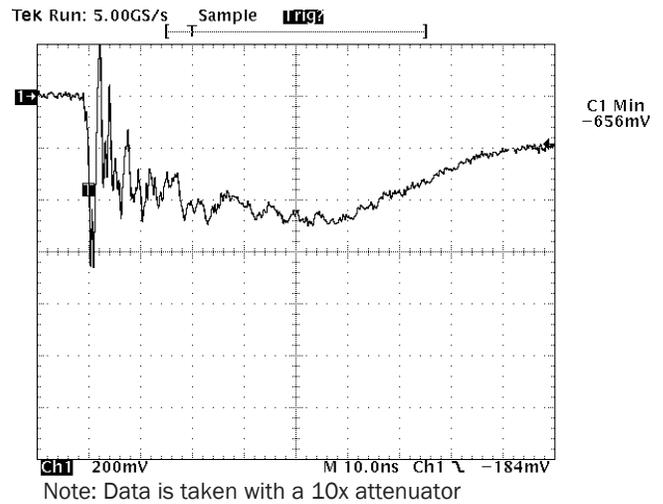## Typical Characteristics

Typical Insertion Loss S21 (Each Line)

CH1 S21   LOG   6 dB / REF 0 dB

1: -12.305 dB
   106.6 MHz

2: -35.996 dB
   800 MHz

3: -38.349 dB
   1.8 GHz

4: -36.250 dB
   2.7 GHz

START .030 MHz   STOP 3000 000000 MHz
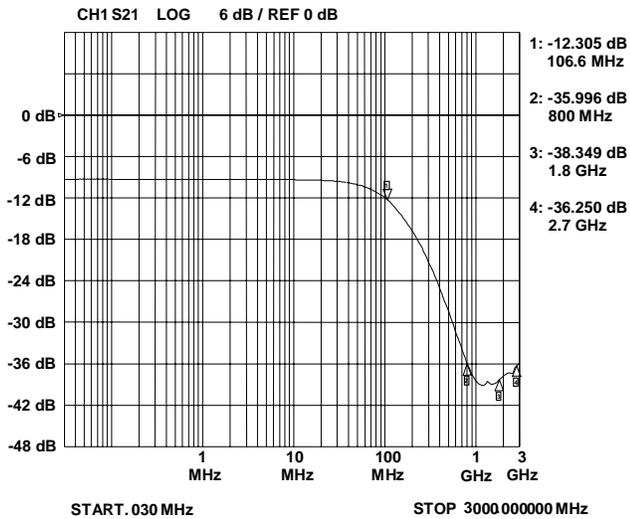
Analog Crosstalk (Each Line)

CH1 S21   LOG   20 dB / REF 0 dB

START .030 MHz   STOP 3000 000000 MHz

ESD Clamping (+8kV Contact)

Tek Run: 5.00GS/s   Sample   Trig?

C1 Max
1.73 V

Ch1   500mV   M 10.0ns Ch1 ∫   960mV

Note: Data is taken with a 10x attenuator

ESD Clamping (-8kV Contact)

Tek Run: 5.00GS/s   Sample   Trig?

C1 Min
−656mV

Ch1   200mV   M 10.0ns Ch1 ∖   −184mV

Note: Data is taken with a 10x attenuator
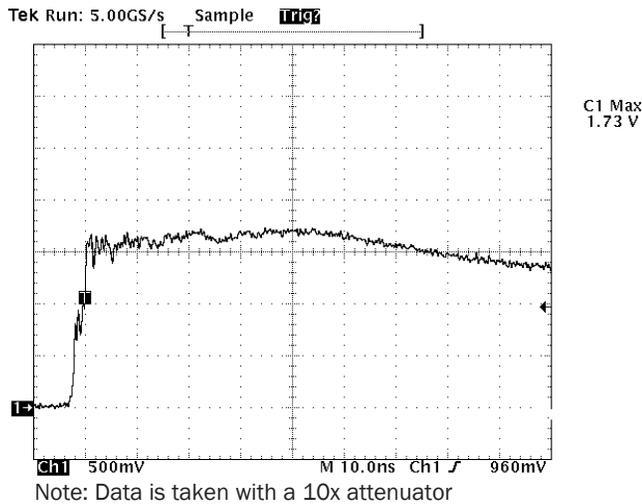
Normalized Capacitance vs. Reverse Voltage
(Normalized to 2.5 volts)
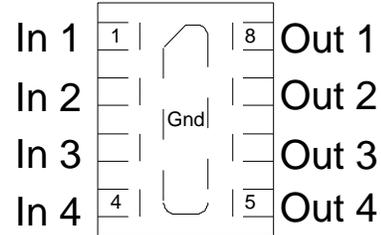
$C_J(V_R) / C_J(V_R=2.5)$

f = 1 MHz

Reverse Voltage - V_R (V)

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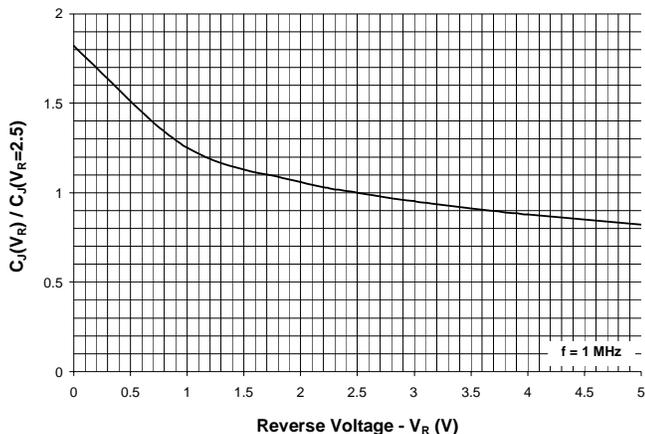
Device Connection

The EClamp2384K is comprised of four identical circuits each consisting of a low pass filter for EMI/RFI suppression and dual TVS diodes for ESD protection. The device is in a 8-pin SLP package. Electrical connection is made to the 8 pins located at the bottom of the device. A center tab serves as the ground connection. The device has a flow through design for easy layout. Pin connections are noted in Figure 1. All path lengths should be kept as short as possible to minimize the effects of parasitic inductance in the board traces. Recommendations for the ground connection are given below.

Ground Connection Recommendation

Parasitic inductance present in the board layout will affect the filtering performance of the device. As frequency increases, the effect of the inductance becomes more dominant. This effect is given by Equation 1.

Equation 1: The Impedance of an Inductor at Frequency XLF

$$XLF(L, f) = 2 * \pi * f * L$$

Where:
L= Inductance (H)
f = Frequency (Hz)

Via connections to the ground plane form rectangular wire loops or ground loop inductance as shown in Figure 2. Ground loop inductance can be reduced by using multiple vias to make the connection to the ground plane. Bringing the ground plane closer to the signal layer (preferably the next layer) also reduces ground loop inductance. Multiple vias in the device ground pad will result in a lower inductive ground loop over two exterior vias. Vias with a diameter d are separated by a distance y run between layers separated by a distance x. The inductance of the loop path is given by Equation 2. Thus, decreasing distance x and y will reduce the loop inductance and result in better high frequency filter characteristics.

Figure 1 - Pin Identification and Configuration (Top Side View)

Pin	Identification
1 - 4	Input Lines
5 - 8	Output Lines
Center Tab	Ground

Figure 2 - Inductance of Rectangular Wire Loops
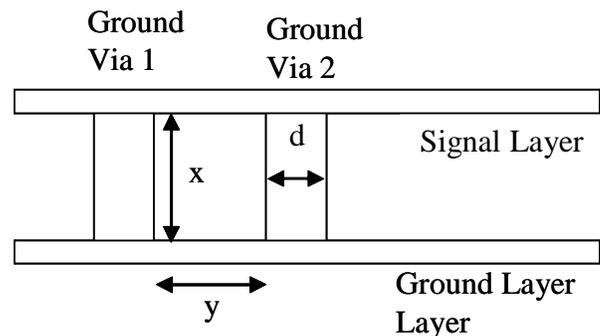
Equation 2: Inductance of Rectangular Wire Loop

$$LRECT(d, x, y) = 10.16 * 10^{-9} * \left[x * \ln\left[\frac{2*y}{d}\right] + y * \ln\left[\frac{2*x}{d}\right] \right]$$

Where:
d = Diameter of the wire (in)
x = Length of wire loop (in)
y = Breath of wire loop (in)

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Applications Information

Figure 3 shows the recommended device layout. The ground pad vias have a diameter of 0.008 inches (0.20 mm) while the two external vias have a diameter of 0.010 inches (0.250mm). The internal vias are spaced approximately evenly from the center of the pad. The designer may choose to use more vias with a smaller diameter (such as 0.005 inches or 0.125mm) since changing the diameter of the via will result in little change in inductance (i.e. the log function in Equation 2 in highly insensitive to parameter d) . Figure 4 shows a typical insertion loss (S21) plot for the device using Semtech's filter evaluation board with 50 Ohm traces and the recommended via configuration.

Figure 4 - Filter Characteristics Using Recommended Layout with Internal Vias

CH1 S21   LOG   6 dB / REF 0 dB

1: -12.305 dB
106.6 MHz

2: -35.996 dB
800 MHz

3: -38.349 dB
1.8 GHz

4: -36.250 dB
2.7 GHz

START .030 MHz   STOP 3000.000000 MHz

Figure 3 - Recommended Layout Using Ground Vias

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EClamp2384K Spice Model

Table 1 - EClamp2384K Spice Parameters			
Parameter	**Unit**	**D1 (TVS)**	**D2 (TVS)**
IS	Amp	5.15E-15	5.15E-15
BV	Volt	7.53	7.53
VJ	Volt	0.75	0.75
RS	Ohm	0.426	0.426
IBV	Amp	1E-3	1E-3
CJO	Farad	23E-12	23E-12
TT	sec	2.541E-9	2.541E-9
M	--	0.256	0.256
N	--	1.1	1.1
EG	eV	1.11	1.11

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Outline Drawing - SLP1713P8
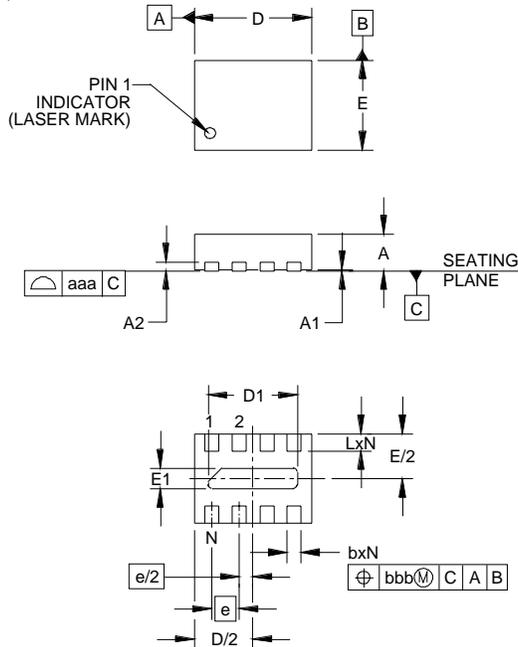
DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.018	.020	.022	0.45	0.50	0.55
A1	.000	.001	.002	0.00	0.02	0.05
A2	(.005)			(0.13)		
b	.006	.008	.010	0.15	0.20	0.25
D	.065	.067	.070	1.65	1.70	1.775
D1	.047	.051	.055	1.20	1.30	1.40
E	.049	.051	.054	1.25	1.30	1.375
E1	.008	.012	.016	0.20	0.30	0.40
e	.016 BSC			0.40 BSC		
L	.008	.010	.012	0.20	0.25	0.30
N	8			8		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern - SLP1713P8
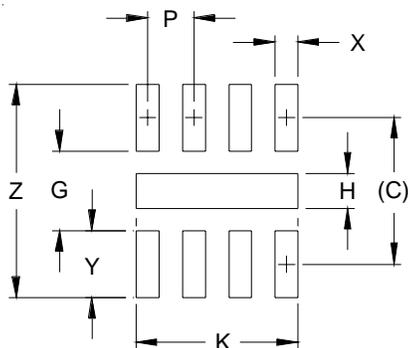
DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.050)	(1.27)
G	.027	0.69
H	.012	0.30
K	.055	1.40
P	.016	0.40
X	.008	0.20
Y	.023	0.58
Z	.073	1.85

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET

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Marking

PIN 1
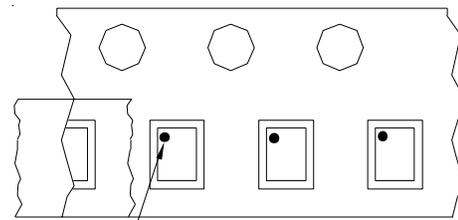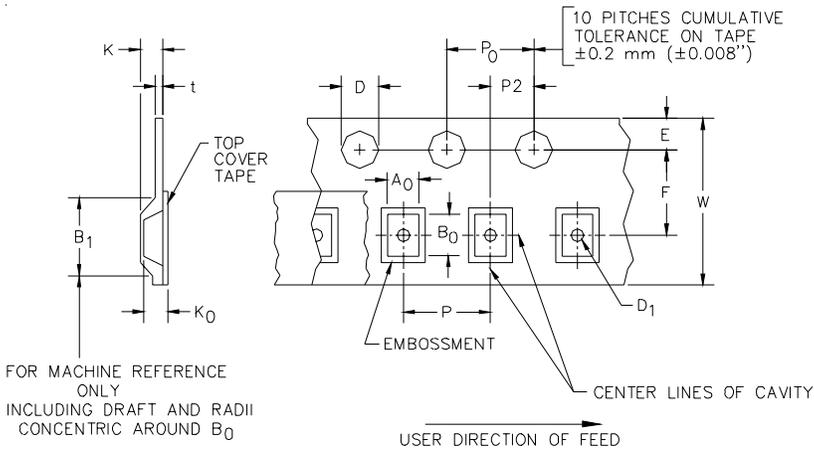INDICATOR

2384K
YYWW
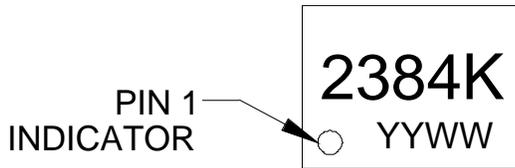
Note: YYWW = Date Code

Ordering Information

Part Number	Qty per Reel	Reel Size
EClamp2384K.TCT	3000	7 Inch

EMIClamp and EClamp are marks of Semtech Corporation

Tape and Reel Specification

10 PITCHES CUMULATIVE TOLERANCE ON TAPE ±0.2 mm (±0.008'')

TOP COVER TAPE

FOR MACHINE REFERENCE ONLY INCLUDING DRAFT AND RADII CONCENTRIC AROUND B0

EMBOSSMENT

CENTER LINES OF CAVITY

USER DIRECTION OF FEED

Pin 1 Location

User Direction of feed

Device Orientation in Tape

A0	B0	K0
1.51 +/-0.05 mm	1.91 +/-0.05 mm	0.66 +/-0.05 mm

Tape Width	B, (Max)	D	D1	E	F	K (MAX)	P	P0	P2	T(MAX)	W
8 mm	4.2 mm (.165)	1.5 + 0.1 mm - 0.0 mm (0.59 +.005 - .000)	0.8 mm ±0.05 (.031)	1.750±.10 mm (.069±.004)	3.5±0.05 mm (.138±.002)	2.4 mm (.094)	4.0±0.1 mm (.157±.004)	4.0±0.1 mm (.157±.004)	2.0±0.05mm (.079±.002)	0.4 mm (.016)	8.0 mm + 0.3 mm - 0.1 mm (.312±.012)

Contact Information

Semtech Corporation
Protection Products Division
200 Flynn Rd., Camarillo, CA 93012
Phone: (805)498-2111   FAX (805)498-3804

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ЭЛЕКТРОННЫХ КОМПОНЕНТОВ

многоканальный

📞 +7 495 668 12 70

✉ info@moschip.ru

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

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Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru   moschip.ru_6
moschip.ru_4   moschip.ru_9