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February 2010

# FDS2672\_F085 N-Channel UltraFET Trench MOSFET 200V, 3.9A, $70m\Omega$

#### **Features**

- Max  $r_{DS(on)} = 70 m\Omega$  at  $V_{GS} = 10 V$ ,  $I_D = 3.9 A$
- Max  $r_{DS(on)} = 80 \text{m}\Omega$  at  $V_{GS} = 6V$ ,  $I_D = 3.5A$
- Fast switching speed
- High performance trench technology for extremely low r<sub>DS(on)</sub>
- Qualified to AEC Q101
- RoHS compliant

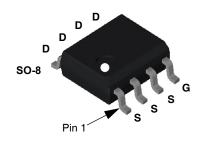
#### **General Description**

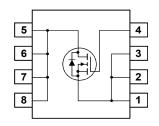
This single N-Channel MOSFET is produced using Fairchild Semiconductor's advanced UltraFET Trench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

#### **Application**

■ DC-DC conversion







#### MOSFET Maximum Ratings T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units	
V <sub>DS</sub>	Drain to Source Voltage		200	V
V <sub>GS</sub>	Gate to Source Voltage		±20	V
I <sub>D</sub>	Drain Current -Continuous	(Note 1a)	3.9	^
	-Pulsed		50	A
E <sub>AS</sub>	Single Pulse Avalanche Energy	(Note 3)	37.5	mJ
n	Power Dissipation	(Note 1a)	2.5	14/
$P_{D}$	Power Dissipation	(Note 1b)	1.0	W
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature		-55 to 150	°C

#### **Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	25	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	125	

#### **Package Marking and Ordering Information**

Device Marking	Device	Reel Size	Tape Width	Quantity
FDS2672	FDS2672_F085	13"	12mm	2500 units

Units

#### Electrical Characteristics T<sub>J</sub> = 25°C unless otherwise noted

**Parameter** 

Off Characteristics								
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	200			V		
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, referenced to 25°C		206		mV/°C		
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 160V, V <sub>GS</sub> =0V V <sub>DS</sub> = 160V, V <sub>GS</sub> =0V T <sub>.I</sub> = 55°C			1 10	μ <b>Α</b> μ <b>Α</b>		
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS} = 100V, V_{GS} = 0V$ $V_{GS} = 20V$			±100	μA nA		

**Test Conditions** 

Min

Тур

Max

#### On Characteristics (Note 2)

Symbol

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	2	2.9	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25°C		-11		mV/°C
		$V_{GS} = 10V, I_D = 3.9A$		59	70	
r <sub>DS(on)</sub>	r <sub>DS(on)</sub> Drain to Source On Resistance	$V_{GS} = 6V, I_D = 3.5A$		63	80	mΩ
		$V_{GS} = 10V, I_D = 3.9A, T_J = 125^{\circ}C$		124	148	
9 <sub>FS</sub>	Forward Transcondductance	$V_{DS} = 10V, I_{D} = 3.9A$		15		S

#### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	1001/1/		1905	2535	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V, f = 1MHz		100	135	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1101112		30	45	pF
$R_g$	Gate Resistance	f = 1MHz		0.7		Ω

#### **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time	., ,,,,,		22	35	ns
t <sub>r</sub>	Rise Time	$V_{DD}$ = 100V, $I_{D}$ = 3.9A $V_{GS}$ = 10V, $R_{GEN}$ = 6 $\Omega$		10	20	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	V <sub>GS</sub> = 10V, K <sub>GEN</sub> = 6Ω		35	56	ns
t <sub>f</sub>	Fall Time			10	20	ns
$Q_{g(TOT)}$	Total Gate Charge at 10V			33	46	nC
Q <sub>gs</sub>	Gate to Source Gate Charge	V <sub>DD</sub> =100V I <sub>D</sub> = 3.9A		11		nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge			7		nC

#### **Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Voltage	$V_{GS} = 0V, I_{S} = 3.9A$	0.75	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 3.9A, di/dt = 100A/μs	67	101	ns
Q <sub>rr</sub>	Reverse Recovery Charge	I <sub>F</sub> = 3.9A, di/dt = 100A/μs	179	269	nC

#### Notes

1. R<sub>θ,JA</sub> is the sum of the junction-to-case and case-to- ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θ,JC</sub> is guaranteed by design while R<sub>θ,CA</sub> is determined by the user's board design.



**a)** 50°C/W (10 sec) 62.5°C/W steady state when mounted on a 1in<sup>2</sup> pad of 2 oz copper



**b)**  $125^{\circ}\text{C/W}$  when mounted on a minimum pad .

Scale 1:1 on letter size paper

- 2: Pulse Test: Pulse Width < 300 us, Duty Cycle < 2.0%.
- 3: Starting  $T_J = 25^{\circ}C$ , L = 3mH,  $I_{AS} = 5A$ ,  $V_{DD} = 100V$ ,  $V_{GS} = 10V$

#### Typical Characteristics T<sub>J</sub> = 25°C unless otherwise noted

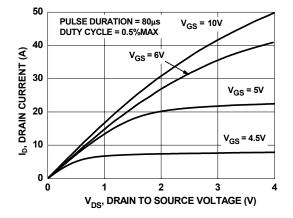


Figure 1. On Region Characteristics

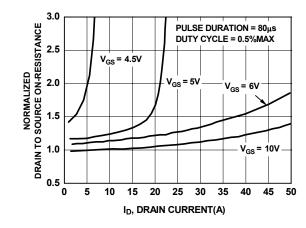


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

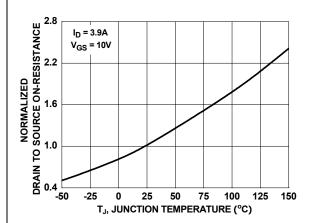


Figure 3. Normalized On Resistance vs Junction Temperature

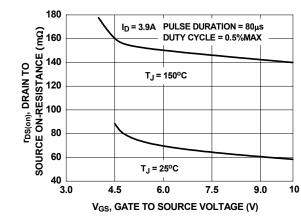


Figure 4. On-Resistance vs Gate to Source Voltage

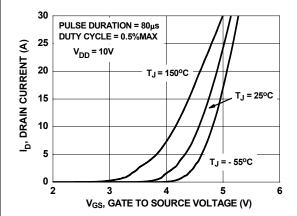


Figure 5. Transfer Characteristics

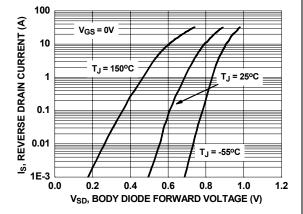


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

#### Typical Characteristics T<sub>J</sub> = 25°C unless otherwise noted

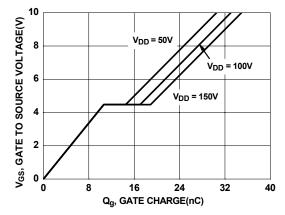


Figure 7. Gate Charge Characteristics

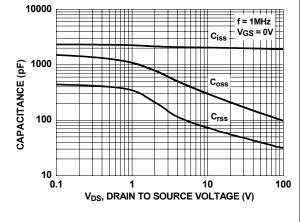


Figure 8. Capacitance vs Drain to Source Voltage

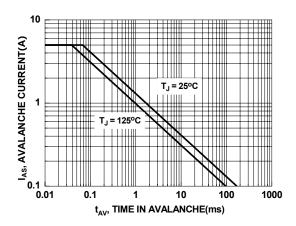


Figure 9. Unclamped Inductive Switching Capability

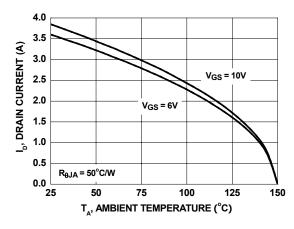


Figure 10. Ambient Continuous Drain Current vs
Case Temperature

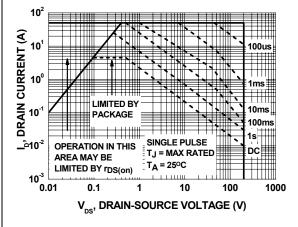


Figure 11. Forward Bias Safe Operating Area

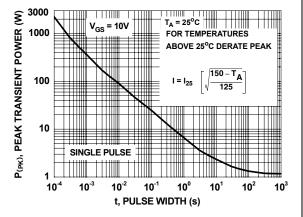


Figure 12. Single Pulse Maximum Power Dissipation



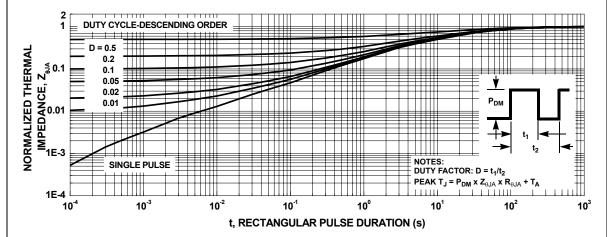


Figure 13. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b Transient thermal response will change depending on the circuit board design





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