

TOSHIBA Field-Effect Transistor Silicon N Channel MOS Type (U-MOSIV)

SSM3K7002BFU

High-Speed Switching Applications

Analog Switch Applications

- Small package
- Low ON-resistance : $R_{DS(ON)} = 3.3 \Omega$ (max) (@ $V_{GS} = 4.5$ V)
- : $R_{DS(ON)} = 2.6 \Omega$ (max) (@ $V_{GS} = 5$ V)
- : $R_{DS(ON)} = 2.1 \Omega$ (max) (@ $V_{GS} = 10$ V)

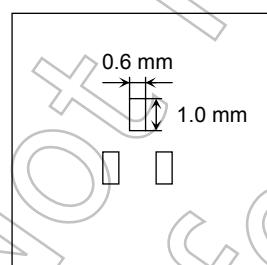
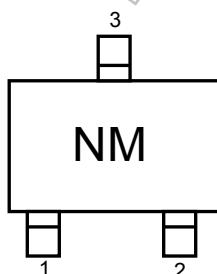
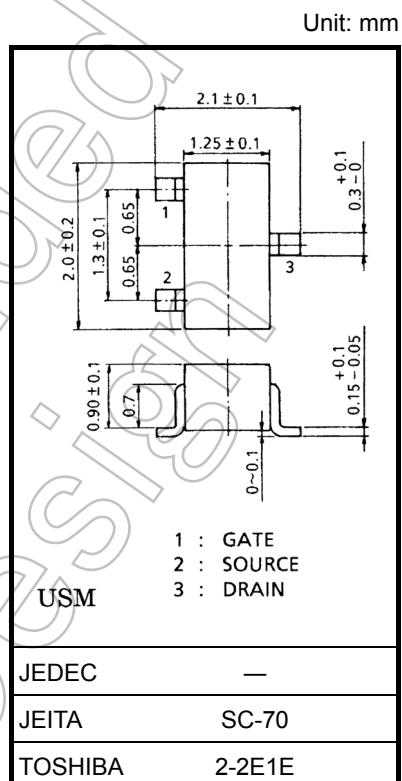
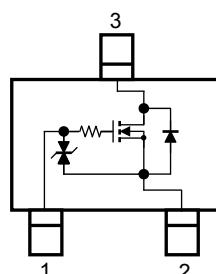
Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	60	V
Gate-source voltage	V_{GSS}	± 20	V
Drain current	DC I_D	200	mA
	Pulse I_{DP}	800	
Drain power dissipation (Ta = 25°C)	P_D (Note 1)	150	mW
Channel temperature	T_{ch}	150	°C
Storage temperature range	T_{stg}	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: mounted on FR4 board

(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 0.6mm² × 3)**Marking****Equivalent Circuit (top view)**

Weight: 6.0 mg (typ.)

Start of commercial production
2009-07

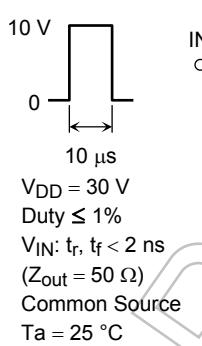
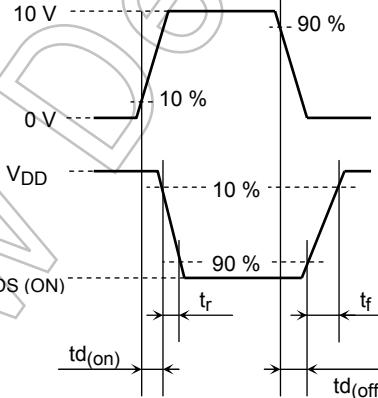
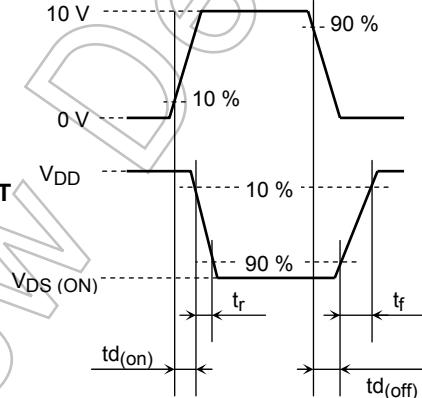
Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit	
Gate leakage current	I _{GSS}	V _{GS} = ± 20 V, V _{DS} = 0 V	—	—	± 10	µA	
Drain-source breakdown voltage	V _{(BR) DSS}	I _D = 10 mA, V _{GS} = 0 V	60	—	—	V	
	V _{(BR) DSX}	I _D = 10 mA, V _{GS} = -10 V	45	—	—		
Drain cutoff current	I _{DS}	V _{DS} = 60 V, V _{GS} = 0 V	—	—	1	µA	
Gate threshold voltage	V _{th}	V _{DS} = 10 V, I _D = 0.25 mA	1.5	—	3.1	V	
Forward transfer admittance	Y _{fs}	V _{DS} = 10 V, I _D = 200 mA (Note 2)	225	—	—	µS	
Drain-source ON-resistance	R _{DS (ON)}	I _D = 500 mA, V _{GS} = 10 V (Note 2)	—	1.62	2.1	Ω	
		I _D = 100 mA, V _{GS} = 5 V (Note 2)	—	1.90	2.6		
		I _D = 100 mA, V _{GS} = 4.5 V (Note 2)	—	2.10	3.3		
Input capacitance	C _{iss}	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz	—	17.0	—	pF	
Reverse transfer capacitance	C _{rss}		—	1.9	—		
Output capacitance	C _{oss}		—	3.6	—		
Switching time	Turn-on delay time	td(on)	V _{DD} = 30 V, I _D = 200 mA, V _{GS} = 0 to 10 V	—	3.3	6.6	ns
	Turn-off delay time	td(off)		—	14.5	40	
Drain-source forward voltage	V _{DSF}	I _D = -200 mA, V _{GS} = 0 V (Note 2)	—	-0.84	-1.2	V	

Note2: Pulse test

Switching Time Test Circuit

(a) Test circuit

(b) V_{IN}(c) V_{OUT}

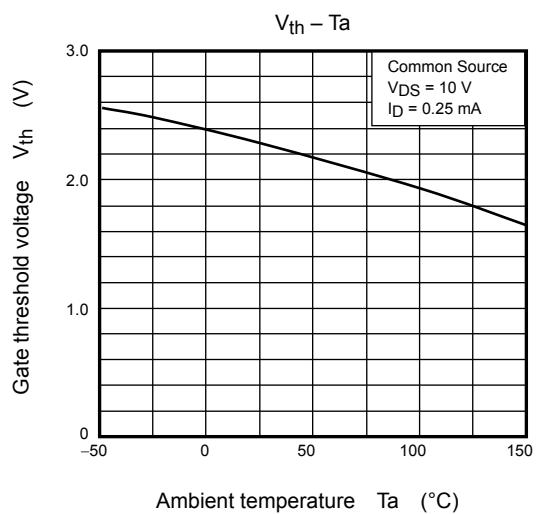
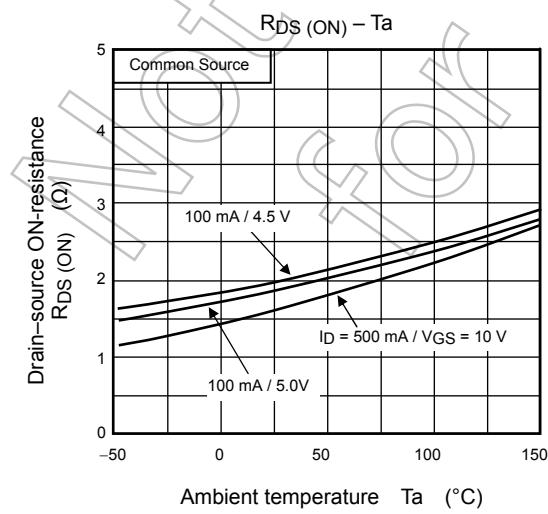
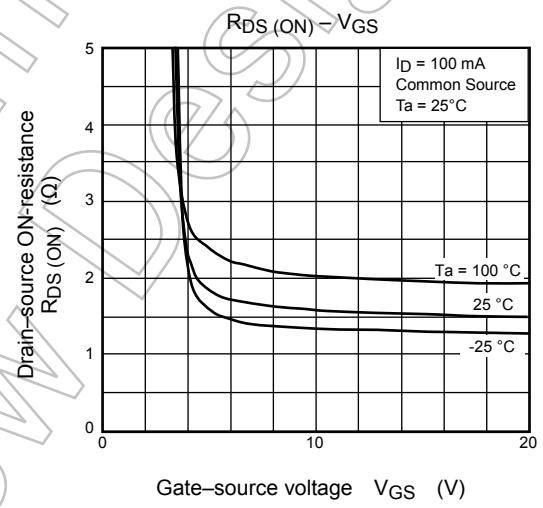
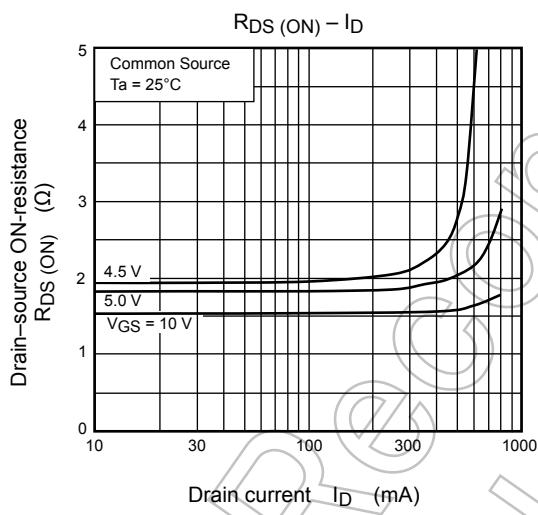
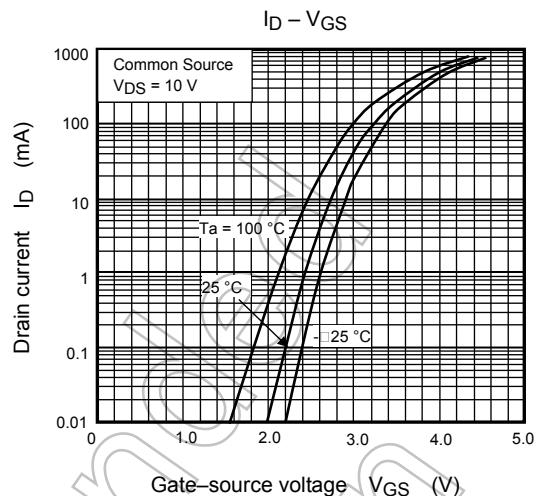
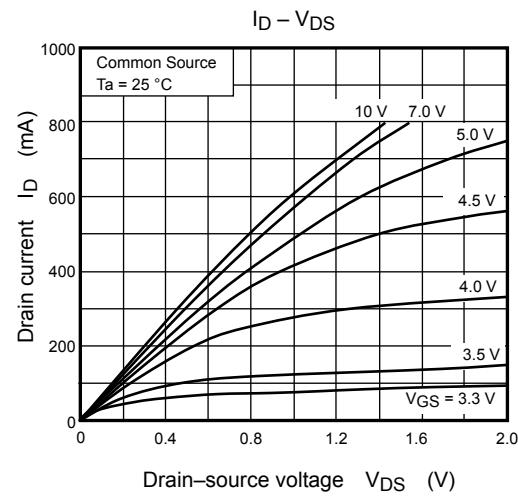
Precaution

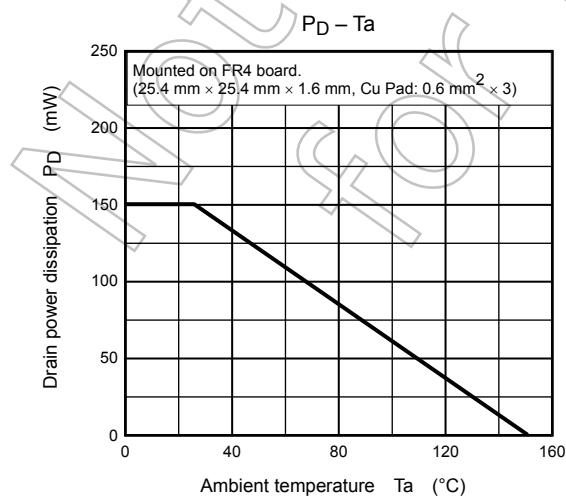
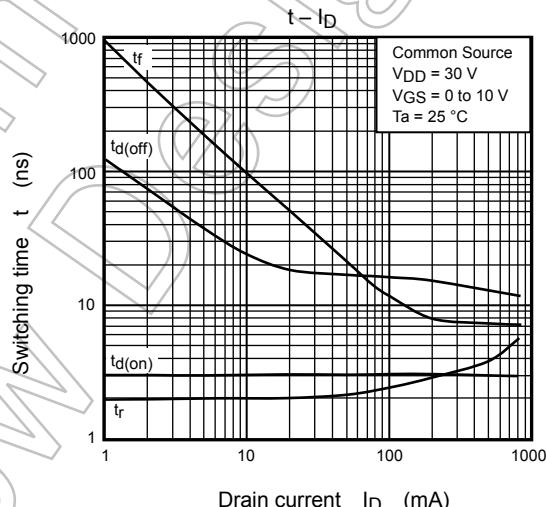
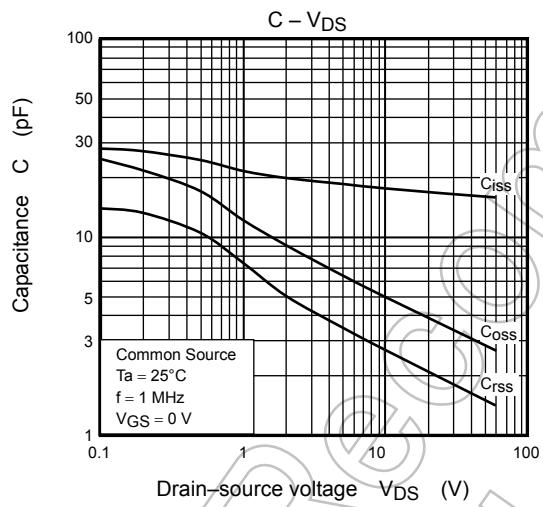
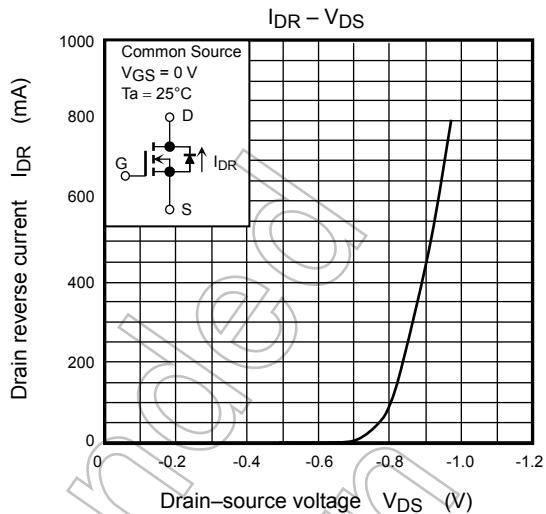
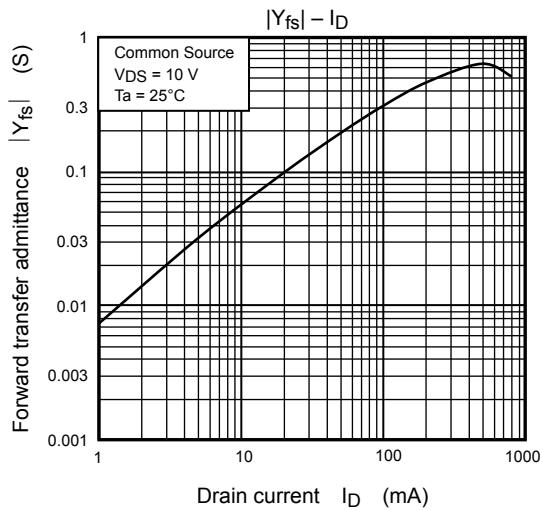
Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to be low (0.25 mA for the SSM3K7002BFU). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th} , and $V_{GS(off)}$ must be lower than V_{th} . This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

Take this into consideration when using the device

Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.





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