# 1 MSPS,12-Bit ADCs

# AD7475/AD7495

## FEATURES AND APPLICATIONS

**Fast throughput rate: 1 MSPS**
**Specified for $V_{DD}$ of 2.7 V to 5.25 V**
**Low power:**
**4.5 mW max at 1 MSPS with 3 V supplies**
**10.5 mW max at 1 MSPS with 5 V supplies**
**Wide input bandwidth:**
**68 dB SNR at 300 kHz input frequency**
**Flexible power/serial clock speed management**
**No pipeline delays**
**High speed serial interface:**
**SPI™-/QSPI™-/MICROWIRE™-/DSP-compatible**
**On-board reference: 2.5 V (AD7495 only)**
**Standby mode: 1 µA max**
**8-lead MSOP and SOIC packages**

**Battery-powered systems**
**Personal digital assistants**
**Medical instruments**
**Mobile communications**
**Instrumentation and control systems**
**Data acquisition systems**
**Optical sensors**

## GENERAL DESCRIPTION

The AD7475/AD7495[1] are 12-bit, high speed, low power, successive-approximation ADCs that operate from a single 2.7 V to 5.25 V power supply with throughput rates up to 1 MSPS. They contain a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies above 1 MHz.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock, allowing the devices to interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$ and conversion is initiated at this point. The conversion time is determined by the SCLK frequency. There are no pipeline delays associated with the part.

The AD7475/AD7495 use advanced design techniques to achieve very low power dissipation at high throughput rates. With 3 V supplies and a 1 MSPS throughput rate, the AD7475 consumes just 1.5 mA, while the AD7495 consumes 2 mA. With 5 V supplies and 1 MSPS, the current consumption is 2.1 mA for the AD7475 and 2.6 mA for the AD7495.

The analog input range for the parts is 0 V to REF IN. The 2.5 V reference for the AD7475 is applied externally to the REF IN pin, while the AD7495 has an on-board 2.5 V reference.

[1]Protected by U.S. Patent No. 6,681,332

**Rev. B**
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## FUNCTIONAL BLOCK DIAGRAMS

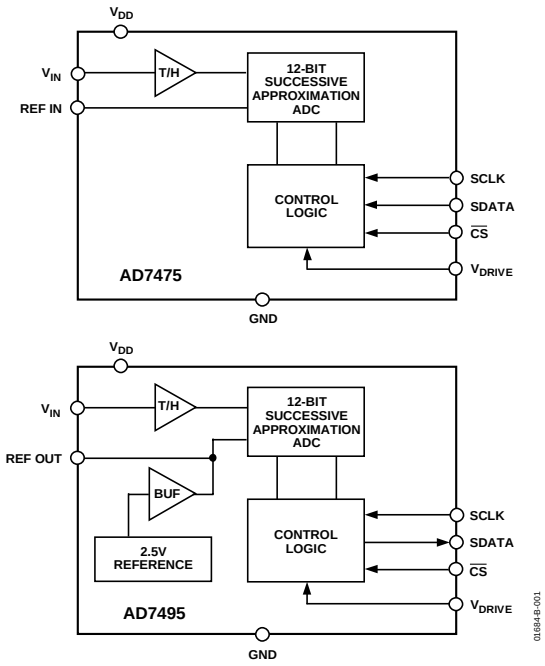


*Figure 1.*

## PRODUCT HIGHLIGHTS

1. The AD7475 offers 1 MSPS throughput rates with 4.5 mW power consumption.
2. Single-supply operation with $V_{DRIVE}$ function. The AD7475/AD7495 operate from a single 2.7 V to 5.25 V supply. The $V_{DRIVE}$ function allows the serial interface to connect directly to either 3 V or 5 V processor systems independent of $V_{DD}$.
3. Flexible power/serial clock speed management. The conversion rate is determined by the serial clock, allowing the conversion time to be reduced through the serial clock speed increase. The parts also feature shutdown modes to maximize power efficiency at lower throughput rates. This allows the average power consumption to be reduced while not converting. Power consumption is 1 µA when in full shutdown.
4. No pipeline delay. The parts feature a standard successive approximation ADC with accurate control of the sampling instant via a $\overline{CS}$ input and once-off conversion control.

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## REVISION HISTORY

**5/05—Rev. A to Rev. B**

Updated Format ..... Universal
Added Patent Information ..... 1
Updated Outline Dimensions ..... 23
Changes to Ordering Guide ..... 24

# AD7475 SPECIFICATIONS

$V_{DD}$ = 2.7 V to 5.25 V, $V_{DRIVE}$ = 2.7 V to 5.25 V, REF IN = 2.5 V, $f_{SCLK}$ = 20 MHz, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 1.**

| Parameter | A Version[1] | B Version[1] | Unit | Test Conditions/Comments |
|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | |
| Signal-to-Noise and Distortion Ratio (SINAD) | 68 | 68 | dB min | $f_{IN}$ = 300 kHz sine wave, $f_{SAMPLE}$ = 1 MSPS |
| Total Harmonic Distortion (THD) | −75 | −75 | dB max | $f_{IN}$ = 300 kHz sine wave, $f_{SAMPLE}$ = 1 MSPS |
| Peak Harmonic or Spurious Noise (SFDR) | −76 | −76 | dB max | $f_{IN}$ = 300 kHz sine wave, $f_{SAMPLE}$ = 1 MSPS |
| Intermodulation Distortion (IMD) | | | | |
| Second-Order Terms | −78 | −78 | dB typ | |
| Third-Order Terms | −78 | −78 | dB typ | |
| Aperture Delay | 10 | 10 | ns typ | |
| Aperture Jitter | 50 | 50 | ps typ | |
| Full Power Bandwidth | 8.3 | 8.3 | MHz typ | @ 3 dB |
| Full Power Bandwidth | 1.3 | 1.3 | MHz typ | @ 0.1 dB |
| DC ACCURACY | | | | |
| Resolution | 12 | 12 | Bits | |
| Integral Nonlinearity | ±1.5 | ±1 | LSB max | @ 5 V (typ @ 3 V) |
| | ±0.5 | ±0.5 | LSB typ | @ 25°C |
| Differential Nonlinearity | +1.5/−0.9 | +1.5/−0.9 | LSB max | @ 5 V guaranteed no missed codes to 12 bits (typ @ 3 V) |
| | ±0.5 | ±0.5 | LSB typ | @ 25°C |
| Offset Error | ±8 | ±8 | LSB max | Typically ±2.5 LSB |
| Gain Error | ±3 | ±3 | LSB max | |
| ANALOG INPUT | | | | |
| Input Voltage Ranges | 0 to REF IN | | V | |
| DC Leakage Current | ±1 | ±1 | µA max | |
| Input Capacitance | 20 | 20 | pF typ | |
| REFERENCE INPUT | | | | |
| REF IN Input Voltage Range | 2.5 | 2.5 | V | ±1% for specified performance |
| DC Leakage Current | ±1 | ±1 | µA max | |
| Input Capacitance | 20 | 20 | pF typ | |
| LOGIC INPUTS | | | | |
| Input High Voltage, $V_{INH}$ | $V_{DRIVE}$ − 1 | $V_{DRIVE}$ − 1 | V min | |
| Input Low Voltage, $V_{INL}$ | 0.4 | 0.4 | V max | |
| Input Current, $I_{IN}$ | ±1 | ±1 | µA max | Typically 10 nA, $V_{IN}$ = 0 V or $V_{DRIVE}$ |
| Input Capacitance, $C_{IN}$[2] | 10 | 10 | pF max | |
| LOGIC OUTPUTS | | | | |
| Output High Voltage, $V_{OH}$ | $V_{DRIVE}$ − 0.2 | | V min | $I_{SOURCE}$ = 200 µA; $V_{DRIVE}$ = 2.7 V to 5.25 V |
| Output Low Voltage, $V_{OL}$ | 0.4 | 0.4 | V max | $I_{SINK}$ = 200 µA |
| Floating-State Leakage Current | ±10 | ±10 | µA max | |
| Floating-State Output Capacitance | 10 | 10 | pF max | |
| Output Coding | Straight (Natural) Binary | | | |
| CONVERSION RATE | | | | |
| Conversion Time | 800 | 800 | ns max | 16 SCLK cycles with SCLK at 20 MHz |
| Track-and-Hold Acquisition Time | 300 | 300 | ns max | Sine wave input |
| | 325 | 325 | ns max | Full-scale step input |
| Throughput Rate | 1 | 1 | MSPS max | See the Serial Interface section |

| Parameter | A Version[1] | B Version[1] | Unit | Test Conditions/Comments |
|---|---|---|---|---|
| POWER REQUIREMENTS | | | | |
| $V_{DD}$ | 2.7/5.25 | 2.7/5.25 | V min/max | |
| $V_{DRIVE}$ | 2.7/5.25 | 2.7/5.25 | V min/max | |
| $I_{DD}$[3] | | | | Digital inputs = 0 V or $V_{DRIVE}$ |
| Normal Mode (Static) | 750 | 750 | μA typ | $V_{DD}$ = 2.7 V to 5.25 V, SCLK on or off |
| Normal Mode (Operational) | 2.1 | 2.1 | mA max | $V_{DD}$ = 4.75 V to 5.25 V, $f_{SAMPLE}$ = 1 MSPS |
| | 1.5 | 1.5 | mA max | $V_{DD}$ = 2.7 V to 3.6 V, $f_{SAMPLE}$ = 1 MSPS |
| Partial Power-Down Mode | 450 | 450 | μA typ | $f_{SAMPLE}$ = 100 kSPS |
| Partial Power-Down Mode | 100 | 100 | μA max | Static |
| Full Power-Down Mode | 1 | 1 | μA max | SCLK on or off |
| Power Dissipation | | | | |
| Normal Mode (Operational) | 10.5 | 10.5 | mW max | $V_{DD}$ = 5 V, $f_{SAMPLE}$ = 1 MSPS |
| | 4.5 | 4.5 | mW max | $V_{DD}$ = 3 V, $f_{SAMPLE}$ = 1 MSPS |
| Partial Power-Down (Static) | 500 | 500 | μW max | $V_{DD}$ = 5 V |
| | 300 | 300 | μW max | $V_{DD}$ = 3 V |
| Full Power-Down | 5 | 5 | μW max | $V_{DD}$ = 5 V |
| | 3 | 3 | μW max | $V_{DD}$ = 3 V |

[1] Temperature ranges for A, B versions: −40°C to +85°C.
[2] Guaranteed by initial characterization.
[3] See the Power vs. Throughput Rate section.

# AD7495 SPECIFICATIONS

$V_{DD}$ = 2.7 V to 5.25 V, $V_{DRIVE}$ = 2.7 V to 5.25 V, $f_{SCLK}$ = 20 MHz, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 2.**

| Parameter | A Version[1] | B Version[1] | Unit | Test Conditions/Comments |
|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | |
| Signal-to-Noise and Distortion (SINAD) | 68 | 68 | dB min | $f_{IN}$ = 300 kHz sine wave, $f_{SAMPLE}$ = 1 MSPS |
| Total Harmonic Distortion (THD) | −75 | −75 | dB max | $f_{IN}$ = 300 kHz sine wave, $f_{SAMPLE}$ = 1 MSPS |
| Peak Harmonic or Spurious Noise (SFDR) | −76 | −76 | dB max | $f_{IN}$ = 300 kHz sine wave, $f_{SAMPLE}$ = 1 MSPS |
| Intermodulation Distortion (IMD) | | | | |
| Second-Order Terms | −78 | −78 | dB typ | |
| Third-Order Terms | −78 | −78 | dB typ | |
| Aperture Delay | 10 | 10 | ns typ | |
| Aperture Jitter | 50 | 50 | ps typ | |
| Full Power Bandwidth | 8.3 | 8.3 | MHz typ | @ 3 dB |
| Full Power Bandwidth | 1.3 | 1.3 | MHz typ | @ 0.1 dB |
| DC ACCURACY | | | | |
| Resolution | 12 | 12 | Bits | |
| Integral Nonlinearity | ±1.5 | ±1 | LSB max | @ 5 V (typ @ 3 V) |
| | ±0.5 | ±0.5 | LSB typ | @ 25°C |
| Differential Nonlinearity | +1.5/−0.9 | +1.5/−0.9 | LSB max | @ 5 V guaranteed no missed codes to 12 bits (typ @ 3 V) |
| | ±0.6 | ±0.6 | LSB typ | @ 25°C |
| Offset Error | ±8 | ±8 | LSB max | Typically ±2.5 LSB |
| Gain Error | ±7 | ±7 | LSB max | Typically ±2.5 LSB |
| ANALOG INPUT | | | | |
| Input Voltage Ranges | 0 to 2.5 | 0 to 2.5 | V | |
| DC Leakage Current | ±1 | ±1 | µA max | |
| Input Capacitance | 20 | 20 | pF typ | |
| REFERENCE OUTPUT | | | | |
| REF OUT Output Voltage | 2.4625/2.5375 | 2.4625/2.5375 | V min/max | |
| REF OUT Impedance | 10 | 10 | Ω typ | |
| REF OUT Temperature Coefficient | 50 | 50 | ppm/°C typ | |
| LOGIC INPUTS | | | | |
| Input High Voltage, $V_{INH}$ | $V_{DRIVE}$ − 1 | $V_{DRIVE}$ − 1 | V min | |
| Input Low Voltage, $V_{INL}$ | 0.4 | 0.4 | V max | |
| Input Current, $I_{IN}$ | ±1 | ±1 | µA max | Typically 10 nA, $V_{IN}$ = 0 V or $V_{DRIVE}$ |
| Input Capacitance, $C_{IN}$[2] | 10 | 10 | pF max | |
| LOGIC OUTPUTS | | | | |
| Output High Voltage, $V_{OH}$ | $V_{DRIVE}$ − 0.2 | | V min | $I_{SOURCE}$ = 200 µA; $V_{DD}$ = 2.7 V to 5.25 V |
| Output Low Voltage, $V_{OL}$ | 0.4 | 0.4 | V max | $I_{SINK}$ = 200 µA |
| Floating-State Leakage Current | ±10 | ±10 | µA max | |
| Floating-State Output Capacitance | 10 | 10 | pF max | |
| Output Coding | Straight (Natural) Binary | | | |
| CONVERSION RATE | | | | |
| Conversion Time | 800 | 800 | ns max | 16 SCLK cycles with SCLK at 20 MHz |
| Track-and-Hold Acquisition Time | 300 | 300 | ns max | Sine wave input |
| | 325 | 325 | ns max | Full-scale step input |
| Throughput Rate | 1 | 1 | MSPS max | See the Serial Interface section |

| Parameter | A Version[1] | B Version[1] | Unit | Test Conditions/Comments |
|---|---|---|---|---|
| POWER REQUIREMENTS | | | | |
| $V_{DD}$ | 2.7/5.25 | 2.7/5.25 | V min/max | |
| $V_{DRIVE}$ | 2.7/5.25 | 2.7/5.25 | V min/max | |
| $I_{DD}$ | | | | Digital inputs = 0 V or $V_{DRIVE}$ |
| Normal Mode (Static) | 1 | 1 | mA typ | $V_{DD}$ = 2.7 V to 5.25 V, SCLK on or off |
| Normal Mode (Operational) | 2.6 | 2.6 | mA max | $V_{DD}$ = 4.75 V to 5.25 V, $f_{SAMPLE}$ = 1 MSPS |
| | 2 | 2 | mA max | $V_{DD}$ = 2.7 V to 3.6 V, $f_{SAMPLE}$ = 1 MSPS |
| Partial Power-Down Mode | 650 | 650 | µA typ | $f_{SAMPLE}$ = 100 kSPS |
| Partial Power-Down Mode | 230 | 230 | µA max | Static |
| Full Power-Down Mode | 1 | 1 | µA max | Static, SCLK on or off |
| Power Dissipation[3] | | | | |
| Normal Mode (Operational) | 13 | 13 | mW max | $V_{DD}$ = 5 V, $f_{SAMPLE}$ = 1 MSPS |
| | 6 | 6 | mW max | $V_{DD}$ = 3 V, $f_{SAMPLE}$ = 1 MSPS |
| Partial Power-Down (Static) | 1.15 | 1.15 | mW max | $V_{DD}$ = 5 V |
| | 690 | 690 | µW max | $V_{DD}$ = 3 V |
| Full Power-Down | 5 | 5 | µW max | $V_{DD}$ = 5 V |
| | 3 | 3 | µW max | $V_{DD}$ = 3 V |

[1] Temperature ranges for A, B versions: −40°C to +85°C.
[2] Guaranteed by initial characterization.
[3] See the Power vs. Throughput Rate section.

# TIMING SPECIFICATIONS[1]

$V_{DD}$ = 2.7 V to 5.25 V, $V_{DRIVE}$ = 2.7 V to 5.25 V, REF IN = 2.5 V (AD7475), $T_A = T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 3.**

| Parameter | Limit at $T_{MIN}$, $T_{MAX}$ | Unit | Description |
|---|---|---|---|
| $f_{SCLK}$[2] | 10 | kHz min | |
| | 20 | MHz max | |
| $t_{CONVERT}$ | 16 × $t_{SCLK}$ | | $t_{SCLK} = 1/f_{SCLK}$ |
| | 800 | ns max | $f_{SCLK}$ = 20 MHz |
| $t_{QUIET}$ | 100 | ns min | Minimum quiet time required between conversions |
| $t_2$ | 10 | ns min | $\overline{CS}$ to SCLK setup time |
| $t_3$[3] | 22 | ns max | Delay from $\overline{CS}$ until SDATA three-state disabled |
| $t_4$ | 40 | ns max | Data access time after SCLK falling edge |
| $t_5$ | 0.4 $t_{SCLK}$ | ns min | SCLK low pulse width |
| $t_6$ | 0.4 $t_{SCLK}$ | ns min | SCLK high pulse width |
| $t_7$ | 10 | ns min | SCLK to data valid hold time |
| $t_8$[4] | 10 | ns min | SCLK falling edge to SDATA high impedance |
| | 45 | ns max | SCLK falling edge to SDATA high impedance |
| $t_9$ | 20 | ns max | $\overline{CS}$ rising edge to SDATA high impedance |
| $t_{POWER-UP}$ | 20 | µs max | Power-up time from full power-down (AD7475) |
| | 650 | µs max | Power-up time from full power-down (AD7495) |

[1] Guaranteed by initial characterization. All input signals are specified with tr = tf = 5 ns (10% to 90% of $V_{DRIVE}$) and timed from a voltage level of 1.6 V.
[2] Mark/space ratio for the SCLK input is 40/60 to 60/40.
[3] Measured with the load circuit of Figure 4 and defined as the time required for the output to cross 0.8 V or 2.0 V.
[4] $t_8$ and $t_9$ are derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 4. The measured number is extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the times, $t_8$ and $t_9$, quoted in the timing characteristics are the true bus relinquish times of the part and are independent of the bus loading.

## TIMING EXAMPLE 1

With $f_{SCLK}$ = 20 MHz and a throughput of 1 MSPS, the cycle time is $t_2 + 12.5(1/f_{SCLK}) + t_{ACQ}$ = 1 µs. With $t_2$ = 10 ns min, $t_{ACQ}$ is 365 ns. The 365 ns satisfies the requirement of 300 ns for $t_{ACQ}$. In Figure 3, $t_{ACQ}$ comprises $2.5(1/f_{SCLK}) + t_8 + t_{QUIET}$, where $t_8$ = 45 ns. This allows a value of 195 ns for $t_{QUIET}$, satisfying the minimum requirement of 100 ns.

## TIMING EXAMPLE 2

With $f_{SCLK}$ = 5 MHz and a throughput of 315 KSPS, the cycle time is $t_2 + 12.5(1/f_{SCLK}) + t_{ACQ}$ = 3.174 µs. With $t_2$ = 10 ns min, $t_{ACQ}$ is 664 ns. The 664 ns satisfies the requirement of 300 ns for $t_{ACQ}$. In Figure 3, $t_{ACQ}$ comprises $2.5(1/f_{SCLK}) + t8 + t_{QUIET}$, where t8 = 45 ns. This allows a value of 119 ns for $t_{QUIET}$, satisfying the minimum requirement of 100 ns. As in this example and with other slower clock values, the signal may already be acquired before the conversion is complete, but it is still necessary to leave 100 ns minimum $t_{QUIET}$ between conversions. In Example 2, the signal should be fully acquired at approximately Point C in Figure 3.

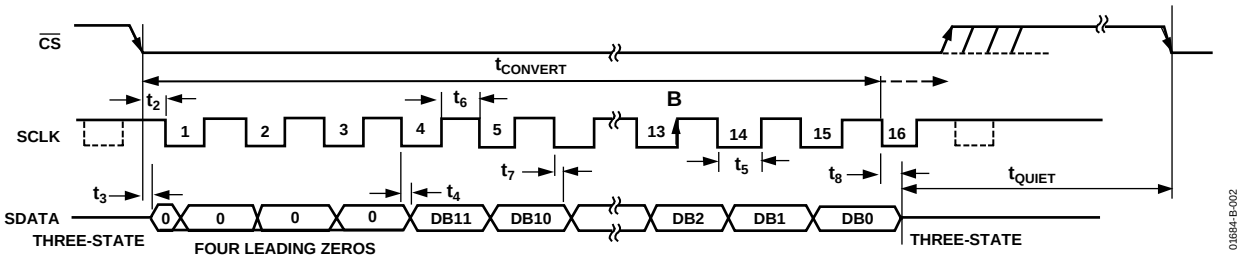



*Figure 2. Serial Interface Timing Diagram*

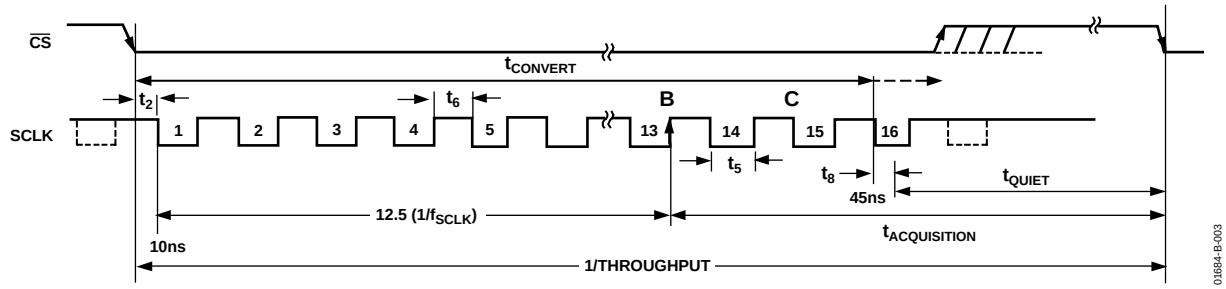



*Figure 3. Serial Interface Timing Example*

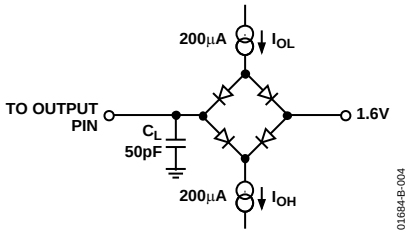



*Figure 4. Load Circuit for Digital Output Timing Specifications*

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C unless otherwise noted.

**Table 4.**

| Parameters | Ratings |
|---|---|
| $V_{DD}$ to GND | −0.3 V to +7 V |
| $V_{DRIVE}$ to GND | −0.3 V to +7 V |
| Analog Input Voltage to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| Digital Input Voltage to GND | −0.3 V to +7 V |
| $V_{DRIVE}$ to $V_{DD}$ | −0.3 V to $V_{DD}$ + 0.3 V |
| Digital Output Voltage to GND | −0.3 V to $V_{DRIVE}$ + 0.3 V |
| REF IN to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| Input Current to Any Pin Except Supplies[1] | ±10 mA |
| Operating Temperature Range | |
| Commercial (A, B Version) | −40°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | 150°C |
| SOIC, MSOP Package, Power Dissipation | 450 mW |
| $\theta_{JA}$ Thermal Impedance | 157°C/W (SOIC) |
| | 205.9°C/W (MSOP) |
| $\theta_{JC}$ Thermal Impedance | 56°C/W (SOIC) |
| | 43.74°C/W (MSOP) |
| Lead Temperature, Soldering | |
| Vapor Phase (60 sec) | 215°C |
| Infrared (15 sec) | 220°C |
| ESD | 4 kV |

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

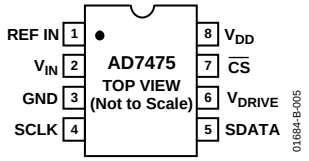



*Figure 5. AD7475 SOIC/MSOP Pin Configuration*

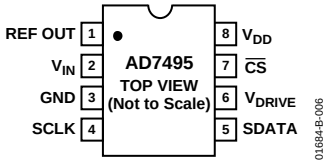



*Figure 6. AD7495 SOIC/MSOP Pin Configuration*

**Table 5. Pin Descriptions**

| Pin No. | Mnemonic | Function |
|---|---|---|
| 1 (AD7475) | REF IN | Reference Input for the AD7475. An external reference must be applied to this input. The voltage range for the external reference is 2.5 V ± 1% for specified performance. A cap of a least 0.1 µF should be placed on the REF IN pin. |
| 1 (AD7495) | REF OUT | Reference Output for the AD7495. A minimum 100 nF capacitance is required from this pin to GND. The internal reference can be taken from this pin, but buffering is required before it is applied elsewhere in a system. |
| 2 | $V_{IN}$ | Analog Input. Single-ended analog input channel. The input range is 0 to REF IN. |
| 3 | GND | Analog Ground. Ground reference point for all circuitry on the AD7475/AD7495. All analog input signals and any external reference signal should be referred to this GND voltage. |
| 4 | SCLK | Serial Clock, Logic Input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the AD7475/AD7495 conversion process. |
| 5 | SDATA | Data Out, Logic Output. The conversion result from the AD7475/AD7495 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream consists of four leading zeros followed by the 12 bits of conversion data, which is provided MSB first. |
| 6 | $V_{DRIVE}$ | Logic Power Supply Input. The voltage supplied at this pin determines the operating voltage for the serial interface of the AD7475/AD7495. |
| 7 | $\overline{CS}$ | Chip Select, Active Low Logic Input. This input provides the dual function of initiating conversions on the AD7475/AD7495 and also frames the serial data transfer. |
| 8 | $V_{DD}$ | Power Supply Input. The $V_{DD}$ range for the AD7475/AD7495 is from 2.7 V to 5.25 V. |

# TERMINOLOGY

**Integral Nonlinearity**
The maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point ½ LSB below the first code transition, and full scale, a point ½ LSB above the last code transition.

**Differential Nonlinearity**
The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

**Offset Error**
The deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, that is, AGND + 0.5 LSB.

**Gain Error**
This is the deviation of the last code transition (111. . . 110) to (111. . . 111) from the ideal (that is, $V_{REF}$ − 1.5 LSB) after the offset error has been adjusted out.

**Track-and-Hold Acquisition Time**
The track-and-hold amplifier returns into track mode on the 13th SCLK rising edge (see the Serial Interface section). The track-and-hold acquisition time is the minimum time required for the track-and-hold amplifier to remain in track mode for its output to reach and settle to within 0.5 LSB of the applied input signal, given a step change to the input signal.

**Signal-to-Noise and Distortion Ratio (SINAD)**
The measured ratio of signal-to-noise and distortion at the output of the analog-to-digital converter (ADC). The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical SINAD ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\ to\ (Noise + Distortion) = (6.02\ N + 1.76)\ \text{dB}$$

For a 12-bit converter, the SINAD is 74 dB.

**Total Harmonic Distortion (THD)**
The ratio of the rms sum of harmonics to the fundamental. For the AD7475/AD7495, THD is defined as

$$THD\,(\text{dB}) = 20 \log \frac{\sqrt{V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + V_5^{\,2} + V_6^{\,2}}}{V_1}$$

where $V_1$ is the rms amplitude of the fundamental and $V_2$, $V_3$, $V_4$, $V_5$, and $V_6$ are the rms amplitudes of the second through the sixth harmonics.

**Peak Harmonic or Spurious Noise**
The ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

**Intermodulation Distortion**
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n is equal to zero. For example, the second-order terms include (fa + fb) and (fa − fb), while the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7475/AD7495 are tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. Like THD, intermodulation distortion is calculated as the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals, expressed in dBs.

# TYPICAL PERFORMANCE CURVES

Figure 7 shows a typical FFT plot for the AD7475 at a 1 MHz sample rate and a 100 kHz input frequency.

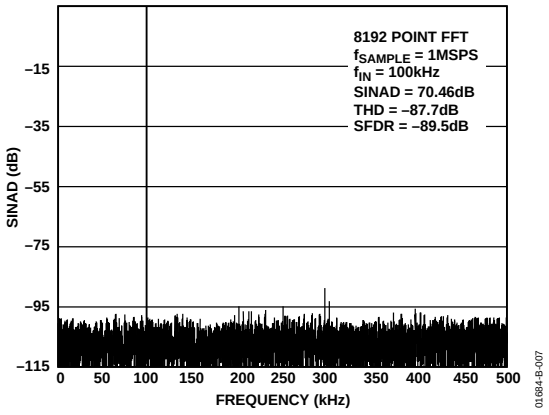



*Figure 7. AD7475 Dynamic Performance*

Figure 8 shows a typical FFT plot for the AD7495 at a 1 MHz sample rate and a 100 kHz input frequency.

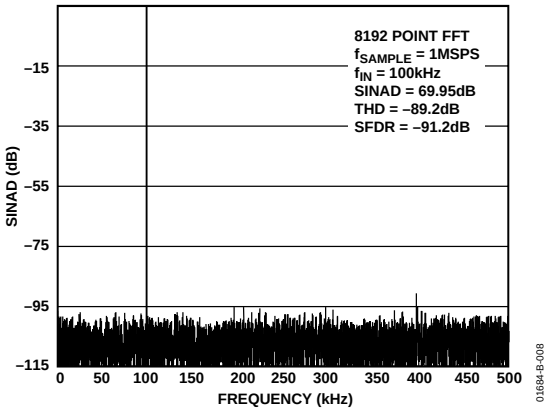



*Figure 8. AD7495 Dynamic Performance*

Figure 9 shows the SINAD performance vs. input frequency for various supply voltages while sampling at 1 MSPS with an SCLK of 20 MHz.

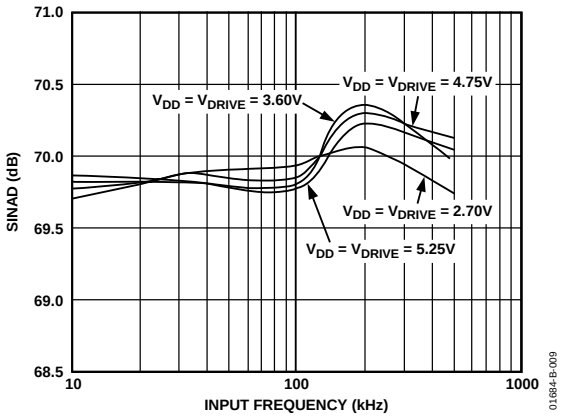



*Figure 9. AD7495 SINAD vs. Input Frequency at 1 MSPS*

# THEORY OF OPERATION

The AD7475/AD7495 are fast, micropower, 12-bit, single-supply analog-to-digital converters (ADCs). The parts can be operated from a 2.7 V to 5.25 V supply. When operated from either a 5 V supply or a 3 V supply, the AD7475/AD7495 are capable of throughput rates of 1 MSPS when provided with a 20 MHz clock.

The AD7475/AD7495 ADCs have an on-chip track-and-hold with a serial interface housed in either an 8-lead SOIC_N or MINI_SO package, features that offer the user considerable space-saving advantages over alternative solutions. The AD7495 also has an on-chip 2.5 V reference. The serial clock input accesses data from the part but also provides the clock source for the successive-approximation ADC. The analog input range is 0 V to REF IN for the AD7475 and 0 V to REF OUT for the AD7495.

The AD7475/AD7495 also feature power-down options to allow power saving between conversions. The power-down feature is implemented across the standard serial interface, as described in the Operating Modes section.

## CONVERTER OPERATION

The AD7475/AD7495 are 12-bit, successive approximation analog-to-digital converters based around a capacitive DAC. The AD7475/AD7495 can convert analog input signals in the range 0 V to 2.5 V. Figure 10 and Figure 12 show simplified schematics of the ADC. The ADC comprises control logic, SAR, and a capacitive DAC, which are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. Figure 10 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in Position A. The comparator is held in a balanced condition and the sampling capacitor acquires the signal on $V_{IN}$.

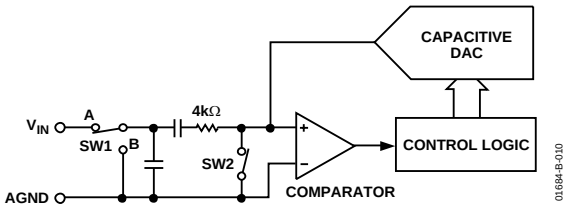



*Figure 10. ADC Acquisition Phase*

When the ADC starts a conversion (see Figure 11), SW2 opens and SW1 moves to Position B causing the comparator to become unbalanced. The control logic and the capacitive DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code.

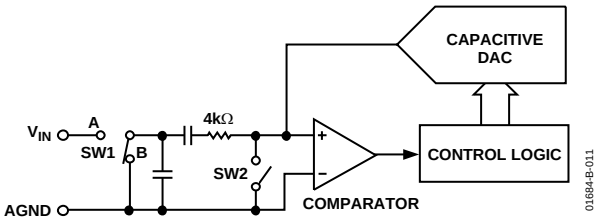



*Figure 11. ADC Conversion Phase*

## ADC TRANSFER FUNCTION

The output coding of the AD7475/AD7495 is straight binary. The designed code transitions occur midway between successive LSB integer values (that is, ½ LSB, $^3/_2$ LSBs, etc.). The LSB size is = $V_{REF}$/4096. The ideal transfer characteristic for the AD7475/AD7495 is shown in Figure 12.

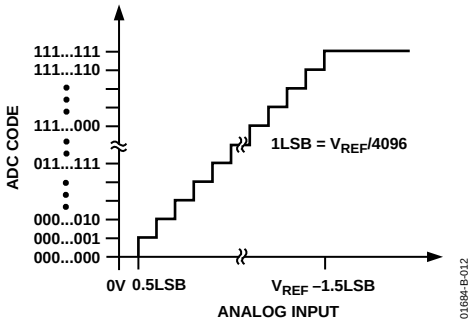



*Figure 12. AD7475/AD7495 Transfer Characteristic*

## TYPICAL CONNECTION DIAGRAM

Figure 13 and Figure 15 show typical connection diagrams for the AD7475 and AD7495, respectively. In both setups the GND pin is connected to the analog ground plane of the system. In Figure 13, REF IN is connected to a decoupled 2.5 V supply from a reference source, the AD780, to provide an analog input range of 0 V to 2.5 V. Although the AD7475 is connected to a $V_{DD}$ of 5 V, the serial interface is connected to a 3 V microprocessor. The $V_{DRIVE}$ pin of the AD7475 is connected to the same 3 V supply of the microprocessor to allow a 3 V logic interface (see the Digital Inputs section.) In Figure 15, the REF OUT pin of the AD7495 is connected to a buffer and then applied to a level-shifting circuit used on the analog input to allow a bipolar signal to be applied to the AD7495. A minimum 100 nF capacitance is required on the REF OUT pin to GND. The conversion result from both ADCs is output in a 16-bit word with four leading zeros followed by the MSB of the 12-bit result. For applications where power consumption is of concern, the power-down modes should be used between conversions or bursts of several conversions to improve power performance. See the Operating Modes section for more information.

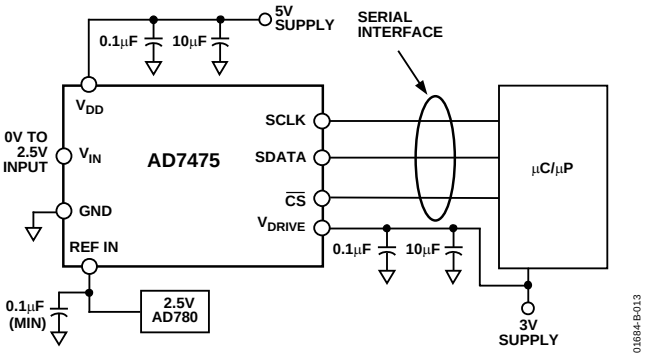



*Figure 13. AD7475 Typical Connection Diagram*

### *Analog Input*

Figure 14 shows an equivalent circuit of the analog input structure of the AD7475/AD7495. The D1 and D2 diodes provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 200 mV. This causes these diodes to become forward-biased and start conducting current into the substrate. The maximum current these diodes can conduct without causing irreversible damage to the part is 20 mA. The capacitor C1 in Figure 14 is typically about 4 pF and can primarily be attributed to pin capacitance. The resistor R1 is a lumped component made up of the on resistance of a switch. This resistor is typically about 100 Ω. The capacitor C2 is the ADC sampling capacitor and has a capacitance of 16 pF, typically. For ac applications, it is recommended to remove high frequency components from the analog input signal using an RC low-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application.

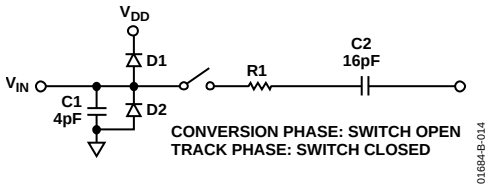



*Figure 14. Equivalent Analog Input Circuit*

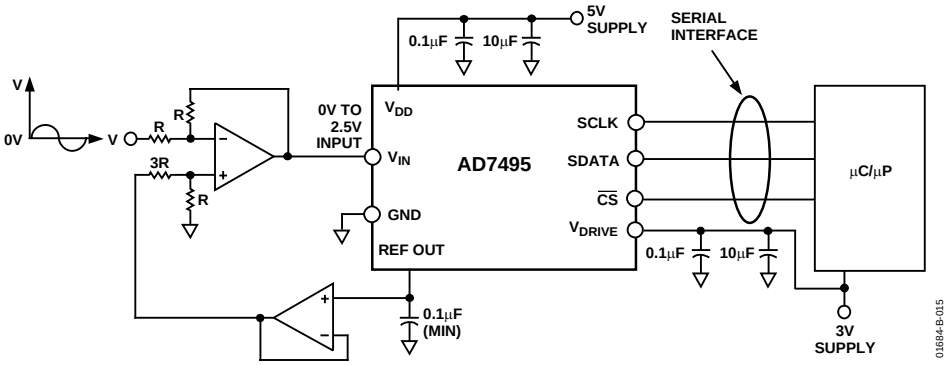



*Figure 15. AD7495 Typical Connection Diagram*

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance depends on the amount of total harmonic distortion (THD) that can be tolerated. The THD increases as the source impedance increases and performance degrades. Figure 16 shows a graph of the total harmonic distortion vs. source impedance for various analog input frequencies.

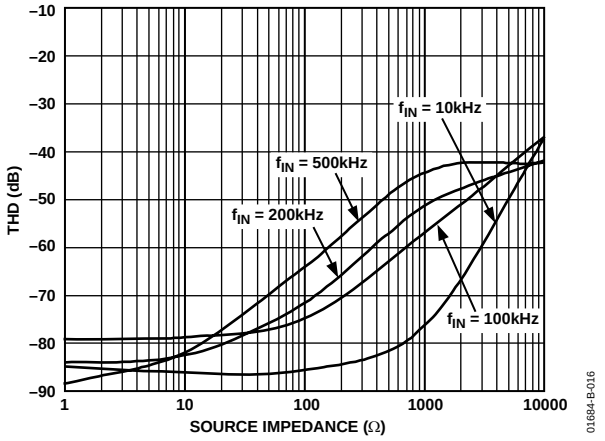



*Figure 16. THD vs. Source Impedance for Various Analog Input Frequencies*

Figure 17 shows a graph of total harmonic distortion vs. analog input frequency for various supply voltages while sampling at 1 MSPS with an SCLK of 20 MHz.

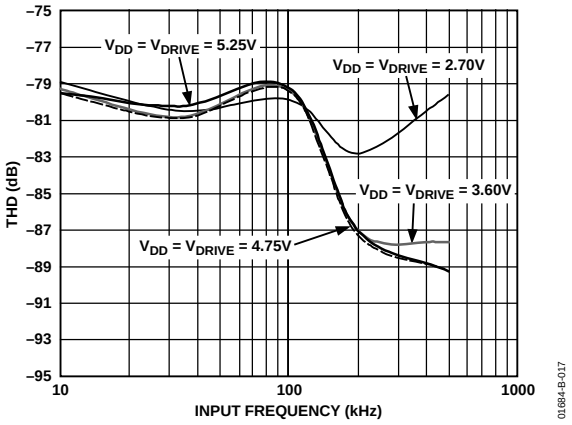



*Figure 17. THD vs. Analog Input Frequency for Various Supply Voltages*

### Digital Inputs

The digital inputs applied to the AD7475/AD7495 are not limited by the maximum ratings, which limit the analog inputs. Instead, the digital inputs applied can go to 7 V and are not restricted by the $V_{DD}$ + 0.3 V limit as on the analog inputs. Another advantage of SCLK and $\overline{CS}$ not being restricted by the $V_{DD}$ + 0.3 V limit is that power supply sequencing issues are avoided. If $\overline{CS}$ or SCLK are applied before $V_{DD}$, there is no risk of latch-up as there would be on the analog inputs if a signal greater than 0.3 V were applied prior to $V_{DD}$.

### $V_{DRIVE}$

The AD7475/AD7495 also has the $V_{DRIVE}$ feature. This feature controls the voltage at which the serial interface operates. $V_{DRIVE}$ allows the ADC to easily interface to both 3 V and 5 V processors.

For example, if the AD7475/AD7495 were operated with a $V_{DD}$ of 5 V, the $V_{DRIVE}$ pin could be powered from a 3 V supply. The AD7475/AD7495 have better dynamic performance with a $V_{DD}$ of 5 V, while still being able to interface to 3 V digital parts. Care should be taken to ensure $V_{DRIVE}$ does not exceed $V_{DD}$ by more than 0.3 V. (See the Absolute Maximum Ratings section.)

### Reference Section

An external reference source should be used to supply the 2.5 V reference to the AD7475. Errors in the reference source result in gain errors in the AD7475 transfer function and add the specified full-scale errors on the part. The AD7475 voltage reference input, REF IN, has a dynamic input impedance. A small dynamic current is required to charge the capacitors in the capacitive DAC during the bit trials. This current is typically 50 μA for a 2.5 V reference. A capacitor of at least 0.1 μF should be placed on the REF IN pin. Suitable reference sources for the AD7475 are the AD780, AD680, AD1582, ADR391, ADR381, ADR431, and ADR03.

The AD7495 contains an on-chip 2.5 V reference. As shown in Figure 18, the voltage that appears at the REF OUT pin is internally buffered before being applied to the ADC; the output impedance of this buffer is typically 10 Ω. The reference is capable of sourcing up to 2 mA. The REF OUT pin should be decoupled to AGND using a 100 nF or greater capacitor.

If the 2.5 V internal reference is used to drive another device that is capable of glitching the reference at critical times, then the reference has to be buffered before driving the device. To ensure optimum performance of the AD7495, it is recommended that the internal reference not be over driven. If an ADC with external reference capability is required, the AD7475 should be used.

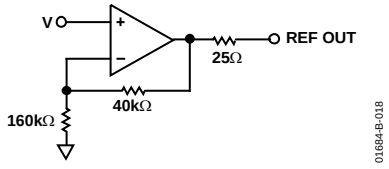



*Figure 18. AD7495 Reference Circuit*

# OPERATING MODES

The AD7475/AD7495 operating mode is selected by controlling the logic state of the $\overline{CS}$ signal during a conversion. There are three possible modes of operation: normal mode, partial power-down mode, and full power-down mode. The point at which $\overline{CS}$ is pulled high after the conversion has been initiated determines which power-down mode, if any, the device enters. Similarly, if already in a power-down mode, $\overline{CS}$ can control whether the device returns to normal operation or remains in power-down. These modes of operation are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for differing application requirements.

## NORMAL MODE

This mode is intended for fastest throughput rate performance, because the user does not have to worry about any power-up times with the AD7475/AD7495 remaining fully powered all the time. Figure 19 shows the general diagram of the AD7475/AD7495 operating in this mode.

The conversion is initiated on the falling edge of $\overline{CS}$, as described in the Serial Interface section. To ensure the part remains fully powered-up at all times, $\overline{CS}$ must remain low until at least 10 SCLK falling edges have elapsed after the falling edge of $\overline{CS}$. If $\overline{CS}$ is brought high any time after the 10th SCLK falling edge, but before the 16th SCLK falling edge, the part remains powered up but the conversion is terminated and SDATA goes back into three-state. Sixteen serial clock cycles are required to complete the conversion and access the conversion result. $\overline{CS}$ may idle high until the next conversion or may idle low until sometime prior to the next conversion (effectively idling $\overline{CS}$ low).

Once a data transfer is complete (SDATA has returned to three-state), another conversion can be initiated after the quiet time, $t_{QUIET}$, has elapsed, by bringing $\overline{CS}$ low again.

## PARTIAL POWER-DOWN MODE

This mode is intended for use in applications where slower throughput rates are required; either the ADC is powered down between each conversion, or a series of conversions may be performed at a high throughput rate and then the ADC is powered down for a relatively long duration between these bursts of several conversions. When the AD7475 is in partial power-down, all analog circuitry is powered down except for the bias current generator; and, in the case of the AD7495, all analog circuitry is powered down except for the on-chip reference and reference buffer.

To enter partial power-down, the conversion process must be interrupted by bringing $\overline{CS}$ high anywhere after the second falling edge of SCLK and before the tenth falling edge of SCLK, as shown in Figure 20. Once $\overline{CS}$ has been brought high in this window of SCLKs, the part enters partial power-down, the conversion that was initiated by the falling edge of $\overline{CS}$ is terminated, and SDATA goes back into three-state. If $\overline{CS}$ is brought high before the second SCLK falling edge, the part remains in normal mode and does not power down. This avoids accidental power-down due to glitches on the $\overline{CS}$ line.

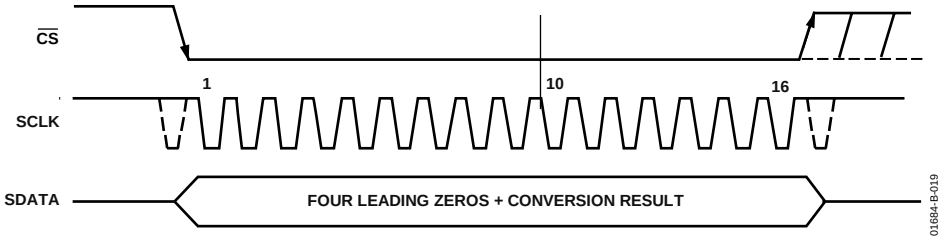



*Figure 19. Normal Mode*

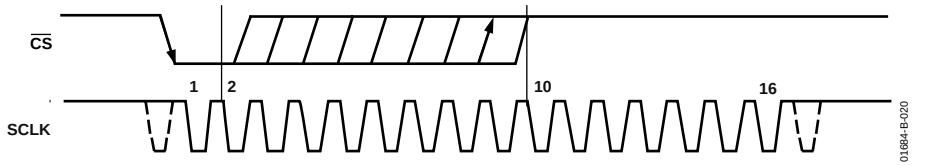



*Figure 20. Entering Partial Power-Down Mode*

To exit this operating mode and power up the AD7475/AD7495 again, a dummy conversion is performed. On the falling edge of $\overline{CS}$, the device begins to power up and continues to power up as long as $\overline{CS}$ is held low until after the falling edge of the tenth SCLK. The device is fully powered up once 16 SCLKs have elapsed, and valid data results from the next conversion, as shown in Figure 21. If $\overline{CS}$ is brought high before the second falling edge of SCLK, the AD7475/AD7495 go back into partial power-down again. This avoids accidental power-up due to glitches on the $\overline{CS}$ line; although the device may begin to power up on the falling edge of $\overline{CS}$, it powers down again on the rising edge of $\overline{CS}$. If in partial power-down and $\overline{CS}$ is brought high between the second and tenth falling edges of SCLK, the device enters full power-down mode.

### *Power-Up Time*

The power-up time of the AD7475/AD7495 from partial power-down is typically 1 µs, which means that with any frequency of SCLK up to 20 MHz, one dummy cycle is sufficient to allow the device to power up from partial power-down. Once the dummy cycle is complete, the ADC is fully powered up and the input signal is acquired properly. The quiet time, $t_{QUIET}$, must still be allowed from the point where the bus goes back into three-state after the dummy conversion to the next falling edge of $\overline{CS}$. When running at a 1 MSPS throughput rate, the AD7475/AD7495 power up and acquire a signal within ±0.5 LSB in one dummy cycle, 1 µs.

When powering up from the power-down mode with a dummy cycle, as in Figure 21, the track-and-hold that was in hold mode while the part was powered down returns to track mode after the first SCLK edge the part receives after the falling edge of $\overline{CS}$. This is shown as Point A in Figure 21. Although at any SCLK frequency one dummy cycle is sufficient to power up the device and acquire $V_{IN}$, it does not necessarily mean that a full dummy cycle of 16 SCLKs must always elapse to power up the device and fully acquire $V_{IN}$; 1 µs is sufficient to power up the device and acquire the input signal. If, for example, a 5 MHz SCLK frequency were applied to the ADC, the cycle time would be 3.2 µs. In one dummy cycle, 3.2 µs, the part would be powered up and $V_{IN}$ fully acquired. However, after 1 µs with a 5 MHz SCLK, only 5 SCLK cycles would have elapsed. At this stage, the ADC would be fully powered up and the signal acquired. In this case, the $\overline{CS}$ can be brought high after the tenth SCLK falling edge and brought low again after a time, $t_{QUIET}$, to initiate the conversion.

## FULL POWER-DOWN MODE

Full power-down mode is intended for use in applications where slower throughput rates are required than that in the partial power-down mode, because power up from a full power-down would not be complete in just one dummy conversion. This mode is more suited to applications where a series of conversions performed at a relatively high throughput rate are followed by a long period of inactivity and therefore power down. When the AD7475/AD7495 are in full power-down, all analog circuitry is powered down.

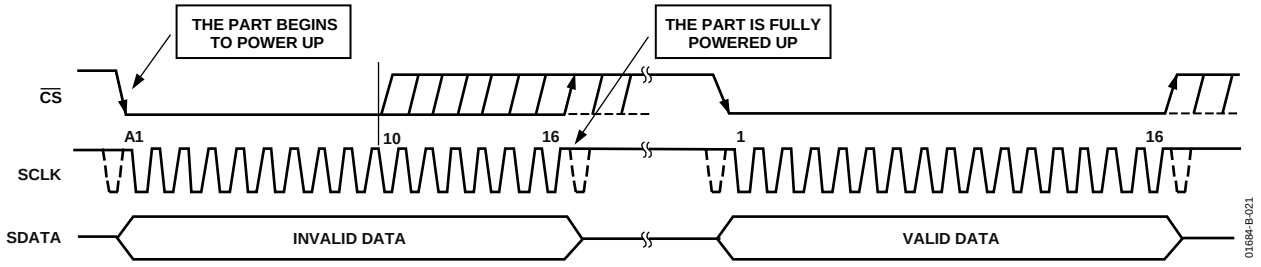



*Figure 21. Exiting Partial Power-Down Mode*

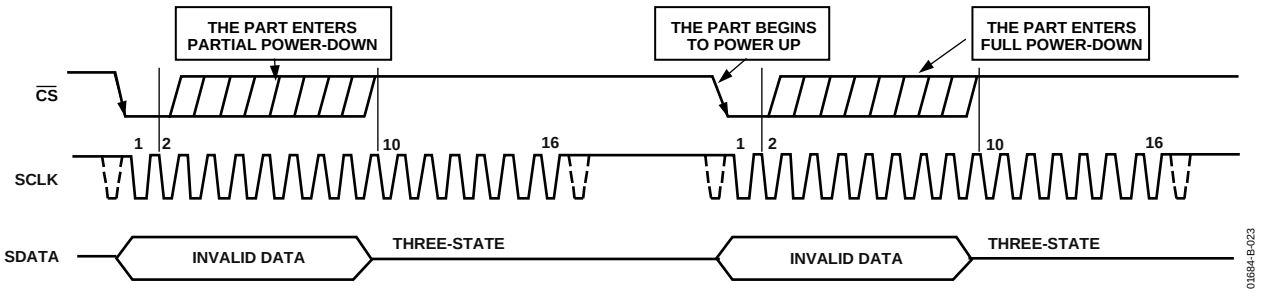



*Figure 22. Entering Full Power-Down Mode*

Full power-down is entered in a way similar to partial power-down, except the timing sequence shown in Figure 20 must be executed twice. The conversion process must be interrupted in a similar fashion by bringing $\overline{CS}$ high anywhere after the second falling edge of SCLK and before the tenth falling edge of SCLK. The device enters partial power-down at this point. To reach full power-down, the next conversion cycle must be interrupted in the same way, as shown in Figure 22. Once $\overline{CS}$ has been brought high in this window of SCLKs, then the part powers down completely.

Note that it is not necessary to complete the 16 SCLKs once $\overline{CS}$ has been brought high to enter a power-down mode.

To exit full power-down, and power up the AD7475/AD7495 again, a dummy conversion is performed as when powering up from partial power-down. On the falling edge of $\overline{CS}$, the device begins to power up and continues to power up as long as $\overline{CS}$ is held low until after the falling edge of the tenth SCLK. The power-up time is longer than one dummy conversion cycle however, and this time, $t_{POWER-UP}$, must elapse before a conversion can be initiated, as shown in Figure 23. See the Timing Specifications section for more information.

When power supplies are first applied to the AD7475/AD7495, the ADC may power up in either of the power-down modes or normal mode. Because of this, it is best to allow a dummy cycle to elapse to ensure the part is fully powered up before attempting a valid conversion. Likewise, if the intent is to keep the part in partial power-down mode immediately after the supplies are applied, then two dummy cycles must be initiated. The first dummy cycle must hold $\overline{CS}$ low until after the tenth SCLK falling edge, as shown in Figure 19. In the second cycle, $\overline{CS}$ must be brought high before the tenth SCLK edge, but after the second SCLK falling edge, as shown in Figure 20. Alternatively, if the intent is to place the part in full power-down mode when the supplies have been applied, then three dummy cycles must be initiated. The first dummy cycle must hold $\overline{CS}$ low until after the tenth SCLK edge, as shown in Figure 19; the second and third dummy cycle place the part in full power-down, as shown in Figure 22. (See the Operating Modes section.) Once supplies are applied to the AD7475, enough time must be allowed for the external reference to power up and charge the reference capacitor to its final value. For the AD7495, enough time should be allowed for the internal reference buffer to charge the reference capacitor. Then, to place the AD7475/ AD7495 in normal mode, a dummy cycle, 1 µs, should be initiated. If the first valid conversion is then performed directly after the dummy conversion, ensure that adequate acquisition time has been allowed. As mentioned earlier, when powering up from the power-down mode, the part returns to track upon the first SCLK edge applied after the falling edge of $\overline{CS}$. However, when the ADC powers up initially after supplies are applied, the track-and-hold is already in track. This means (assuming one has the facility to monitor the ADC supply current) if the ADC powers up in the desired mode of operation, and a dummy cycle is not required to change mode, then neither is a dummy cycle required to place the track-and-hold into track. If no current monitoring facility is available, the relevant dummy cycle(s) should be performed to ensure the part is in the required mode.

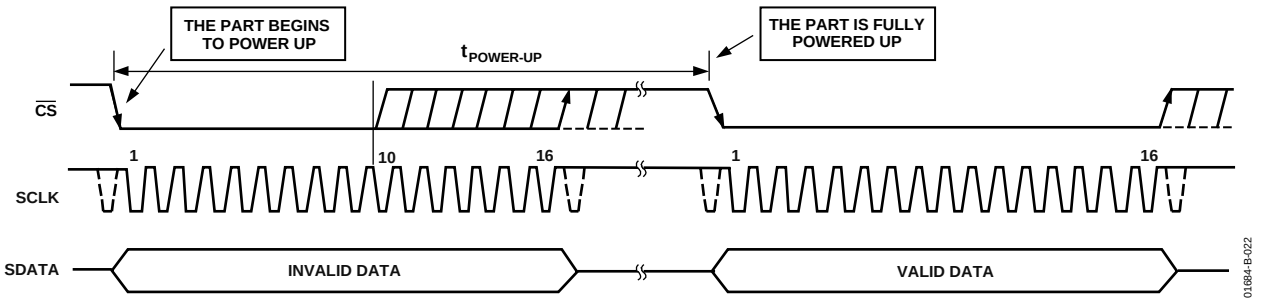



*Figure 23. Exiting Full Power-Down Mode*

## POWER VS. THROUGHPUT RATE

By using the partial power-down mode on the AD7475/AD7495 when not converting, the average power consumption of the ADC decreases at lower throughput rates. Figure 24 shows how, as the throughput rate is reduced, the part remains in its partial power-down state longer and the average power consumption over time drops accordingly.

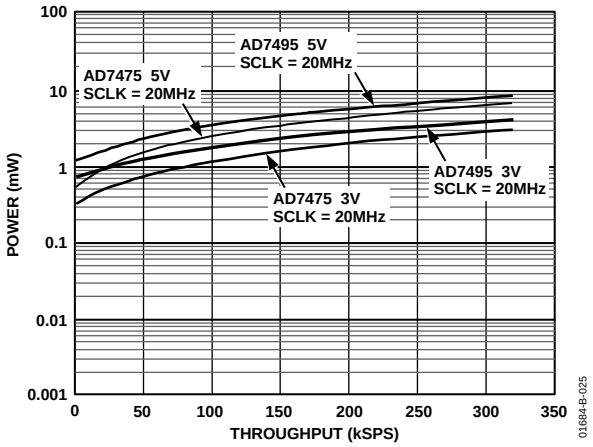



*Figure 24. Power vs. Throughput for Partial Power Down*

For example, if the AD7495 is operated in a continuous sampling mode with a throughput rate of 100 kSPS and an SCLK of 20 MHz ($V_{DD}$ = 5 V), and the device is placed in partial power-down mode between conversions, then the power consumption is calculated as follows. The maximum power dissipation during normal operation is 13 mW ($V_{DD}$ = 5 V). If the power-up time from partial power-down is one dummy cycle, that is, 1 µs, and the remaining conversion time is another cycle, that is, 1 µs, then the AD7495 can be said to dissipate 13 mW for 2 µs during each conversion cycle. For the remainder of the conversion cycle, 8 µs, the part remains in partial power-down mode. The AD7495 dissipates 1.15 mW for the remaining 8 µs of the conversion cycle. If the throughput rate is 100 kSPS, and the cycle time is 10 µs, the average power dissipated during each cycle is (2/10) × (13 mW) + (8/10) × (1.15 mW) = 3.52 mW. If $V_{DD}$ = 3 V, SCLK = 20 MHz and the device is again in partial power-down mode between conversions, the power dissipated during normal operation is 6 mW.

The AD7495 dissipates 6 mW for 2 µs during each conversion cycle and 0.69 mW for the remaining 8 µs where the part is in partial power-down. With a throughput rate of 100 kSPS, the average power dissipated during each conversion cycle is (2/10) × (6 mW) + (8/10) × (0.69 mW) = 1.752 mW. Figure 24 shows the power vs. throughput rate when using partial power-down mode between conversions with both 5 V and 3 V supplies for both the AD7475 and AD7495. For the AD7475, partial power-down current is lower than that of the AD7495.

Full power-down mode is intended for use in applications with slower throughput rates than required for partial power-down mode. It is necessary to leave 650 µs for the AD7495 to be fully powered up from full power-down before initiating a conversion. Current consumptions between conversions is typically less than 1 µA.

Figure 25 shows a typical graph of current vs. throughput for the AD7495 while operating in different modes. At slower throughput rates, for example, 10 SPS to 1 kSPS, the AD7495 was operated in full power-down mode. As the throughput rate increased, up to 100 kSPS, the AD7495 was operated in partial power-down mode, with the part being powered down between conversions. With throughput rates from 100 kSPS to 1 MSPS, the part operated in normal mode, remaining fully powered up at all times.

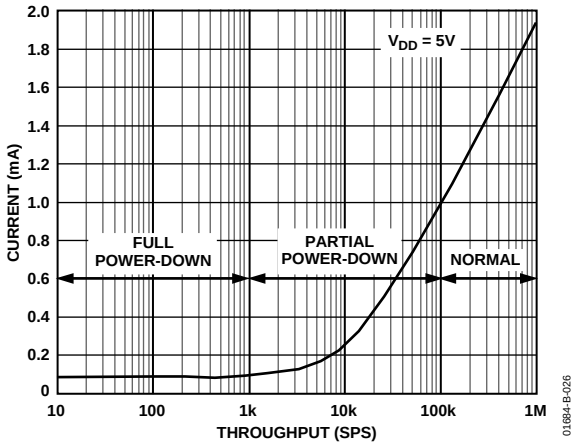



*Figure 25. Typical AD7495 Current vs. Throughput*

# SERIAL INTERFACE

Figure 26 shows the detailed timing diagram for serial interfacing to the AD7475/AD7495. The serial clock provides the conversion clock and also controls the transfer of information from the AD7475/AD7495 during conversion.

$\overline{CS}$ initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode and takes the bus out of three-state. The analog input is sampled at this point.

The conversion is also initiated at this point and requires 16 SCLK cycles to complete. Once 13 SCLK falling edges have elapsed, the track-and-hold goes back into track on the next SCLK rising edge, as shown in Figure 26 at Point B. On the 16th SCLK falling edge, the SDATA line goes back into three-state. If the rising edge of $\overline{CS}$ occurs before 16 SCLKs have elapsed, the conversion is terminated and the SDATA line goes back into three-state, as shown in Figure 27; otherwise SDATA returns to three-state on the 16th SCLK falling edge, as shown in Figure 26.

Sixteen serial clock cycles are required to perform the conversion process and to access data from the AD7475/AD7495. $\overline{CS}$ going low provides the first leading zero to be read in by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges beginning with the second leading zero; thus the first falling clock edge on the serial clock has the second leading zero provided. The final bit in the data transfer is valid on the 16th falling edge, having been clocked out on the previous (15th) falling edge.

In applications with a slower SCLK, it may be possible to read in data on each SCLK rising edge, although the first leading zero still has to be read on the first SCLK falling edge after the $\overline{CS}$ falling edge. Therefore, the first rising edge of SCLK after the $\overline{CS}$ falling edge provides the second leading zero and the 15th rising SCLK edge has DB0 provided. This method may not work with most microprocessors/DSPs, but could possibly be used with FPGAs and ASICs.

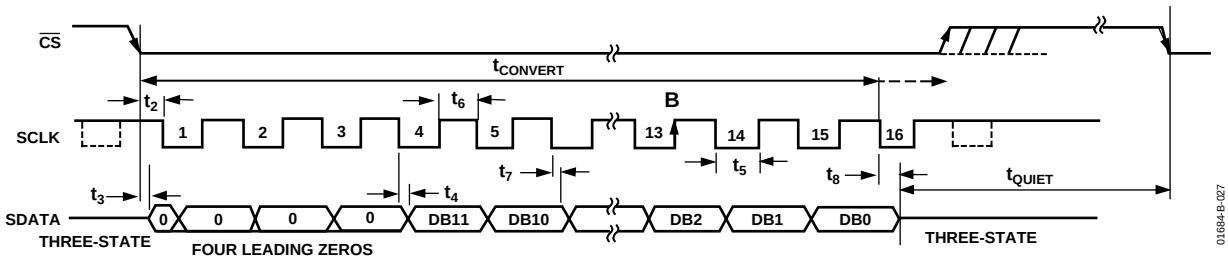



*Figure 26. Serial Interface Timing Diagram*

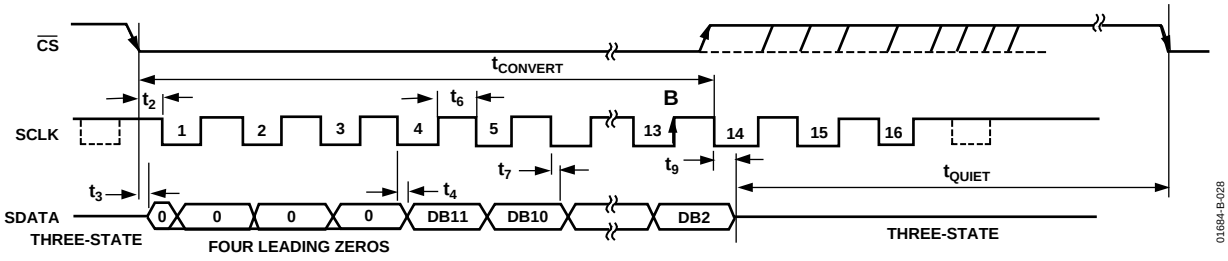



*Figure 27. Serial Interface Timing Diagram — Conversion Termination*

# MICROPROCESSOR INTERFACING

The serial interface on the AD7475/AD7495 allows the parts to be directly connected to a range of many different microprocessors. This section explains how to interface the AD7475/AD7495 with some of the more common microcontroller and DSP serial interface protocols.

## AD7475/AD7495 TO TMS320C5x/C54x

The serial interface on the TMS320C5x/C54x uses a continuous serial clock and frame synchronization signals to synchronize the data transfer operations with peripheral devices like the AD7475/AD7495. The $\overline{CS}$ input allows easy interfacing between the TMS320C5x/C54x and the AD7475/AD7495 without any glue logic required. The serial port of the TMS320C5x/C54x is set up to operate in burst mode with internal CLKX (Tx serial clock) and FSX (Tx frame sync). The serial port control register (SPC) must have the following setup: FO = 0, FSM = 1, MCM = 1, and TXM = 1. The format bit, FO, may be set to 1 to set the word length to 8 bits, in order to implement the power-down modes on the AD7475/AD7495.

The connection diagram is shown in Figure 28. Note that for signal processing applications, it is imperative that the frame synchronization signal from the TMS320C5x/C54x provide equidistant sampling. The $V_{DRIVE}$ pin of the AD7475/AD7495 takes the same supply voltage as that of the TMS320C5x/C54x. This allows the ADC to operate at a higher voltage than the serial interface, that is, TMS320C5x/C54x, if necessary.

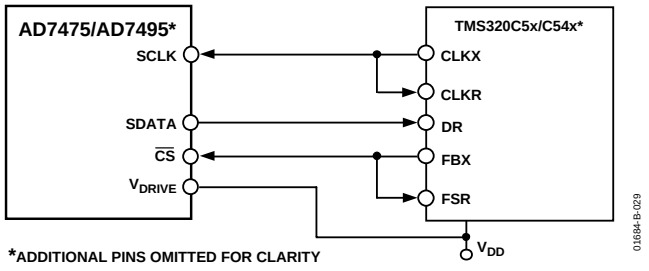



*Figure 28. Interfacing to the TMS320C5x/54x*

## AD7475/AD7495 TO ADSP-21xx

The ADSP-21xx family of DSPs is interfaced directly to the AD7475/AD7495 without any glue logic required. The $V_{DRIVE}$ pin of the AD7475/AD7495 takes the same supply voltage as that of the ADSP-21xx. This allows the ADC to operate at a higher voltage than the serial interface, that is, ADSP-21xx, if necessary.

The SPORT control register should be set up as shown in Table 6.

**Table 6.**

| SPORT Control Register Bits | Function |
|---|---|
| TFSW = RFSW = 1 | Alternate framing |
| INVRFS = INVTFS = 1 | Active low frame signal |
| DTYPE = 00 | Right-justify data |
| SLEN = 1111 | 16-bit data words |
| ISCLK = 1 | Internal serial clock |
| TFSR = RFSR = 1 | Frame every word |
| IRFS = 0 | |
| ITFS = 1 | |

To implement the power-down modes, SLEN should be set to 1001 to issue an 8-bit SCLK burst.

The connection diagram is shown in Figure 29. The ADSP-21xx has the TFS and RFS of the SPORT tied together, with TFS set as an output and RFS set as an input. The DSP operates in alternate framing mode and the SPORT control register is set up as described. The frame synchronization signal generated on the TFS is tied to $\overline{CS}$ and, as with all signal processing applications, equidistant sampling is necessary. However, in this example, the timer interrupt is used to control the sampling rate of the ADC and, under certain conditions, equidistant sampling may not be achieved.

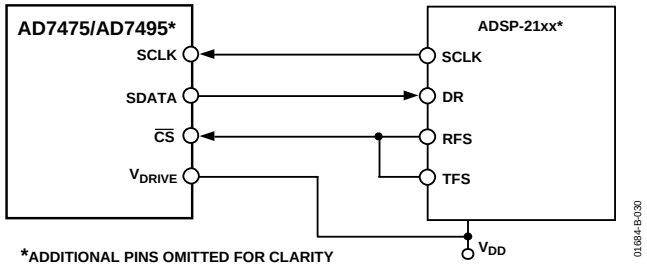



*Figure 29. Interfacing to the ADSP-21xx*

The timer registers are loaded with a value that provides an interrupt at the required sample interval. When an interrupt is received, a value is transmitted with TFS/DT (ADC control word). The TFS is used to control the RFS, and therefore, the reading of data. The frequency of the serial clock is set in the SCLKDIV register. When the instruction to transmit with TFS is given, (that is, AX0 = TX0), the state of the SCLK is checked. The DSP waits until the SCLK has gone high, low, and high before transmission starts. If the timer and SCLK values are chosen such that the instruction to transmit occurs on or near the rising edge of SCLK, the data can be transmitted or it can wait until the next clock edge.

For example, the ADSP-2111 has a master clock frequency of 16 MHz. If the SCLKDIV register is loaded with the value 3, an SCLK of 2 MHz is obtained, and eight master clock periods elapse for every one SCLK period. If the timer registers are loaded with the value 803, 100.5 SCLKs occur between interrupts and subsequently between transmit instructions. This situation results in nonequidistant sampling because the transmit instruction is occurring on a SCLK edge. If the number of SCLKs between interrupts is a whole integer figure of N, equidistant sampling is implemented by the DSP.

## AD7475/AD7495 TO DSP56xxx

The connection diagram in Figure 30 shows how the AD7475/AD7495 can be connected to the synchronous serial interface (SSI) of the DSP56xxx family of devices from Motorola. The SSI is operated in synchronous mode (SYN bit in CRB = 1) with internally generated 1-bit clock period frame sync for both Tx and Rx (Bits FSL1 = 1 and FSL0 = 0 in CRB). Set the word length to 16 by setting Bits WL1 = 1 and WL0 = 0 in CRA. To implement the power-down modes on the AD7475/AD7495, the word length can be changed to 8 bits by setting Bit WL1 = 0 and Bit WL0 = 0 in CRA. For signal processing applications, it is imperative that the frame synchronization signal from the DSP56xxx provide equidistant sampling. The $V_{DRIVE}$ pin of the AD7475/AD7495 takes the same supply voltage as that of the DSP56xxx. This allows the ADC to operate at a voltage higher than the serial interface, that is, DSP56xxx, if necessary.

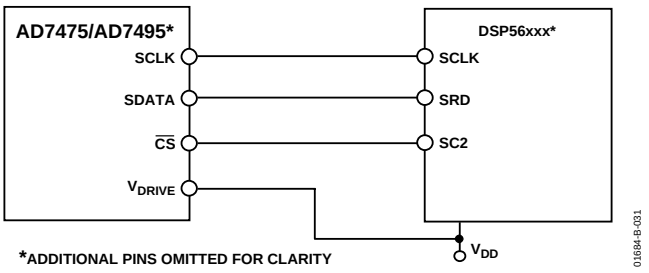



*Figure 30. Interfacing to the DSP56xxx*

## AD7475/AD7495 TO MC68HC16

The serial peripheral interface (SPI) on the MC68HC16 is configured for master mode (MSTR) = 1, clock polarity bit (CPOL) = 1, and the clock phase bit (CPHA) = 0. The SPI is configured by writing to the SPI control register (SPCR), as described in the *68HC16 User Manual.* The serial transfer takes place as a 16-bit operation when the size bit in the SPCR register is set to size = 1. To implement the power-down modes with an 8-bit transfer, set size = 0. (A connection diagram is shown in Figure 31.) The $V_{DRIVE}$ pin of the AD7475/AD7495 takes the same supply voltage as that of the MC68HC16. This allows the ADC to operate at a higher voltage than the serial interface, that is, the MC68HC16, if necessary.

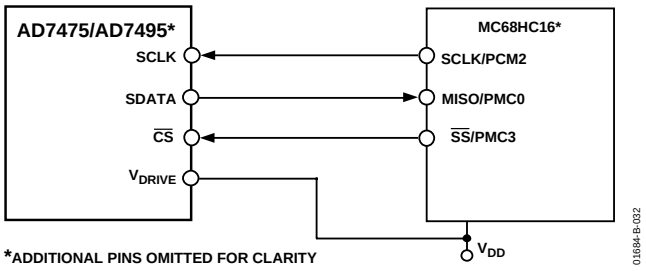
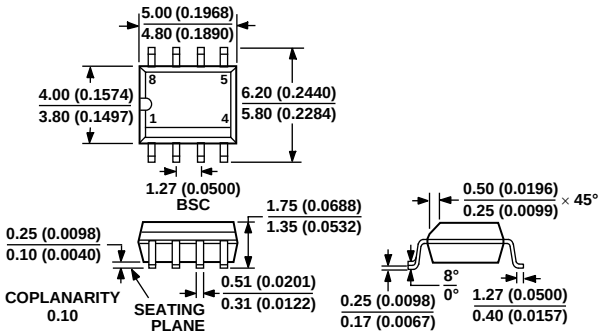



*Figure 31. Interfacing to the MC68HC16*

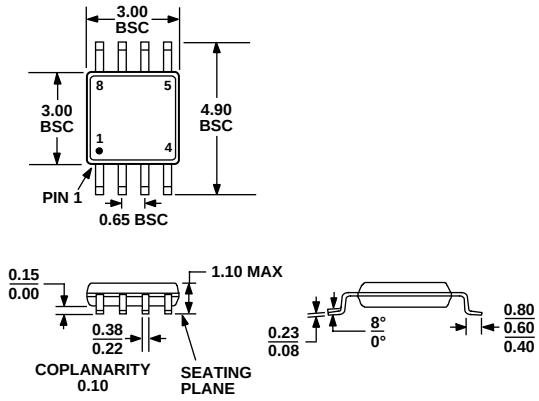
# OUTLINE DIMENSIONS




**COMPLIANT TO JEDEC STANDARDS MS-012-AA**

**CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN**

*Figure 32. 8-Lead Standard Small Outline Package [SOIC_N]*
*Narrow Body*
*(R-8)*
*Dimensions shown in millimeters and (inches)*




**COMPLIANT TO JEDEC STANDARDS MO-187-AA**

*Figure 33. 8-Lead Mini Small Outline Package [MINI_SO]*
*(RM-8)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Range | Linearity Error (LSB)[1] | Package Option[2] | Branding Information |
|---|---|---|---|---|
| AD7475AR | −40°C to +85°C | ±1.5 | SO-8 | |
| AD7475AR-REEL | −40°C to +85°C | ±1.5 | SO-8 | |
| AD7475AR-REEL7 | −40°C to +85°C | ±1.5 | SO-8 | |
| AD7475BR | −40°C to +85°C | ±1 | SO-8 | |
| AD7475BR-REEL | −40°C to +85°C | ±1 | SO-8 | |
| AD7475BR-REEL7 | −40°C to +85°C | ±1 | SO-8 | |
| AD7475ARM | −40°C to +85°C | ±1.5 | RM-8 | C9A |
| AD7475ARM-REEL | −40°C to +85°C | ±1.5 | RM-8 | C9A |
| AD7475ARM-REEL7 | −40°C to +85°C | ±1.5 | RM-8 | C9A |
| AD7475BRM | −40°C to +85°C | ±1 | RM-8 | C9B |
| AD7475BRM-REEL | −40°C to +85°C | ±1 | RM-8 | C9B |
| AD7475BRM-REEL7 | −40°C to +85°C | ±1 | RM-8 | C9B |
| AD7475BRMZ[3] | −40°C to +85°C | ±1 | RM-8 | C3C |
| AD7475BRMZ-REEL[3] | −40°C to +85°C | ±1 | RM-8 | C3C |
| AD7475BRMZ-REEL7[3] | −40°C to +85°C | ±1 | RM-8 | C3C |
| AD7495AR | −40°C to +85°C | ±1.5 | SO-8 | |
| AD7495AR-REEL | −40°C to +85°C | ±1.5 | SO-8 | |
| AD7495AR-REEL7 | −40°C to +85°C | ±1.5 | SO-8 | |
| AD7495BR | −40°C to +85°C | ±1 | SO-8 | |
| AD7495BR-REEL | −40°C to +85°C | ±1 | SO-8 | |
| AD7495BR-REEL7 | −40°C to +85°C | ±1 | SO-8 | |
| AD7495BRZ[3] | −40°C to +85°C | ±1 | SO-8 | |
| AD7495BRZ-REEL[3] | −40°C to +85°C | ±1 | SO-8 | |
| AD7495BRZ-REEL7[3] | −40°C to +85°C | ±1 | SO-8 | |
| AD7495ARM | −40°C to +85°C | ±1.5 | RM-8 | CCA |
| AD7495ARM-REEL | −40°C to +85°C | ±1.5 | RM-8 | CCA |
| AD7495ARM-REEL7 | −40°C to +85°C | ±1.5 | RM-8 | CCA |
| AD7495ARMZ[3] | −40°C to +85°C | ±1.5 | RM-8 | C3B |
| AD7495ARMZ-REEL[3] | −40°C to +85°C | ±1.5 | RM-8 | C3B |
| AD7495ARMZ-REEL7[3] | −40°C to +85°C | ±1.5 | RM-8 | C3B |
| AD7495BRM | −40°C to +85°C | ±1 | RM-8 | CCB |
| AD7495BRM-REEL | −40°C to +85°C | ±1 | RM-8 | CCB |
| AD7495BRM-REEL7 | −40°C to +85°C | ±1 | RM-8 | CCB |
| EVAL-AD7495CB[4] | | | | Evaluation Board |
| EVAL-AD7475CB | | | | Evaluation Board |
| EVAL-CONTROL BRD2[5] | | | | Controller Board |

[1] Linearity error here refers to integral linearity error.
[2] SO = SOIC; RM = MSOP.
[3] Z = Pb-free part.
[4] This can be used as a standalone evaluation board or in conjunction with the evaluation controller board for evaluation/demonstration purposes.
[5] The evaluation board controller is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

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