

## FEATURES

High linearity: supports modulations to 1024 QAM

Tx IF range: 200 MHz to 700 MHz

Tx RF range: 800 MHz to 4000 MHz

Tx power control: 25 dB

SPI controlled interface

32-lead, 5 mm × 5 mm LFCSP package

## APPLICATIONS

Point to point communications

Satellite communications

Wireless microwave backhaul systems

## FUNCTIONAL BLOCK DIAGRAM

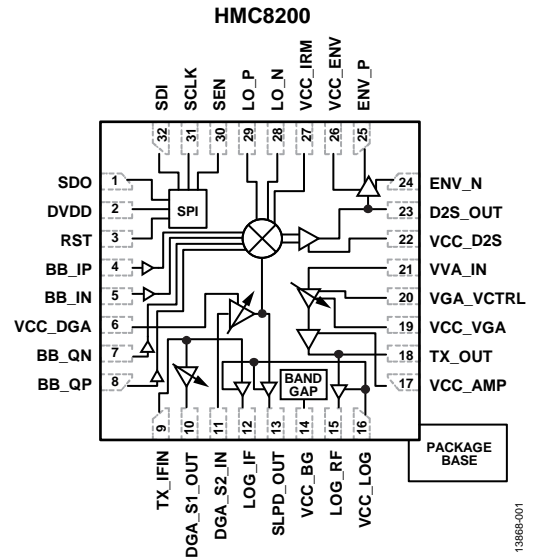


Figure 1.

## GENERAL DESCRIPTION

The [HMC8200LP5ME](#) is a highly integrated intermediate frequency (IF) transmitter chip that converts the industry standard 300 MHz to 400 MHz IF input signals to an 800 MHz to 4000 MHz single-ended radio frequency (RF) signal at its output.

The IF transmitter chip is housed in a compact 5 mm × 5 mm LFCSP package and supports complex modulations up to 1024 QAM. The [HMC8200LP5ME](#) simultaneously reduces the design complexity of traditional microwave radios while realizing significant size and cost improvements.

With IF input power ranges from  $-31$  dBm to  $+4$  dBm, the [HMC8200LP5ME](#) provides 35 dB of digital gain control in 1 dB steps and an analog voltage gain amplifier (VGA) continuously controls the transmitter output power from  $-20$  dBm to  $+5$  dBm.

The device also features three integrated power detectors. The first detector (LOG\_IF) can be utilized to monitor the IF input power. The second detector (SLPD\_OUT) is a square law power detector that monitors the power entering the mixer. The third power detector (LOG\_RF) is used to monitor the output power, which can be used for fine output power adjustment.

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## REVISION HISTORY

### 6/2017—Rev. C to Rev. D

|                                         |    |
|-----------------------------------------|----|
| Changes to Table 5.....                 | 7  |
| Changes to Read Example Section.....    | 18 |
| Changes to Figure 61 and Figure 62..... | 19 |

### 2/2017—Rev. B to Rev. C

|                                  |    |
|----------------------------------|----|
| Changes to Figure 60.....        | 18 |
| Updated Outline Dimensions ..... | 25 |

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

### 6/2016—v01.0216 to Rev. B

|                                                                |           |
|----------------------------------------------------------------|-----------|
| Updated Format.....                                            | Universal |
| Added Pin Configuration Diagram; Renumbered Sequentially ..... | 7         |
| Added Ordering Guide.....                                      | 22        |

## SPECIFICATIONS

T<sub>A</sub> = 25°C, IF frequency = 350 MHz, local oscillator (LO) input signal level = 0 dBm, RF input signal level = -31 dBm per tone, DGA setting (dec) = 35 (maximum gain), VGA setting = 3.3 V (maximum gain), sideband select = lower sideband, unless otherwise noted.

### ELECTRICAL CHARACTERISTICS: 800 MHz TO 1800 MHz RF FREQUENCY RANGE

Table 1.

| Parameter                                | Min | Typ | Max  | Unit  |
|------------------------------------------|-----|-----|------|-------|
| OPERATING CONDITIONS                     |     |     |      |       |
| LO Frequency Range                       | 300 |     | 2300 | MHz   |
| IF Frequency Range                       | 200 |     | 700  | MHz   |
| IF INPUT INTERFACE                       |     |     |      |       |
| Input Impedance                          |     | 50  |      | Ω     |
| Return Loss                              |     | 20  |      | dB    |
| LOG IF Power Detector 1 dB Dynamic Range |     | 50  |      | dB    |
| LOG IF Power Detector Range              | -30 |     | +10  | dBm   |
| LOG IF Power Detector Slope              |     | 37  |      | mV/dB |
| Square Log Power Detector Range          |     | 17  |      | dB    |
| RF OUTPUT INTERFACE                      |     |     |      |       |
| Input Impedance                          |     | 50  |      | Ω     |
| Return Loss                              | 7   | 13  |      | dB    |
| LOG Power Detector 1 dB Dynamic Range    |     | 50  |      | dB    |
| LOG Power Detector Range                 | -25 |     | +10  | dBm   |
| LOG Power Detector Slope                 |     | 37  |      | mV/dB |
| LO INPUT INTERFACE                       |     |     |      |       |
| Input Impedance                          |     | 50  |      | Ω     |
| Return Loss                              | 7   | 12  |      | dB    |
| DYNAMIC PERFORMANCE                      |     |     |      |       |
| Conversion Gain                          | 30  | 34  |      | dB    |
| Digital VGA Dynamic Range                | 30  | 35  |      | dB    |
| Analog VGA Dynamic Range                 | 23  | 27  |      | dB    |
| Sideband Rejection <sup>1</sup>          | 28  | 32  |      | dBc   |
| Noise Figure                             |     | 6   |      | dB    |
| Output Third-Order Intercept (OIP3)      | 28  | 31  |      | dBm   |
| Output 1 dB Compression Point (OP1dB)    | 11  | 15  |      | dBm   |
| LO to RF Rejection <sup>1</sup>          |     | 30  |      | dBc   |
| IF to RF Rejection                       | 56  | 63  |      | dBc   |
| POWER SUPPLY                             |     |     |      |       |
| Supply Voltage                           |     |     |      |       |
| V <sub>CCx</sub>                         |     | 3.3 |      | V     |
| VCC_VGA <sup>2</sup>                     |     | 3.3 |      | V     |
| Supply Current                           |     |     |      |       |
| V <sub>CCx</sub>                         |     | 540 |      | mA    |
| VCC_VGA <sup>2</sup>                     |     | 11  |      | μA    |

<sup>1</sup> Measurement was taken uncalibrated.

<sup>2</sup> VCC\_VGA can be adjusted from 3.3 V (maximum gain) to 0 V (minimum gain) to control the RF VGA.

**ELECTRICAL CHARACTERISTICS: 1800 MHz TO 2800 MHz RF FREQUENCY RANGE**

Table 2.

| Parameter                                | Min  | Typ | Max  | Unit     |
|------------------------------------------|------|-----|------|----------|
| <b>OPERATING CONDITIONS</b>              |      |     |      |          |
| LO Frequency Range                       | 1300 |     | 3300 | MHz      |
| IF Frequency Range                       | 200  |     | 700  | MHz      |
| <b>IF INPUT INTERFACE</b>                |      |     |      |          |
| Input Impedance                          |      | 50  |      | $\Omega$ |
| Return Loss                              |      | 20  |      | dB       |
| LOG IF Power Detector 1 dB Dynamic Range |      | 50  |      | dB       |
| LOG IF Power Detector Range              | -30  |     | +10  | dBm      |
| LOG IF Power Detector Slope              |      | 37  |      | mV/dB    |
| Square Log Power Detector Range          |      | 17  |      | dB       |
| <b>RF OUTPUT INTERFACE</b>               |      |     |      |          |
| Input Impedance                          |      | 50  |      | $\Omega$ |
| Return Loss                              | 12   | 15  |      | dB       |
| LOG Power Detector 1 dB Dynamic Range    |      | 50  |      | dB       |
| LOG Power Detector Range                 | -25  |     | +10  | dBm      |
| LOG Power Detector Slope                 |      | 37  |      | mV/dB    |
| <b>LO INPUT INTERFACE</b>                |      |     |      |          |
| Input Impedance                          |      | 50  |      | $\Omega$ |
| Return Loss                              | 8    | 15  |      | dB       |
| <b>DYNAMIC PERFORMANCE</b>               |      |     |      |          |
| Conversion Gain                          | 28   | 32  |      | dB       |
| Digital VGA Dynamic Range                | 30   | 35  |      | dB       |
| Analog VGA Dynamic Range                 | 22   | 26  |      | dB       |
| Sideband Rejection <sup>1</sup>          | 28   | 32  |      | dBc      |
| Noise Figure                             |      | 5.5 |      | dB       |
| Output Third-Order Intercept (OIP3)      | 25   | 28  |      | dBm      |
| Output 1 dB Compression Point (OP1dB)    | 10   | 15  |      | dBm      |
| LO to RF Rejection <sup>1</sup>          |      | 34  |      | dBc      |
| IF to RF Rejection                       | 55   | 58  |      | dBc      |
| <b>POWER SUPPLY</b>                      |      |     |      |          |
| Supply Voltage                           |      |     |      |          |
| V <sub>CCx</sub>                         |      | 3.3 |      | V        |
| VCC_VGA <sup>2</sup>                     |      | 3.3 |      | V        |
| Supply Current                           |      |     |      |          |
| V <sub>CCx</sub>                         |      | 540 |      | mA       |
| VCC_VGA <sup>2</sup>                     |      | 11  |      | $\mu$ A  |

<sup>1</sup> Measurement was taken uncalibrated.<sup>2</sup> VCC\_VGA can be adjusted from 3.3 V (maximum gain) to 0 V (minimum gain) to control the RF VGA.

**ELECTRICAL CHARACTERISTICS: 2800 MHz TO 4000 MHz RF FREQUENCY RANGE**

Table 3.

| Parameter                                | Min  | Typ | Max  | Unit     |
|------------------------------------------|------|-----|------|----------|
| <b>OPERATING CONDITIONS</b>              |      |     |      |          |
| LO Frequency Range                       | 2300 |     | 4500 | MHz      |
| IF Frequency Range                       | 200  |     | 700  | MHz      |
| <b>IF INPUT INTERFACE</b>                |      |     |      |          |
| Input Impedance                          |      | 50  |      | $\Omega$ |
| Return Loss                              |      | 20  |      | dB       |
| LOG IF Power Detector 1 dB Dynamic Range |      | 50  |      | dB       |
| LOG IF Power Detector Range              | -30  |     | +10  | dBm      |
| LOG IF Power Detector Slope              |      | 37  |      | mV/dB    |
| Square Log Power Detector Range          |      | 17  |      | dB       |
| <b>RF OUTPUT INTERFACE</b>               |      |     |      |          |
| Input Impedance                          |      | 50  |      | $\Omega$ |
| Return Loss                              | 15   | 23  |      | dB       |
| LOG Power Detector 1 dB Dynamic Range    |      | 50  |      | dB       |
| LOG Power Detector Range                 | -25  |     | +10  | dBm      |
| LOG Power Detector Slope                 |      | 37  |      | mV/dB    |
| <b>LO INPUT INTERFACE</b>                |      |     |      |          |
| Input Impedance                          |      | 50  |      | $\Omega$ |
| Return Loss                              | 12   | 17  |      | dB       |
| <b>DYNAMIC PERFORMANCE</b>               |      |     |      |          |
| Conversion Gain                          | 22   | 30  |      | dB       |
| Digital VGA Dynamic Range                | 30   | 35  |      | dB       |
| Analog VGA Dynamic Range                 | 20   | 25  |      | dB       |
| Sideband Rejection <sup>1</sup>          | 22   | 30  |      | dBc      |
| Noise Figure                             |      | 5.5 |      | dB       |
| Output Third-Order Intercept (OIP3)      | 20   | 26  |      | dBm      |
| Output 1 dB Compression Point (OP1dB)    | 7    | 14  |      | dBm      |
| LO to RF Rejection <sup>1</sup>          |      | 32  |      | dBc      |
| IF to RF Rejection                       | 50   | 55  |      | dBc      |
| <b>POWER SUPPLY</b>                      |      |     |      |          |
| Supply Voltage                           |      |     |      |          |
| V <sub>CCx</sub>                         |      | 3.3 |      | V        |
| VCC_VGA <sup>2</sup>                     |      | 3.3 |      | V        |
| Supply Current                           |      |     |      |          |
| V <sub>CCx</sub>                         |      | 540 |      | mA       |
| VCC_VGA <sup>2</sup>                     |      | 11  |      | $\mu$ A  |

<sup>1</sup> Measurement was taken uncalibrated.<sup>2</sup> VCC\_VGA can be adjusted from 3.3 V (maximum gain) to 0 V (minimum gain) to control the RF VGA.

## ABSOLUTE MAXIMUM RATINGS

Table 4.

| Parameter                                                        | Rating           |
|------------------------------------------------------------------|------------------|
| IF Input                                                         | 10 dBm           |
| LO Input                                                         | 10 dBm           |
| V <sub>CCx</sub>                                                 | -0.5 V to +5.5 V |
| Digital Input/Output                                             | -0.3 V to +3.6 V |
| Maximum Junction Temperature to Maintain 1 Million Hour MTTF     | 150°C            |
| Thermal Resistance (R <sub>TH</sub> ), Junction to Ground Paddle | 11°C/W           |
| Temperature                                                      |                  |
| Operating                                                        | -40°C to +85°C   |
| Storage                                                          | -65°C to +150°C  |
| Maximum Peak Reflow Temperature (MSL3)                           | 260°C            |
| ESD Sensitivity (Human Body Model)                               | 2000 V (Class 2) |

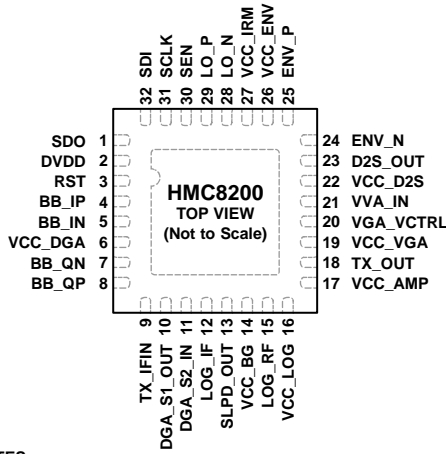
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES  
 1. CONNECT EXPOSED GROUND PADDLE TO RF/DC GROUND.

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

| Pin No. | Mnemonic     | Description                                                                                                                                                           |
|---------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1       | SDO          | SPI Serial Data Output.                                                                                                                                               |
| 2       | DVDD         | SPI Digital Supply (3.3 V <sub>DC</sub> ). Refer to Figure 64 for the required external components.                                                                   |
| 3       | RST          | SPI Reset. Connect to logic high for normal operation.                                                                                                                |
| 4, 5    | BB_IP, BB_IN | Positive and Negative Filter Baseband IF I Inputs.                                                                                                                    |
| 6       | VCC_DGA      | Power Supply for the Digital Variable Gain Amplifier (3.3 V <sub>DC</sub> ). Refer to Figure 64 for the required external components.                                 |
| 7, 8    | BB_QN, BB_QP | Negative and Positive Filter Baseband IF Q Inputs.                                                                                                                    |
| 9       | TX_IFIN      | Transmit (Tx) IF Input, Intermediate Frequency Input Port. This pin is matched to 50 Ω.                                                                               |
| 10      | DGA_S1_OUT   | Power Supply for the First Stage Digital Gain Amplifier (3.3 V <sub>DC</sub> ). This pin is matched to 50 Ω. Refer to Figure 64 for the required external components. |
| 11      | DGA_S2_IN    | Second Stage Digital Gain Amplifier Input.                                                                                                                            |
| 12      | LOG_IF       | IF Log Detector Output.                                                                                                                                               |
| 13      | SLPD_OUT     | Square Law Detector Output.                                                                                                                                           |
| 14      | VCC_BG       | Band Gap Supply. Power Supply Voltage for the Bias Controller (3.3 V <sub>DC</sub> ). Refer to Figure 64 for the required external components.                        |
| 15      | LOG_RF       | RF Log Detector Output.                                                                                                                                               |
| 16      | VCC_LOG      | RF Log Detector Supply (3.3 V <sub>DC</sub> ). Refer to Figure 64 for the required external components.                                                               |
| 17      | VCC_AMP      | Power Supply for the RF Output Amplifier (3.3 V <sub>DC</sub> ). Refer to Figure 64 for the required external components.                                             |
| 18      | TX_OUT       | Tx Chip Output.                                                                                                                                                       |
| 19      | VCC_VGA      | Power Supply for the Variable Gain Amplifier (3.3 V <sub>DC</sub> ). Refer to Figure 64 for the required external components.                                         |
| 20      | VGA_VCTRL    | VGA Control Voltage. Refer to Figure 64 for the required external components.                                                                                         |
| 21      | VVA_IN       | VVA Intermediate Frequency Input Port. This pin is matched to 50 Ω.                                                                                                   |
| 22      | VCC_D2S      | Differential to Single Amplifier Supply. Refer to Figure 64 for the required external components.                                                                     |
| 23      | D2S_OUT      | Differential to Single Amplifier Intermediate Frequency Output Port. This pin is matched to 50 Ω.                                                                     |
| 24, 25  | ENV_N, ENV_P | Envelope Detector Outputs.                                                                                                                                            |
| 26      | VCC_ENV      | Envelope Detector Supply (3.3 V <sub>DC</sub> ). Refer to Figure 64 for the required external components.                                                             |
| 27      | VCC_IRM      | Power Supply for the Mixer Output (3.3 V <sub>DC</sub> ). Refer to Figure 64 for the required external components.                                                    |
| 28, 29  | LO_N, LO_P   | Local Oscillator Inputs. These pins are ac-coupled and matched to 50 Ω.                                                                                               |
| 30      | SEN          | SPI Serial Enable.                                                                                                                                                    |
| 31      | SCLK         | SPI Clock Digital Input.                                                                                                                                              |
| 32      | SDI          | SPI Serial Data Input.                                                                                                                                                |
|         | EPAD         | Exposed Pad. Connect exposed ground paddle to RF/dc ground.                                                                                                           |

TYPICAL PERFORMANCE CHARACTERISTICS

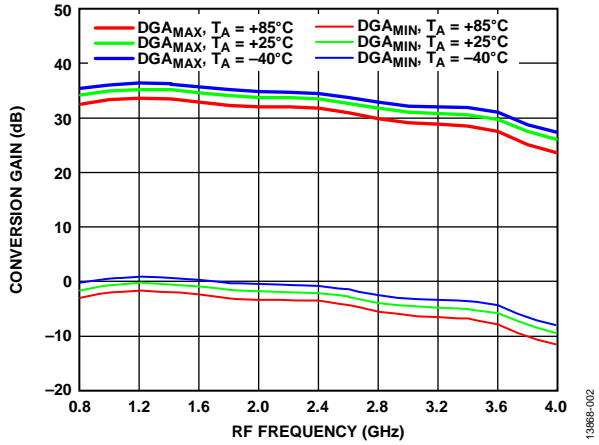


Figure 3. Conversion Gain vs. RF Frequency over Temperature, Lower Sideband

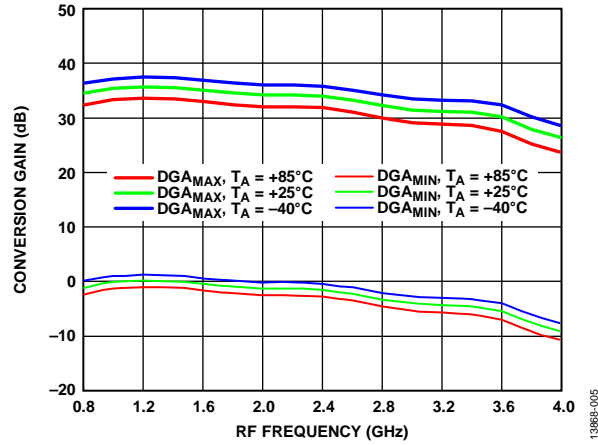


Figure 6. Conversion Gain vs. RF Frequency over Temperature, Upper Sideband

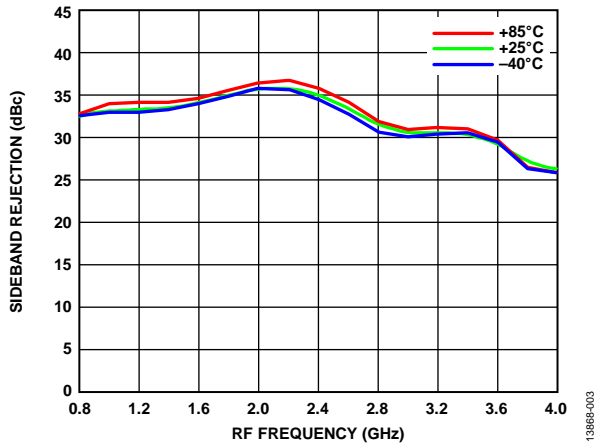


Figure 4. Sideband Rejection vs. RF Frequency over Temperature, Lower Sideband

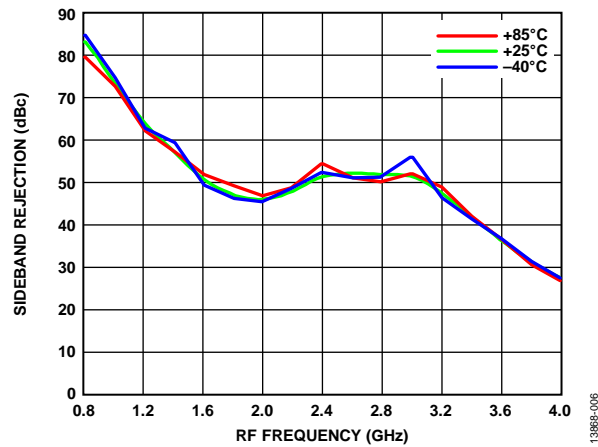


Figure 7. Sideband Rejection vs. RF Frequency over Temperature, Upper Sideband

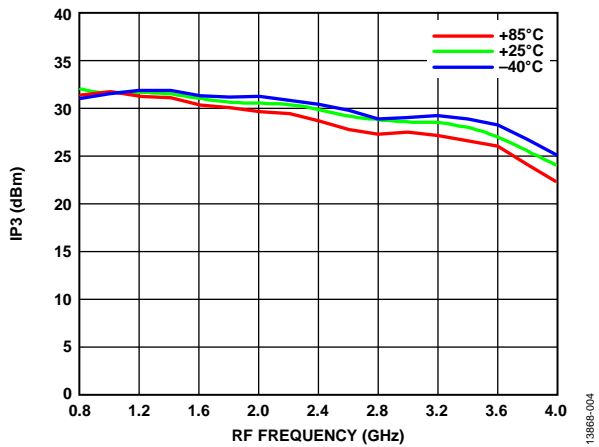


Figure 5. Output IP3 vs. RF Frequency over Temperature, Lower Sideband

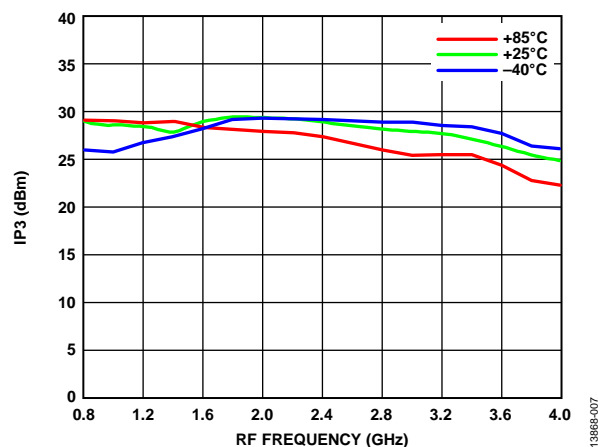


Figure 8. Output IP3 vs. RF Frequency over Temperature, Upper Sideband



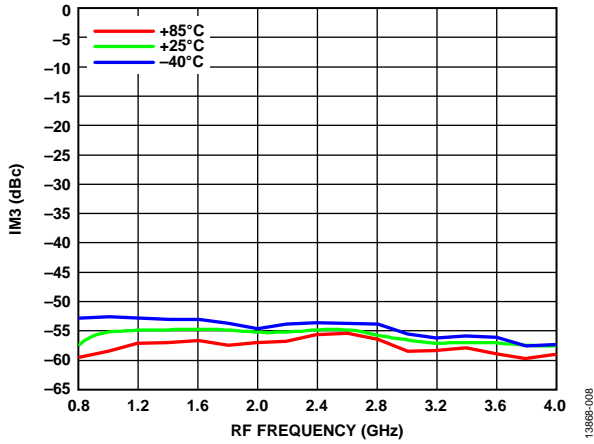


Figure 9. IM3 vs. RF Frequency over Temperature, Lower Sideband

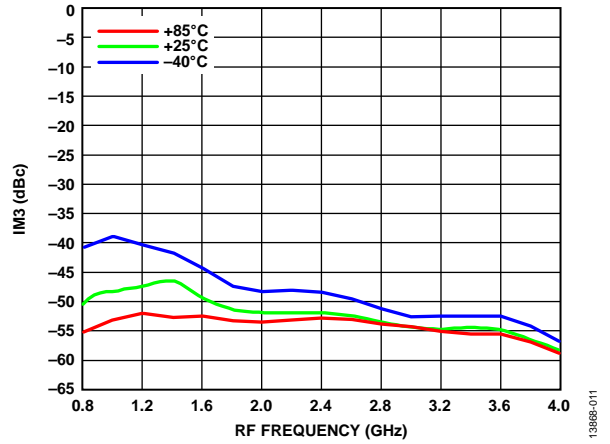


Figure 12. IM3 vs. RF Frequency over Temperature, Upper Sideband

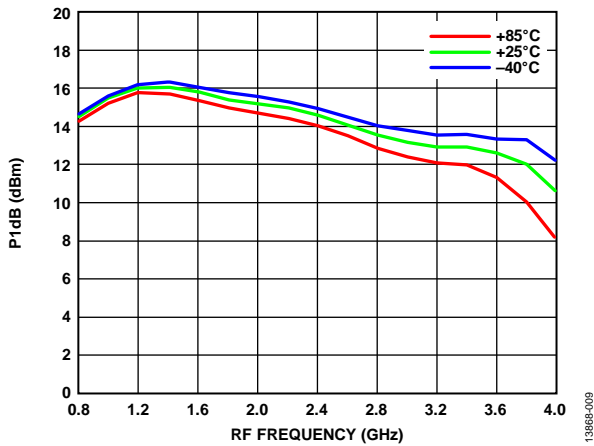


Figure 10. Output P1dB vs. RF Frequency over Temperature, Lower Sideband

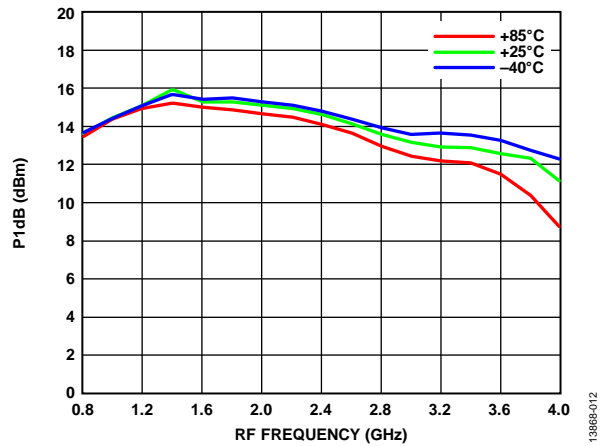


Figure 13. Output P1dB vs. RF Frequency over Temperature, Upper Sideband

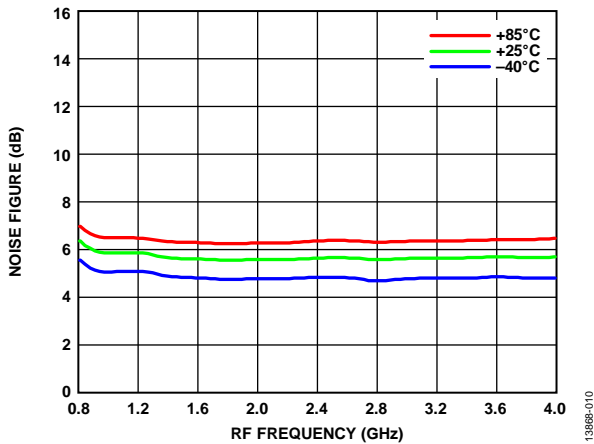


Figure 11. Noise Figure vs. RF Frequency over Temperature, Lower Sideband

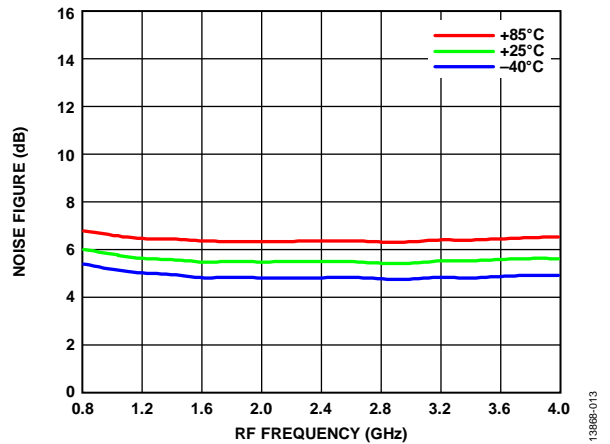


Figure 14. Noise Figure vs. RF Frequency over Temperature, Upper Sideband

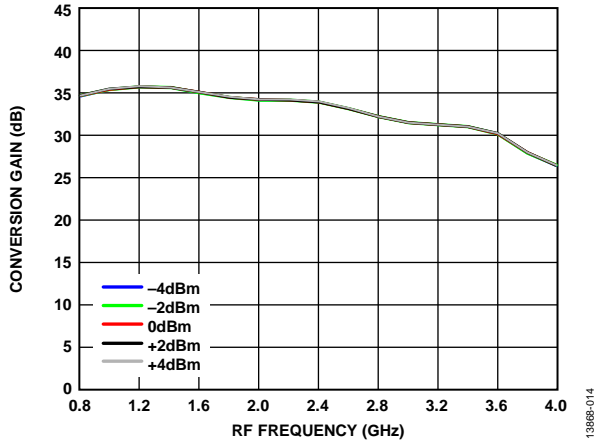


Figure 15. Conversion Gain vs. RF Frequency at Various LO Powers

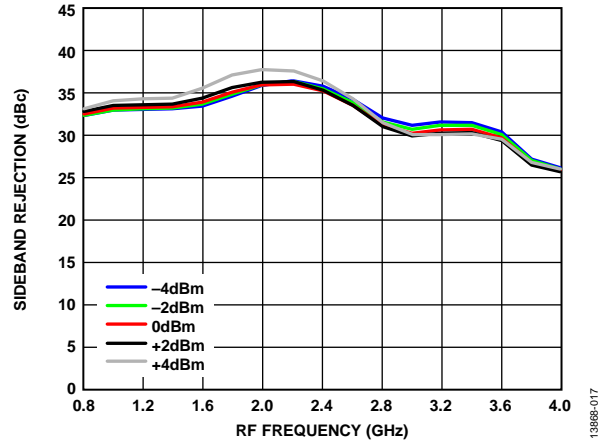


Figure 18. Sideband Rejection vs. RF Frequency at Various LO Powers

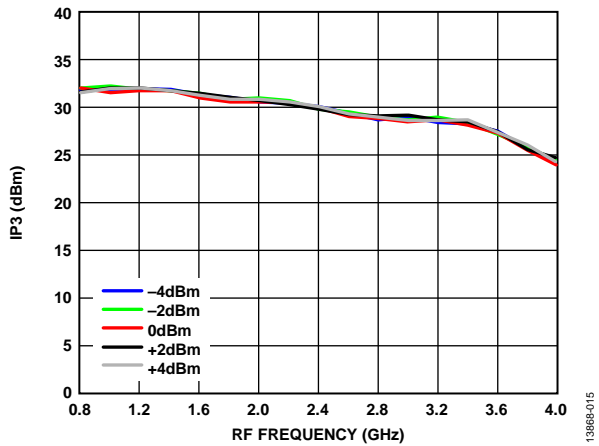


Figure 16. Output IP3 vs. RF Frequency at Various LO Powers

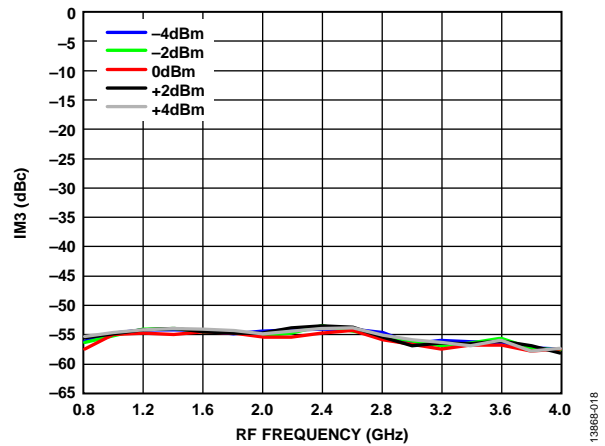


Figure 19. IM3 vs. RF Frequency at Various LO Powers

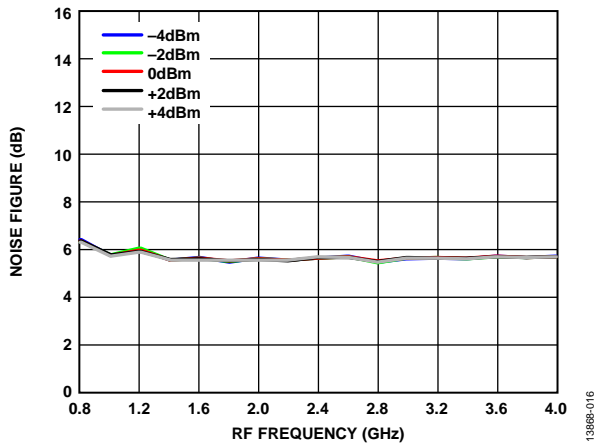


Figure 17. Noise Figure vs. RF Frequency at Various LO Powers

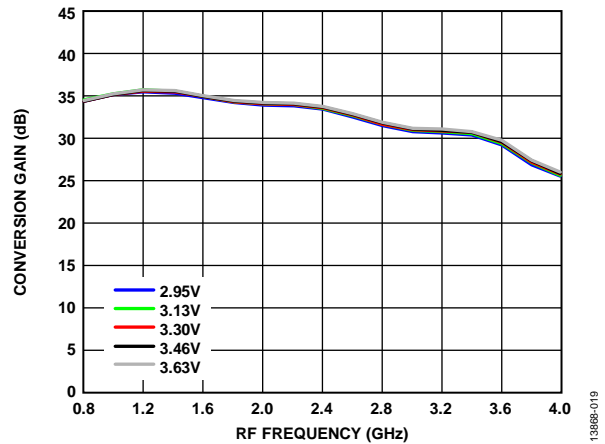


Figure 20. Conversion Gain vs. RF Frequency at Various  $V_{CCx}$

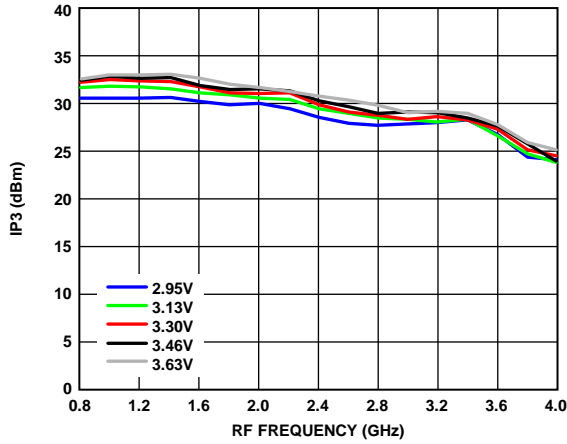


Figure 21. Output IP3 vs. RF Frequency at Various  $V_{CCX}$

13986-020

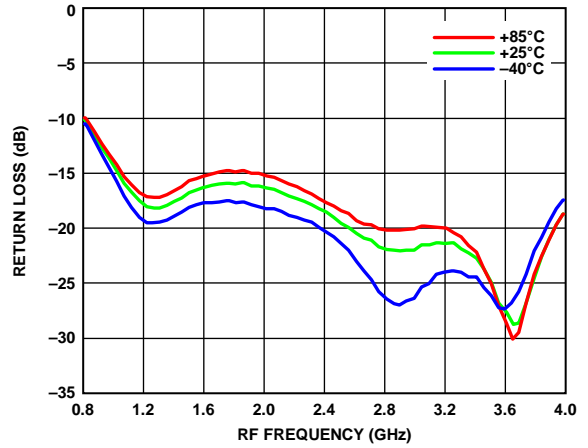


Figure 24. RF Return Loss vs. RF Frequency over Temperature

13986-023

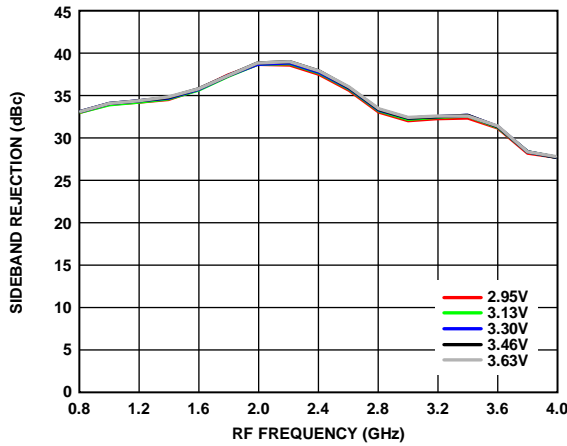


Figure 22. Sideband Rejection vs. RF Frequency at Various  $V_{CCX}$

13986-021

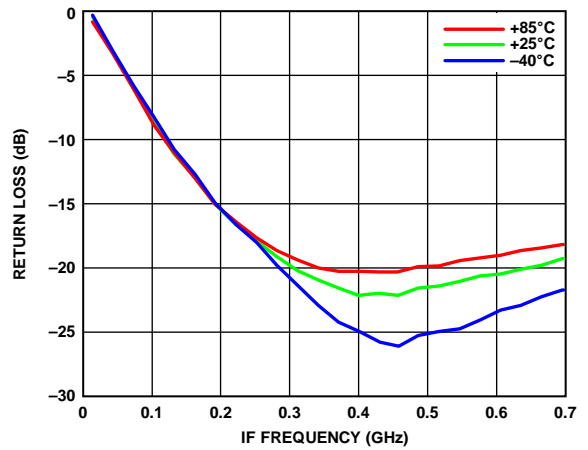


Figure 25. IF Return Loss vs. RF Frequency over Temperature

13986-024

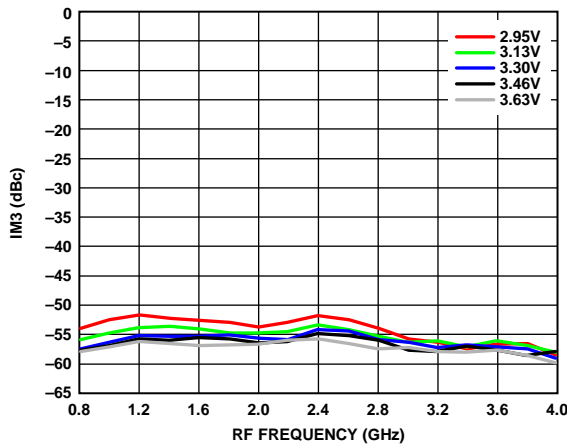


Figure 23. IM3 vs. RF Frequency at Various  $V_{CCX}$

13986-022

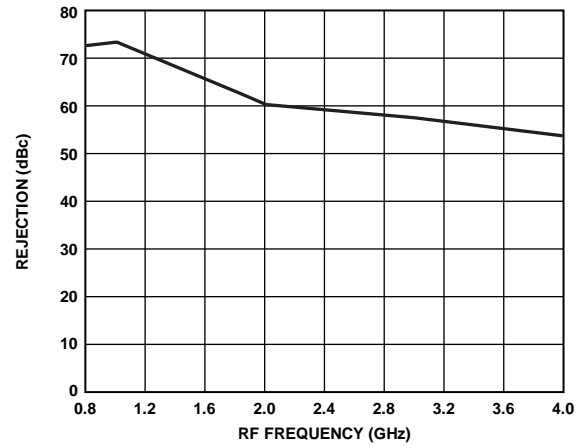


Figure 26. IF to RF Rejection vs. RF Frequency at 25°C

13986-025

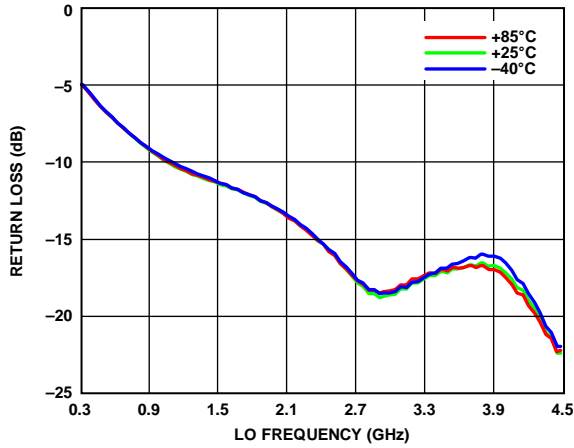


Figure 27. LO Return Loss vs. RF Frequency over Temperature

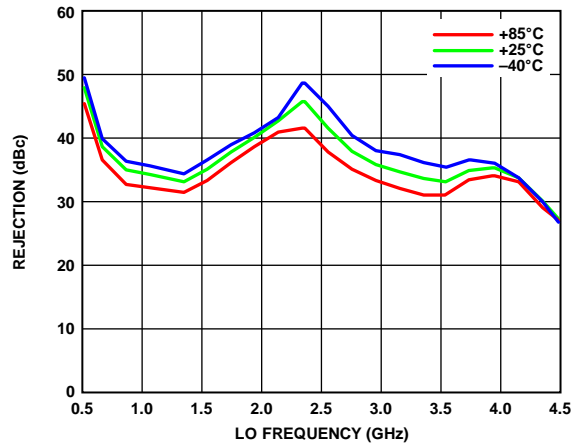


Figure 28. LO to RF Rejection vs. LO Frequency over Temperature, Measurement Uncalibrated for LO Leakage

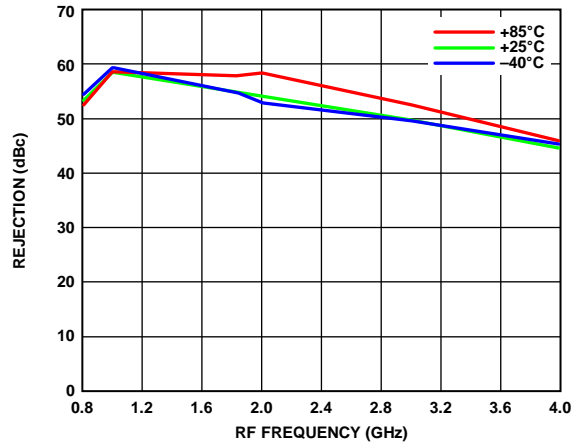


Figure 29. IF to RF Rejection vs. RF Frequency over Temperature, Measured at the Input of the External Low-Pass Filter After C55, see Figure 64

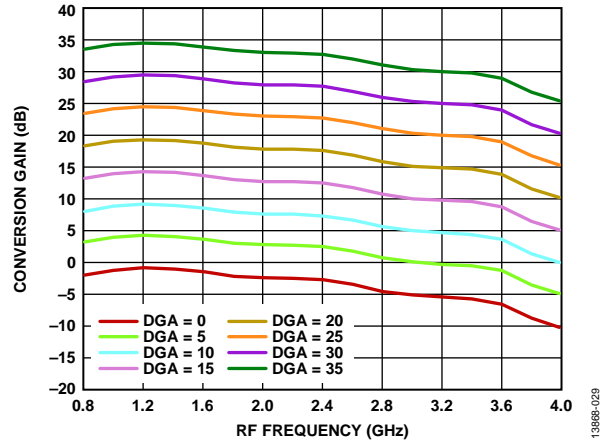


Figure 30. Conversion Gain vs. RF Frequency over DGA Word, Measurement Conducted with VCC\_VGA = 3.3 V (Maximum Gain) on RF VGA

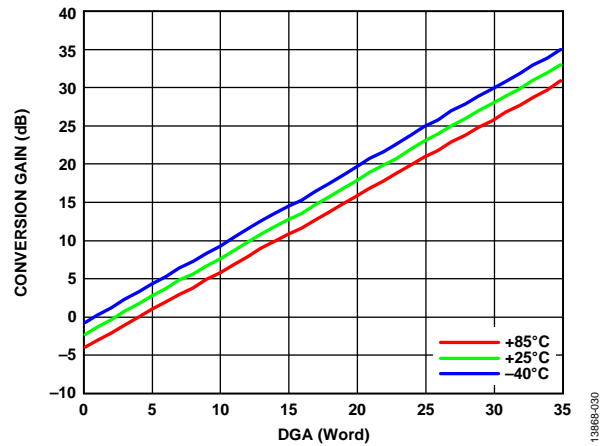


Figure 31. Conversion Gain vs. DGA Word over Temperature, Measurement Conducted with VCC\_VGA = 3.3 V (Maximum Gain) on RF VGA, RF = 2 GHz

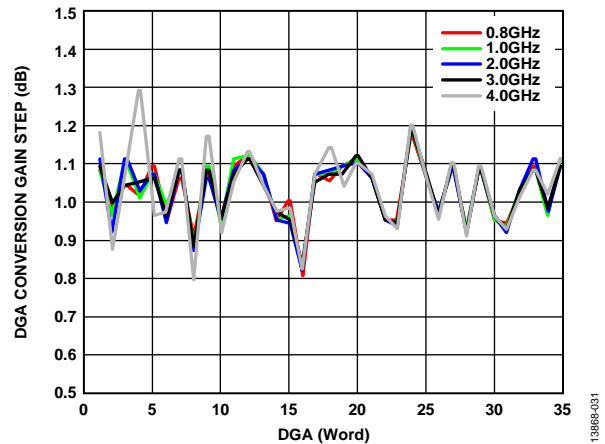


Figure 32. Conversion Gain Step vs. DGA Word over RF Frequency

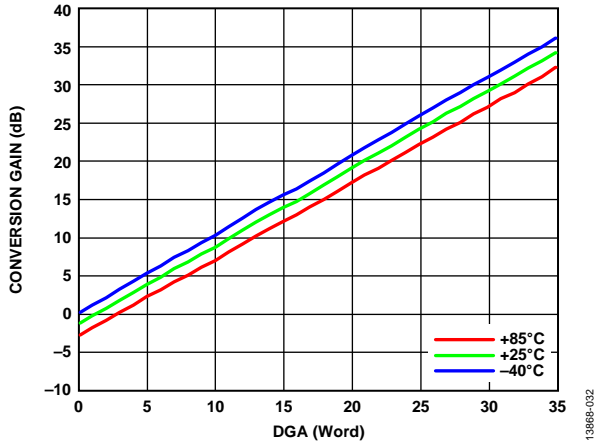


Figure 33. Conversion Gain vs. DGA Word over Temperature, RF = 1 GHz, Measurement Conducted with VCC\_VGA = 3.3 V (Maximum Gain) on RF VGA

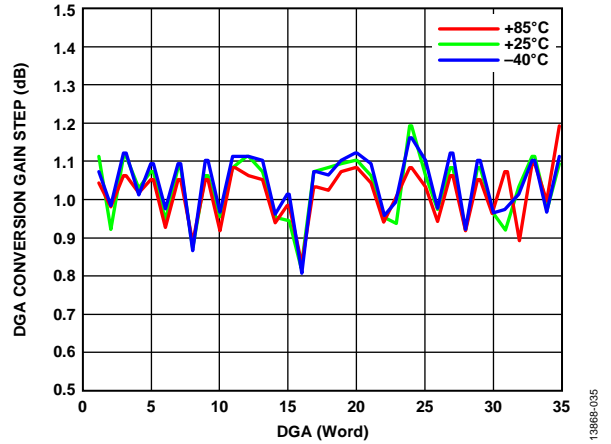


Figure 36. Conversion Gain Step vs. DGA Word over Temperature, RF = 2 GHz

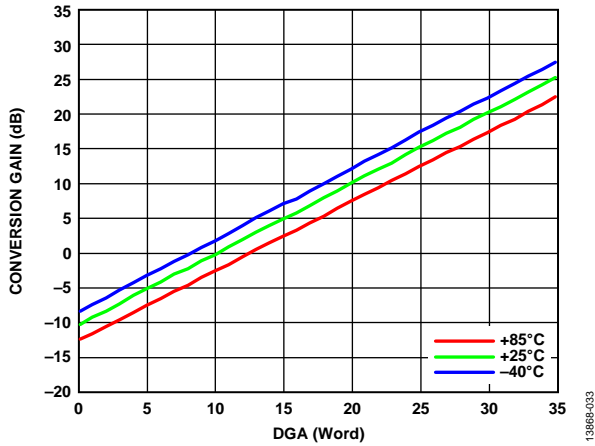


Figure 34. Conversion Gain vs. DGA Word over Temperature, RF = 4 GHz, Measurement Conducted with VCC\_VGA = 3.3 V (Maximum Gain) on RF VGA

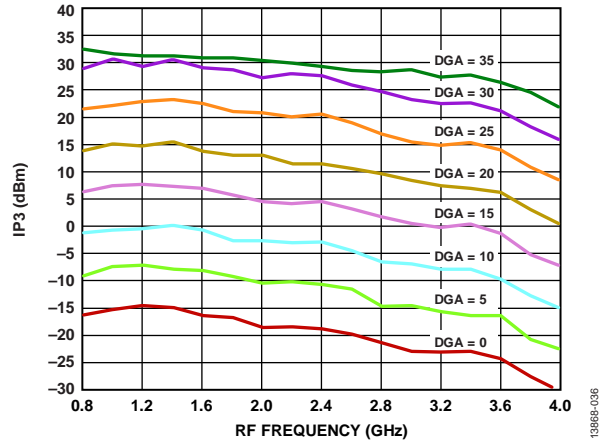


Figure 37. Output IP3 vs. RF Frequency over DGA Word, Measurement Conducted with VCC\_VGA = 3.3 V (Maximum Gain) on RF VGA

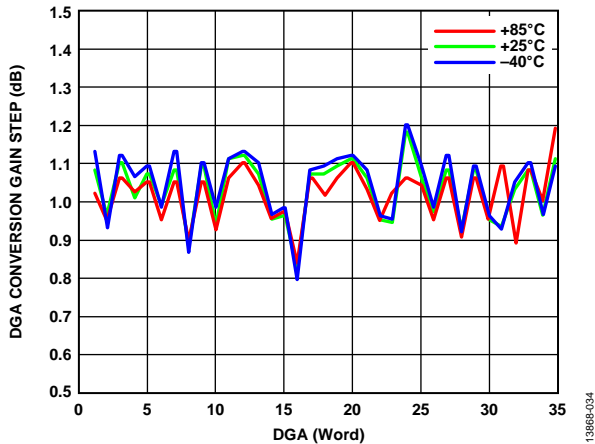


Figure 35. Conversion Gain Step vs. DGA Word over Temperature, RF = 1 GHz, Measurement Conducted with VCC\_VGA = 3.3 V (Maximum Gain) on RF VGA

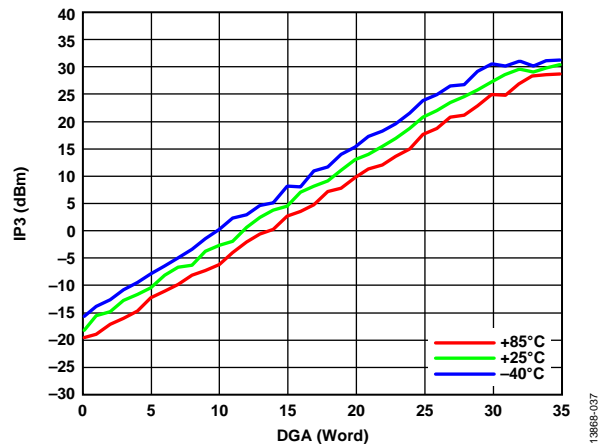


Figure 38. Output IP3 vs. DGA Word over Temperature, RF = 2 GHz, Measurement Conducted with VCC\_VGA = 3.3 V (Maximum Gain) on RF VGA

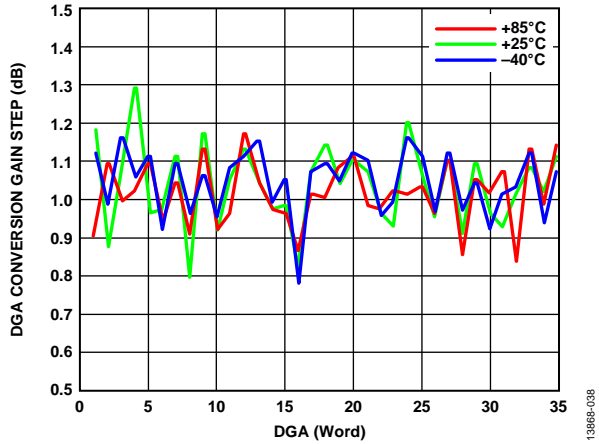


Figure 39. Conversion Gain Step vs. DGA Word over Temperature, RF = 4 GHz

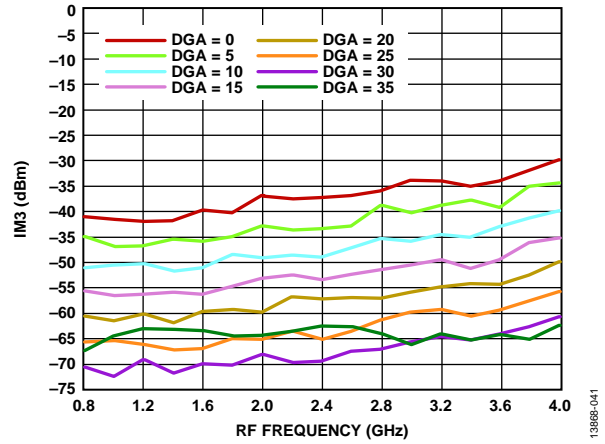


Figure 42. IM3 vs. RF Frequency over DGA Word, Measurement Conducted with VCC\_VGA = 3.3 V (Maximum Gain) on RF VGA

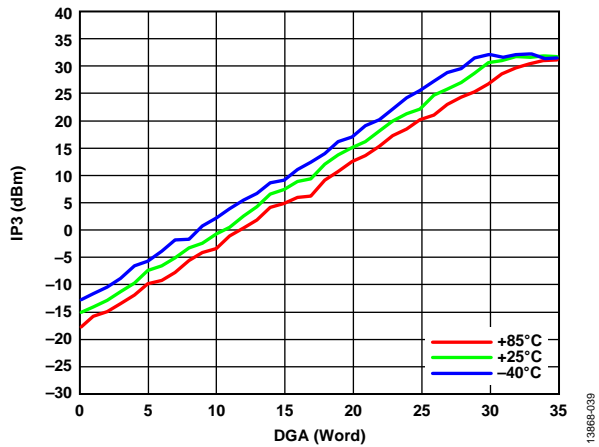


Figure 40. Output IP3 vs. DGA Word over Temperature, RF = 1 GHz, Measurement Conducted with VCC\_VGA = 3.3 V (Maximum Gain) on RF VGA

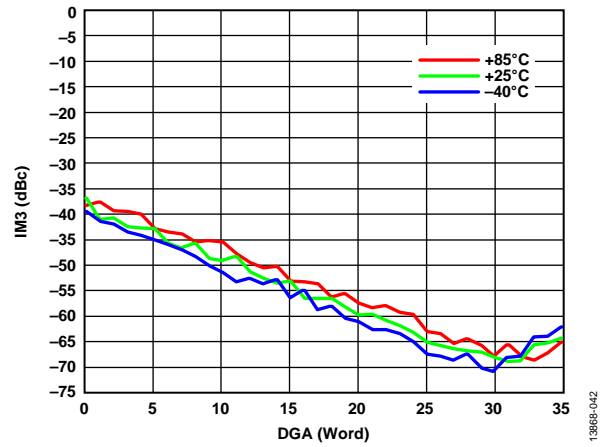


Figure 43. IM3 vs. DGA Word over Temperature, RF = 2 GHz, Measurement Conducted with VCC\_VGA = 3.3 V (Maximum Gain) on RF VGA

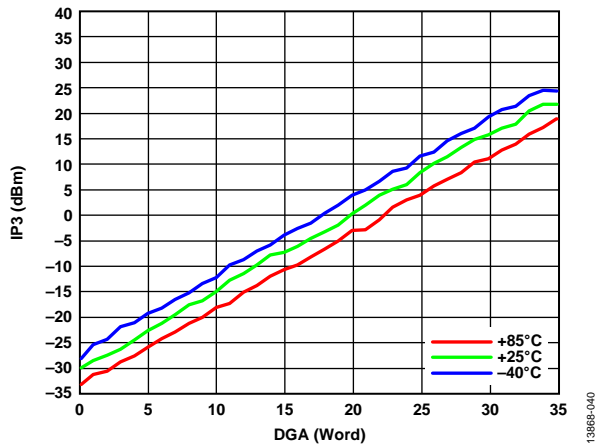


Figure 41. Output IP3 vs. DGA Word over Temperature, RF = 4 GHz, Measurement Conducted with VCC\_VGA = 3.3 V (Maximum Gain) on RF VGA

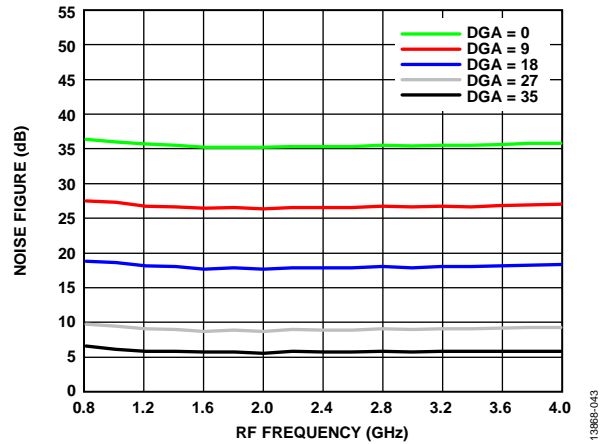


Figure 44. Noise Figure vs. RF Frequency over DGA Word at VCC\_VGA = 3.3 V

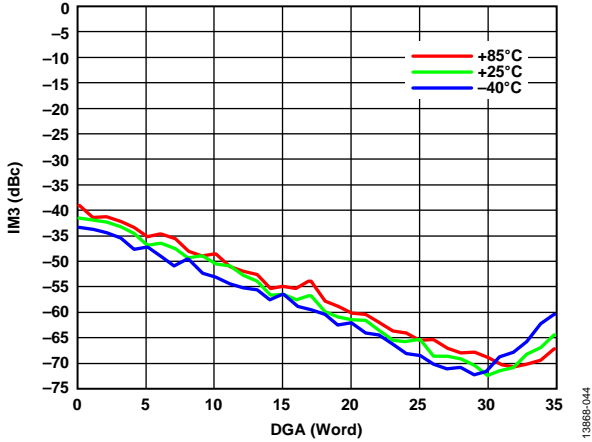


Figure 45. IM3 vs. DGA Word over Temperature, RF = 1 GHz, Measurement Conducted with VCC\_VGA = 3.3 V (Maximum Gain) on RF VGA

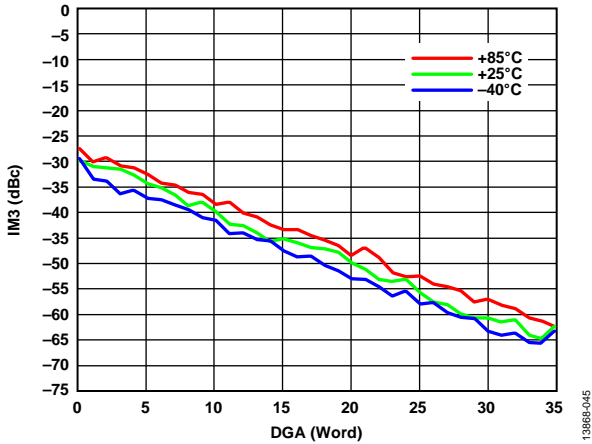


Figure 46. IM3 vs. DGA Word over Temperature, RF = 4 GHz, Measurement Conducted with VCC\_VGA = 3.3 V (Maximum Gain) on RF VGA

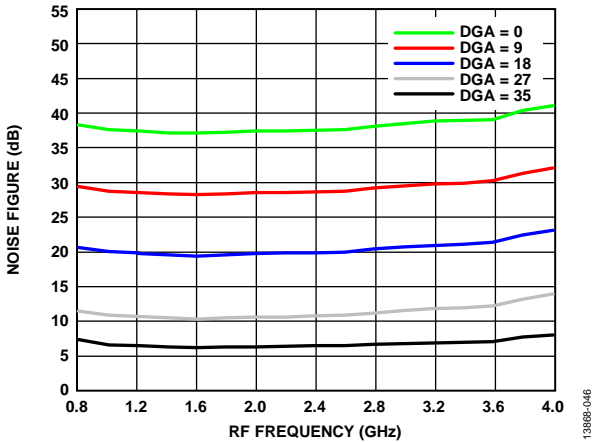


Figure 47. Noise Figure vs. RF Frequency over DGA Word at VCC\_VGA = 1.5 V

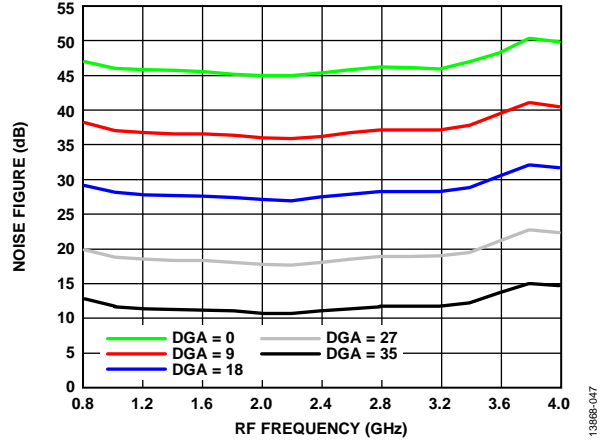


Figure 48. Noise Figure vs. RF Frequency over DGA Word at VCC\_VGA = 0 V

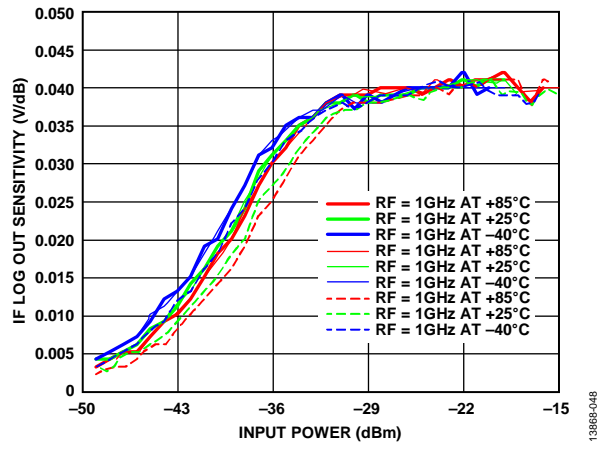


Figure 49. Log IF Detector Sensitivity vs. Input Power over Temperature and RF Frequency

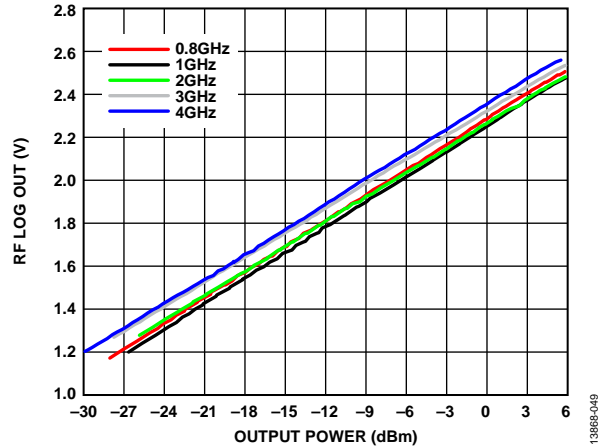


Figure 50. Log RF Detector vs. Output Power over RF Frequency

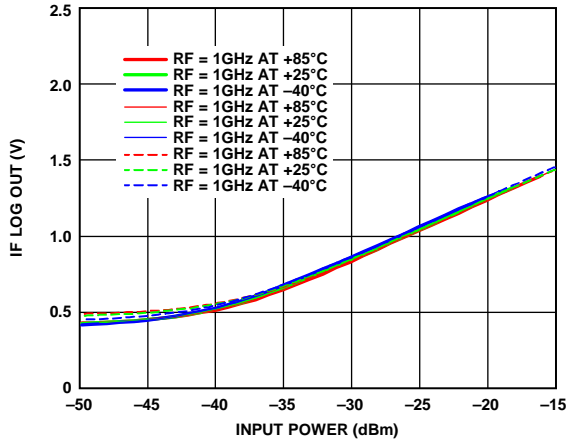


Figure 51. Log IF Detector Output vs. Input Power over Temperature and RF Frequency

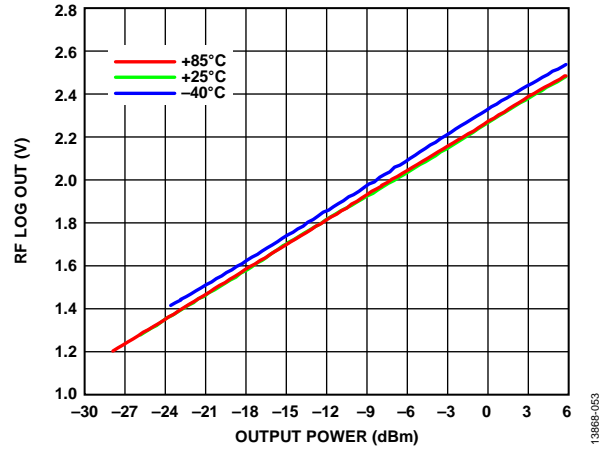


Figure 54. Log RF Detector vs. Output Power over Temperature, RF = 2 GHz

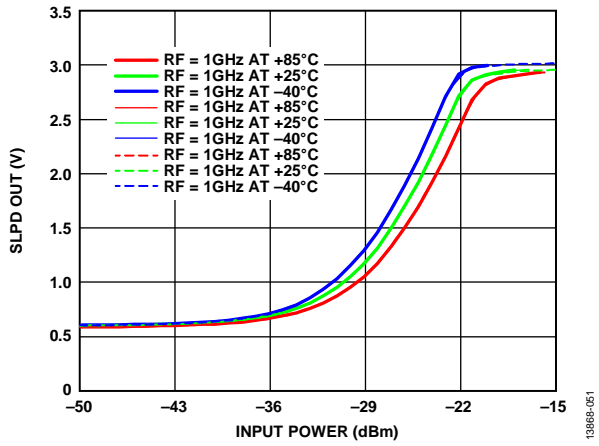


Figure 52. Square Law Detector Output vs. Input Power over Temperature and RF Frequency

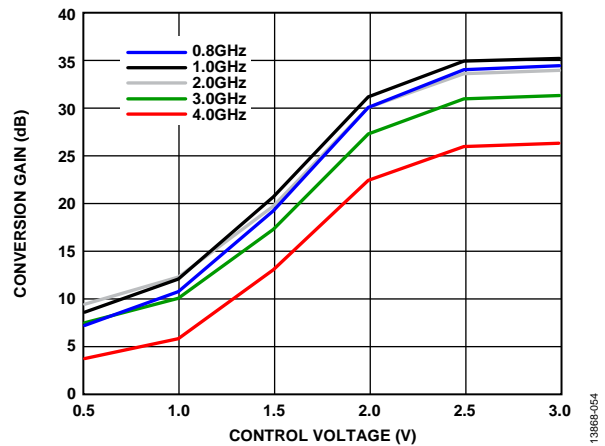


Figure 55. Conversion Gain vs. VGA Control Voltage over RF Frequency, Measurement Conducted with DGA = 35 (Maximum Gain) on IF DGA

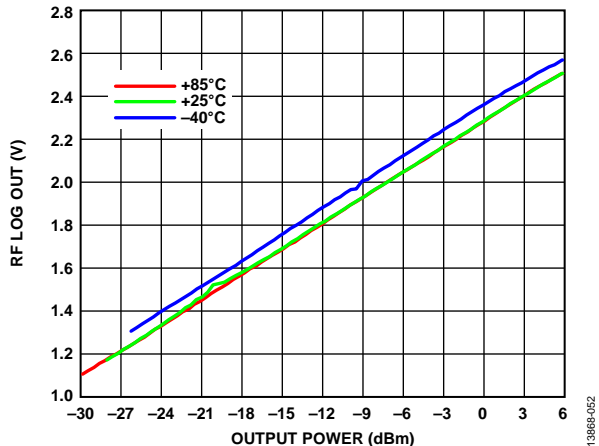


Figure 53. Log RF Detector vs. Output Power over Temperature, RF = 0.8 GHz

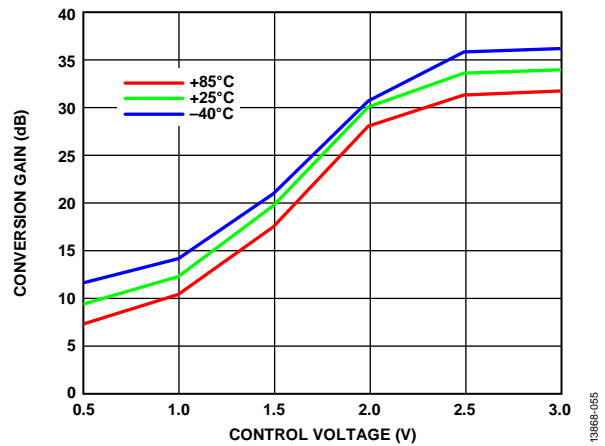


Figure 56. Conversion Gain vs. VGA Control Voltage over Temperature, RF = 2 GHz, Measurement Conducted with DGA = 35 (Maximum Gain) on IF DGA



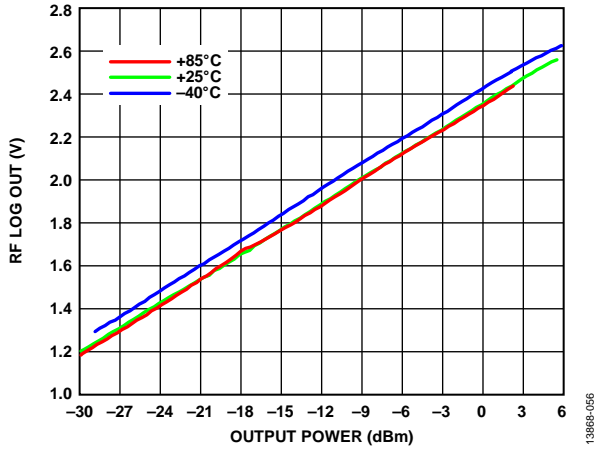


Figure 57. Log RF Detector vs. Output Power over Temperature, RF = 4 GHz

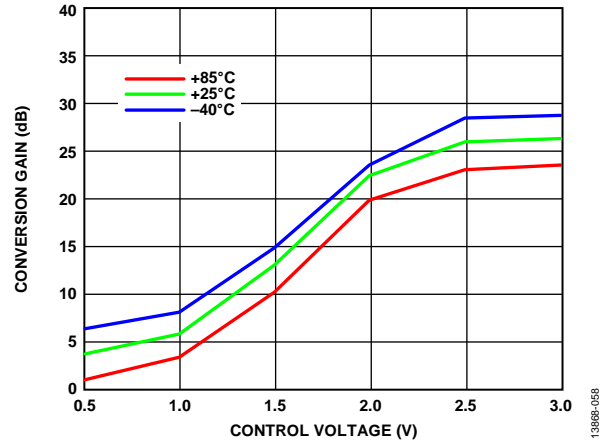


Figure 59. Conversion Gain vs. VGA Control Voltage over Temperature, RF = 4 GHz, Measurement Conducted with DGA = 35 (Maximum Gain) on IF DGA

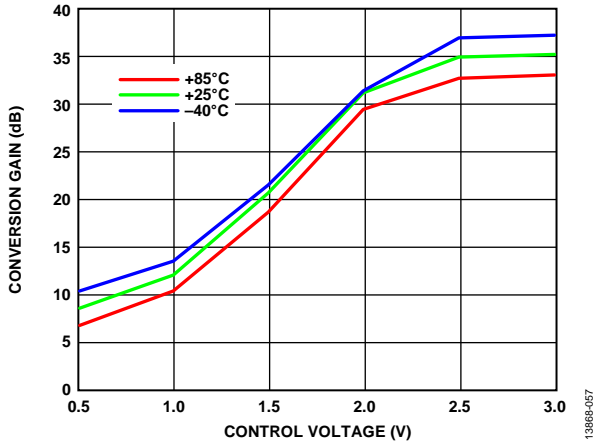


Figure 58. Conversion Gain vs. VGA Control Voltage over Temperature, RF = 1 GHz, Measurement Conducted with DGA = 35 (Maximum Gain) on IF DGA

## THEORY OF OPERATION

The **HMC8200LP5ME** is a highly integrated intermediate frequency (IF) transceiver chip that converts intermediate frequency to a single-ended radio frequency (RF) signal at its output. The intermediate frequency (IF) can be supplied to the **HMC8200LP5ME** single ended or through the baseband differential inputs.

The single-ended input of the **HMC8200LP5ME** utilizes an input digital gain amplifier (DGA) that is controlled via SPI, which feeds the IF signals to an image reject mixer. At the input of the device before the DGA, an intermediate log power detector can be used to monitor input power levels into the device. A square law detector follows the DGA to monitor the power entering the mixer. See the Register Array Assignments and Serial Interface section for more information regarding the DGA.

The baseband differential inputs of the **HMC8200LP5ME** feed the intermediate frequency directly into the image reject mixer. It is recommended that when using the single-ended input, do not leave the baseband differential inputs connected. The local oscillator port can either be driven single ended through LO\_N or differentially through the combination of LO\_N and LO\_P. If Driving the local oscillator port differentially improves the LO to RF rejection.

The IF is then converted to RF, which is followed by an amplifier. Next, the amplified RF signal is fed off chip to a low-pass filter. The external filter path feeds back into a variable gain amplifier (VGA) that is voltage controlled. The output of the VGA drives a final amplifier that is the output of the device. An RF log detector is connected to the output of the final amplifier to monitor the output power of the **HMC8200LP5ME**.

The **HMC8200LP5ME** utilizes an input low noise amplifier (LNA) cascaded with a VGA, which can either be controlled by the internal AGC or external voltages, that feeds the RF signals to an image reject mixer. The local oscillator port can either be driven single ended through LO\_N or differentially through the combination of LO\_N and LO\_P.

The radio frequency is then converted to intermediate frequencies, which can either feed off chip via baseband differential outputs or feed on chip into a programmable band-pass filter. It is recommended during IF mode operation that the baseband outputs be unconnected.

The programmable band-pass filter on chip has four programmable bandwidths (14 MHz, 28 MHz, 56 MHz, and 112 MHz). The programmable band-pass filter has the capability to adjust the center frequency.

From the factory, a filter calibration is conducted and the center frequency of the filter is set to 140 MHz.

This calibration can be recalled via SPI control or the customer can adjust the center frequency, but the calibration value must be stored off chip (see the Register Array Assignments section). An external filter option can be utilized to allow the customer to select other filter bandwidths/responses that are not available on chip. The external filter path coming from the image reject mixer feeds into an amplifier that has differential outputs. The output of the external filter can be fed back into the chip, which is then connected to another amplifier.

A VGA follows immediately after the band-pass filter. Control the IF VGA either by the AGC or external voltages. The output of the variable gain amplifier is the output of the device.

## REGISTER ARRAY ASSIGNMENTS AND SERIAL INTERFACE

The register arrays for the **HMC8200LP5ME** are organized into seven registers of 16 bits. Using the serial interface, the arrays are written or read one row at a time, as shown in Figure 61 and Figure 62. Figure 61 shows the sequence of signals on the enable (SEN), CLK, and data (SDI) lines to write one 16-bit array of data to a single register. The enable line goes low, the first of 24 data bits is placed on the data line, and the data is sampled on the rising edge of the clock. The data line should remain stable for at least 2 ns after the rising edge of CLK. The device supports a serial interface running up to 10 MHz, the interface is 3.3 V CMOS logic.

A write operation requires 24 data bits and 24 clock pulses, as shown in Figure 61. The 24 data bits contain the 3-bit chip address, followed by the 5-bit register array number, and finally the 16-bit register data. After the 24th clock pulses of the write operation, the enable line returns high to load the register array on the IC.

A read operation requires 24 data bits and 48 clock pulses, as shown in Figure 62. For every register read operation, a write to Register 7 is required first. The data written should contain the 3-bit chip address, followed by the 5-bit register number for Register 7, and finally the 5-bit number of the register to be read. The remaining 11 bits should be logic zeroes. When the read operation is initiated, the data is available on the data output (SDO) pin.

### Read Example

If reading Register 2, write the following 24 bits to initiate the read operation. The output data bits are placed on the data line during the rising edge of the clock.

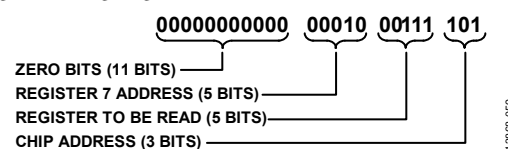


Figure 60. Sample Bits to Initiate Read

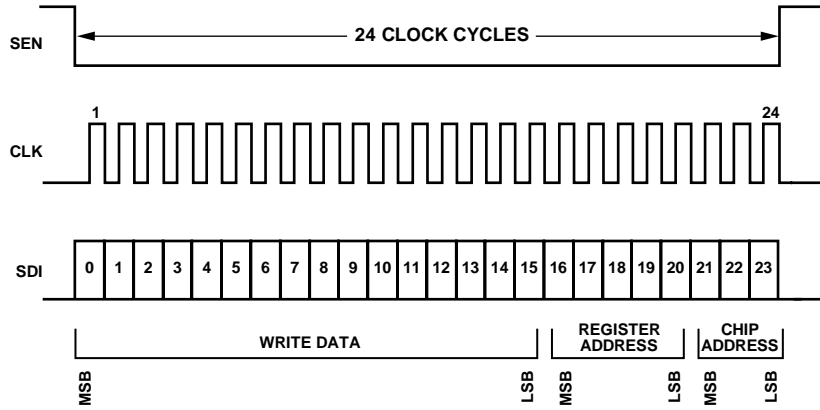


Figure 61. Timing Diagram, SPI Register Write

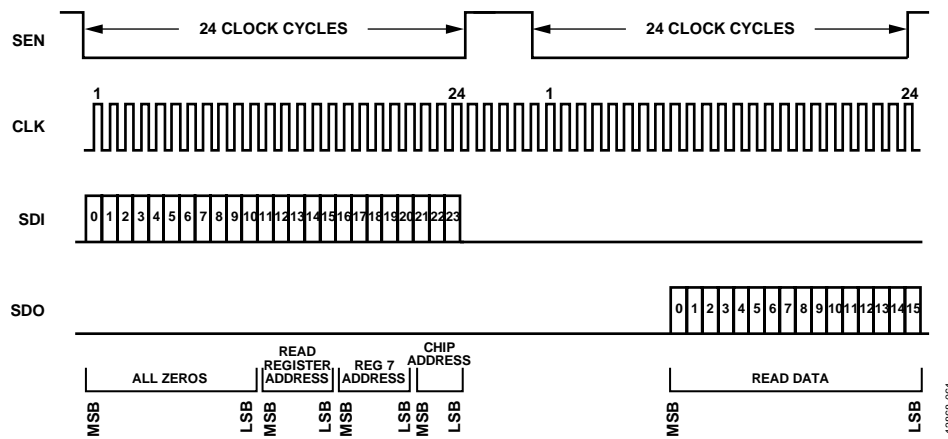


Figure 62. Timing Diagram, SPI Register Read

## REGISTER DESCRIPTIONS

### REGISTER ARRAY ASSIGNMENTS

In the Access columns (Table 6 through Table 12), R means read, W means write, and R/W means read/write.

#### Enable Bits

Table 6. Enable Register, (Address 0x01)

| Bit No. | Bit Name            | Description                                                                  | Reset | Access |
|---------|---------------------|------------------------------------------------------------------------------|-------|--------|
| [15:13] | Reserved            | Not used                                                                     | 0x6   | R/W    |
| 12      | LOG_IF_EN           | Log intermediate frequency (IF) detector enable<br>0 = disable<br>1 = enable | 0x1   | R/W    |
| 11      | D2SE_EN             | Differential to single (after mixer) enable<br>0 = disable<br>1 = enable     | 0x1   | R/W    |
| 10      | Factory diagnostics | 0 = Logic 0 for normal operation                                             | 0x0   | R/W    |
| 9       | CM_BUFFER_EN        | Common-mode buffer enable<br>0 = disable<br>1 = enable                       | 0x0   | R/W    |
| 8       | Factory Diagnostics | 1 = Logic 1 for normal operation                                             | 0x1   | R/W    |
| 7       | LOG_DET_EN          | Log detector enable<br>0 = disable<br>1 = enable                             | 0x1   | R/W    |
| 6       | MS_EN               | Square detector enable<br>0 = disable<br>1 = enable                          | 0x1   | R/W    |
| 5       | ENVELOPE_EN         | Envelope detector enable<br>0 = enable<br>1 = disable                        | 0x1   | R/W    |
| 4       | VGA_EN              | Variable gain amplifier (VGA) enable<br>0 = disable<br>1 = enable            | 0x1   | R/W    |
| 3       | IRM_EN              | Image reject mixer enable<br>0 = disable<br>1 = enable                       | 0x1   | R/W    |
| 2       | IRM_IQ_EN           | IQ line enable<br>0 = disable<br>1 = enable                                  | 0x0   | R/W    |
| 1       | DGA_EN              | Digital gain amplifier (DGA) enable<br>0 = disable<br>1 = enable             | 0x1   | R/W    |
| 0       | LPF_EN              | Low-pass filter enable<br>0 = disable<br>1 = enable                          | 0x0   | R/W    |

**Digital Gain Amplifier: DGA Control**

Table 7. Digital Gain Amplifier (Address 0x03)

| Bit No. | Bit Name | Description                                                                                                   | Reset | Access |
|---------|----------|---------------------------------------------------------------------------------------------------------------|-------|--------|
| 15      | Reserved | Not used                                                                                                      | 0x0   | R/W    |
| [14:9]  | DGA_CTRL | Override SPI FIL2_FRQ_SET and use 8-bit word from OTP<br>0 = minimum gain<br>1 = ...<br>100011 = maximum gain | 0x0   | R/W    |
| [8:0]   | Reserved | Not used                                                                                                      | 0x0   | R/W    |

**Digital Gain Amplifier: Amplifier Current, Envelope Level, and VGA Attenuation Bias**

Table 8. Digital Gain Amplifier, (Address 0x04)

| Bit No. | Bit Name     | Description          | Reset   | Access |
|---------|--------------|----------------------|---------|--------|
| [15:9]  | Reserved     | Not used             | 0000111 | R/W    |
| [8:7]   | AMP_CUR      | Amplifier current    | 11      | R/W    |
| [6:2]   | ENV_LVL      | Envelope level       | 11100   | R/W    |
| [1:0]   | VGA_ATT_BIAS | VGA attenuation bias | 10      | R/W    |

**Image Reject Mixer: Sideband, and Polarity and Offset for I**

Table 9. Image Reject Mixer Register, (Address 0x05)

| Bit No. | Bit Name          | Description                                                | Reset | Access |
|---------|-------------------|------------------------------------------------------------|-------|--------|
| [15:12] | Reserved          | Reserved<br>Logic 0010 for normal operation                | 0010  |        |
| 11      | IRM_IS            | Image sideband<br>0 = upper sideband<br>1 = lower sideband | 1     | R/W    |
| [10:9]  | Reserved          | Reserved<br>Logic 01 for normal operation                  | 01    | R/W    |
| 8       | OFFSET_POLARITY_I | Offset Polarity I                                          | 0     | R/W    |
| [7:0]   | IRM_OFFSET_I      | Image reject mixer offset for I                            | 0x0   | R/W    |

**Image Reject Mixer: Polarity and Offset for Q**

Table 10. Image Reject Mixer Register, (Address 0x06)

| Bit No. | Bit Name          | Description                     | Reset   | Access |
|---------|-------------------|---------------------------------|---------|--------|
| [15:9]  | Reserved          | Not used                        | 1111000 | R/W    |
| 8       | OFFSET_POLARITY_Q | Offset Polarity Q               | 0       | R/W    |
| [7:0]   | IRM_OFFSET_Q      | Image reject mixer offset for Q | 0x0     | R/W    |

**Phase I: Adjust**

Table 11. Phase I Register, (Address 0x08)

| Bit No. | Bit Name    | Description    | Reset   | Access |
|---------|-------------|----------------|---------|--------|
| [15:9]  | Reserved    | Not used       | 1111000 | R/W    |
| [8:0]   | I_PHASE_ADJ | I phase adjust | 0x0     | R/W    |

**Phase Q: Adjust**

Table 12. Phase Q Register, (Address 0x09)

| Bit No. | Bit Name    | Description    | Reset   | Access |
|---------|-------------|----------------|---------|--------|
| [15:9]  | Reserved    | Not used       | 1111000 | R/W    |
| [8:0]   | Q_PHASE_ADJ | Q phase adjust | 0x0     | R/W    |

### EVALUATION PRINTED CIRCUIT BOARD (PCB)

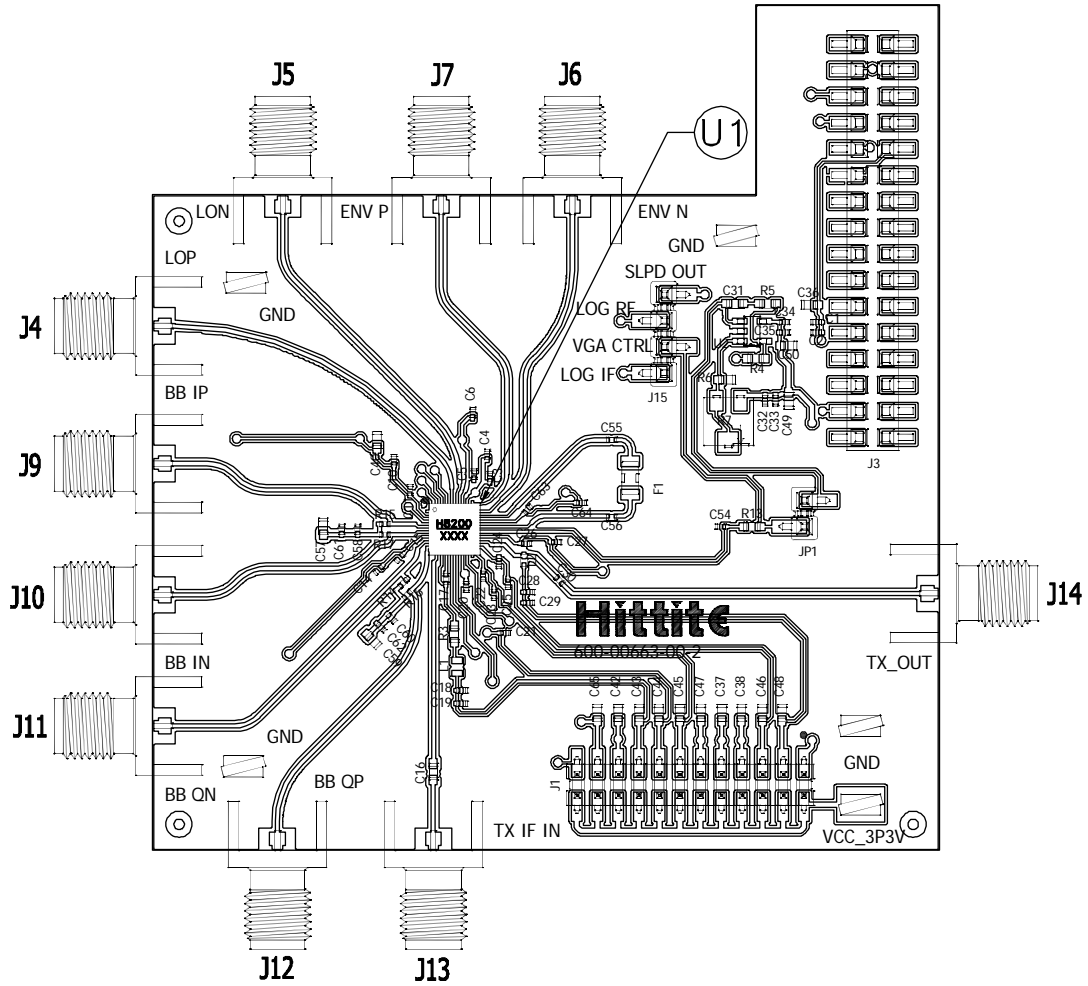


Figure 63. Evaluation PCB

13865-063

EVALUATION PCB SCHEMATIC

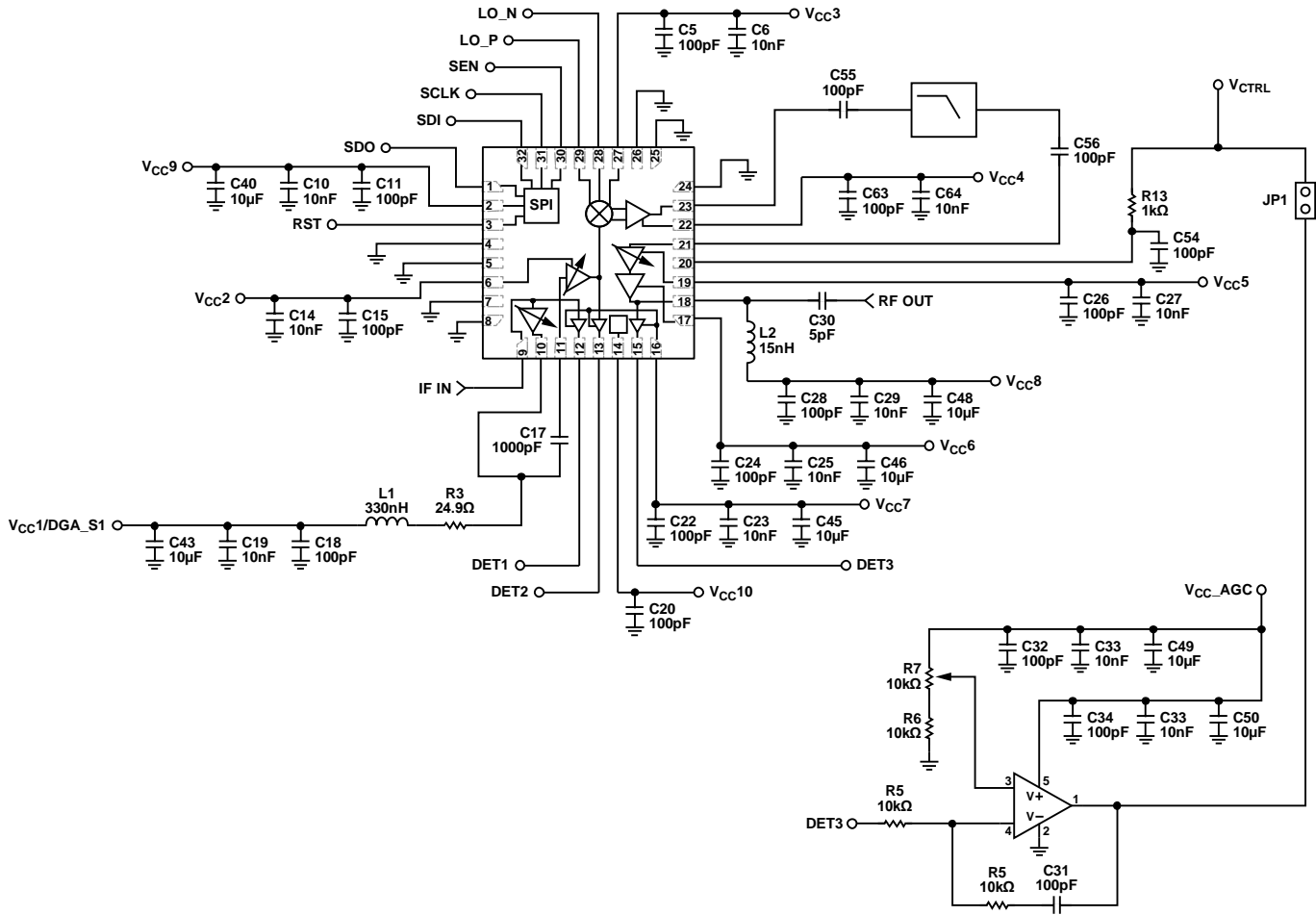
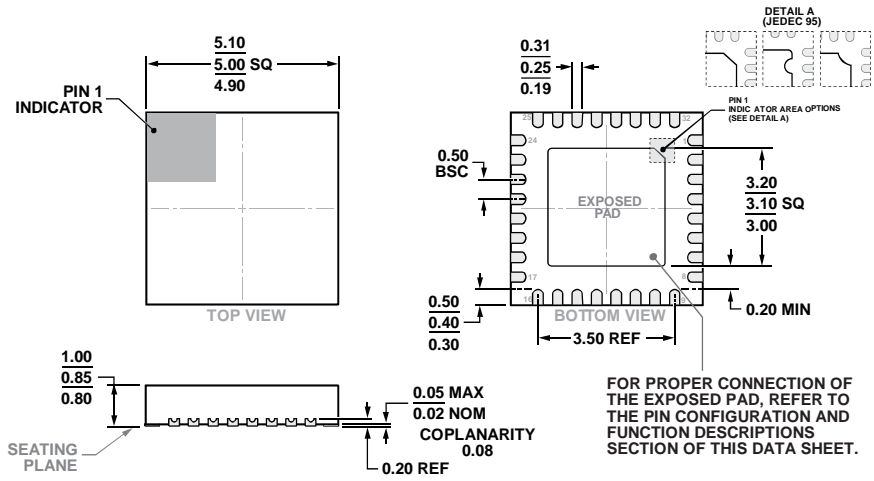


Figure 64. PCB Schematic/Typical Applications Circuit

13868-062



# OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

Figure 65. 32-Lead Lead Frame Chip Scale Package [LFCSP]  
5 mm × 5 mm Body, 0.85 mm Package Height  
(CP-32-27)

Dimensions shown in millimeters

## ORDERING GUIDE

| Model <sup>1,2</sup> | Temperature Range | MSL Rating <sup>3</sup> | Package Description          | Package Option | Branding <sup>4</sup> | Quantity |
|----------------------|-------------------|-------------------------|------------------------------|----------------|-----------------------|----------|
| HMC8200LP5ME         | -40°C to +85°C    | MSL3                    | 32-Lead LFCSP, Tape and Reel | CP-32-27       | H8200<br>XXXX         | 50       |
| HMC8200LP5METR       | -40°C to +85°C    | MSL3                    | 32-Lead LFCSP, Tape and Reel | CP-32-27       | H8200<br>XXXX         | 500      |
| EK1HMC8200LP5M       |                   |                         | Evaluation Kit               |                |                       |          |

<sup>1</sup> All products listed in the ordering guide are RoHS compliant.

<sup>2</sup> The HMC8200LP5ME lead finish is NiPdAu.

<sup>3</sup> See the Absolute Maximum Ratings section.

<sup>4</sup> XXXX is the 4-digit lot number.

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Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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