



SY10/100EP16U

2.5/3.3V Precision ECL Differential Receiver/Driver

General Description

The SY10/100EP16U is a 2.5/3.3V, high-speed, fully differential ECL Receiver/Driver that can process clock signals as fast as 3GHz or data patterns up to 2.5Gbps.

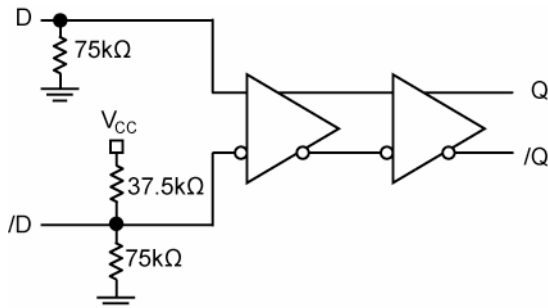
The differential input includes an internal 75k Ω pull-down resistor on both the true and complement inputs and a 37.5k Ω pull-up resistor in the complement input only. For AC-coupled input interface and single-ended applications, an integrated voltage reference (V_{BB}) is provided. Single-ended CLK input operation is limited to $V_{CC} \geq 3.0V$ in PECL mode, or $V_{EE} \leq -3.0V$. The V_{BB} pin should be used only as a bias for the SY10/100EP16U since its current sink/source capability is limited. Whenever used, the V_{BB} pin should be bypassed to the most positive supply voltage. The output is 800mV ECL, with fast rise/fall times guaranteed to be less than 200ps.

When the inputs are left open, the internal input clamps will force the Q output low.

The SY10/100EP16U operates from a 2.5V $\pm 5\%$ or 3.3V $\pm 10\%$ supply and is guaranteed over the full industrial temperature range ($-40^{\circ}C$ to $+85^{\circ}C$). The SY100EP16V is part of Micrel's high-speed, Precision Edge[®] product line.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Functional Block Diagram



Precision Edge[®]

Features

- Precision 800mV ECL Receiver/Driver
- 10K and 100K ECL compatible I/O
- Guaranteed AC performance over temperature and voltage:
 - DC-to > 2.5Gbps throughput
 - 240ps typical propagation delay (D-to-Q)
 - <200ps rise/fall times
- Ultra-low jitter design
 - < 0.3ps_{RMS} random jitter
- PECL and NECL operation capability
- PECL operating range: $V_{CC} = 2.375V$ to $3.63V$ with $V_{EE} = 0V$
- NECL operating range: $V_{CC} = 0V$ with $V_{EE} = -2.375V$ to $-3.63V$
- 2.5V $\pm 5\%$ or 3.3V $\pm 10\%$ power supply operation
- Industrial temperature range: $-40^{\circ}C$ to $+85^{\circ}C$
- Available in 8-pin (2mm x 2mm) MLF[®], 8-pin MSOP, 8-pin SOIC packages

Applications

- All SONET clock and data distribution
- Fibre Channel clock and data distribution
- Gigabit Ethernet clock and data distribution
- Backplane distribution

Markets

- Storage
- ATE
- Test and measurement
- Enterprise networking equipment
- High-end servers
- Access
- Metro area network equipment

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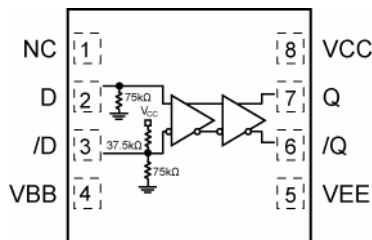
Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10EP16UMG	MLF-8	Industrial	161 with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY10EP16UMGTR ⁽²⁾	MLF-8	Industrial	161 with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY100EP16UMG	MLF-8	Industrial	160 with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY100EP16UMGTR ⁽²⁾	MLF-8	Industrial	160 with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY10EP16UZG	SOIC-8	Industrial	HEP16U with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY10EP16UZGTR ⁽²⁾	SOIC-8	Industrial	HEP16U with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY100EP16UZG	SOIC-8	Industrial	XEP16U with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY100EP16UZTR ⁽²⁾	SOIC-8	Industrial	XEP16U with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY10EP16UKG	MSOP-8	Industrial	HP16U with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY10EP16UKGTR ⁽²⁾	MSOP-8	Industrial	HP16U with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY100EP16UKG	MSOP-8	Industrial	XP16U with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY100EP16UKGTR ⁽²⁾	MSOP-8	Industrial	XP16U with Pb-Free bar-line indicator	NiPdAu Pb-Free

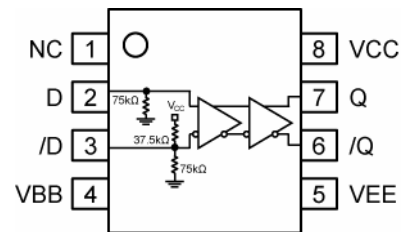
Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^\circ\text{C}$, DC Electricals only.
2. Tape and Reel.

Pin Configuration



8-Pin MLF[®] (MLF-8)



**8-pin SOIC (SOIC-8)
8-pin MSOP (MSOP-8)**

Pin Description

Pin Number	Pin Name	Pin Function
2, 3	D, /D	ECL Inputs. The D input has an internal 75k Ω pull-down resistor and the /D has an internal 37.5k Ω pull-up and a 75k Ω pull-down resistor.
7, 6	Q, /Q	ECL Outputs. Terminate with 50 Ω to V_{CC} -2V. See "Output Interface Applications" section for more details.
4	V_{BB}	Reference Output Voltage: This reference is typically used to bias the unused inverting input for single-ended input applications, or as the termination point for AC-coupled differential input applications. V_{BB} reference value is approximately V_{CC} - 1.42V, and tracks V_{CC} 1:1. Maximum sink/source capability for V_{BB} is 0.50mA. For single ended inputs, connect to the unused input through a 50 Ω resistor. Decouple the V_{BB} pin with a 0.01 μ F capacitor to V_{CC} .
8	V_{CC}	Positive Power Supply: Bypass with 0.1 μ F//0.01 μ F low ESR capacitors as close to the V_{CC} pin as possible.
5	V_{EE}	Negative Power Supply: V_{EE} and exposed pad must be tied to the most negative supply. Exposed pad is available for 8-pin MLF [®] package only.

Absolute Maximum Ratings⁽¹⁾

Supply Voltage	
PECL Mode (V_{CC})	+6V
NECL Mode (V_{EE})	-6V
Current (I_{BB})	
Source or Sink current on V_{BB}	± 0.5 mA
Input Voltage (V_{IN})	
PECL Mode	V_{CC} to 0V
NECL Mode	0V to V_{EE}
Output Current (I_{OUT})	
Continuous	50mA
Surge	100mA
Lead Temperature (soldering, 20sec.)	260°C
Storage Temperature (T_s)	-65°C to +150°C

Operating Ratings⁽²⁾

Supply Voltage (V_{CC})	
PECL Mode ($V_{EE} = 0$ V)	+2.375V to +3.60V
Supply Voltage (V_{EE})	
NECL Mode ($V_{CC} = 0$ V)	-2.375V to -3.60V
Ambient Temperature (T_A)	-40°C to +125°C
Junction Thermal Resistance	
MLF [®] (θ_{JA})	90°C/W
MSOP (θ_{JA})	160°C/W
SOIC (θ_{JA})	99°C/W

10EP DC Electrical Characteristics⁽³⁾

$V_{CC} = 2.5V \pm 5\%$, $V_{EE} = 0V$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated⁽⁴⁾

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		17	25		17	25		17	25	mA
V_{OH}	Output HIGH Voltage ⁽⁵⁾	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{OL}	Output LOW Voltage ⁽⁵⁾	565	740	865	630	805	930	690	865	990	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) ^(6,7)	1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	D /D	0.5 -150		0.5 -150			0.5 -150			μA

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
4. Input and output parameters vary 1:1 with V_{CC} .
5. All loading with 50 Ω to $V_{CC}-2.0V$.
6. Do not use V_{BB} at $V_{CC} < 3.0$. Single ended input CLK pin operation is limited to $V_{CC} \geq 3.0V$ in PECL mode.
7. V_{IHCMR} (min) varies 1:1 with V_{EE} , V_{IHCMR} (max) varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

10EP DC Electrical Characteristics⁽⁸⁾
 $V_{CC} = 3.3V \pm 10\%$, $V_{EE} = 0V$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated⁽⁹⁾

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		17	25		17	25		17	25	mA
V_{OH}	Output HIGH Voltage ⁽¹⁰⁾	2165	2290	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage ⁽¹⁰⁾	1365	1540	1665	1430	1605	1730	1490	1665	1790	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1365		1690	1430		1755	1490		1815	mV
V_{BB}	Output Voltage Reference ⁽¹¹⁾	1790	1890	1990	1855	1955	2055	1915	2015	2115	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) ⁽¹²⁾	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	D /D	0.5 -150		0.5 -150			0.5 -150			μA

10EP DC Electrical Characteristics⁽⁸⁾
 $V_{CC} = 0V$, $V_{EE} = -3.63V$ to $-2.375V$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated⁽⁹⁾

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		17	25		17	25		17	25	mA
V_{OH}	Output HIGH Voltage ⁽¹⁰⁾	-1135	-1010	-885	-1070	-945	-820	-1010	-885	-760	mV
V_{OL}	Output LOW Voltage ⁽¹⁰⁾	-1935	-1760	-1635	-1870	-1695	-1570	-1810	-1635	-1510	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1210		-885	-1145		-820	-1085		-760	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1935		-1610	-1870		-1545	-1810		-1485	mV
V_{BB}	Output Voltage Reference ⁽¹³⁾	-1510	-1410	-1310	-1445	-1345	-1245	-1385	-1285	-1185	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) ⁽¹²⁾	V_{EE} +1.2		0	V_{EE} +1.2	0		V_{EE} +1.2	0		V
I_{IH}	Input HIGH Current			150							μA
I_{IL}	Input LOW Current	D /D	0.5 -150			0.5 -150		0.5 -150			μA

Notes:

8. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
9. Input and output parameters vary 1:1 with V_{CC} .
10. All loading with 50Ω to $V_{CC}-2.0V$.
11. Single ended input CLK pin operation is limited to $V_{CC} \geq 3.0V$ in PECL mode.
12. V_{IHCMR} (min) varies 1:1 with V_{EE} , V_{IHCMR} (max) varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
13. Single ended input CLK pin operation is limited to $V_{CC} \leq -3.0V$ in NECL mode.

100EP DC Electrical Characteristics⁽¹⁴⁾
 $V_{CC} = 2.5V \pm 5\%$, $V_{EE} = 0V$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated.⁽¹⁵⁾

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		21	30		21	30		21	30	mA
V_{OH}	Output HIGH Voltage ⁽¹⁶⁾	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{OL}	Output LOW Voltage ⁽¹⁶⁾	555	730	900	555	730	900	555	730	900	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) ^(17, 18)	1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	D /D	0.5 -150		0.5 -150			0.5 -150			μA

100EP DC Electrical Characteristics⁽¹⁴⁾
 $V_{CC} = 3.3V \pm 10\%$, $V_{EE} = 0V$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated.⁽¹⁵⁾

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		21	30		21	30		21	30	mA
V_{OH}	Output HIGH Voltage ⁽¹⁶⁾	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage ⁽¹⁶⁾	1355	1530	1700	1355	1530	1700	1355	1530	1700	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1355		1700	1355		1700	1355		1700	mV
V_{BB}	Output Voltage Reference ⁽¹⁹⁾	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) ⁽¹⁸⁾	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	D /D	0.5 -150		0.5 -150			0.5 -150			μA

Notes:

14. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
15. Input and output parameters vary 1:1 with V_{CC} .
16. All loading with 50Ω to $V_{CC}-2.0V$.
17. Do not use V_{BB} at $V_{CC} < 3.0$. Single ended input CLK pin operation is limited to $V_{CC} \geq 3.0V$ in PECL mode.
18. V_{IHCMR} (min) varies 1:1 with V_{EE} , V_{IHCMR} (max) varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
19. Single ended input CLK pin operation is limited to $V_{CC} \geq 3.0V$ in PECL mode.

100EP DC Electrical Characteristics⁽²⁰⁾

$V_{CC} = 0V$, $V_{EE} = -3.63V$ to $-2.375V$; $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise stated.⁽²¹⁾

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		21	30		21	30		21	30	mA
V_{OH}	Output HIGH Voltage ⁽²²⁾	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
V_{OL}	Output LOW Voltage ⁽²²⁾	-1945	-1770	-1600	-1945	-1770	-1600	-1945	-1770	-1600	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1165		-880	-1165		-880	-1165		-880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1945		-1600	-1945		-1600	-1945		-1600	mV
V_{BB}	Output Voltage Reference ⁽²³⁾	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) ⁽²⁴⁾	$V_{EE} + 1.2$		0	$V_{EE} + 1.2$		0	$V_{EE} + 1.2$		0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	D /D	0.5 -150		50 -150			50 -150			μA

Notes:

20. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
21. Input and output parameters vary 1:1 with V_{CC} .
22. All loading with 50Ω to $V_{CC}-2.0V$.
23. Single ended input CLK pin operation is limited to $V_{CC} \leq -3.0V$ in NECL mode.
24. V_{IHCMR} (min) varies 1:1 with V_{EE} , V_{IHCMR} (max) varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

AC Electrical Characteristics

$V_{CC} = 0V$, $V_{EE} = -3.63V$ to $-2.375V$; $V_{CC} = 2.375V$ to $3.63V$, $V_{EE} = 0V$; $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise stated.⁽²⁵⁾

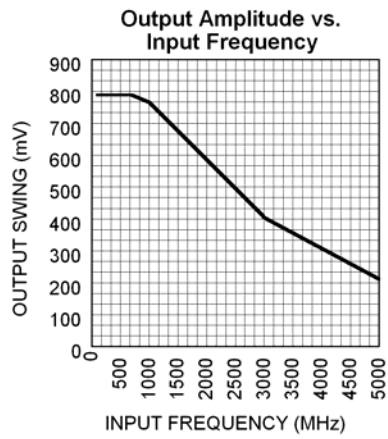
Symbol	Parameters	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{MAX}	Maximum Frequency		2.5			2.5			2.5		Gbps
		3	4		3	4		3	4		GHz
t _{PLH} t _{PHL}	Propagation Delay to Output Differential D→Q, /Q (Figure 1)	150	220	300	170	240	320	190	260	330	ps
t _{Skew}	Duty Cycle Skew ⁽²⁶⁾		5	20		5	20		5	20	ps
t _{JITTER}	CLOCK Random Jitter (RMS) @ = 1.0GHz @ = 1.5GHz @ = 2.0GHz @ = 2.5GHz @ = 3.0GHz @ = 3.5GHz		0.134 0.077 0.115 0.117 0.122 0.123	0.2 0.2 0.2 0.2 0.2 0.2		0.147 0.104 0.141 0.132 0.143 0.145	0.3 0.3 0.3 0.3 0.3 0.3		0.166 0.145 0.153 0.156 0.177 0.202	0.3 0.3 0.3 0.3 0.3 0.3	ps
V _{PP}	Input Voltage Swing (Differential Configuration)	150	800	1200	150	800	1200	150	800	1200	mV
t _r , t _f	Output Rise/Fall Times (20% to 80%) Q, /Q	70	120	170	80	130	180	100	150	200	ps

Notes:

25. Measured using a 750mV source, 50% duty cycle input. 50 Ω to V_{CC} -2V loading.
26. Skew is measured between outputs under identical transitions. It is defined only for differential operation where the delays are measured from the cross point of the inputs to the cross point of the outputs.

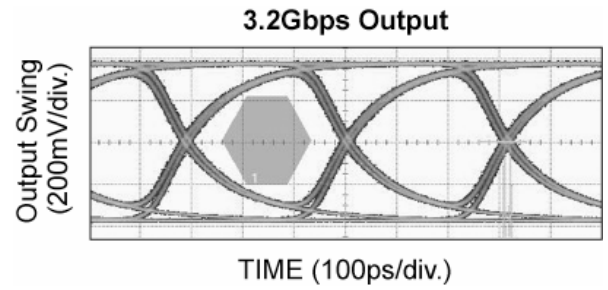
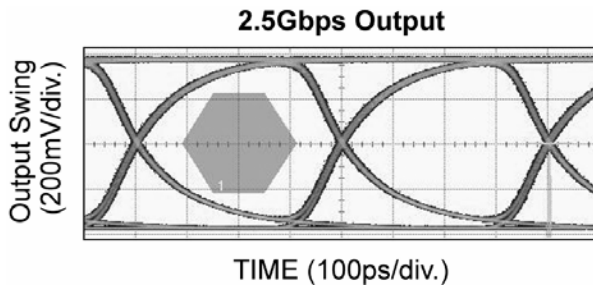
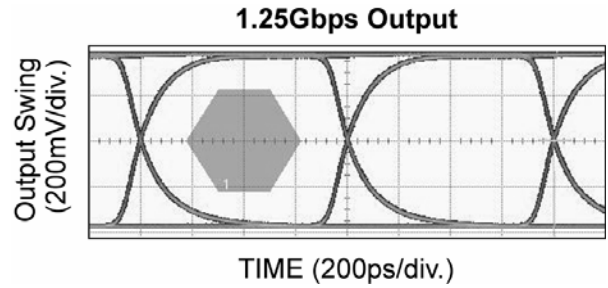
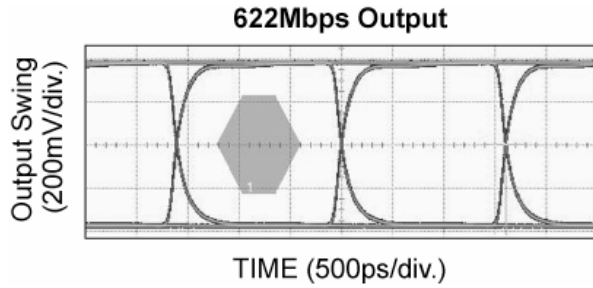
Typical Characteristics

$V_{CC} = 2.5V$, $GND = 0V$, $V_{IN} = 800mV$, $R_L = 50\Omega$ to $V_{CC}-2V$, $T_A = 25^\circ C$, unless otherwise stated.



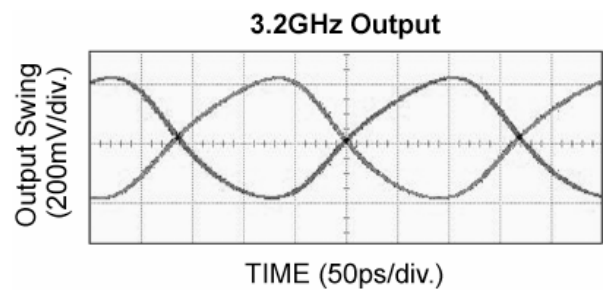
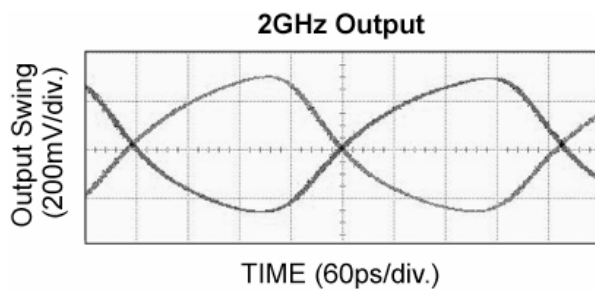
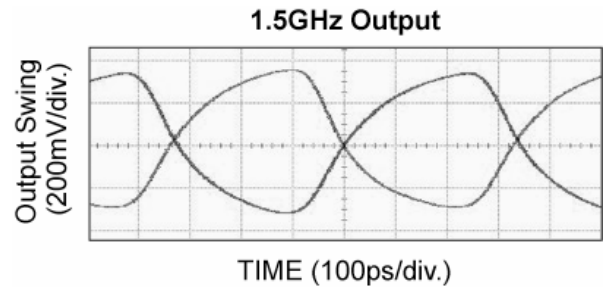
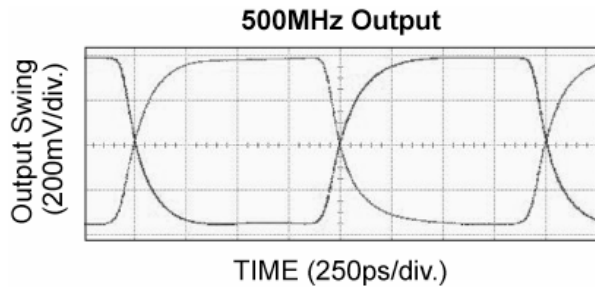
Functional Characteristics

$V_{CC} = 2.5V$, $GND = 0V$, 100k version, $V_{IN} = 150mV$, Data Pattern: $2^{23}-1$, $R_L = 50\Omega$ to $V_{CC}-2V$, $T_A = 25^\circ C$, unless otherwise stated.



Functional Characteristics (continued)

$V_{CC} = 2.5V$, $GND = 0V$, 100k version, $V_{IN} = 150mV$, $R_L = 50\Omega$ to $V_{CC}-2V$, $T_A = 25^\circ C$, unless otherwise stated.



Single-Ended and Differential Swings



Figure 1a. Single-Ended Swing

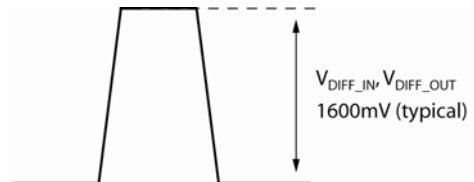


Figure 1b. Differential Swing

Output Interface Applications

ECL outputs have very low output impedance (open emitter), and small signal swing which results in low EMI. ECL is ideal for driving 50Ω-and-100Ω-controlled impedance transmission lines. There are several techniques in terminating the ECL output, as shown in Figure 2a and 2b.

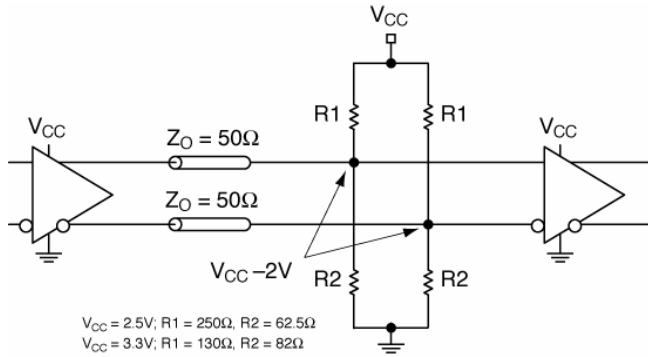


Figure 2a. Parallel Termination-Thevenin Equivalent

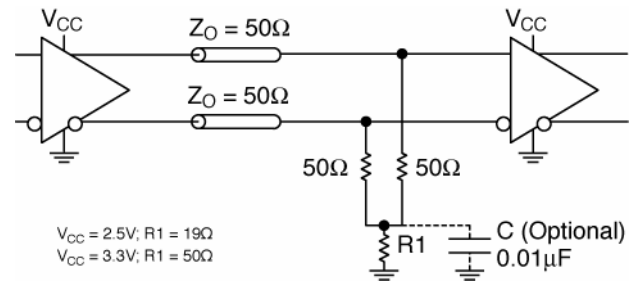
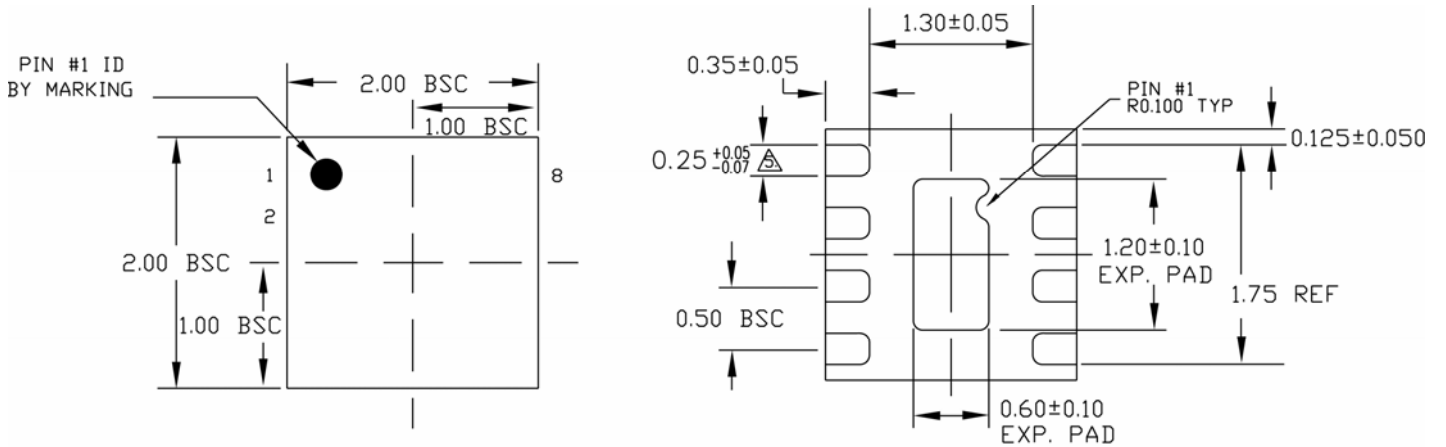


Figure 2b. Three-Resistor “Y-Termination”

Related Product and Support Documents

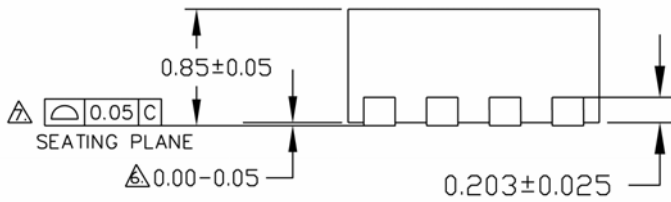
Part Number	Function	Datasheet Link
HBW Solutions	New Products and Termination Application Notes	http://www.micrel.com/page.do?page=/product-info/as/HBWsolutions.shtml

Package Information



TOP VIEW

BOTTOM VIEW

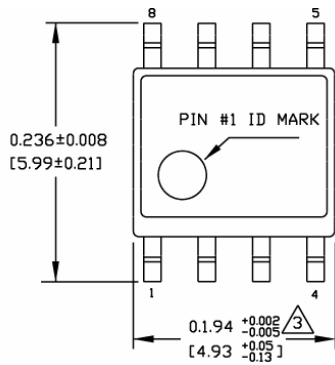


SIDE VIEW

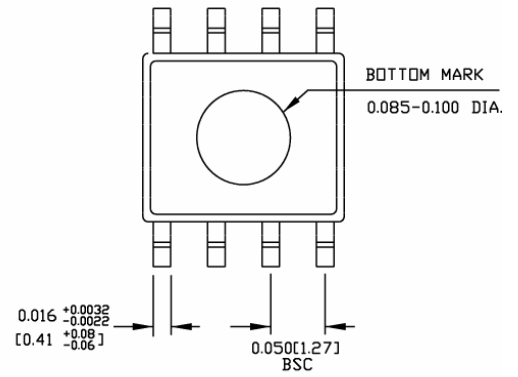
- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
 2. MAX. PACKAGE WARPAGE IS 0.05 mm.
 3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
 4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
- △ DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
- △ APPLIED ONLY FOR TERMINALS.
- △ APPLIED FOR EXPOSED PAD AND TERMINALS.

Rev. B

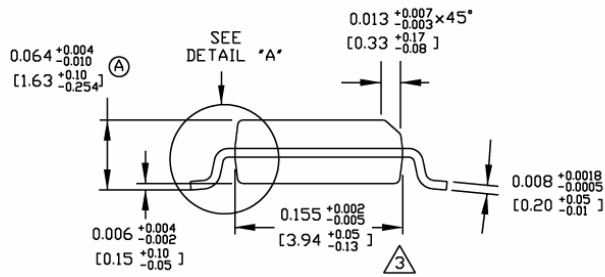
8-Pin (2mm x 2mm) MLF® (MLF-8)



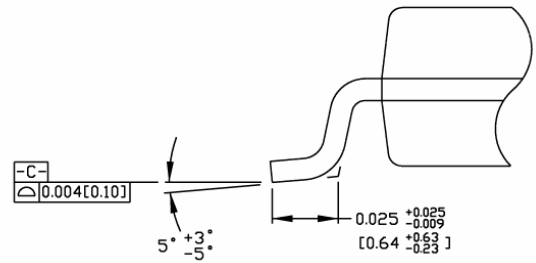
TOP VIEW



BOTTOM VIEW



END VIEW

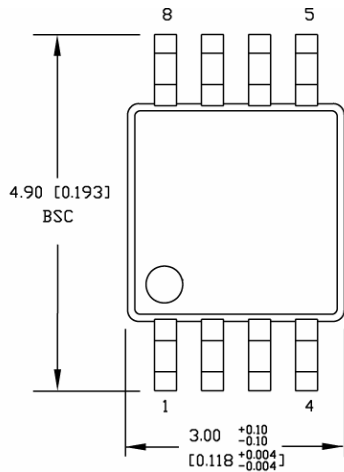


DETAIL "A"

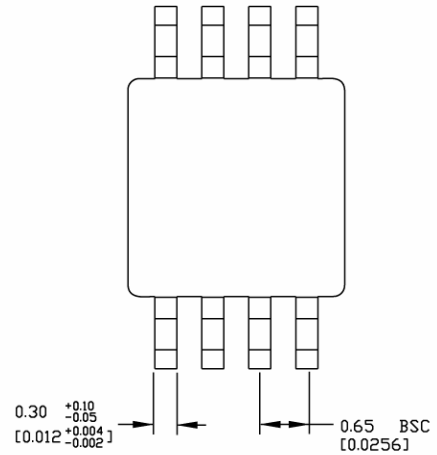
NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.010[0.25] PER SIDE.

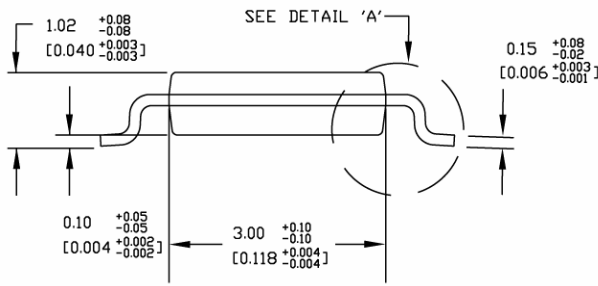
8-Pin SOIC (SOIC-8)



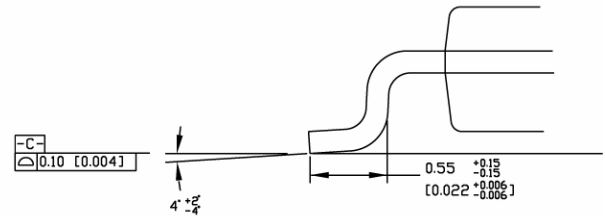
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL A

NOTES:

1. DIMENSIONS ARE IN MM [INCHES].
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.20 [0.008] PER SIDE.

8-Pin MSOP (MSOP-8)

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<http://moschip.ru/get-element>

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