

N-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^{b, c}	Q_g (Typ.)
60	0.010 at $V_{GS} = 10$ V	16	45
	0.0125 at $V_{GS} = 6$ V	14.4	

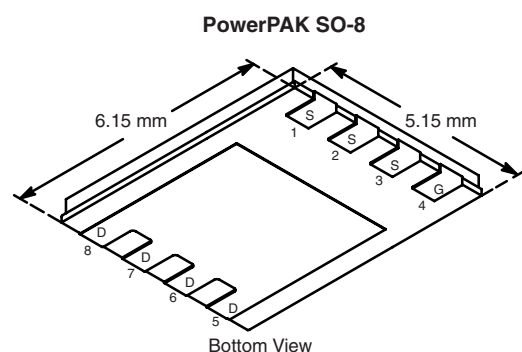
FEATURES

- Halogen-free
- TrenchFET[®] Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested


RoHS
COMPLIANT

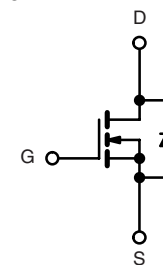
APPLICATIONS

- Primary Side Switch for 24 V DC/DC Applications
- Secondary Synchronous Rectifier



Bottom View

Ordering Information: Si7370ADP-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C)	$T_C = 25$ °C	I_D	50 ^a	A
	$T_C = 70$ °C		50 ^a	
	$T_A = 25$ °C		16 ^{b, c}	
	$T_A = 70$ °C		12.9 ^{b, c}	
Pulsed Drain Current		I_{DM}	50	A
Continuous Source-Drain Diode Current	$T_C = 25$ °C	I_S	50 ^a	
	$T_A = 25$ °C		4.4 ^{b, c}	
Avalanche Current		I_{AS}	50	mJ
Single Pulse Avalanche Energy		E_{AS}	125	
Maximum Power Dissipation	$T_C = 25$ °C	P_D	69.4	W
	$T_C = 70$ °C		44.4	
	$T_A = 25$ °C		5.2 ^{b, c}	
	$T_A = 70$ °C		3.3 ^{b, c}	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}			260	

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	$t \leq 10$ s	R_{thJA}	19	24	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.5	1.8	

Notes:

a. Package Limited.

b. Surface Mounted on 1" x 1" FR4 board.

c. $t = 10$ s.

d. See Solder Profile (<http://www.vishay.com/ppg?73461>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

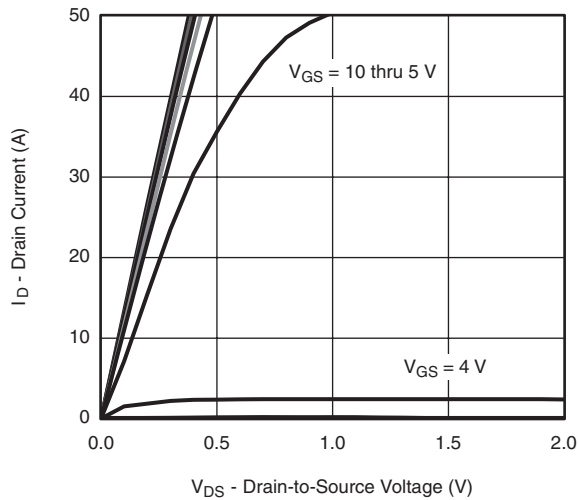
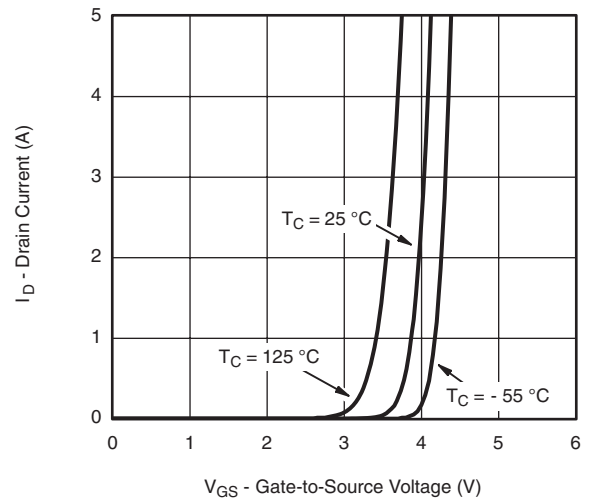
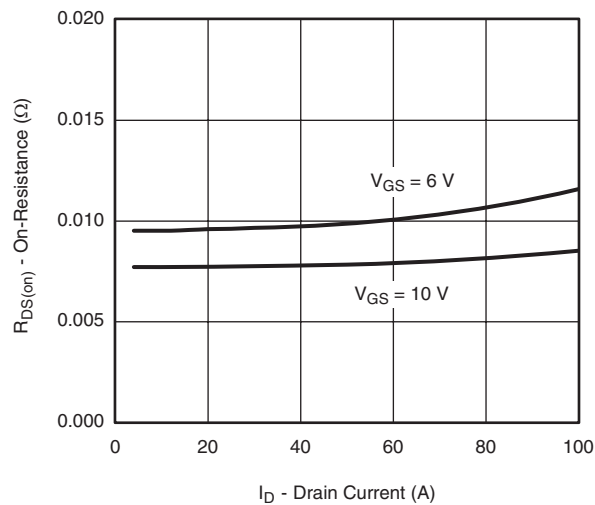
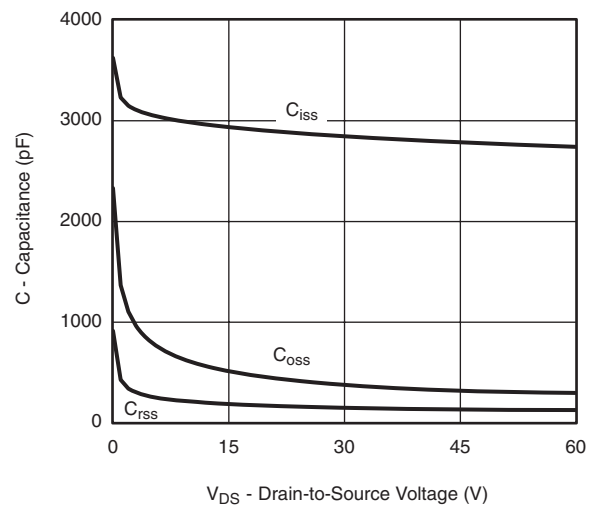
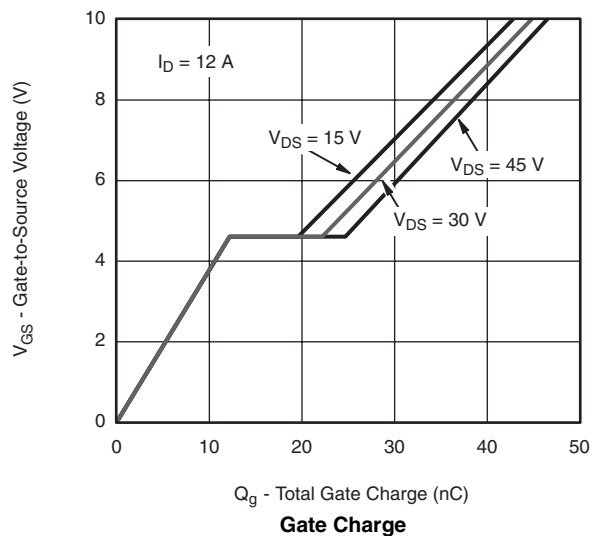
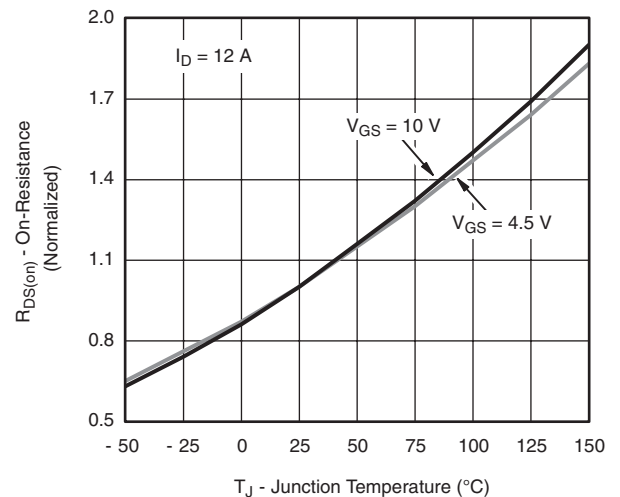
f. Maximum under Steady State conditions is 65 °C/W.

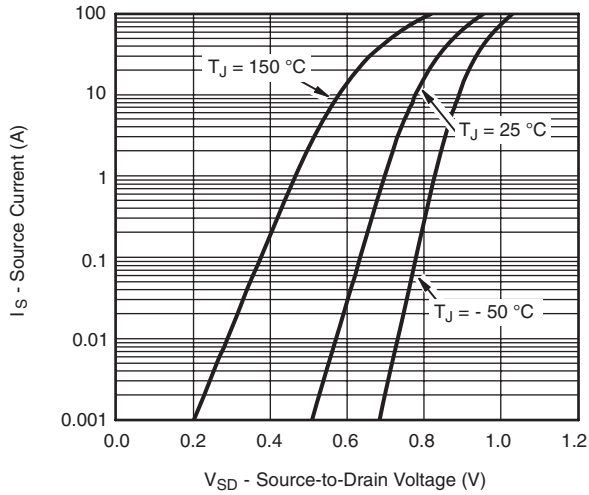
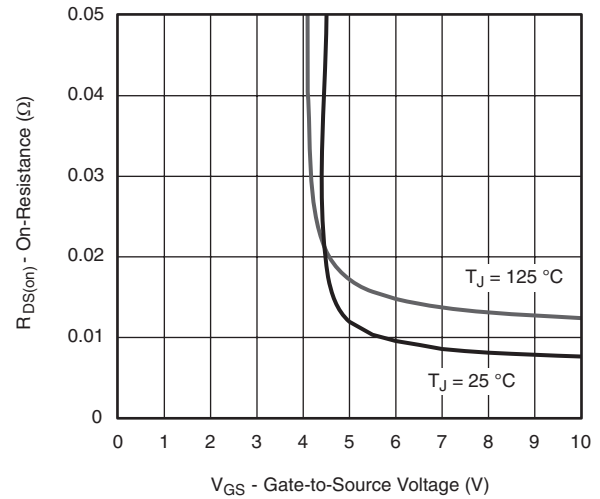
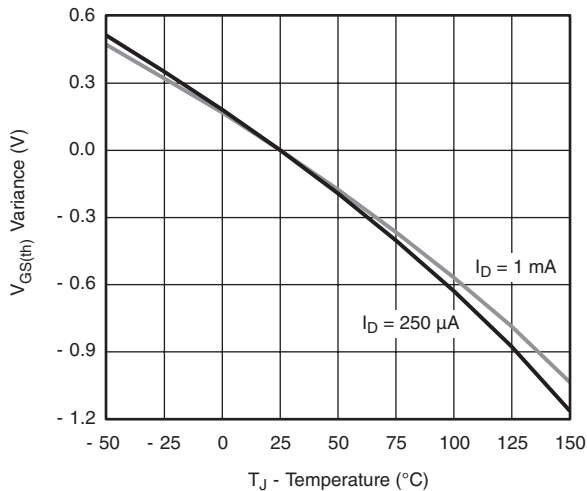
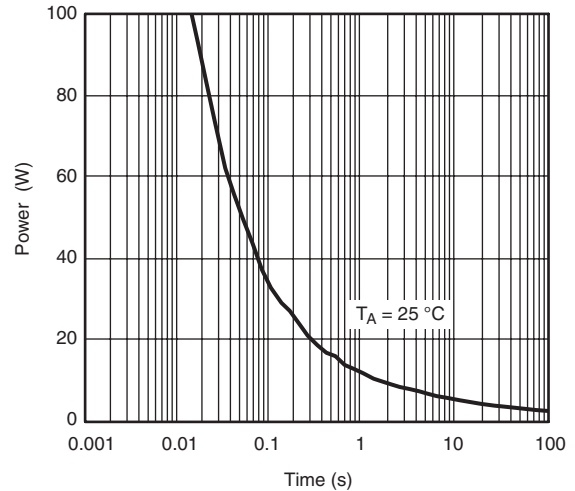
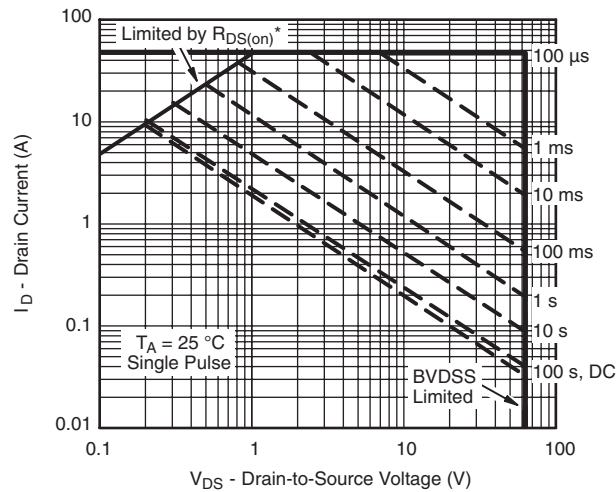
SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	60			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		60		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 9.8		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2.0		4.5	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V			1	μA
		V _{DS} = 60 V, V _{GS} = 0 V, T _J = 55 °C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	50			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 12 A		0.008	0.010	Ω
		V _{GS} = 6 V, I _D = 10 A		0.010	0.0125	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 10 A		50		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 30 V, V _{GS} = 0 V, f = 1 MHz		2850		pF
Output Capacitance	C _{oss}			375		
Reverse Transfer Capacitance	C _{rss}			150		
Total Gate Charge	Q _g	V _{DS} = 30 V, V _{GS} = 10 V, I _D = 12 A		45	70	nC
Gate-Source Charge	Q _{gs}			12.2		
Gate-Drain Charge	Q _{gd}			10		
Gate Resistance	R _g	f = 1 MHz	0.2	0.75	1.5	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 30 V, R _L = 30 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _g = 1 Ω		20	30	ns
Rise Time	t _r			9	18	
Turn-Off Delay Time	t _{d(off)}			40	60	
Fall Time	t _f			20	30	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 30 V, R _L = 30 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _g = 1 Ω		25	40	
Rise Time	t _r			14	25	
Turn-Off Delay Time	t _{d(off)}			35	55	
Fall Time	t _f			20	30	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			50	A
Pulse Diode Forward Current ^a	I _{SM}				50	
Body Diode Voltage	V _{SD}	I _S = 3 A		0.75	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 3 A, dI/dt = 100 A/μs, T _J = 25 °C		35	60	ns
Body Diode Reverse Recovery Charge	Q _{rr}			45	70	nC
Reverse Recovery Fall Time	t _a			22		ns
Reverse Recovery Rise Time	t _b			13		

Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

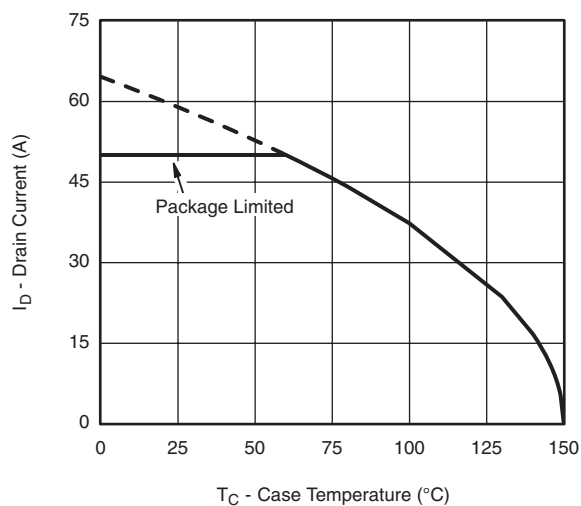
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current and Gate Voltage****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

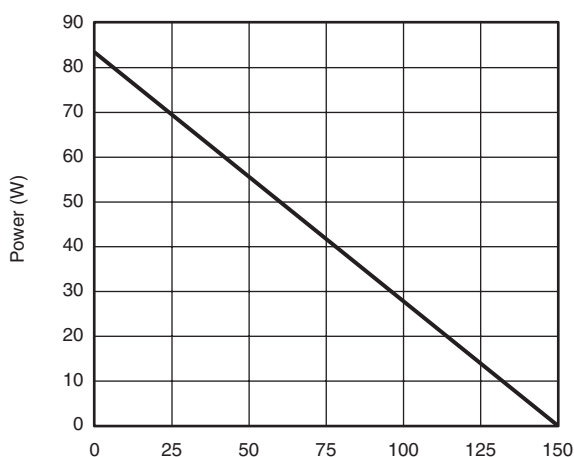
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power, Junction-to-Ambient*** $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified**Safe Operating Area, Junction-to-Ambient**



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

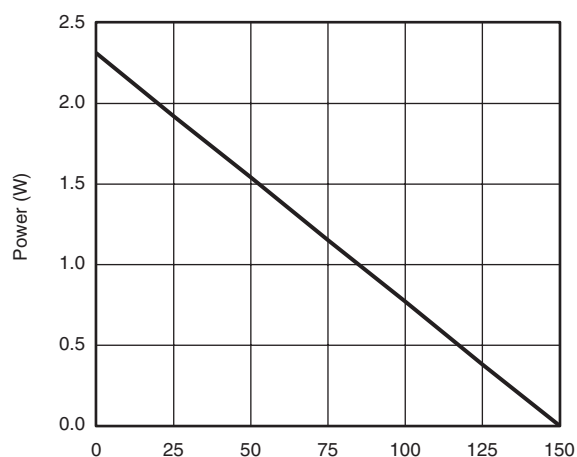


Current Derating*



T_J - Junction Temperature (°C)

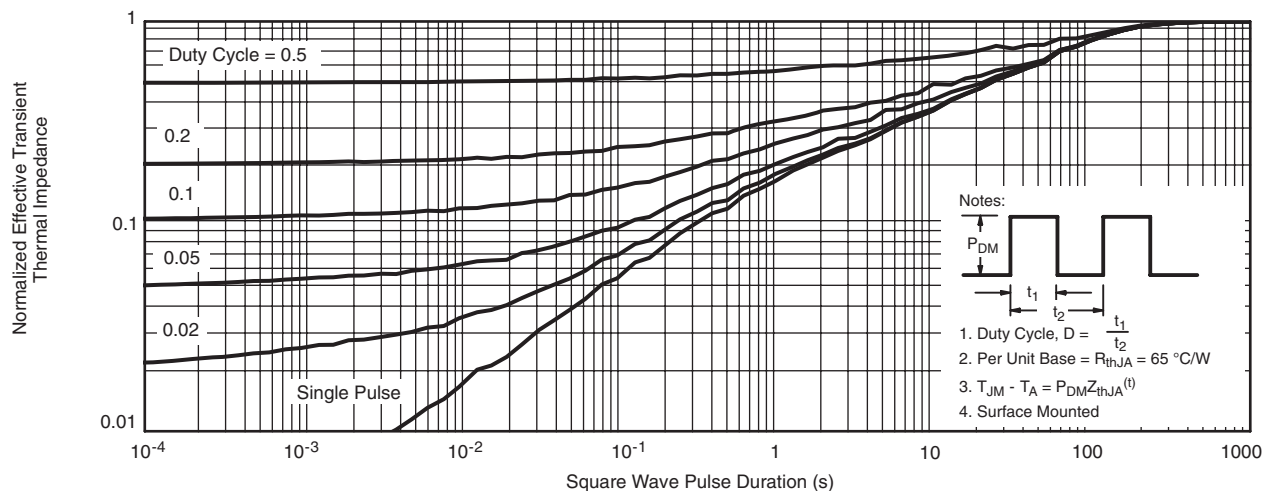
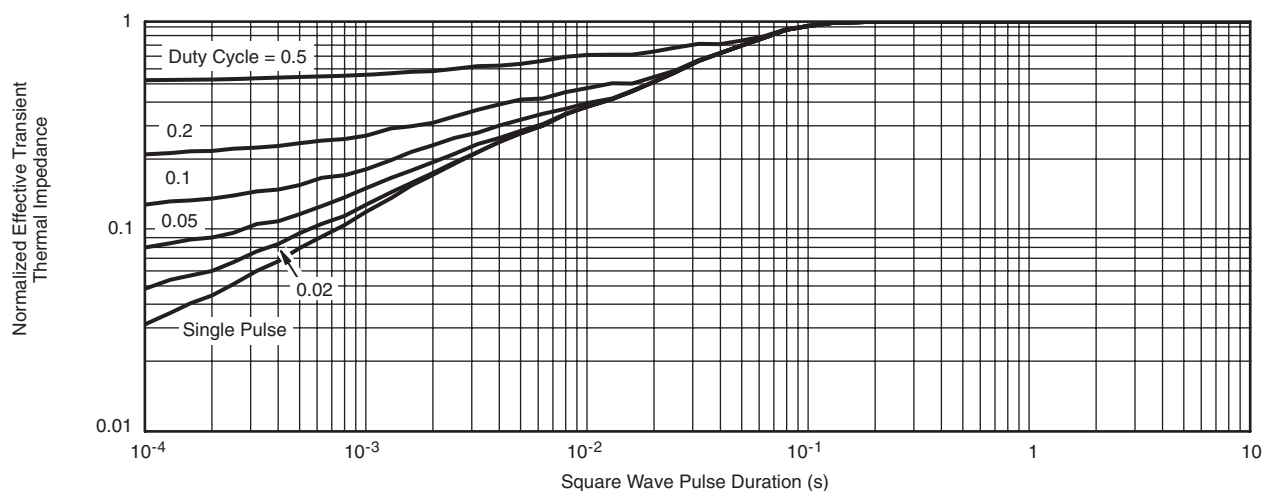
Power, Junction-to-Case



T_J - Junction Temperature (°C)

Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case**

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