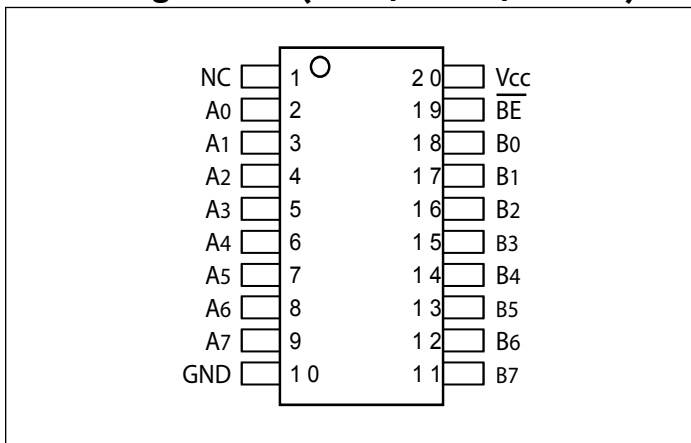


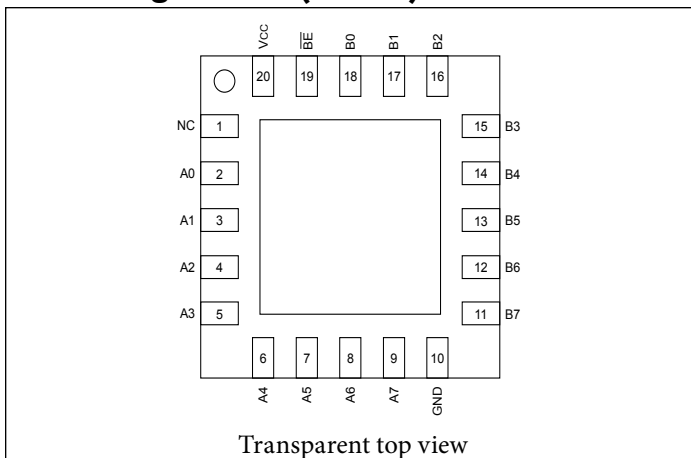
Features

- Near-Zero propagation delay
- 5-ohm switches connect inputs to outputs
- Fast Switching Speed: 4.5ns (max.)
- Ultra-Low Quiescent Power (0.2µA Typical)
 - Ideally suited for notebook applications
- TTL-compatible control of inputs levels
- ESD protection (2kV Human Body Model and 200V Machine Model)
- Packaging (Pb-free & Green):
 - 20-pin SOIC (S)
 - 20-pin QSOP (Q)
 - 20-pin UQFN (ZUA)
 - 20-pin TSSOP (L)

Pin Configuration (SOIC, QSOP, TSSOP)



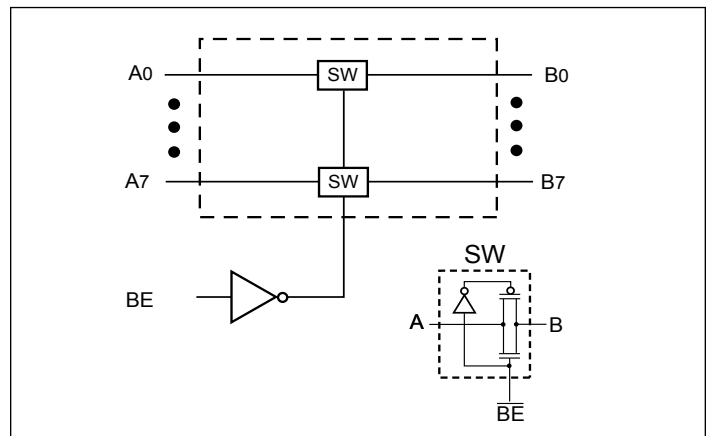
Pin Configuration (UQFN)



Description

The PI3B3245 is a 3.3V 8-bit, 2-port bus switch designed with a low On-Resistance (5-ohm) allowing inputs to be connected directly to outputs. The bus switch creates no additional propagational delay or additional ground bounce noise. The switches are turned ON by the Bus Enable (\overline{BE}) input signal.

Block Diagram



Truth Table

Function	\overline{BE}	A0-7
Disconnect	H	Hi-Z
Connect	L	B0-7

Note:

H = High Voltage Level, L = Low Voltage Level, Hi-Z = High Impedance

Pin Description

Pin Name	Description
\overline{BE}	Bus Enable Input (Active LOW)
A0-7	Bus A
B0-7	Bus B
GND	Ground ⁽¹⁾
V _{CC}	Power

Note 1: UQFN20 package die supply ground is connected to both GND pin and exposed center pad. GND pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region.

Absolute Maximum Ratings

Parameter	Min.	Max.	Units
Storage Temperature	-65	150	°C
Ambient Temperature with Power Applied	-40	85	°C
Supply Voltage to Ground Potential	-0.5	4.6	V
DC Input Voltage	-0.5	4.6	V
DC Output Current	-	120	mA
Power Dissipation	-	0.5	W

Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 3.3\text{V} \pm 10\%$)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level	-0.5		0.8	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}, V_{IN} = V_{CC}$			± 1	μA
I_{IL}	Input LOW Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND}$			± 1	μA
I_{OZH}	High Impedance Output Current	$0 \leq A_N, B_N \leq V_{CC}$			± 1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18 \text{ mA}$			-1.2	V
R_{ON}	Switch On Resistance ⁽³⁾	$V_{CC} = \text{Min.}, V_{IN} = 0.0\text{V}, I_{ON} = 48\text{mA}$ or 64mA		5	8	Ω
		$V_{CC} = \text{Min.}, V_{IN} = 2.4\text{V}, I_{ON} = 15\text{mA}$		10	17	

Notes:

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 3.3\text{V}$, $T_A = 25^{\circ}\text{C}$ ambient and maximum loading.
- Measured by the voltage drop between A and B pin at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A,B) pins.

Capacitance ($T_A = 25^{\circ}\text{C}$, $f = 1 \text{ MHz}$)

Parameters ⁽¹⁾	Description	Test Conditions	Typ.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	3.0	pF
C_{OFF}	A/B Capacitance, Switch Off	$V_{IN} = 0\text{V}$	8.0	pF
C_{ON}	A/B Capacitance, Switch On	$V_{IN} = 0\text{V}$	16.0	pF

Notes:

- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Units
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$	$V_{IN} = \text{GND or } V_{CC}$		0.1	3.0	μA
ΔI_{CC}	Supply Current per Input HIGH	$V_{CC} = \text{Max.}$	$V_{IN} = 3.0\text{V}^{(3)}$			750	μA

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at $V_{CC} = 3.3\text{V}$, $+25^\circ\text{C}$ ambient.
3. Per TTL driven input (control input only); A and B pins do not contribute to I_{CC} .

Switching Characteristics over Operating Range

Parameters	Description	Test Conditions	Com.		Units
			Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay ^(1,2) Ax to Bx, Bx to Ax	CL = 50 pF RL = 500Ω		0.25	ns
t_{PZH} t_{PZL}	Bus Enable Time $\overline{\text{BE}}$ to Ax or Bx		1.0	4.0	
t_{PHZ} t_{PLZ}	Bus Disable Time $\overline{\text{BE}}$ to Ax or Bx		1.0	4.5	

Notes:

1. This parameter is guaranteed but not tested on Propagation Delays.
2. The bus switch contributes no propagational delay other than the RC delay of the On-Resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

Applications Information

Logic Inputs

The logic control inputs can be driven up to +3.6V regardless of the supply voltage. For example, given a + 3.3V supply, A_N may be driven low to 0V and high to 3.6V. Driving B_N Rail-to-Rail® minimizes power consumption.

Power-Supply Sequencing and Hot-Plug Information

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V_{CC} and GND before applying signals to input/output or control pins.

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

PI3B3245

Part Marking

S Package



YY: Year
WW: Workweek
1st X: Assembly Site Code
2nd X: Wafer Fab Site Code

Q Package



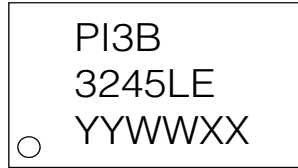
YY: Year
WW: Workweek
1st X: Assembly Site Code
2nd X: Fab Site Code
Bar above fab code means Cu wire
Without bar above fab code means Au wire

ZUA Package



YY: Year
WW: Workweek
1st X: Assembly Site Code
2nd X: Fab Site Code

L Package



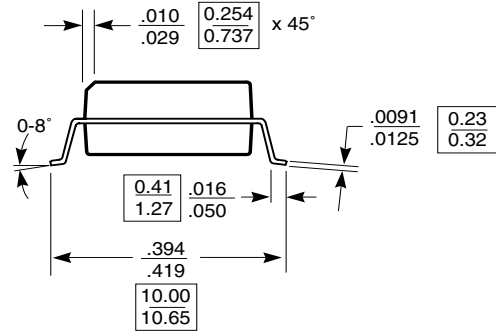
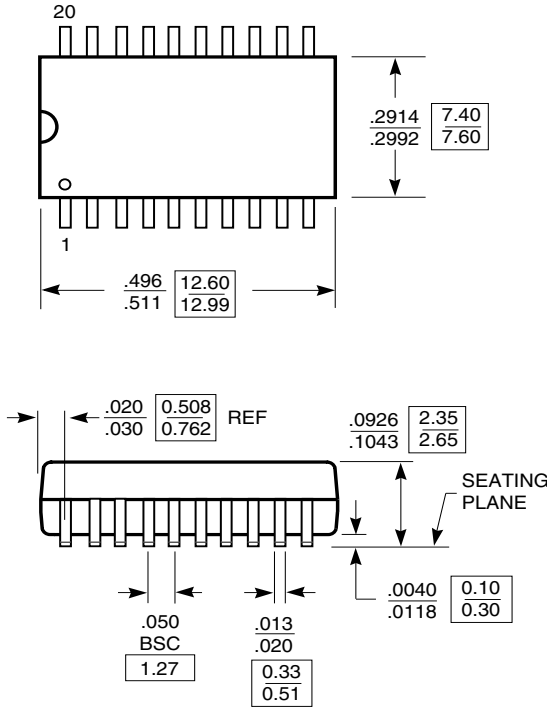
YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

PI3B3245

Packaging Mechanical: 20-SOIC (S)

DOCUMENT CONTROL NO.
PD - 1006

REVISION: D
DATE: 03/09/05



X.XX DENOTES CONTROLLING
X.XX DIMENSIONS IN MILLIMETERS

Notes:
 1) Controlling dimensions in millimeters.
 2) Ref: JEDEC MS-013D/AC



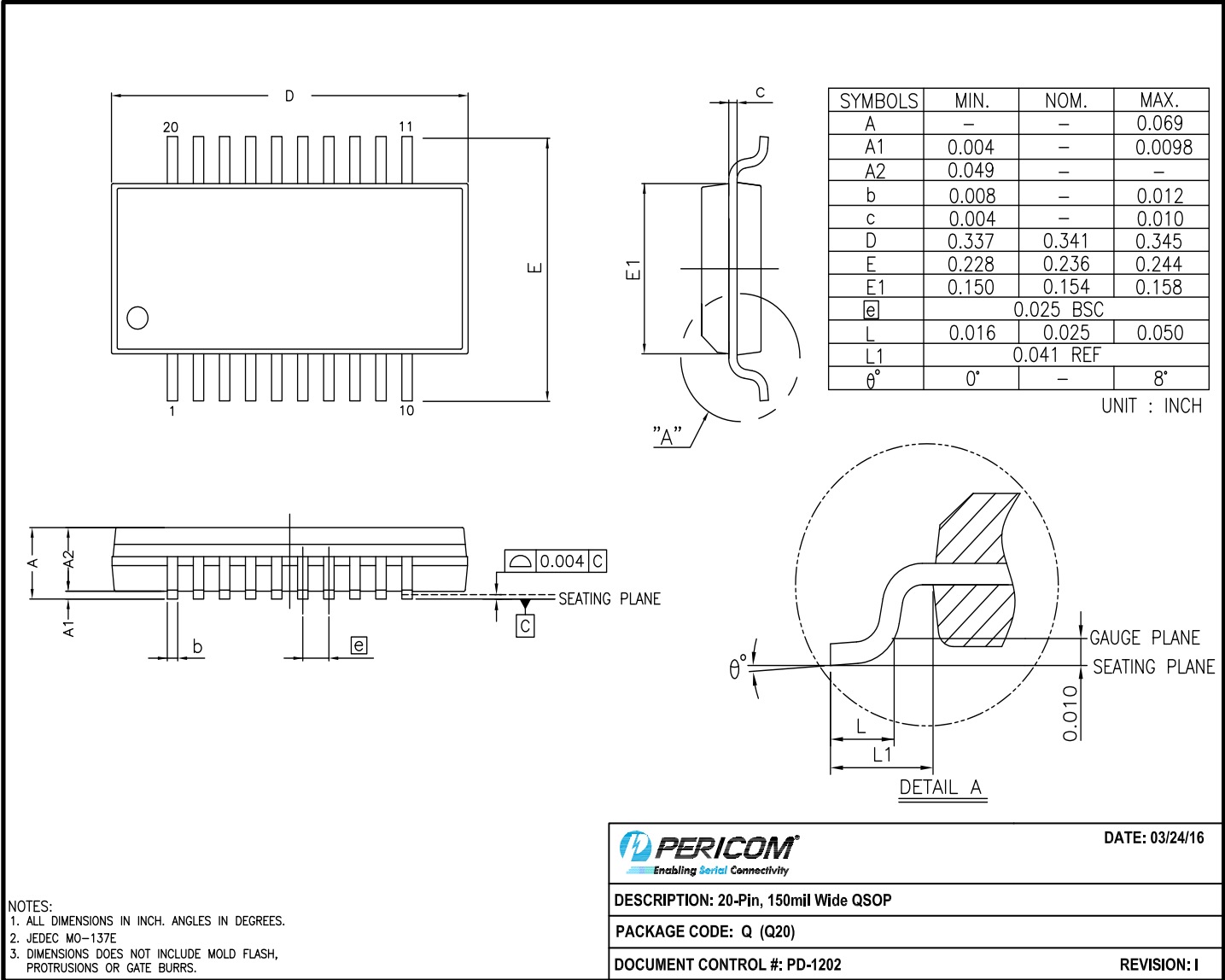
Pericom Semiconductor Corporation
 3545 N. 1st Street, San Jose, CA 95134
 1-800-435-2335 • www.pericom.com

DESCRIPTION: 20-Pin, 300-Mil Wide, SOIC

PACKAGE CODE: S

PI3B3245

Packaging Mechanical: 20-QSOP (Q)



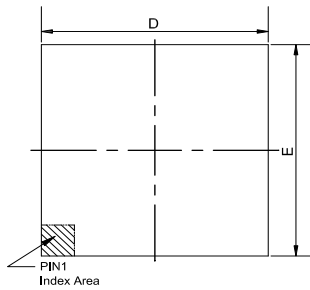
NOTES:
 1. ALL DIMENSIONS IN INCH. ANGLES IN DEGREES.
 2. JEDEC MO-137E
 3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

		DATE: 03/24/16
DESCRIPTION: 20-Pin, 150mil Wide QSOP		
PACKAGE CODE: Q (Q20)		
DOCUMENT CONTROL #: PD-1202	REVISION: I	

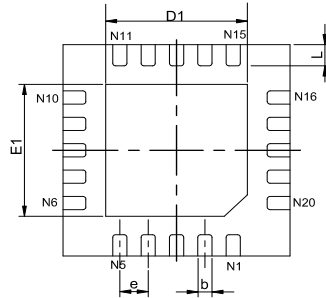
16-0057

PI3B3245

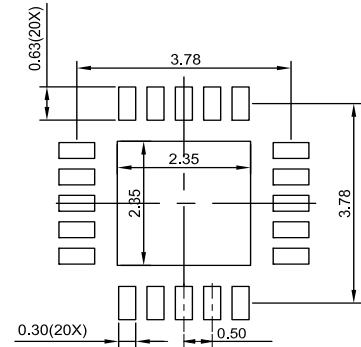
Packaging Mechanical: 20-UQFN (ZUA)



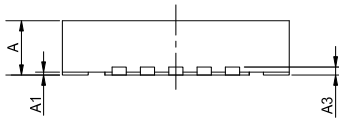
TOP VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN(unit:mm)



SIDE VIEW

PKG. DIMENSIONS(MM)			
SYMBOL	Min	NOM	Max
A	0.55	0.60	0.65
A1	0.00	0.02	0.05
A3	0.15 REF		
D	3.95	4.00	4.05
E	3.95	4.00	4.05
D1	2.40	2.50	2.60
E1	2.40	2.50	2.60
b	0.20	0.25	0.30
e	0.50 BSC		
L	0.35	0.40	0.45

Note:

1. Comly with JEDEC MO-248K, except 'A3', 'D1' and 'E1'.

PI3B3245

Packaging Mechanical: 20-TSSOP (L)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
C	0.09	—	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	—	—
θ	0°	—	8°

NOTES:
 1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.
 2. JEDEC MO-153F
 3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

PERICOM
Enabling Serial Connectivity

DATE: 03/31/16

DESCRIPTION: 20-Pin, 173mil Wide TSSOP

PACKAGE CODE: L (L20)

DOCUMENT CONTROL #: PD-1311

REVISION: G

16-0074

For latest package info.

please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

Ordering Information

Ordering Code	Package Code	Package Type
PI3B3245SEX	S	20-pin, 300Mil Wide (SOIC)
PI3B3245QEX	Q	20-pin, 150mil Wide (QSOP)
PI3B3245ZUAEX	ZUA	20-pin, 4x4 (UQFN)
PI3B3245LEX	L	20-pin, 173mil Wide (TSSOP)

Notes:

- EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
- See <http://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free. Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel

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