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**July 2016** 

## FDMT80040DC

# N-Channel Dual Cool<sup>TM</sup> 88 PowerTrench<sup>®</sup> MOSFET 40 V, 420 A, 0.56 m $\Omega$

#### **Features**

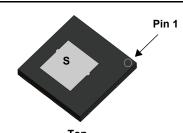
- Max  $r_{DS(on)}$  = 0.56 m $\Omega$  at  $V_{GS}$  = 10 V,  $I_D$  = 64 A
- Max  $r_{DS(on)} = 0.9 \text{ m}\Omega$  at  $V_{GS} = 6 \text{ V}$ ,  $I_D = 47 \text{ A}$
- Advanced Package and Silicon Combination for Low r<sub>DS(on)</sub> and High Efficiency
- Next Generation Enhanced Body Diode Technology, Engineered for Soft Recovery
- Low Profile 8x8mm MLP Package
- MSL1 Robust Package Design
- 100% UIL Tested
- RoHS Compliant

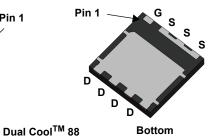
### **General Description**

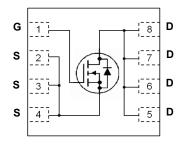
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process. Advancements in both silicon and Dual Cool  $^{TM}$  package technologies have been combined to offer the lowest  $r_{DS(on)}$  while maintaining excellent switching performance by extremely low Junction-to-Ambient thermal resistance.

### **Applications**

- OringFET / Load Switching
- Synchronous Rectification
- DC-DC Conversion







## **MOSFET Maximum Ratings** $T_A = 25$ °C unless otherwise noted.

Symbol	Paramo	eter		Ratings	Units
$V_{DS}$	Drain to Source Voltage			40	V
$V_{GS}$	Gate to Source Voltage			±20	V
	Drain Current -Continuous	T <sub>C</sub> = 25 °C	(Note 5)	420	
	-Continuous	T <sub>C</sub> = 100 °C	(Note 5)	265	Λ.
ID	-Continuous	T <sub>A</sub> = 25 °C	(Note 1a)	64	A
	-Pulsed		(Note 4)	2644	
E <sub>AS</sub>	Single Pulse Avalanche Energy		(Note 3)	2773	mJ
В	Power Dissipation	T <sub>C</sub> = 25 °C		156	W
$P_{D}$	Power Dissipation	T <sub>A</sub> = 25 °C	(Note 1a)	3.2	VV
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Tempera	ture Range		-55 to +150	°C

#### **Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Top Source)	1.6	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Bottom Drain)	0.8	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	81	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1i)	15	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1j)	21	
$R_{\theta,JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1k)	9	

#### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
80040DC	FDMT80040DC	Dual Cool <sup>TM</sup> 88	13"	13.3 mm	3000 units

# **Electrical Characteristics** $T_J$ = 25 $^{\circ}$ C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
Off Chara	acteristics					
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 μA, referenced to 25 °C		21		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 32 V, V <sub>GS</sub> = 0 V			10	μΑ
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±100	nA

#### **On Characteristics**

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	2.0	2.7	4.0	V
$\Delta V_{GS(th)}$ $\Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25 °C		-9		mV/°C
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 64 A		0.44	0.56	
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 6 V, I <sub>D</sub> = 47 A		0.63	0.9	mΩ
, ,		$V_{GS} = 10 \text{ V}, I_D = 64 \text{ A}, T_J = 125 ^{\circ}\text{C}$		0.66	0.84	
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 64 A		278		S

#### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V = 20 V V = 0 V		18650	26110	pF	l
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, f = 1 MHz		5540	7760	pF	1
C <sub>rss</sub>	Reverse Transfer Capacitance			304	1210	pF	1
$R_{\alpha}$	Gate Resistance		0.1	1.8	3.6	Ω	1

#### **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time			63	101	ns
t <sub>r</sub>	Rise Time	V <sub>DD</sub> = 20 V, I <sub>D</sub> = 64	1 A,	62	100	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	V <sub>GS</sub> = 10 V, R <sub>GEN</sub>	= 6 Ω	101	162	ns
t <sub>f</sub>	Fall Time			43	69	ns
$Q_{g(TOT)}$	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V		241	338	nC
$Q_{g(TOT)}$	Total Gate Charge	V <sub>GS</sub> = 0 V to 6 V	V <sub>DD</sub> = 20 V,	149	209	nC
Q <sub>gs</sub>	Gate to Source Charge		I <sub>D</sub> = 64 A	76		nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge			35		nC

#### **Drain-Source Diode Characteristics**

V	Source to Drain Diode Forward Voltage	$V_{GS} = 0 V, I_S = 2.6 A$ (Note 2)	0.67	1.1	V
$V_{SD}$	Source to Drain Diode 1 of ward voltage	$V_{GS} = 0 \text{ V}, I_S = 64 \text{ A}$ (Note 2)	0.77	1.2	'
t <sub>rr</sub>	Reverse Recovery Time	I <sub>E</sub> = 64 A, di/dt = 100 A/μs	94	151	ns
Q <sub>rr</sub>	Reverse Recovery Charge	ης – 04 A, αναι – 100 Ανμs	219	351	nC

#### **Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Top Source)	1.6	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Bottom Drain)	0.8	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1c)	26	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1d)	34	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1e)	14	°C // //
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1f)	16	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1g)	26	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1h)	60	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1i)	15	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1j)	21	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1k)	9	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1I)	11	

#### NOTES

1. R<sub>8JA</sub> is determined with the device mounted on a FR-4 board using a specified pad of 2 oz copper as shown below. R<sub>8CA</sub> is determined by the user's board design.



a. 38 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 81 °C/W when mounted on a minimum pad of 2 oz copper

- c. Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in  $^2$  pad of 2 oz copper
- d. Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper
- e. Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- f. Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
- g. 200FPM Airflow, No Heat Sink,1 in<sup>2</sup> pad of 2 oz copper
- h. 200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper
- i. 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in  $^2$  pad of 2 oz copper
- j. 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper
- $k.\ 200 FPM\ Airflow,\ 45.2x41.4x11.7mm\ Aavid\ Thermalloy\ Part\ \#\ 10-L41B-11\ Heat\ Sink,\ 1\ in^2\ pad\ of\ 2\ oz\ copper$
- I. 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
- 2. Pulse Test: Pulse Width < 300  $\mu$ s, Duty cycle < 2.0%.
- 3.  $E_{AS}$  of 2773mJ is based on starting  $T_J$  = 25 °C; N-ch: L = 3 mH,  $I_{AS}$  = 43 A,  $V_{DD}$  = 40 V,  $V_{GS}$  = 10 V. 100% test at L = 0.3 mH,  $I_{AS}$  = 93 A.
- 4. Pulsed Id please refer to Fig 11 SOA graph for more details.
- 5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

#### Typical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted.

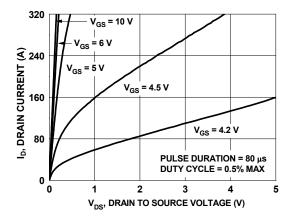


Figure 1. On Region Characteristics

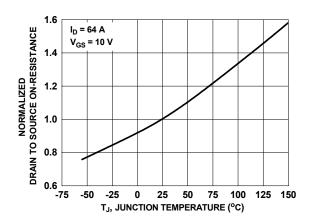


Figure 3. Normalized On Resistance vs. Junction Temperature

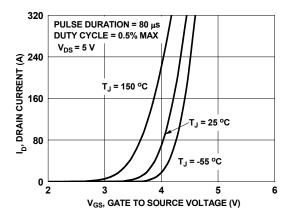


Figure 5. Transfer Characteristics

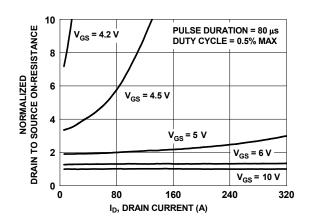


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

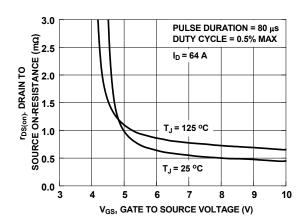


Figure 4. On-Resistance vs. Gate to Source Voltage

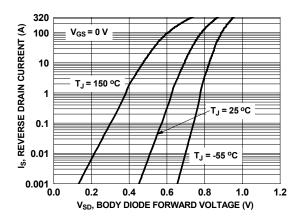


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

# Typical Characteristics $T_J$ = 25 °C unless otherwise noted.

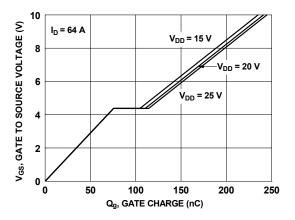


Figure 7. Gate Charge Characteristics

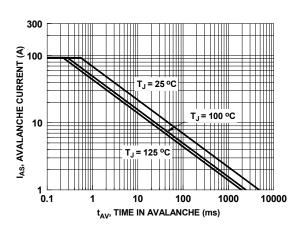


Figure 9. Unclamped Inductive Switching Capability

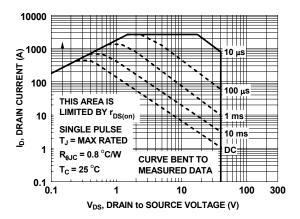


Figure 11. Forward Bias Safe Operating Area

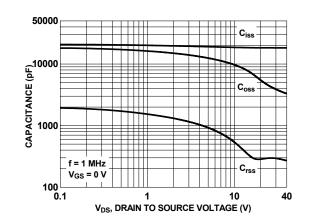


Figure 8. Capacitance vs Drain to Source Voltage

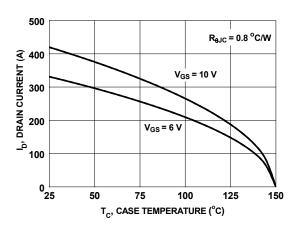


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

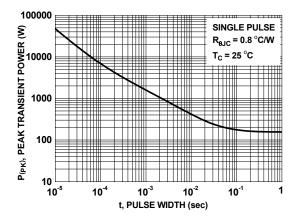


Figure 12. Single Pulse Maximum Power Dissipation

## **Typical Characteristics** $T_J = 25$ °C unless otherwise noted.

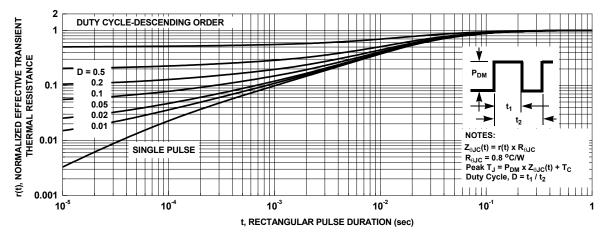
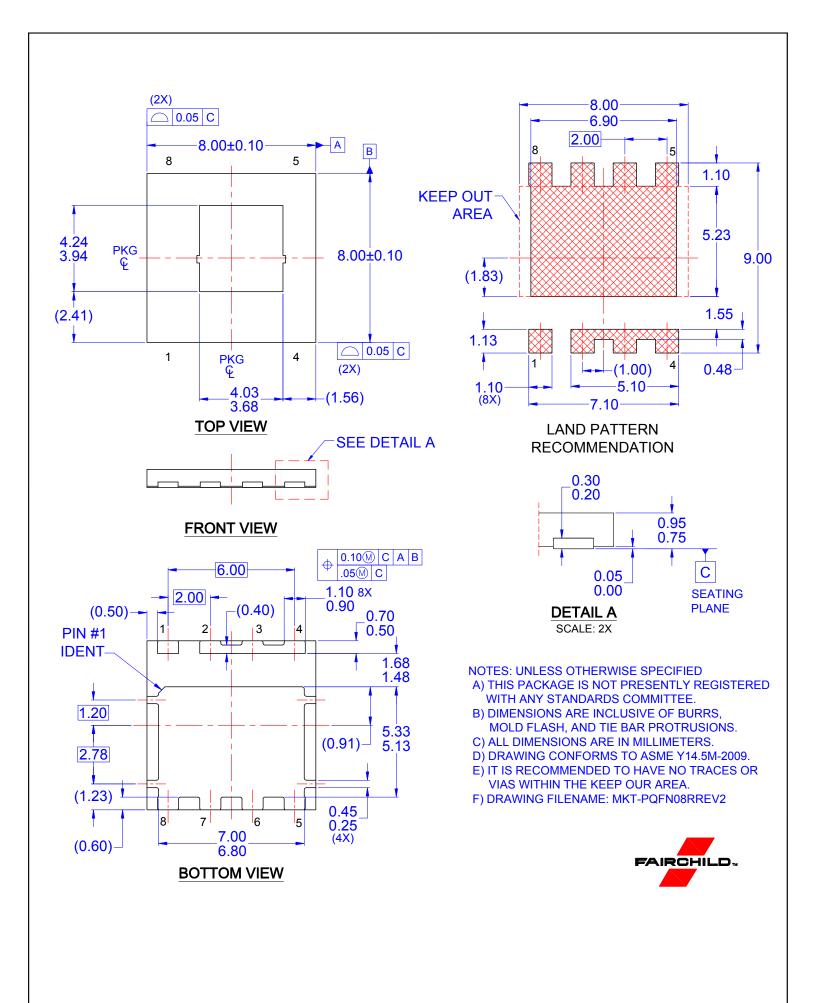


Figure 13. Junction-to-Case Transient Thermal Response Curve



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