2N6284 (NPN); 2N6286, 2N6287 (PNP)

Preferred Device

Darlington Complementary Silicon Power Transistors

These packages are designed for general−purpose amplifier and low−frequency switching applications.

Features

- High DC Current Gain @ I_C = 10 Adc −
  h_{FE} = 2400 (Typ) − 2N6284
  = 4000 (Typ) − 2N6287
- Collector−Emitter Sustaining Voltage −
  $V_{CEO(sus)}$ = 100 Vdc (Min)
- Monolithic Construction with Built−In Base−Emitter Shunt Resistors
- Pb−Free Packages are Available*

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage 2N6286 2N6284/87	V_{CEO}	80 100	Vdc
Collector−Base Voltage 2N6286 2N6284/87	V_{CB}	80 100	Vdc
Emitter−Base Voltage	V_{EB}	5.0	Vdc
Collector Current − Continuous Peak	I_C	20 40	Adc
Base Current	I_B	0.5	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	160 0.915	W W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS (Note 1)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.09	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. Indicates JEDEC Registered Data.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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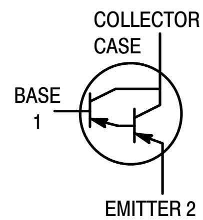
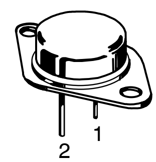
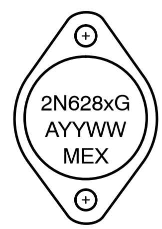
20 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 100 VOLTS, 160 WATTS



MARKING DIAGRAM



TO−204AA (TO−3)
CASE 1−07
STYLE 1



2N628x	=	Device Code x = 4, 6 or 7
G	=	Pb−Free Package
A	=	Location Code
YY	=	Year
WW	=	Work Week
MEX	=	Country of Orgin

ORDERING INFORMATION

Device	Package	Shipping
2N6284	TO−3	100 Units/Tray
2N6284G	TO−3 (Pb−Free)	100 Units/Tray
2N6286	TO−3	100 Units/Tray
2N6286G	TO−3 (Pb−Free)	100 Units/Tray
2N6287	TO−3	100 Units/Tray
2N6287G	TO−3 (Pb−Free)	100 Units/Tray

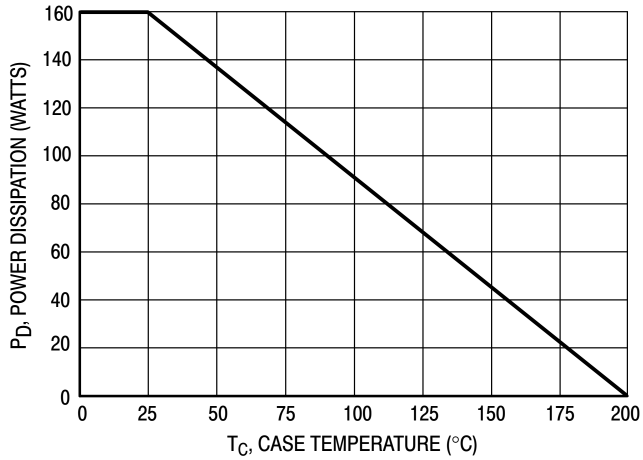


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted) (Note 2)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (I_C = 0.1 Adc, I_B = 0) 2N6286 / 2N6284, 2N6287	$V_{CEO(sus)}$	80 / 100	– / –	Vdc
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0) / (V_{CE} = 50 Vdc, I_B = 0)	I_{CEO}	– / –	1.0 / 1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) / (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	– / –	0.5 / 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS (Note 3)				
DC Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc) / (I_C = 20 Adc, V_{CE} = 3.0 Vdc)	h_{FE}	750 / 100	18,000 / –	–
Collector−Emitter Saturation Voltage (I_C = 10 Adc, I_B = 40 mAdc) / (I_C = 20 Adc, I_B = 200 mAdc)	$V_{CE(sat)}$	– / –	2.0 / 3.0	Vdc
Base−Emitter On Voltage (I_C = 10 Adc, V_{CE} = 3.0 Vdc)	$V_{BE(on)}$	–	2.8	Vdc
Base−Emitter Saturation Voltage (I_C = 20 Adc, I_B = 200 mAdc)	$V_{BE(sat)}$	–	4.0	Vdc
DYNAMIC CHARACTERISTICS				
Magnitude of Common Emitter Small−Signal Short−Circuit Forward Current Transfer Ratio (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)	$\lvert h_{fe} \rvert$	4.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) 2N6284 / 2N6286, 2N6287	C_{ob}	– / –	400 / 600	pF
Small−Signal Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)	h_{fe}	300	–	–

2. Indicates JEDEC Registered Data.
3. Pulse test: Pulse Width = 300 μs, Duty Cycle = 2%

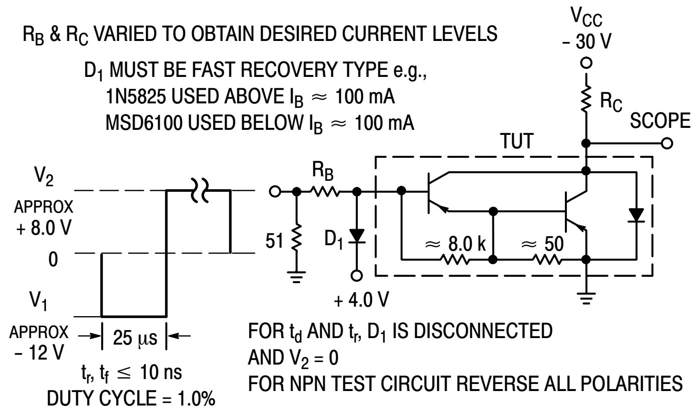


Figure 2. Switching Times Test Circuit

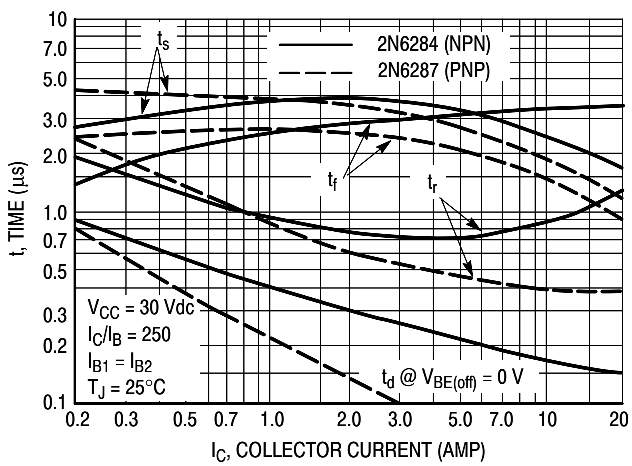


Figure 3. Switching Times

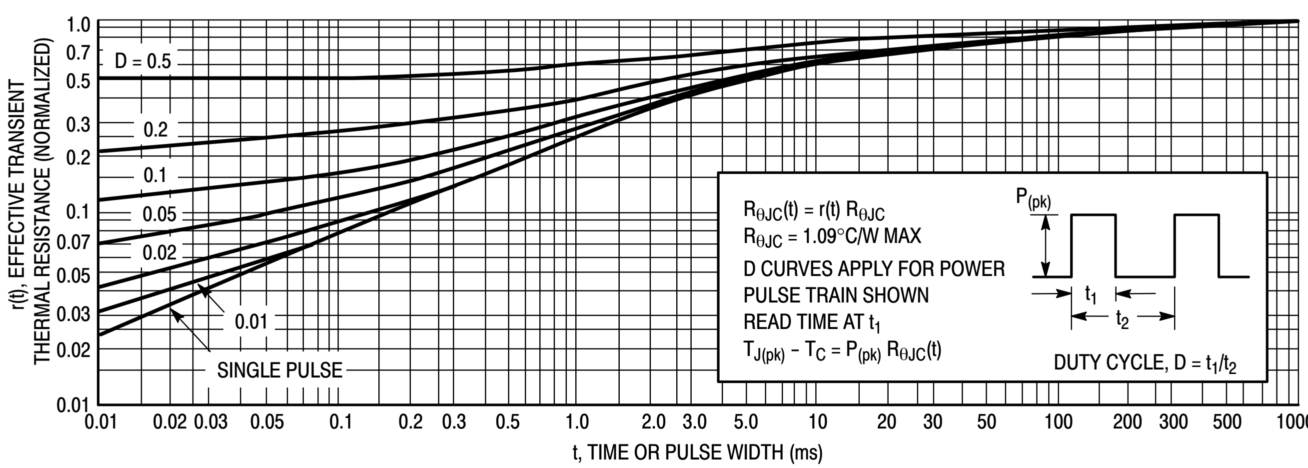


Figure 4. Thermal Response

ACTIVE−REGION SAFE OPERATING AREA

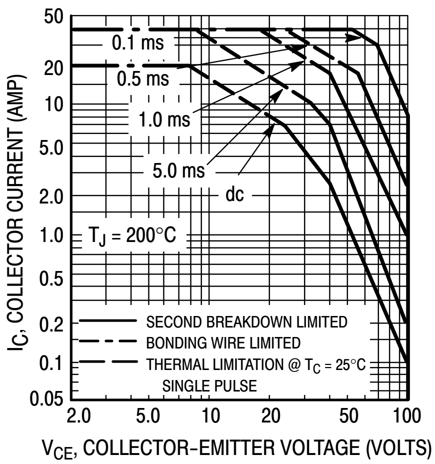


Figure 5. 2N6284, 2N6287

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e. the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

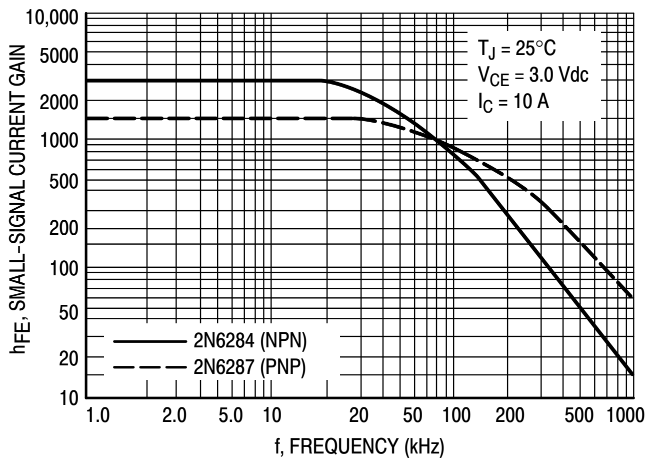


Figure 6. Small−Signal Current Gain

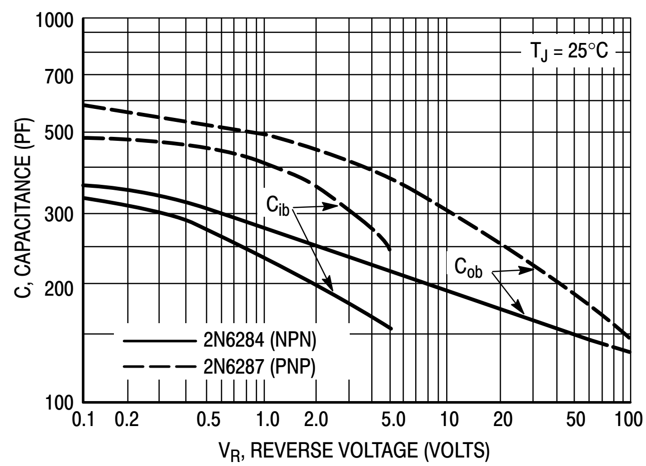
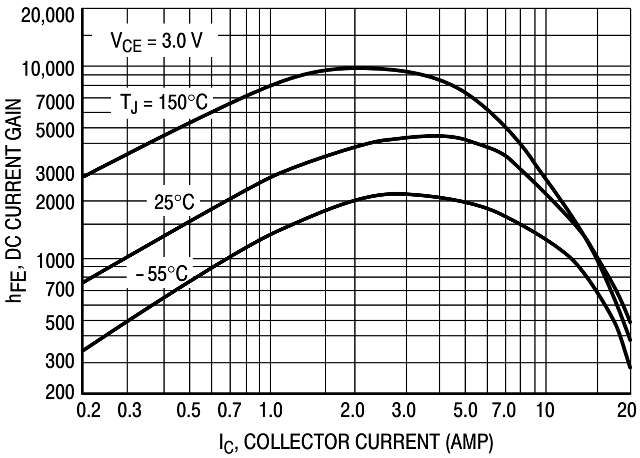


Figure 7. Capacitance

NPN
2N6284



PNP
2N6287

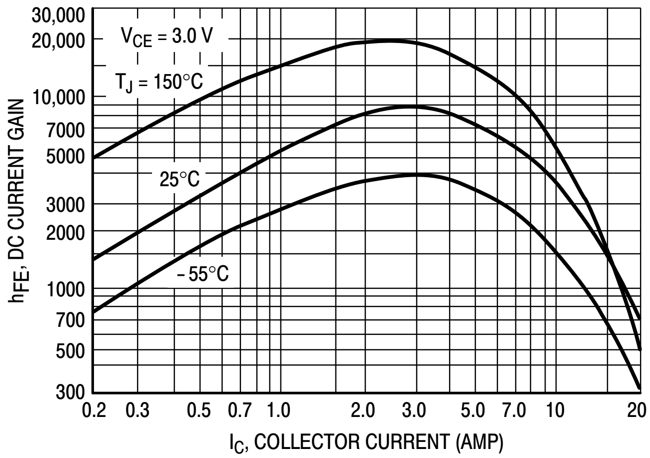
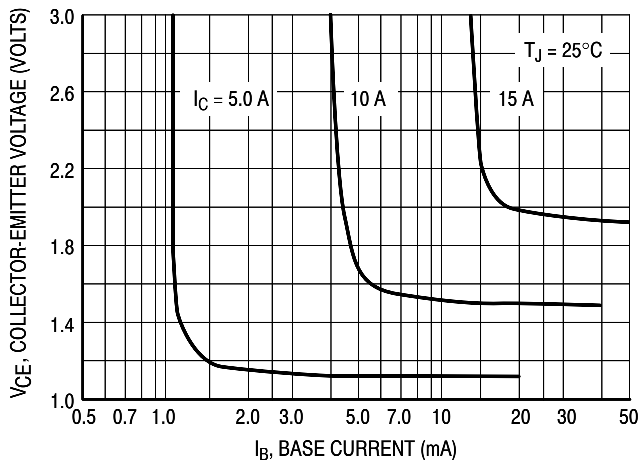


Figure 8. DC Current Gain



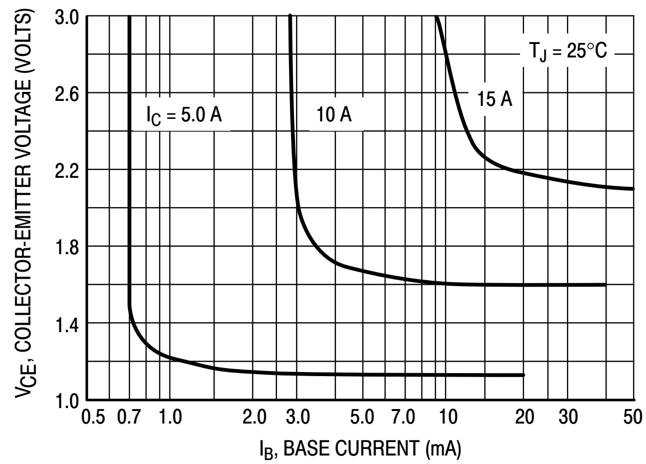
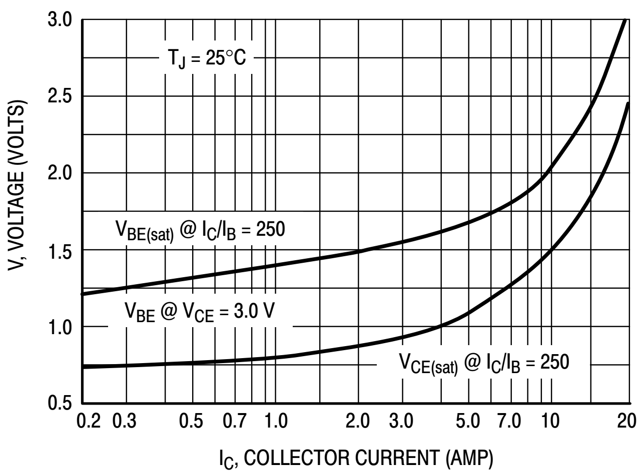


Figure 9. Collector Saturation Region



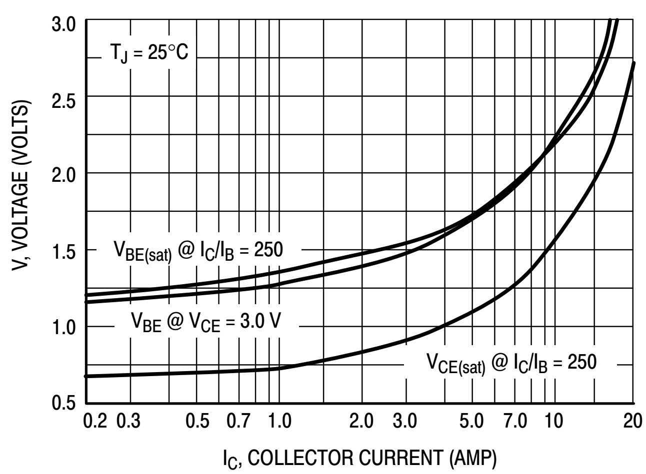
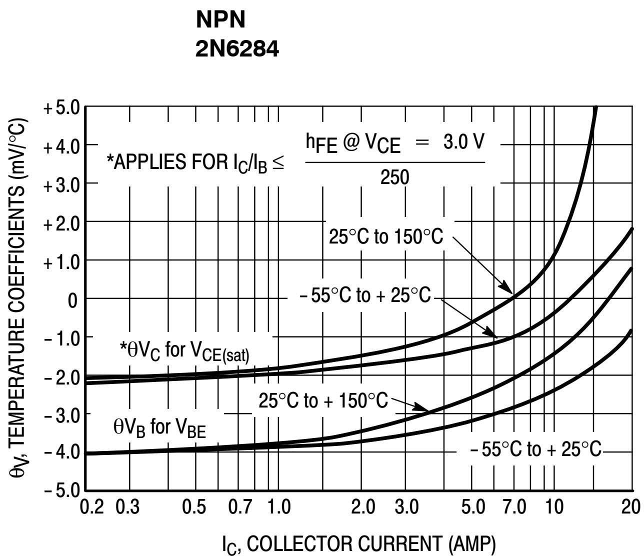


Figure 10. "On" Voltages



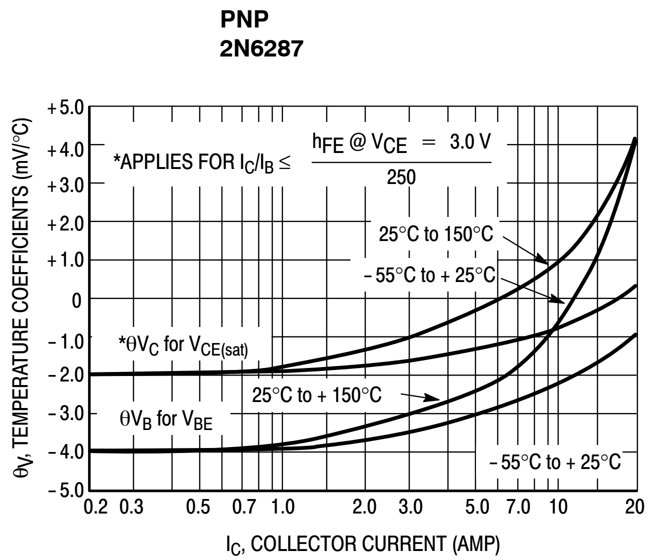
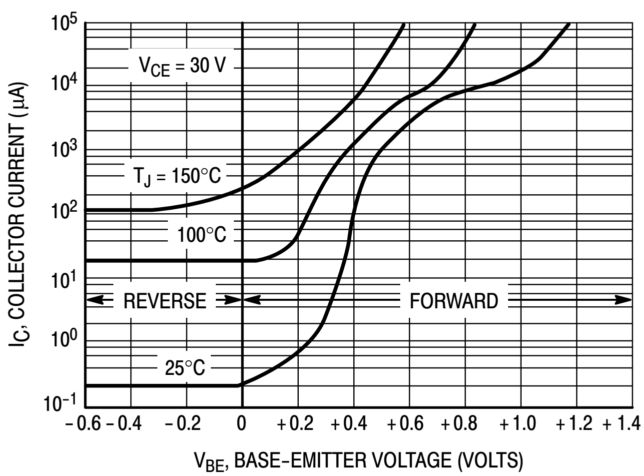


Figure 11. Temperature Coefficients



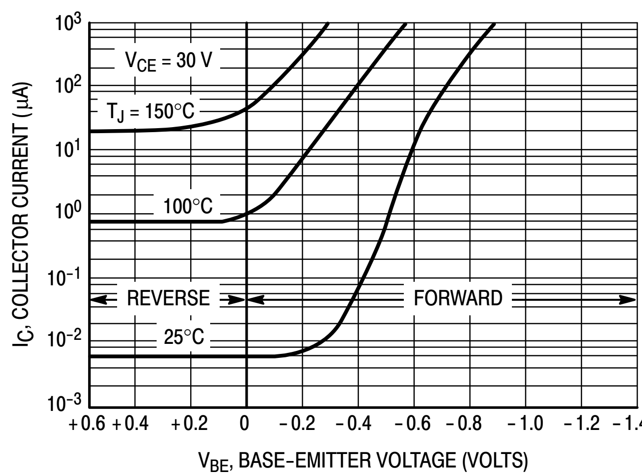
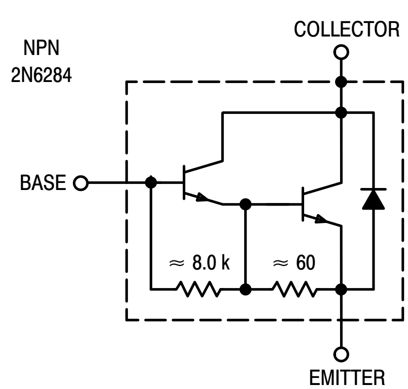


Figure 12. Collector Cut−Off Region



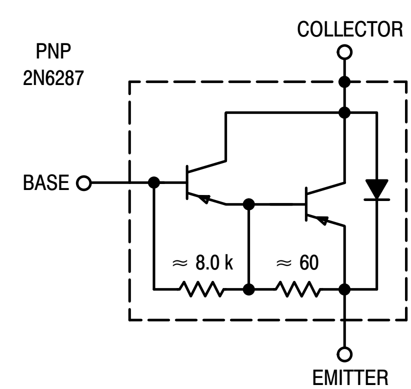
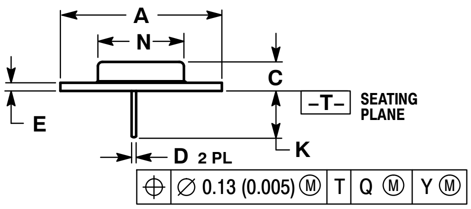
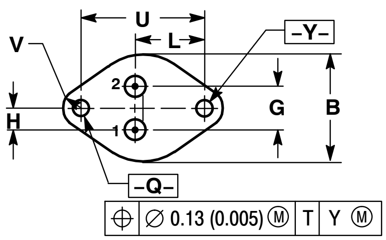


Figure 13. Darlington Schematic

PACKAGE DIMENSIONS

TO−204 (TO−3)
CASE 1−07
ISSUE Z





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO−204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

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