

ADD-A-PAK Generation VII Power Modules Thyristor/Diode and Thyristor/Thyristor, 95 A



ADD-A-PAK

FEATURES

- High voltage
- Industrial standard package
- UL pending
- 3500 V_{RMS} isolating voltage
- Low thermal resistance
- Totally lead (Pb)-free
- Designed and qualified for industrial level



RoHS
COMPLIANT

PRODUCT SUMMARY

$I_{T(AV)}$ or $I_{F(AV)}$	95 A
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MECHANICAL DESCRIPTION

The ADD-A-PAK Generation VII, new generation of ADD-A-PAK module, combines the excellent thermal performances obtained by the usage of exposed direct bonded copper substrate, with advanced compact simple package solution and simplified internal structure with minimized number of interfaces.

BENEFITS

- Excellent thermal performances obtained by the usage of exposed direct bonded copper substrate
- Up to 1600 V
- High surge capability
- Easy mounting on heatsink

ELECTRICAL DESCRIPTION

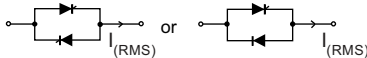
These modules are intended for general purpose high voltage applications such as high voltage regulated power supplies, lighting circuits, temperature and motor speed control circuits, UPS and battery charger.

MAJOR RATINGS AND CHARACTERISTICS

SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_{T(AV)}$ or $I_{F(AV)}$	85 °C	95	A
$I_{O(RMS)}$	As AC switch	210	
I_{TSM} , I_{FSM}	50 Hz 60 Hz	2000 2094	
I^2t	50 Hz 60 Hz	20 18.26	kA ² s
$I^2\sqrt{t}$		200	kA ² √s
V_{RRM}	Range	400 to 1600	V
T_{Stg}		- 40 to 125	°C
T_J			

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS					
TYPE NUMBER	VOLTAGE CODE	V _{RRM} , MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	V _{RSM} , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	V _{DRM} , MAXIMUM REPETITIVE PEAK OFF-STATE VOLTAGE, GATE OPEN CIRCUIT V	I _{RRM} , I _{DRM} AT 125 °C mA
VSK.91	04	400	500	400	15
	06	600	700	600	
	08	800	900	800	
	10	1000	1100	1000	
	12	1200	1300	1200	
	14	1400	1500	1400	
	16	1600	1700	1600	

ON-STATE CONDUCTION						
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average on-state current (thyristors)	I _{T(AV)}	180° conduction, half sine wave, T _C = 85 °C			95	A
Maximum average forward current (diodes)	I _{F(AV)}					
Maximum continuous RMS on-state current, as AC switch	I _{O(RMS)}				210	
Maximum peak, one-cycle non-repetitive on-state or forward current	I _{TSM} or I _{FSM}	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial T _J = T _J maximum	2000	
		t = 8.3 ms				
		t = 10 ms	100 % V _{RRM} reapplied		1682	
		t = 8.3 ms			1760	
Maximum I ² t for fusing	I ² t	t = 10 ms	No voltage reapplied	Initial T _J = T _J maximum	20	kA ² s
		t = 8.3 ms				
		t = 10 ms	100 % V _{RRM} reapplied		14.14	
		t = 8.3 ms			12.91	
Maximum I ² √t for fusing	I ² √t (1)	t = 0.1 ms to 10 ms, no voltage reapplied T _J = T _J maximum			200	kA ² √s
Maximum value or threshold voltage	V _{T(TO)} (2)	Low level (3)	T _J = T _J maximum	0.97	V	
		High level (4)		1.1		
Maximum value of on-state slope resistance	r _t (2)	Low level (3)	T _J = T _J maximum	2.76	mΩ	
		High level (4)		2.38		
Maximum peak on-state or forward voltage	V _{TM}	I _{TM} = π × I _{T(AV)}	T _J = 25 °C	1.73	V	
	V _{FM}	I _{FM} = π × I _{F(AV)}				
Maximum non-repetitive rate of rise of turned on current	di/dt	T _J = 25 °C, from 0.67 V _{DRM} , I _{TM} = π × I _{T(AV)} , I _g = 500 mA, t _r < 0.5 μs, t _p > 6 μs			150	A/μs
Maximum holding current	I _H	T _J = 25 °C, anode supply = 6 V, resistive load, gate open circuit			250	mA
Maximum latching current	I _L	T _J = 25 °C, anode supply = 6 V, resistive load			400	

Notes(1) I²t for time t_x = I²√t × √t_x(2) Average power = V_{T(TO)} × I_{T(AV)} + r_t × (I_{T(RMS)})²(3) 16.7 % × π × I_{AV} < I < π × I_{AV}(4) I > π × I_{AV}



TRIGGERING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum peak gate power	P _{GM}			12	W
Maximum average gate power	P _{G(AV)}			3.0	
Maximum peak gate current	I _{GM}			3.0	A
Maximum peak negative gate voltage	- V _{GM}			10	V
Maximum gate voltage required to trigger	V _{GT}	T _J = - 40 °C	Anode supply = 6 V resistive load	4.0	
		T _J = 25 °C		2.5	
		T _J = 125 °C		1.7	
Maximum gate current required to trigger	I _{GT}	T _J = - 40 °C	Anode supply = 6 V resistive load	270	mA
		T _J = 25 °C		150	
		T _J = 125 °C		80	
Maximum gate voltage that will not trigger	V _{GD}	T _J = 125 °C, rated V _{DRM} applied		0.25	V
Maximum gate current that will not trigger	I _{GD}	T _J = 125 °C, rated V _{DRM} applied		6	mA

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak reverse and off-state leakage current at V_{RRM} , V_{DRM}	I_{RRM} , I_{DRM}	$T_J = 125\text{ }^{\circ}\text{C}$, gate open circuit	15	mA
RMS insulation voltage	V_{INS}	50 Hz, 1 s	3500	V
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = 125\text{ }^{\circ}\text{C}$, linear to 0.67 V_{DRM}	1000	V/ μ s

THERMAL AND MECHANICAL SPECIFICATIONS					
PARAMETER		SYMBOL	TEST CONDITIONS	VALUES	UNITS
Junction operating and storage temperature range		T _J , T _{Stg}		- 40 to 125	°C
Maximum internal thermal resistance, junction to case per leg		R _{thJC}	DC operation	0.22	°C/W
Typical thermal resistance, case to heatsink per module		R _{thCS}	Mounting surface flat, smooth and greased	0.1	
Mounting torque ± 10 %	to heatsink		A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound.	4	Nm
	busbar			3	
Approximate weight				75	g
				2.7	oz.
Case style			JEDEC	TO-240AA compatible	

ΔR CONDUCTION PER JUNCTION											
DEVICES	SINE HALF WAVE CONDUCTION					RECTANGULAR WAVE CONDUCTION					UNITS
	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	
VSK.91..	0.04	0.048	0.063	0.085	0.125	0.033	0.052	0.067	0.088	0.127	°C/W

Note

- Table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

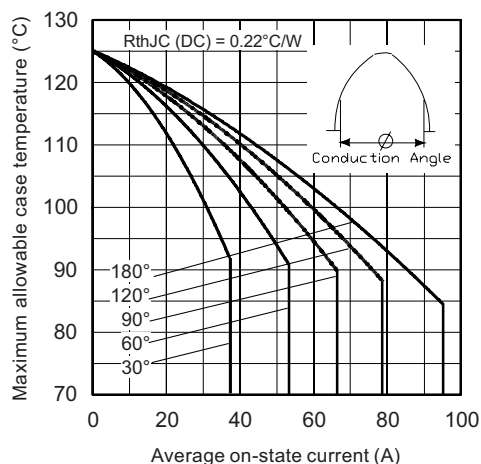


Fig. 1 - Current Ratings Characteristics

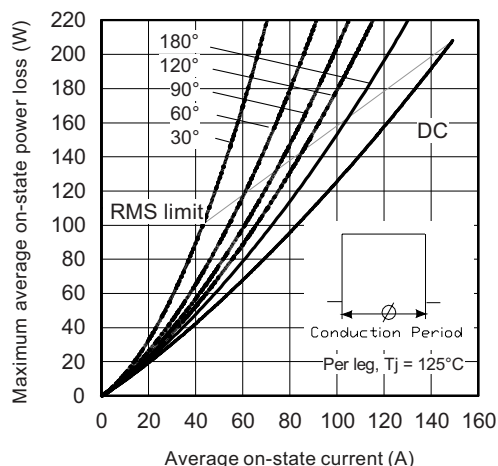


Fig. 4 - On-State Power Loss Characteristics

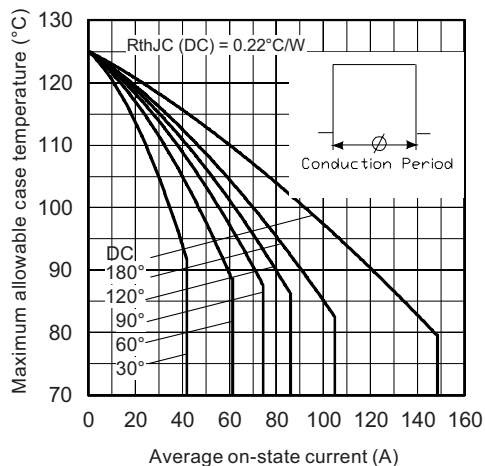


Fig. 2 - Current Ratings Characteristics

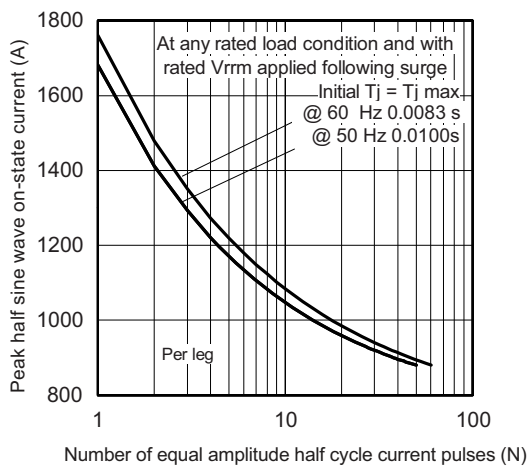


Fig. 5 - Maximum Non-Repetitive Surge Current

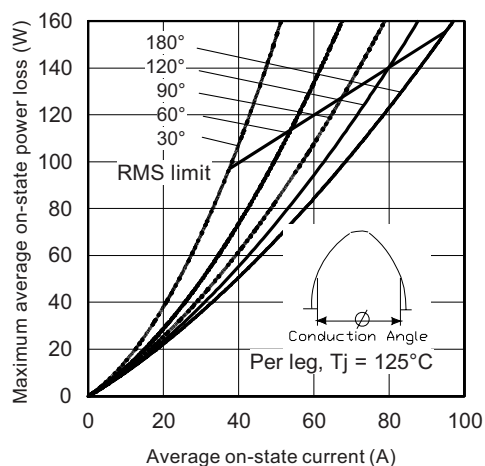


Fig. 3 - On-State Power Loss Characteristics

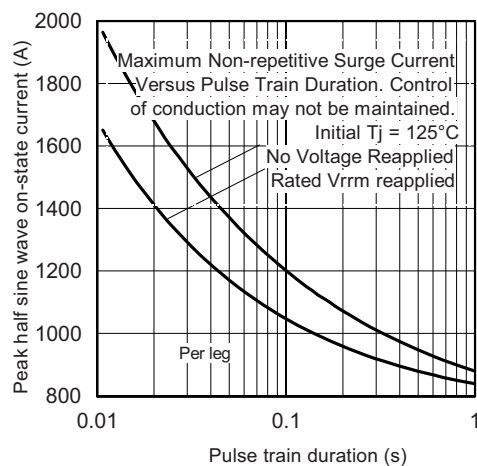


Fig. 6 - Maximum Non-Repetitive Surge Current

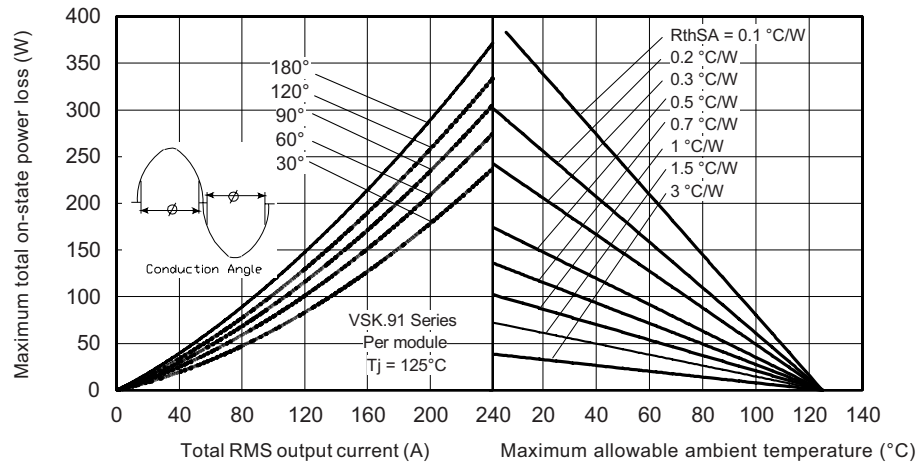


Fig. 7 - On-State Power Loss Characteristics

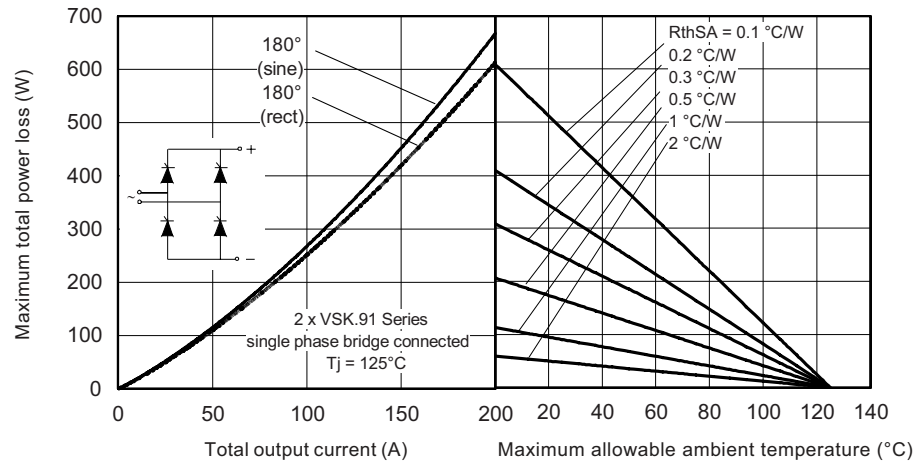


Fig. 8 - On-State Power Loss Characteristics

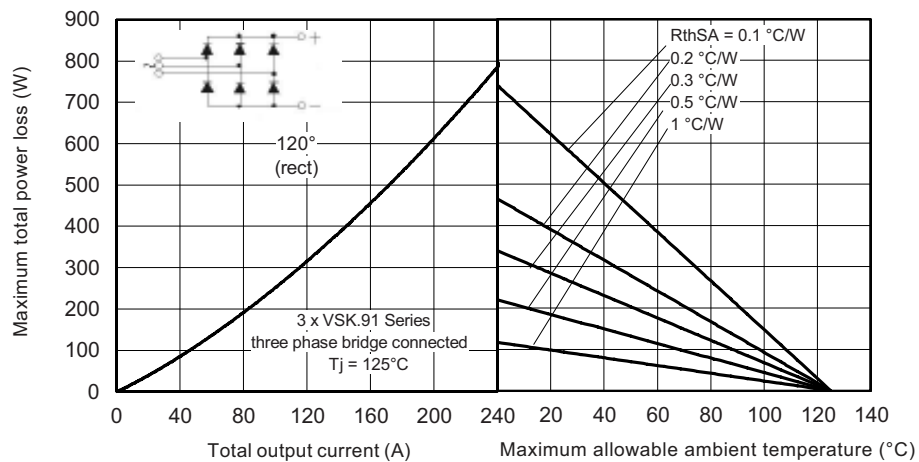


Fig. 9 - On-State Power Loss Characteristics

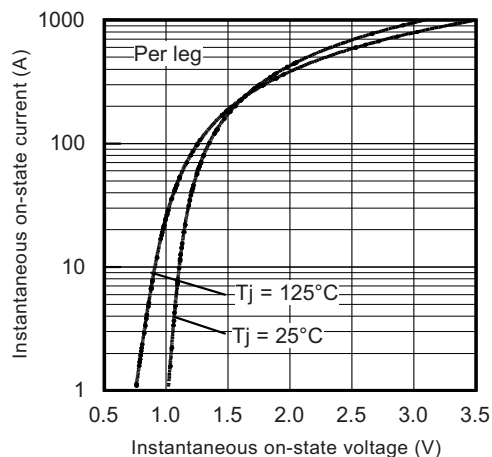


Fig. 10 - On-State Voltage Drop Characteristics

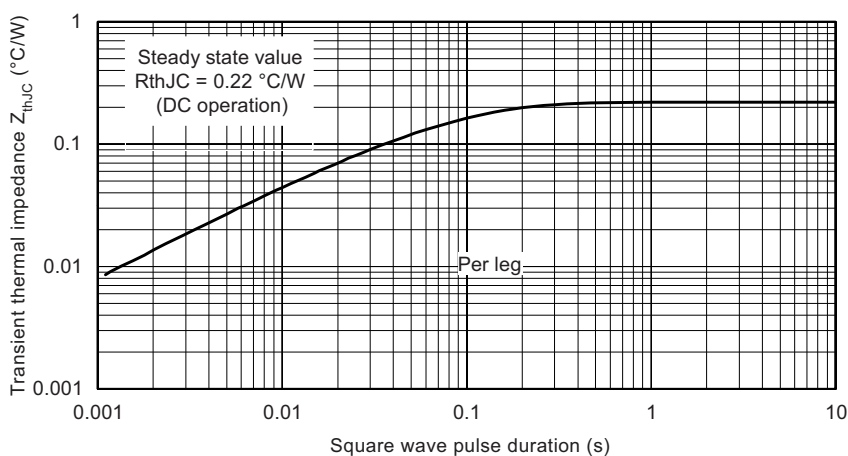


Fig. 11 - Thermal Impedance Z_{thJC} Characteristics

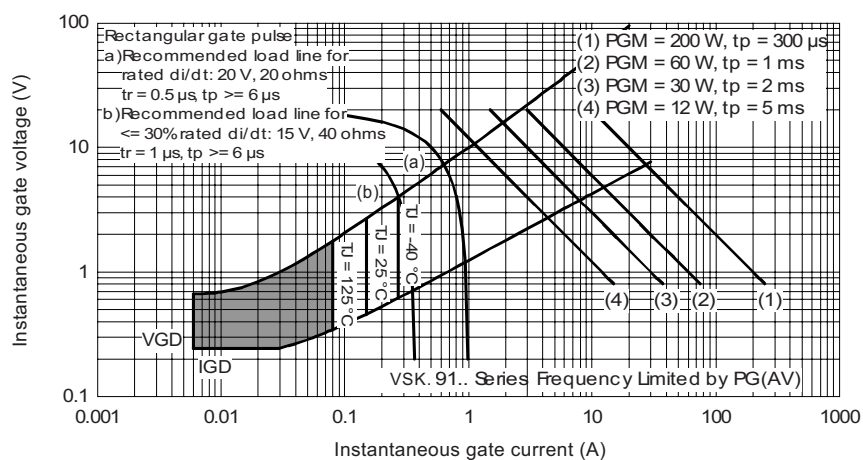
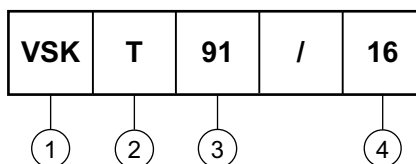


Fig. 12 - Gate Characteristics

Device code



- 1** - Module type
- 2** - Circuit configuration (see end of datasheet)
- 3** - Current code (95 A)
- 4** - Voltage code (see Voltage Ratings table)

- To order the optional hardware go to www.vishay.com/doc?95172

The diagrams show the internal wiring for four relay types:

- VSKT:** Features three relays (1, 2, 3) and six terminals (4, 5, 6, 7, 8, 9). Terminal (1) is connected to relay 1. Terminal (2) is connected to relay 2. Terminal (3) is connected to relay 3. Terminals (4), (5), (6), (7), (8), and (9) are connected to the common terminals of relays 1, 2, and 3 respectively.
- VSKH:** Features three relays (1, 2, 3) and six terminals (4, 5, 6, 7, 8, 9). Terminal (1) is connected to relay 1. Terminal (2) is connected to relay 2. Terminal (3) is connected to relay 3. Terminals (4), (5), (6), (7), (8), and (9) are connected to the common terminals of relays 1, 2, and 3 respectively.
- VSKL:** Features three relays (1, 2, 3) and six terminals (4, 5, 6, 7, 8, 9). Terminal (1) is connected to relay 1. Terminal (2) is connected to relay 2. Terminal (3) is connected to relay 3. Terminals (4), (5), (6), (7), (8), and (9) are connected to the common terminals of relays 1, 2, and 3 respectively.
- VSKN:** Features three relays (1, 2, 3) and six terminals (4, 5, 6, 7, 8, 9). Terminal (1) is connected to relay 1. Terminal (2) is connected to relay 2. Terminal (3) is connected to relay 3. Terminals (4), (5), (6), (7), (8), and (9) are connected to the common terminals of relays 1, 2, and 3 respectively.

Dimensions

<http://www.vishay.com/doc?95368>



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