0.8% Accuracy, Voltage Detector with Delay Function

NO.EA-306-160309

OUTLINE

The RP300x is a CMOS-based voltage detector (VD) IC with a built-in output delay circuit. Internally, a single IC consists of a voltage reference unit, a comparator, a resistor net for setting detector threshold, a manual reset circuit, an output delay circuit and an output driver transistor.

The RP300x is available in internally fixed detector threshold type. When the V_{DD} voltage becomes lower than the preset voltage, the RP300xxxxA/C generates a "L" reset signal and the RP300xxxxB (custom IC[*1]) generates a "H" reset signal. The detector threshold accuracy is as high as ±1.0% when $-V_{SET}$[*2] < 1.7 V and ±0.8% when 1.7 V ≤ $-V_{SET}$.

The reset output signal remains asserted for 50 ms, 100 ms (custom IC) or 200 ms after the V_{DD} voltage rises above the threshold voltage or when manual reset is canceled. The RP300x is designed to ignore fast transients on the V_{DD} pin. The output delay time accuracy is as high as ±5.0%.

The RP300x is available in an Nch open drain output type or in a CMOS output type.

The RP300x is offered in an ultra-small DFN(PLP)1010-4B package or in a SOT-23-5 package.

[*1] For more information about a custom IC, please contact our sales representatives.
[*2] $-V_{SET}$ is defined as a preset detector threshold.

FEATURES

- Supply Current ······ Typ. 0.95 μA ($-V_{SET}$ = 3.08 V, V_{DD} = 3.18 V)
- Operating Voltage Range ······ 0.72 V to 5.50 V (25°C)
- Detector Threshold Range ······ 1.1 V, 2.32 V, 2.63 V, 2.7 V, 2.8 V, 2.93 V, 3.08 V, 3.4 V (34), 4.38 V (43), 4.6 V (46)
- Detector Threshold Accuracy ······ ±1.0% ($-V_{SET}$ < 1.7 V), ±0.8% (1.7 V ≤ $-V_{SET}$)
- Detector Threshold Temperature Coefficient ······ Typ. ±50 ppm/°C
- Released Output Delay Time ······ Typ. 50 ms, 100 ms (custom IC), 200 ms
- Released Output Delay Time Accuracy ······ ±5% (25°C), ±15% (−40°C to 85°C)
- Package ······ DFN(PLP)1010-4B, SOT-23-5
- Output Type ······ Nch Open Drain output, CMOS Output
- Reset Signal ······ Active-low, Active-high (custom IC)

APPLICATIONS

- Voltage monitoring for handheld communication equipment, camera and VCRs.
- Voltage monitoring for battery-powered equipment

BLOCK DIAGRAMS

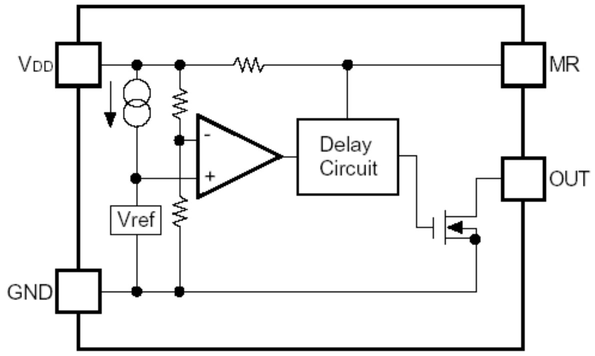


Figure 1. RP300xxxxA/B (Nch Open Drain Output)

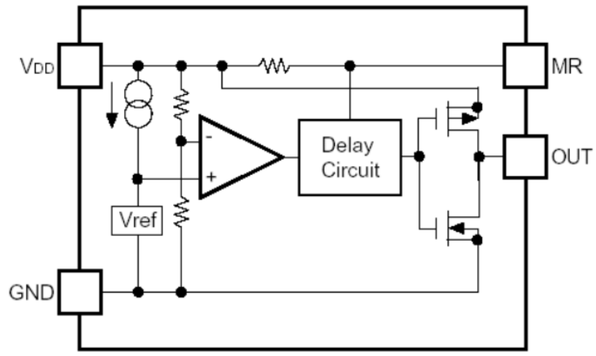


Figure 2. RP300xxxxC (CMOS Output)

SELECTION GUIDE

With the RP300x, the detector threshold, the package type, the released output delay time and the output type are user-selectable options.

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
RP300Kxxy∗(z)-TR	DFN(PLP)1010-4B	10,000 pcs	Yes	Yes
RP300Nxxy∗(z)-TR-FE	SOT-23-5	3,000 pcs	Yes	Yes

xx: Specify $-V_{SET}$ from 1.1 V (11), 2.32 V (23), 2.63 V (26), 2.7 V (27), 2.8 V (28), 2.93 V (29), 3.08 V (30), 3.4 V (34), 4.38 V (43), 4.6 V (46).

z: If $-V_{SET}$ includes the 3rd digit, indicate the digit of 0.01 V.
Ex. If $-V_{SET}$ is 2.63 V, indicate as RP300x26xx3-TR-x.

y: Specify the released output delay time.
(A) 50 ms
(B) 100 ms (custom IC)
(D) 200 ms

∗: Specify the output type.
(A) Nch Open Drain Output
(B) Nch Open Drain Inverting Output (custom IC)
(C) CMOS Output

PIN CONFIGULATIONS

● **DFN(PLP)1010-4B** ● **SOT- 23-5**

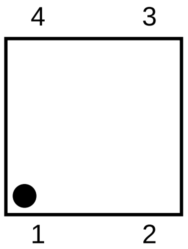


Figure 3. Top View

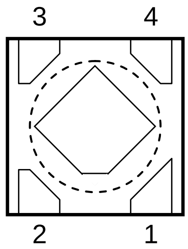


Figure 4. Bottom View

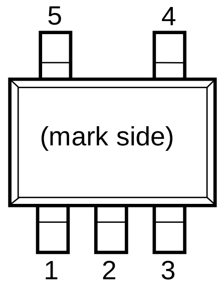


Figure 5. Mark Side

PIN DESCRIPTION

RP300K: DFN(PLP)1010-4B

Pin No.	Symbol	Pin Description
1	OUT	Output Pin RP300xxxxA/C: asserts an active-low reset signal when a voltage drops below the detector threshold. RP300xxxxB: asserts an active-high reset signal when a voltage drops below the detector threshold. (custom IC)
2	MR	Manual Reset Input Pin: active-low
3	GND	Ground Pin
4	V_{DD}	Input Pin

The tab on the bottom of the package enhances thermal performance and is electrically connected to GND (substarate level). It is recommended that the tab be connected to the ground plane on the board. If not, the tab can be left open.

RP300N: SOT-23-5

Pin No.	Symbol	Description
1	MR	Manual Reset Input Pin: active-low
2	GND	Ground Pin
3	NC	No Connection
4	OUT	Output Pin RP300xxxxA/C: asserts an active-low reset signal when a voltage drops below the detector threshold. RP300xxxxB: asserts an active-high reset signal when a voltage drops below the detector threshold. (custom IC)
5	V_{DD}	Input Pin

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating		Unit
V_{IN}	Input Voltage	6.0		V
OUT	Output Voltage (Nch Open Drain Output)	−0.3 to 6.0		V
	Output Voltage (CMOS Output)	−0.3 to V_{DD} +0.3		
MR	Manual Reset Pin	−0.3 to V_{DD} +0.3		V
I_{OUT}	Output Current	20		mA
P_D	Power Dissipation (Standard Land Pattern)[*3]	DFN(PLP)1010-4B	400	mW
		SOT-23-5	420	
Ta	Operating Temperature Range	−40 to +85		°C
Tstg	Storage Temperature Range	−55 to +125		°C

[*3] Refer to the next page for detailed information about Power Dissipation.

ABSOLUTE MAXIMUM RATINGS
Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING CONDITIONS (ELECTRICAL CHARACTERISTICS)
All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

POWER DISSIPATION (DFN(PLP)1010-4B)

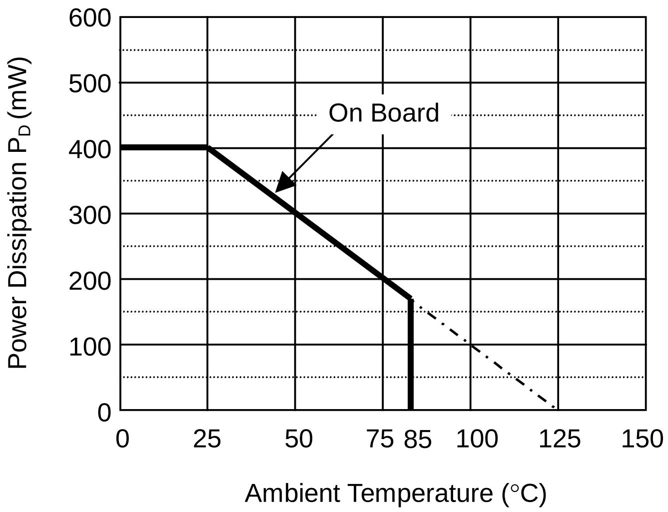
Power Dissipation (P_D) of the package is dependent on PCB material, layout, and environmental conditions. The following conditions are used in this measurement.

Measurement Conditions

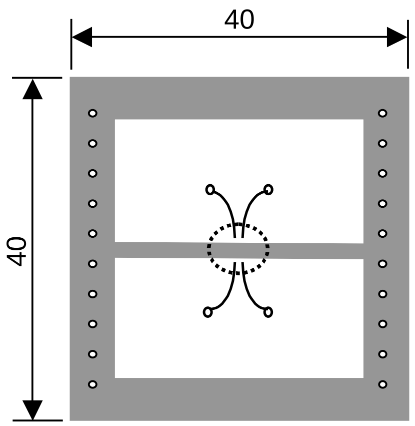
	Standard Land Pattern
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Double-sided)
Board Dimensions	40 mm x 40 mm x 1.6 mm
Copper Ratio	Top side: Approx. 50%, Back side: Approx. 50%
Through-holes	ϕ 0.54 mm x 24 pcs

Measurement Result: (Ta = 25°C, Tjmax = 125°C)

	Standard Land Pattern
Power Dissipation	400 mW
Thermal Resistance	θja = (125 −25°C) / 0.4 W = 250°C/W
	θjc = 67°C/W



Power Dissipation



Measurement Board Pattern

IC Mount Area (Unit : mm)

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POWER DISSIPATION (SOT-23-5)

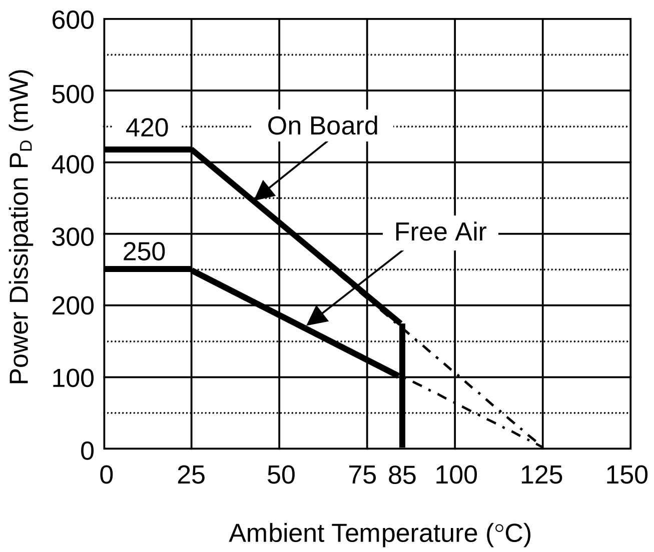
Power Dissipation (P_D) of the package is dependent on PCB material, layout, and environmental conditions. The following conditions are used in this measurement. This data is taken from SOT-23-6.

Measurement Conditions

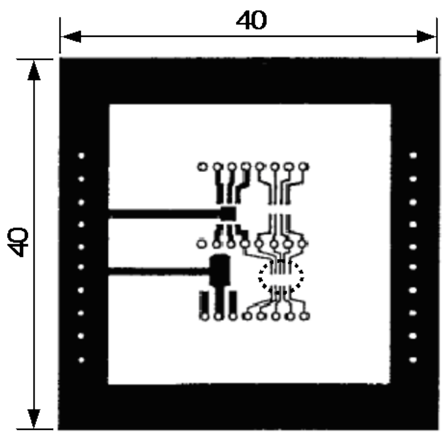
	Standard Land Pattern
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Double-sided)
Board Dimensions	40 mm x 40 mm x 1.6 mm
Copper Ratio	Top side: Approx. 50%, Back side: Approx. 50%
Through-holes	ϕ 0.5 mm x 44 pcs

Measurement Result: (Ta = 25°C, Tjmax = 125°C)

	Standard Land Pattern	**Free Air**
Power Dissipation	420 mW	250 mW
Thermal Resistance	θja = (125 − 25°C) / 0.42 W = 238°C/W	400°C/W



Power Dissipation



Measurement Board Pattern

IC Mount Area (Unit: mm)

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ELECTRICAL CHARACTERISTICS

The specifications surrounded by ☐ are guaranteed by design engineering at $-40°C \le Ta \le 85°C$.

RP300x (Ta = 25°C)

Symbol	Item	Conditions		Min.	Typ.	Max.	Unit
$-V_{DET}$ *4	Detector Threshold (Ta = 25°C)	$-V_{SET}$ *4 < 1.7 V		×0.99		×1.010	V
		1.7 V ≤ $-V_{SET}$		×0.992		×1.008	V
	Detector Threshold (−40°C ≤ Ta ≤ 85°C)	$-V_{SET}$ < 1.7 V		×0.982		×1.018	V
		1.7 V ≤ $-V_{SET}$		×0.984		×1.016	V
I_{SS1}	Supply Current 1	$V_{DD} = -V_{SET} - 0.1$ V, I_{OUT} = 0 A				3.2	μA
I_{SS2}	Supply Current 2	$V_{DD} = -V_{SET} + 0.1$ V, I_{OUT} = 0 A				3.1	μA
V_{DD}	Operating Voltage	Ta = 25°C		0.72		5.5	V
		−40°C ≤ Ta ≤ 85°C		0.80		5.5	V
I_{OUT}	Output Current (Driver Output Pin)	Nch $V_{DD} = -V_{SET} - 0.1$ V V_{DS} = 0.3 V	$-V_{SET}$ ≥ 1.1 V	0.45			mA
			$-V_{SET}$ ≥ 1.6 V	2.5			mA
			$-V_{SET}$ ≥ 2.7 V	4.8			mA
		Nch Inverting*5 $V_{DD} = -V_{SET} + 0.1$ V V_{DS} = 0.3 V	$-V_{SET}$ ≥ 1.1 V	0.45			mA
			$-V_{SET}$ ≥ 1.4 V	2.5			mA
			$-V_{SET}$ ≥ 2.5 V	4.8			mA
		Pch CMOS $V_{DD} = -V_{SET} + 0.1$ V V_{DS} = −0.3 V	$-V_{SET}$ ≥ 1.1 V	−0.15			mA
			$-V_{SET}$ ≥ 1.6 V	−0.45			mA
			$-V_{SET}$ ≥ 2.7 V	−0.8			mA
I_{LEAK}	Nch Driver Leakage Current	V_{DD} = 5.5 V V_{DS} = 5.5 V	RP300xxxxA/C			0.15	μA
		$V_{DD} = -V_{SET} - 0.1$ V V_{DS} = 5.5 V	RP300xxxxB*6				
R_{MR}	MR Pin Pull-up Resistance			0.21	0.45	0.90	MΩ
V_{IH}	MR Pin Input Voltage "H"	$V_{DD} \ge -V_{SET} + 0.1$ V		0.75 ×V_{DD}			V
V_{IL}	MR Pin Input Voltage "L"	$V_{DD} \ge -V_{SET} + 0.1$ V				0.4	V
tdelay*8	Released Output Delay Time	V_{DD} = 0.8 V → $-V_{SET}$ +1.0 V	RP300xxxAx	47.5	50	52.5	ms
			RP300xxxBx*7	95	100	105	ms
			RP300xxxDx	190	200	210	ms
		−40°C ≤ Ta ≤ 85°C		tset*8 ×0.85		tset× 1.15	%
$\Delta -V_{DET}/\Delta Ta$	Detector Threshold Temperature Coefficient	−40°C ≤ Ta ≤ 85°C			±50		ppm /°C

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C) except Detector Threshold Temperature Coefficient.
*4 $-V_{DET}$ is defined as an actual detector threshold and $-V_{SET}$ is defined as a preset detector threshold.
*5 Nch open drain inverting output type is only applicable to the RP300xxxxB which is a custom IC.
*6 The RP300xxxxB is a custom IC. *7 The RP300xxxBx is a custom IC.
*8 tdelay is defined as an actual released output delay time and tset is defined as a preset released output delay time.

TIMING CHART

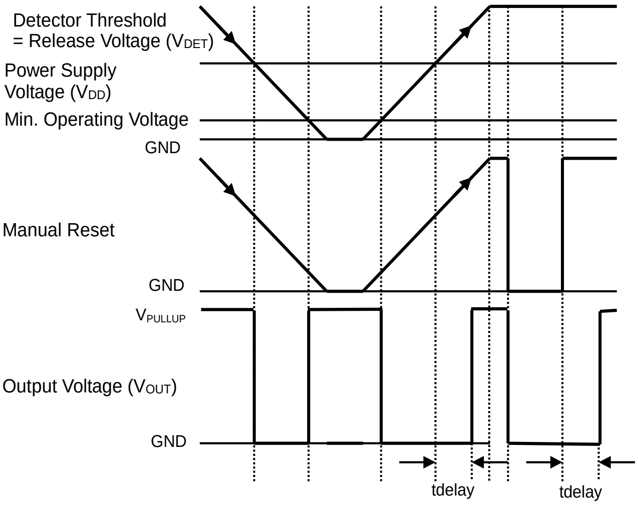

Figure 6. RP300xxxxA Timing Chart

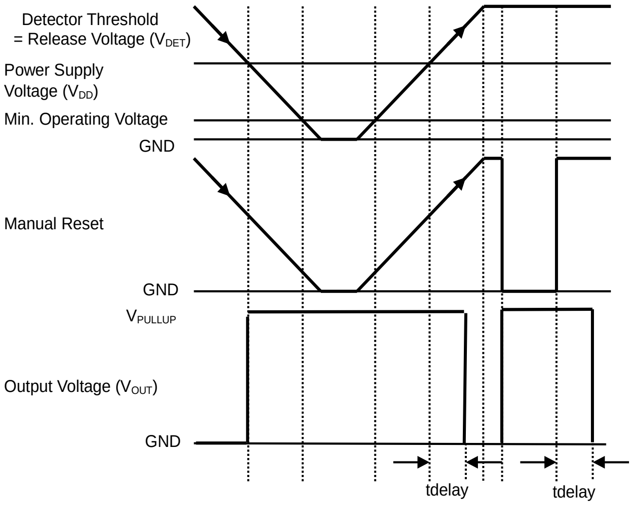

Figure 7. RP300xxxxB Timing Chart

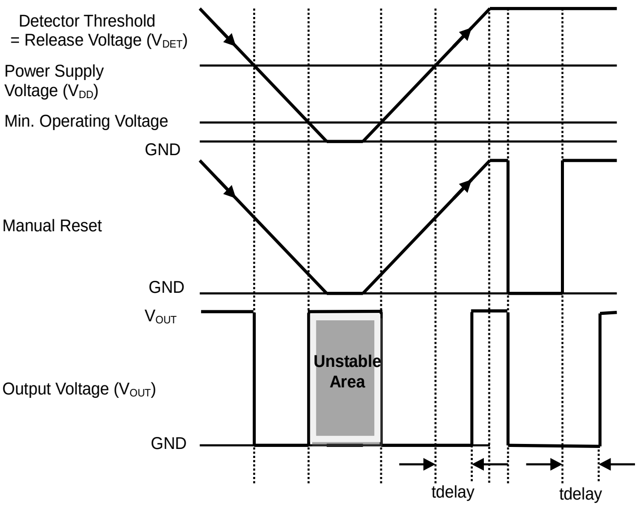

Figure 8. RP300xxxxC Timing Chart

Release Output Delay Time (tdelay)

tdelay is defined as follows.

1. Nch Open Drain Output

   Release output delay time starts after the OUT pin is pulled up to 5.5 V with a 470 kΩ resistor, and the V_{DD} voltage is shifted from 0.8 V to $-V_{SET}$ + 1.0 V. It ends when the output voltage reaches 1.0 V.

2. Nch Open Drain Inverting Output (custom IC)

   Release output delay time starts after the OUT pin is pulled up to 5.5 V with a 470 kΩ resistor, and the V_{DD} voltage is shifted from 0.8 V to $-V_{SET}$ + 1.0 V. It ends when the output voltage reaches V_{DD} / 2 V.

3. CMOS Output

   Release output delay time starts when the V_{DD} voltage is shifted from 0.8 V to $-V_{SET}$ + 1.0 V and ends when the output voltage reaches V_{DD} / 2 V.

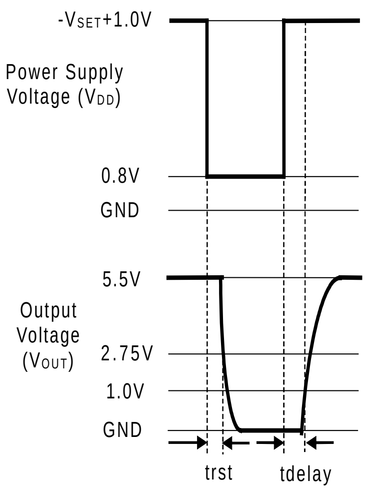

Figure 9. Nch Open Drain Output

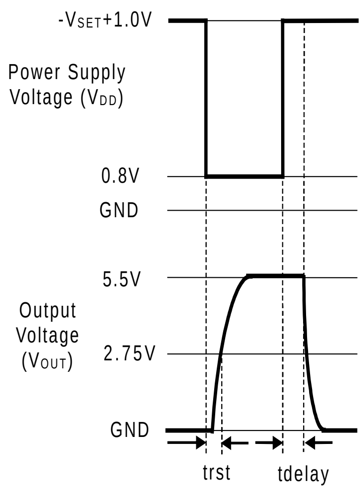

Figure 10. Nch Open Drain Inverting Output

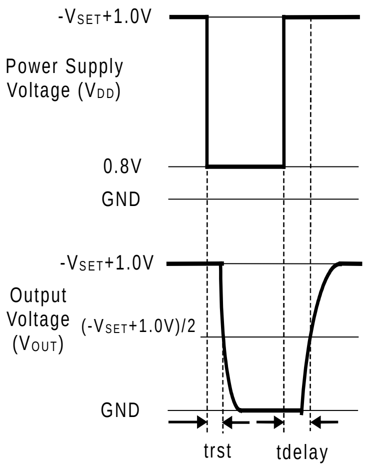

Figure 11. CMOS Output

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THEORY OF OPERATION

RP300xxxxA/C

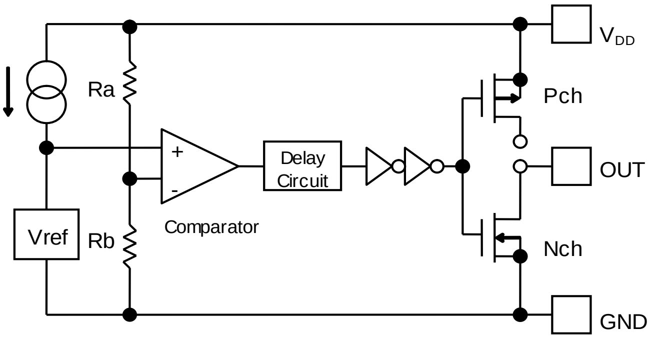

Figure 12. Block Diagram

- For CMOS Output, the Nch Tr. drain and the Pch Tr. drain are connected to the OUT pin inside the IC.
- For Nch Open Drain Output, the Nch Tr. drain is connected to the OUT pin inside the IC. Pull up the OUT pin or V_{DD} pin to the external voltage level.

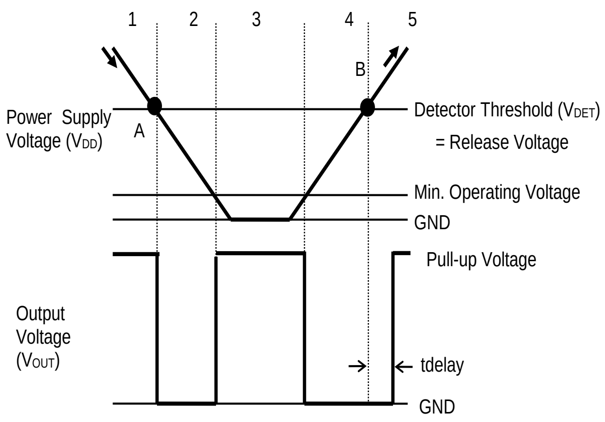

Figure 13. Timing Chart (A Ver.)

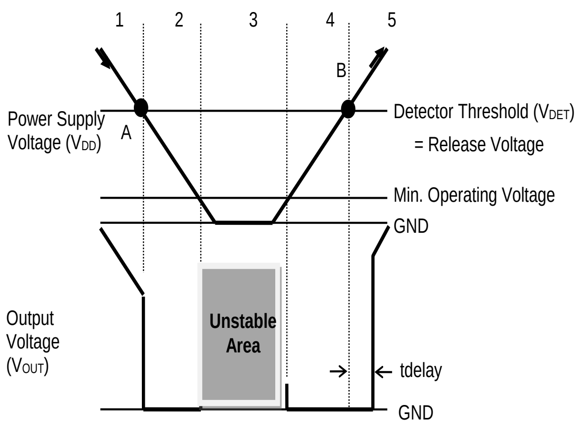

Figure 14. Timing Chart (C Ver.)

1. The output voltage is equalized to the V_{DD} voltage (CMOS Output), or to the pull-up voltage (Nch Open Drain Output).
2. The V_{DD} voltage drops to the detector threshold (A point) which means
   Vref ≥ V_{DD} x Rb / (Ra + Rb). The comparator output shifts from “L” to “H” voltage and the output voltage will be equalized to the GND voltage.
3. If the V_{DD} voltage is lower than the minimum operating voltage, the output voltage becomes unstable (CMOS Output). The output voltage is equalized to the pull-up voltage (Nch Open Drain Output).
4. The output voltage is equalized to the GND voltage.
5. The V_{DD} voltage becomes higher than the release voltage (B point) which means
   Vref < V_{DD} x Rb / (Ra + Rb), and the comparator output shifts from “H” to “L” voltage, and the output voltage is equalized to the V_{DD} voltage (CMOS Output) or to the pull-up voltage (Nch Open Drain Output).

   Note: There’s no hysteresis between the V_{DD} voltage and the released voltage.

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RP300xxxxB

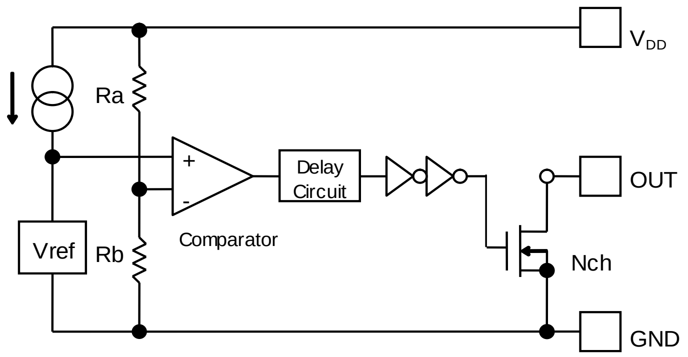

Figure 15. Block Diagram

・ The Nch Tr. drain is connected to the OUT pin inside the IC. Pull up the OUT pin or V_{DD} pin to the external voltage level.

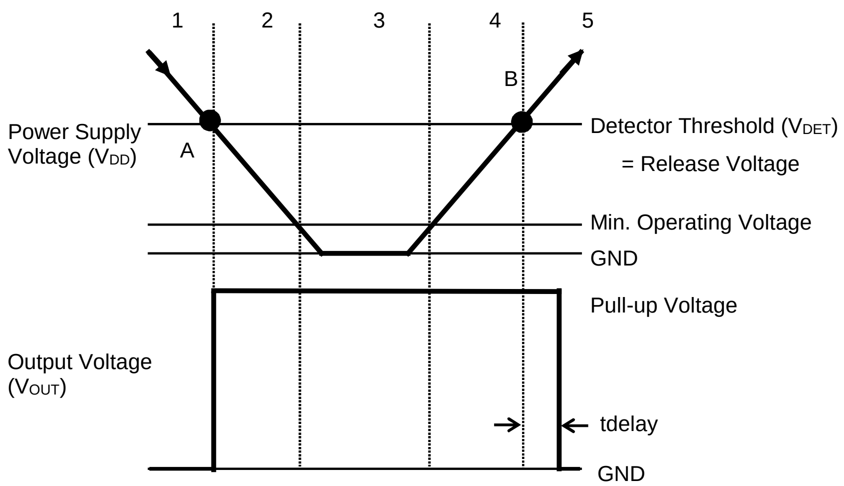

Figure 16. Timing Chart

1. The output voltage is equalized to the GND voltage.
2. The V_{DD} voltage drops to the detector threshold (A point) which means Vref ≥ V_{DD} x Rb / (Ra + Rb). The comparator output shifts from “H” to “L” voltage and the output voltage shifts from the pull-up voltage to “L” voltage.
3. If the V_{DD} voltage is lower than the minimum operating voltage, the output voltage is equalized to the pull-up voltage.
4. The output voltage is equalized to the pull-up voltage.
5. The V_{DD} voltage becomes higher than the release voltage (B point) which means Vref < V_{DD} x Rb / (Ra + Rb). The comparator output shifts from “L” to “H” voltage, and the output voltage is equalized to the GND voltage.

Note: There’s no hysteresis between the V_{DD} voltage and the released voltage.

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Detector Operation vs. Glitch Input Voltage

The RP300x has built-in rejection of fast transients on the V_{DD} pins. The rejection of transients depends on both the duration and the amplitude of the transient. The amplitude of the transient is measured from the bottom of the transient to the negative threshold voltage of the RP300x, as shown in Figure 18.

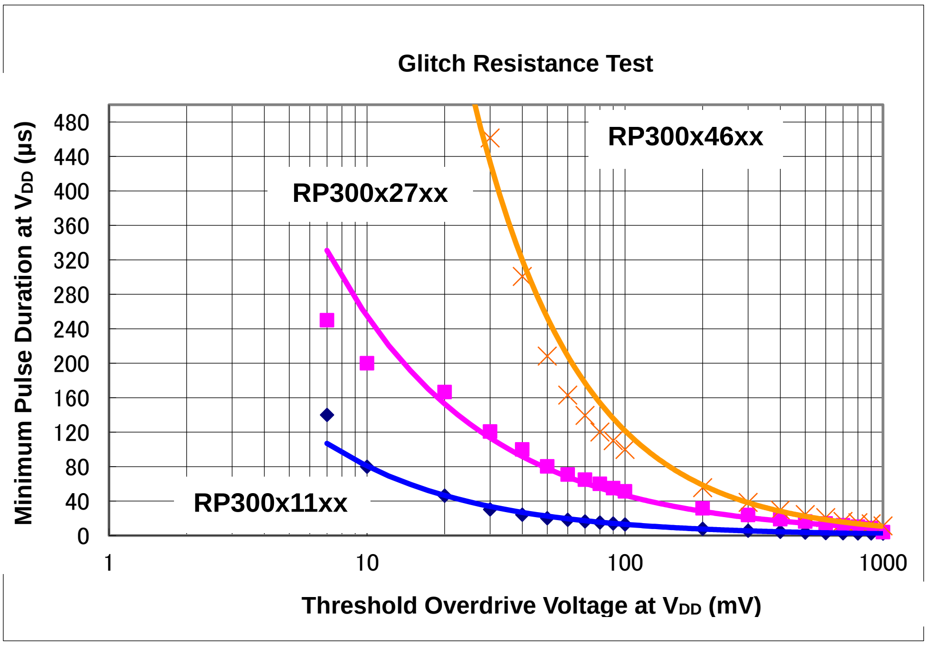


Figure 17. Minimum Pulse Duration at V_{DD} vs. Overdrive Voltage at V_{DD}

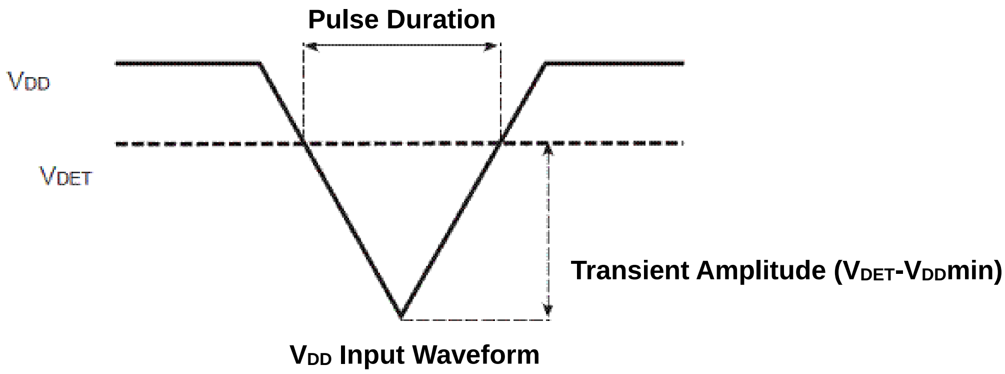


Figure 18. Voltage Transient Measurement

The RP300x does not respond to transients that are fast duration/ low amplitude or long duration/ small amplitude. Figure 17 shows the relationship between the transient amplitude and duration needed to trigger a reset. Any combination of duration and amplitude above the curve generates a reset signal.

TEST CIRCUITS

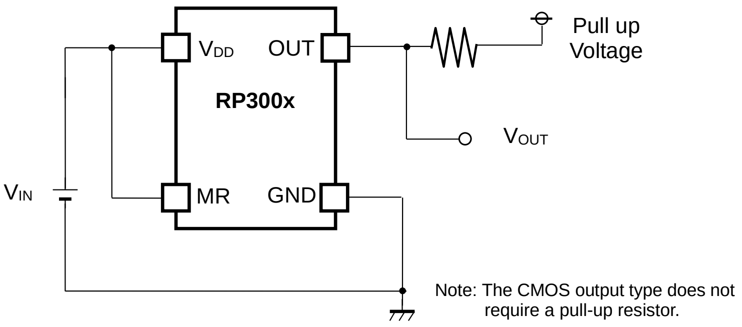


Figure 19. Basic Test Circuit

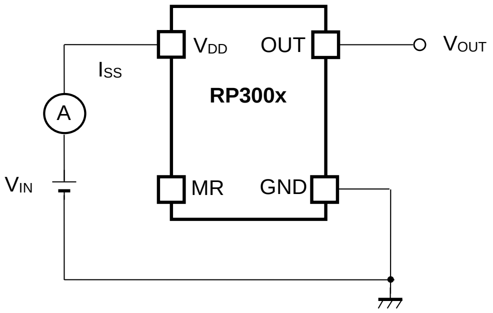


Figure 20. Test Circuit for Supply Current

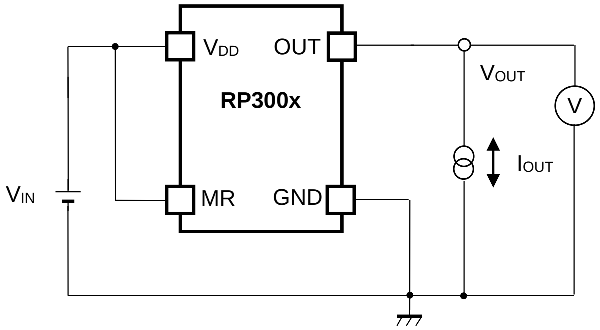


Figure 21. Test Circuit for Output Current

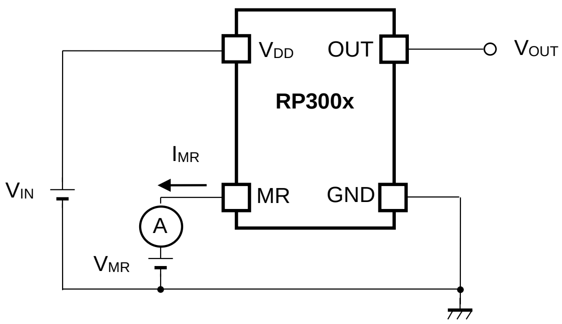
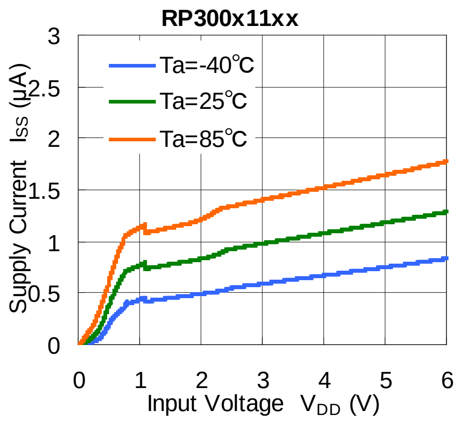
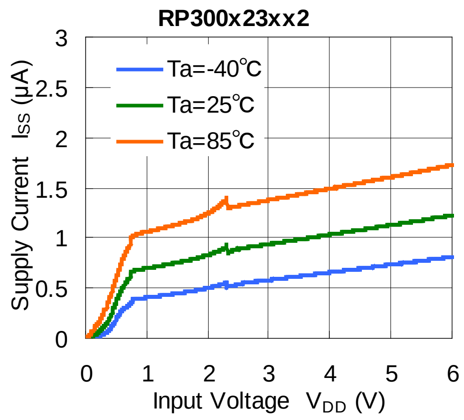


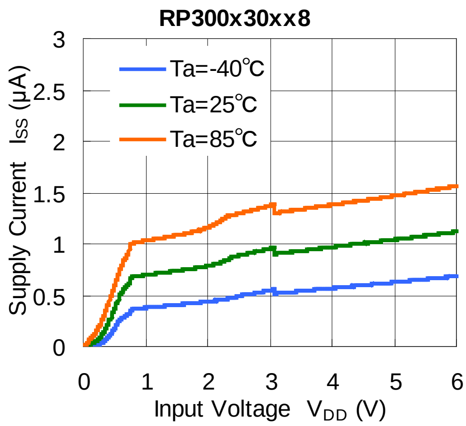
Figure 22. MR Pin Pull-up Resistor

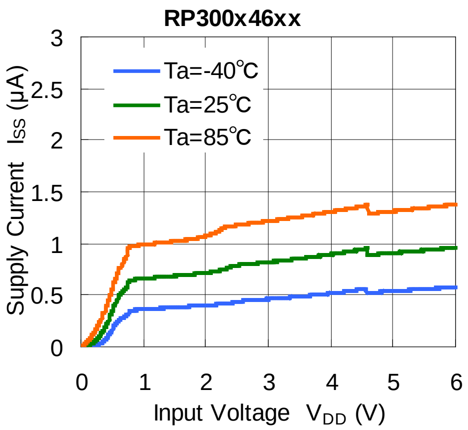
TYPICAL CHARACTERISTICS

1) Supply Current vs. Input Voltage

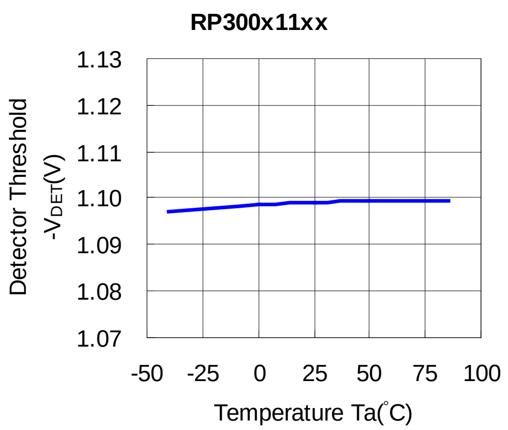


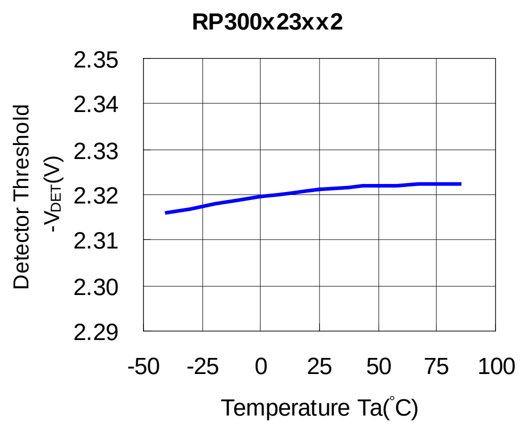




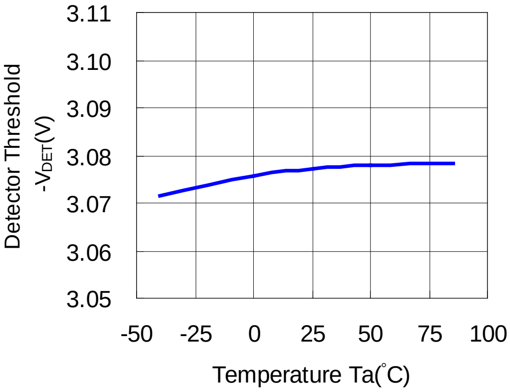


2) Detector Threshold vs. Temperature

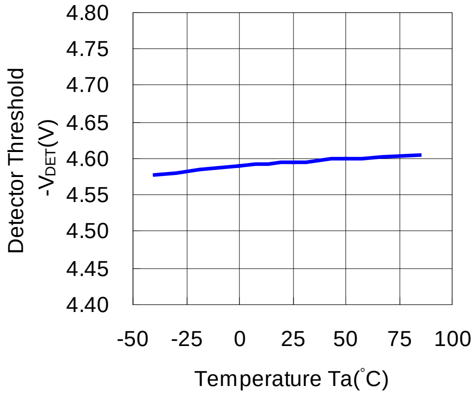




RP300x30xx8

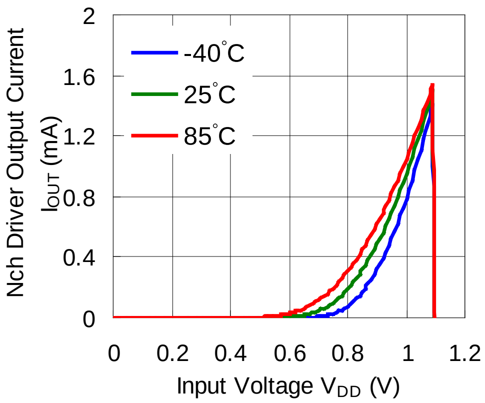


RP300x46xx

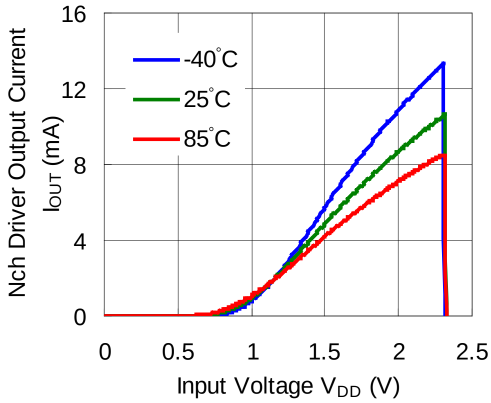


3) Nch Driver Output Current vs. Input Voltage

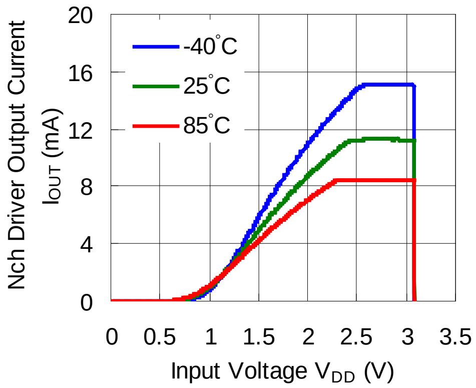
RP300x11xA/xC



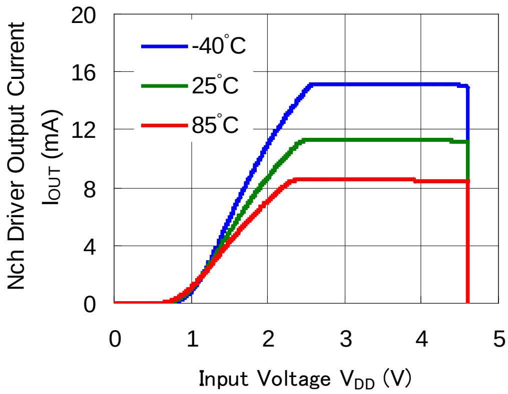
RP300x23xA2/xC2



RP300x30xA8/xC8



RP300x46xA/xC



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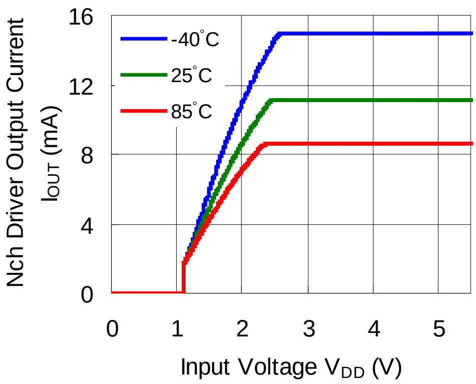
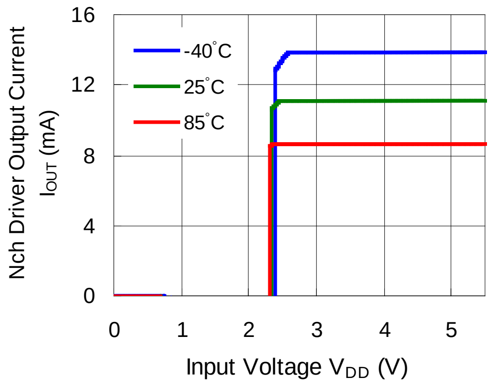
Nch Driver Inverting Output (custom IC)

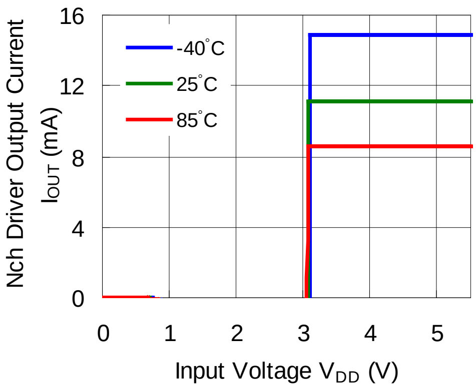
RP300x11xB



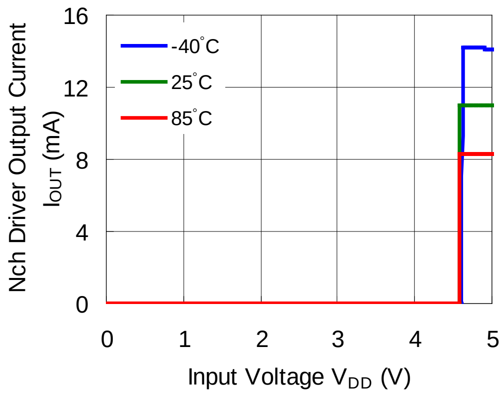
RP300x23xB2



RP300x30xB8

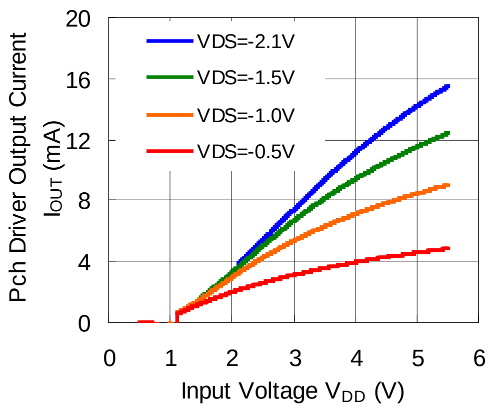


RP300x46xB

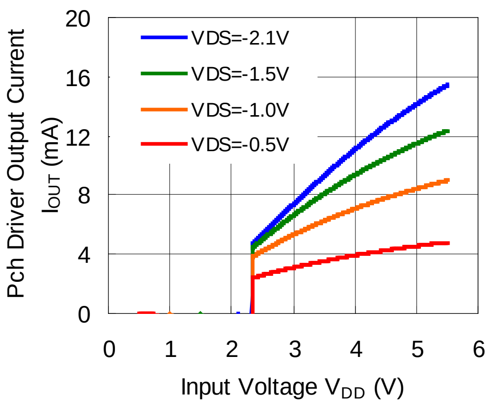


4) Pch Driver Output Current vs. Input Voltage

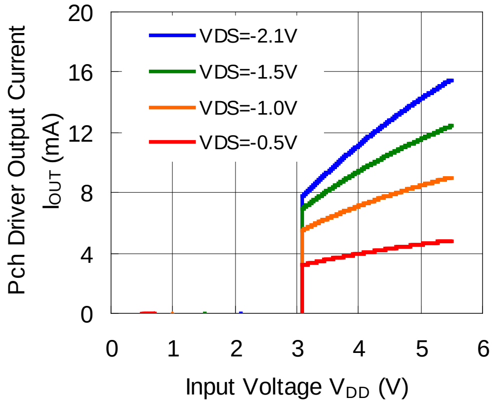
RP300x11xC



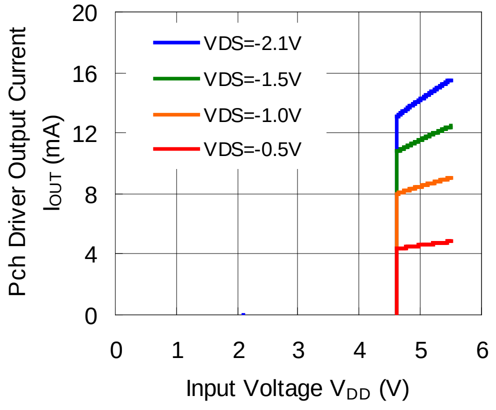
RP300x23xC2



RP300x30xC8

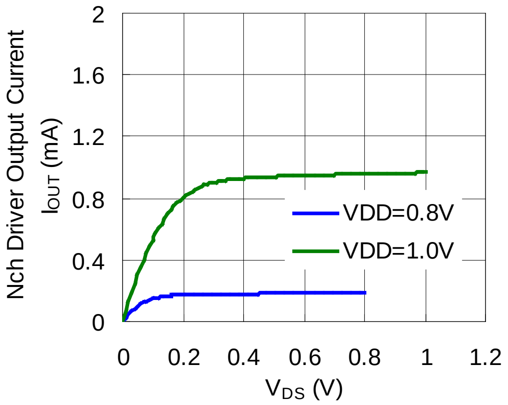


RP300x46xC

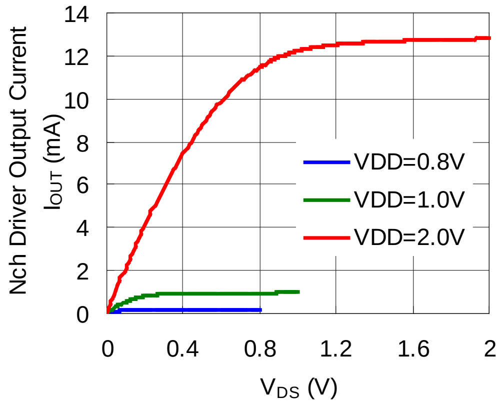


5) Nch Driver Output Current vs. V_{DS}

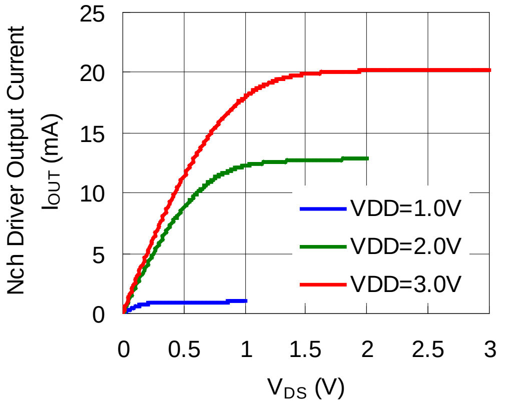
RP300x11xA/xC



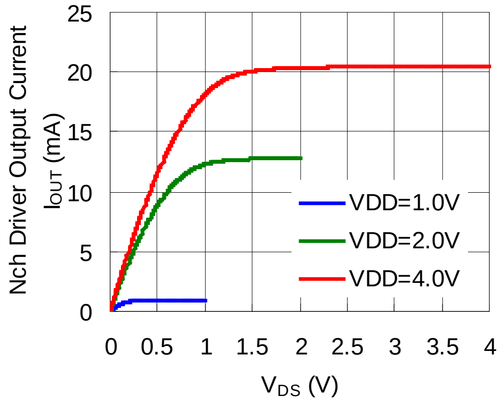
RP300x23xA2/xC2



RP300x30xA8/xC8

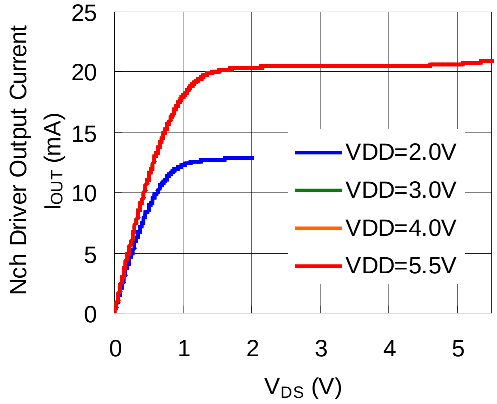


RP300x46xA/xC

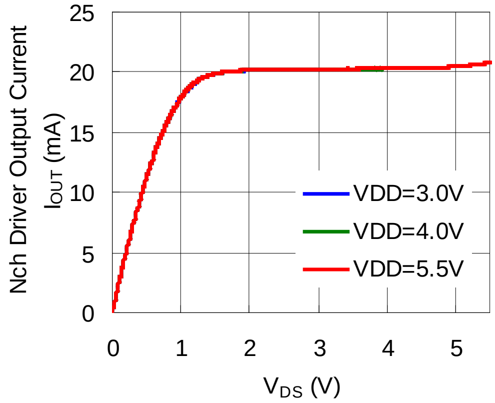


Nch Driver Inverting Output (custom IC)

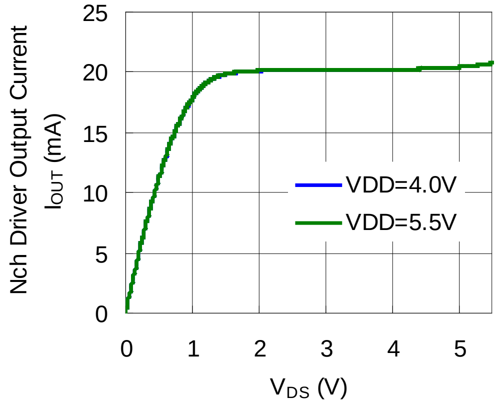
RP300x11xB



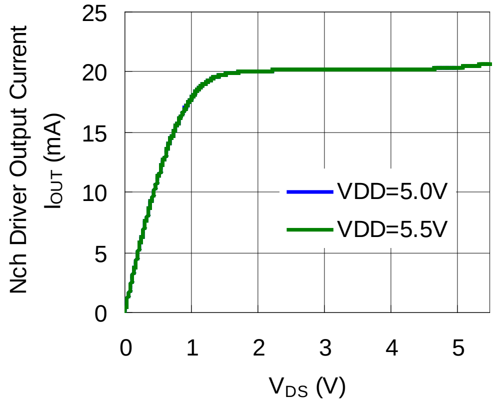
RP300x23xB2



RP300x30xB8

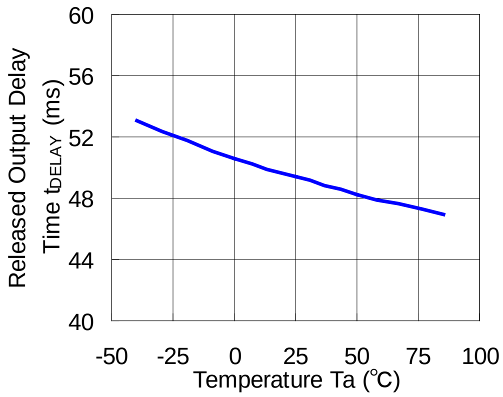


RP300x46xB

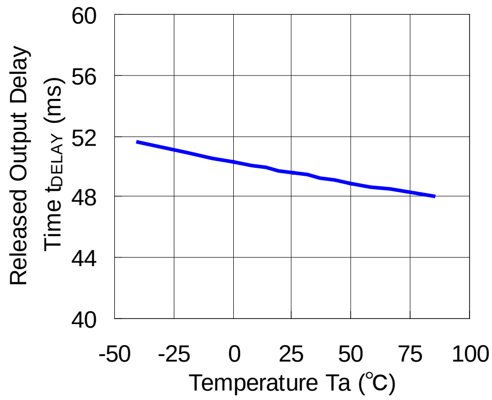


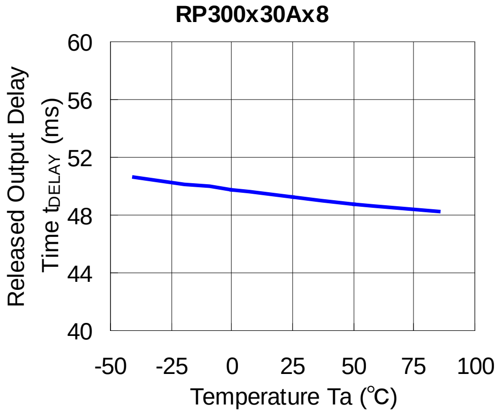
6) Released Output Delay Time vs. Temperature

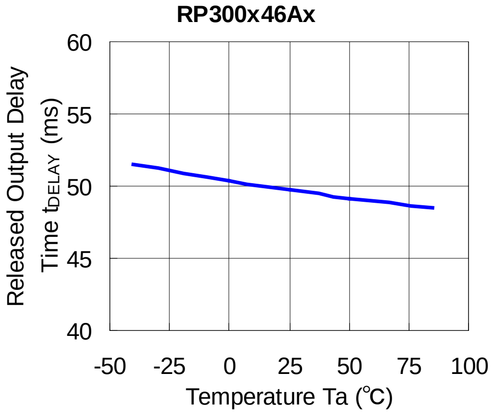
RP300x11Ax

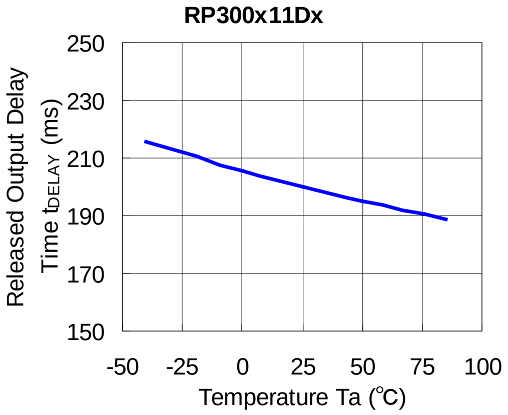


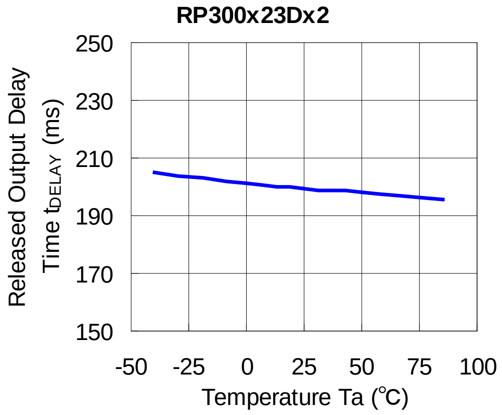
RP300x23Ax2

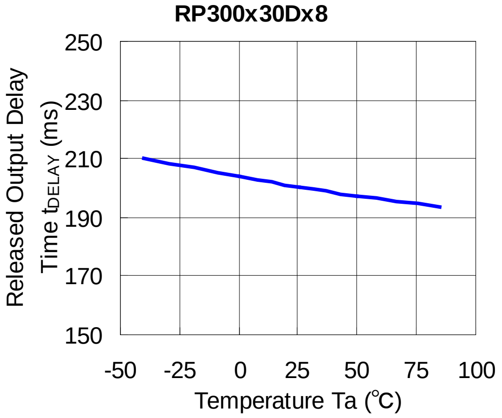


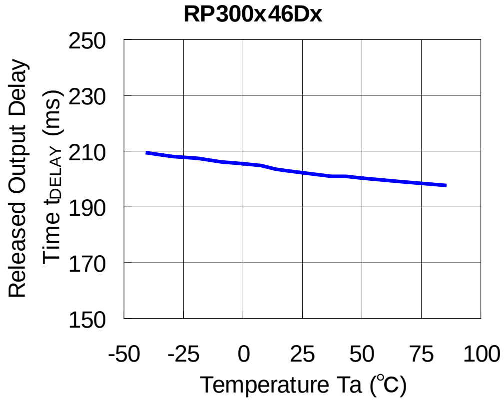

RP300x30Ax8
Released Output Delay Time t_{DELAY} (ms)
60
56
52
48
44
40
-50
-25
0
25
50
75
100
Temperature Ta (℃)


RP300x46Ax
Released Output Delay Time t_{DELAY} (ms)
60
55
50
45
40
-50
-25
0
25
50
75
100
Temperature Ta (℃)


RP300x11Dx
Released Output Delay Time t_{DELAY} (ms)
250
230
210
190
170
150
-50
-25
0
25
50
75
100
Temperature Ta (℃)


RP300x23Dx2
Released Output Delay Time t_{DELAY} (ms)
250
230
210
190
170
150
-50
-25
0
25
50
75
100
Temperature Ta (℃)


RP300x30Dx8
Released Output Delay Time t_{DELAY} (ms)
250
230
210
190
170
150
-50
-25
0
25
50
75
100
Temperature Ta (℃)


RP300x46Dx
Released Output Delay Time t_{DELAY} (ms)
250
230
210
190
170
150
-50
-25
0
25
50
75
100
Temperature Ta (℃)

TECHNICAL NOTES

When connecting resistors to the device's input pin

When connecting a resistor (R1) to an input of this device, the input voltage decreases by [Device's Consumption Current] x [Resistance Value] only. And, the cross conduction current*[1], which occurs when changing from the detecting state to the release state, is decreased the input voltage by [Cross Conduction Current] x [Resistance Value] only. And then, this device will enter the re-detecting state if the input voltage reduction is larger than the difference between the detector voltage and the released voltage.

When the input resistance value is large and the VDD is gone up at mildly in the vicinity of the released voltage, repeating the above operation may result in the occurrence of output.

As shown in Figure A/B, set R1 to become 100 kΩ or less as a guide, and connect C_{IN} of 0.1 μF and more to between the input pin and GND. Besides, make evaluations including temperature properties under the actual usage condition, with using the evaluation board like this way. As a result, make sure that the cross conduction current has no problem.

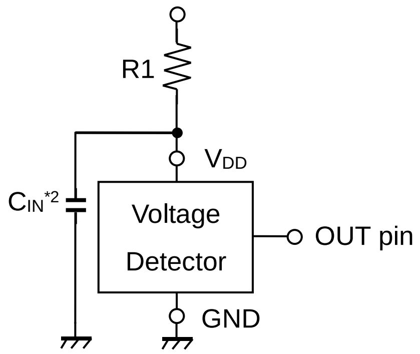


Figure A

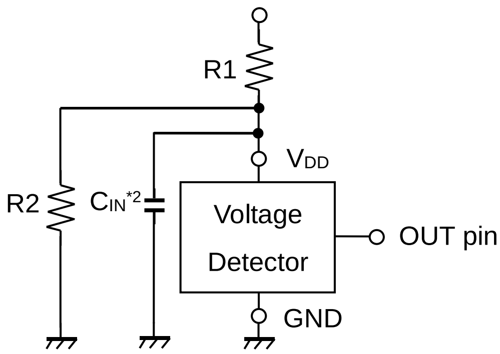


Figure B

*[1] In the CMOS output type, a charging current for OUT pin is included.

*[2] Note the bias dependence of capacitors.

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