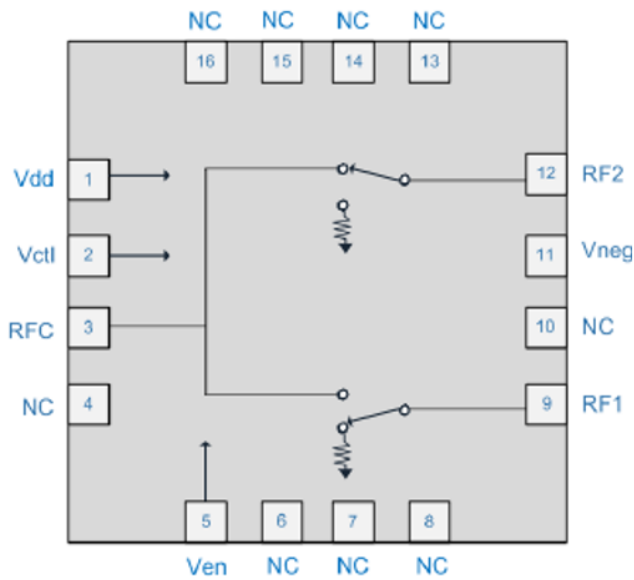


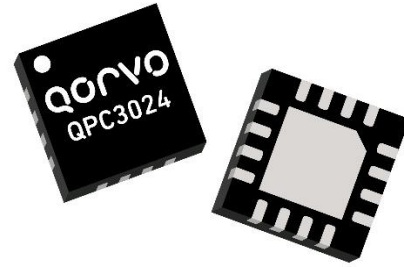
### Product Overview

The QPC3024 is a 75Ω Silicon on Insulator (SOI) single-pole, double throw (SPDT) switch designed for use in CATV, satellite set top, and other high performance communications systems. It offers a high isolation symmetric topology with excellent linearity and power handling capability. No blocking caps are necessary on the RF ports. The design is non-reflective such that RF ports 1 and 2 are terminated in in the off-state. The  $V_{EN}$  pin allows for a terminated “all-off state”. Applying a negative voltage to the  $V_{NEG}$  pin will turn the negative voltage generator off and allow for external supply input.

### Functional Block Diagram



Top View



16 Pad 4 x 4 mm QFN Package

### Key Features

- 5 MHz to 3000 MHz Operation
- Symmetric SPDT
- Non-Reflective (RF1, RF2)
- Terminated All-Off State
- No Blocking Caps Required Unless Voltage on RF Line
- High Isolation: >65 dB at 1.2 GHz
- High Input IP3: >60 dBm
- Option to Turn Off Negative Voltage Generator and Supply  $V_{NEG}$  Externally
- 2 kV ESD
- +1.8 V Logic Compatible

### Applications

- MDU Amplifiers
- Point To Point
- Optical Nodes
- Set Top Box
- PCTV
- Multi-tuner DVR

### Ordering Information

Part No.	Description
QPC3024SQ	Sample bag with 25 pieces
QPC3024SR	7" Reel with 100 pieces
QPC3024TR13	13" Reel with 2500 pieces
QPC3024PCK	5 – 3000 MHz PCBA with 5 pc. sample bag

### Absolute Maximum Ratings

Parameter	Rating
Control Voltage ( $V_{CTL}$ , $V_{EN}$ )	+6.0 V
Supply Voltage ( $V_{DD}$ )	+6.0 V
External Negative Supply ( $V_{NEG}$ )	-6.0 V
Maximum CW Input Power at 25°C	+36 dBm
Maximum CW Input Power, Terminated Port	+28 dBm
Junction Temperature	+125°C
Storage Temperature Range	-40 to +150°C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

### Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage, $V_{DD}$	+2.7	+3	+5.5	V
Supply Voltage, $V_{NEG}$	-5.5	-5	-3	V
Temperature Range	-40		+105	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

### Electrical Specifications

Parameter	Conditions <sup>(1)</sup>	Min	Typ	Max	Units
Frequency Range		5		3000	MHz
Insertion Loss	5 MHz		0.38		dB
	50 MHz		0.42		
	1.2 GHz		0.82		
	2 GHz		0.83		
	3 GHz		1.4		
Isolation (RFC to RF1/RF2)	5 MHz		75		dB
	50 MHz		70		
	1.2 GHz		66		
	2 GHz		66		
	3 GHz		56		
Isolation (RF1 to RF2)	5 MHz		75		dB
	50 MHz		70		
	1.2 GHz		56		
	2 GHz		52		
	3 GHz		45		
Return Loss (RFC On-state)	5 MHz		33		dB
	50 MHz		32		
	1.2 GHz		15		
	2 GHz		17		
	3 GHz		13		
Return Loss (RF1/RF2 Off-state) Terminated Ports	5 MHz		40		dB
	50 MHz		39		
	1.2 GHz		19		
	2 GHz		18		
	3 GHz		25		

Notes:

1. Test Conditions Unless Otherwise Specified:  $T_A = +25^\circ\text{C}$ ,  $V_{CTL} = 0/+5\text{ V}$ ,  $V_{DD} = +5\text{ V}$ , 75 Ω system.

### Electrical Specifications (cont'd.)

Parameter	Conditions <sup>(1)</sup>	Min	Typ	Max	Units
Input IP3 <sup>(2)</sup>	1 GHz +12 dBm input power per tone, 1 MHz tone spacing		61		dBm
Input 1dB Compression Point <sup>(2)</sup>	1 GHz		36		
Input 0.1dB Compression Point <sup>(2)</sup>	1 GHz		36		
CSO	130 Channel, Flat Tilt, +42 dBmV/ch		>100		dBc
CTB	130 Channel, Flat Tilt, +42 dBmV/ch		>90		
Turn On Time	90% VDD to steady state harmonics		7.4		μs
Settling Time	50% control to steady state harmonics		3.8		
Switching Speed	50% control to 10/90% RF		1.5		
NVG Spurs	Internal NVG on (F<10MHz)		-113		dBm
Harmonics-2nd	5 MHz		-77		dBc
	17 MHz		-82		
	170 MHz		-95		
	800 MHz		-106		
Harmonics-3rd	5 MHz		-93		dBc
	17 MHz		-115		
	170 MHz		-119		
	800 MHz		-121		

Notes:

1. Test Conditions Unless Otherwise Specified: T<sub>A</sub> = +25 °C, V<sub>CTL</sub> = 0/+5 V, V<sub>DD</sub> = +5 V, V<sub>NEG</sub> = -5 V, 75 Ω system. Drive RFC, RFx output.
2. Tested at 50Ω.

### Electrical Specifications - Power Supply

Parameter	Conditions <sup>(1)</sup>	Min	Typ	Max	Units
Supply Current (I <sub>DD</sub> )	V <sub>DD</sub> = +5.0V		130	200	μA
Control Current (I <sub>CTL</sub> , I <sub>EN</sub> )	V <sub>CTL</sub> = +5.0V		0.5	5	μA
Low Control Voltage (V <sub>CTL</sub> , V <sub>EN</sub> )	+1.8V Logic compatible	0		0.63	V
High Control Voltage (V <sub>CTL</sub> , V <sub>EN</sub> )		1.1		VDD	V

### Maximum Operating Power

Input	State	VEN	Power at 85C (dBm)	Power at 105C (dBm)	Theta-J (°C/W)
RFC, RF1/2	On	Low	34 <sup>(1)</sup>	31 <sup>(1)</sup>	125
RFC	Both Off	High	30	27	N/A
RF1/2	Off	Low or High	27	24	77
RF1/2 (Simultaneous)	Both Off	High	29 <sup>(2)</sup>	26 <sup>(2)</sup>	50

Notes:

1. Assuming load VSWR <3:1, for high VSWR loads, this value reduces by 3dB.
2. Total power in both loads being driving simultaneously.

### Power Supply Sequencing Requirements

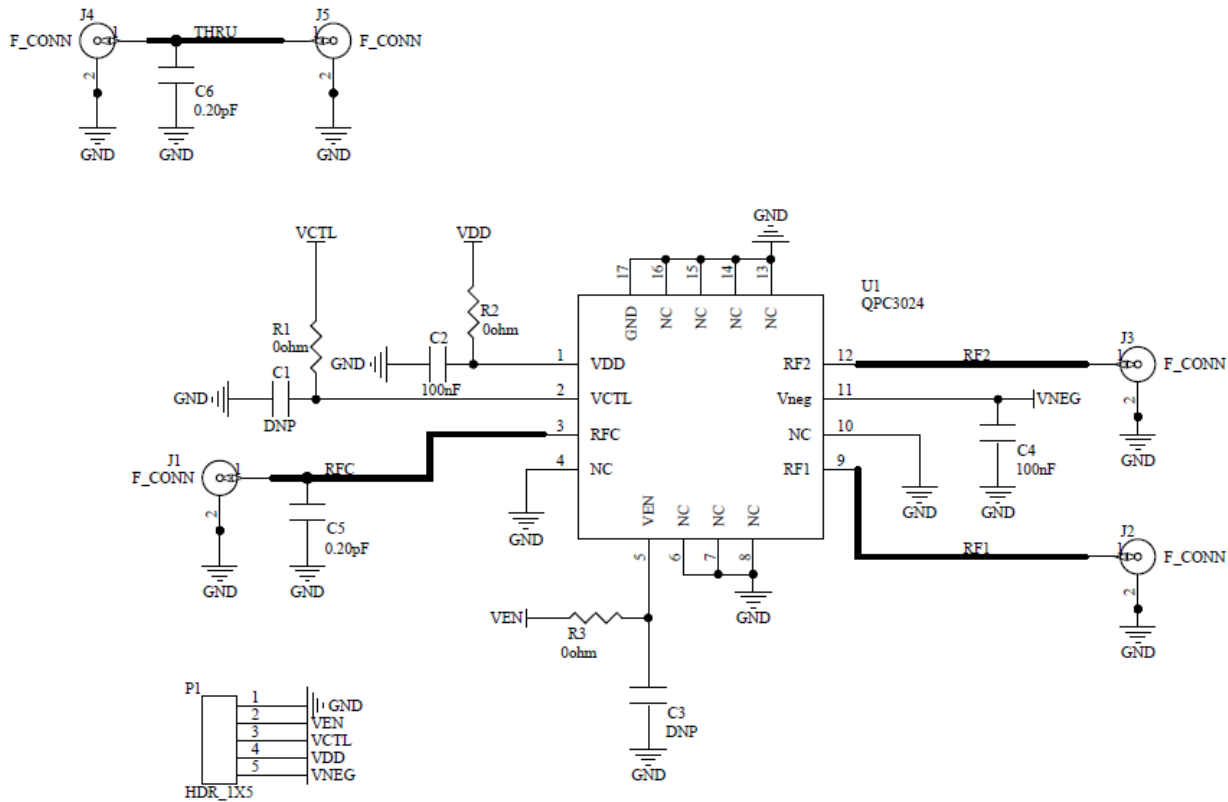
No power supply sequencing is required if VCTL or VEN are less than 4.1V. When VCTL and VEN are greater than 4.1V, for best reliability, apply V<sub>DD</sub> before the applying the control voltage.

If the internal Negative Voltage Generator (NVG) is disabled by applying a negative voltage on V<sub>NEG</sub>, V<sub>DD</sub> must be power cycled after changing V<sub>NEG</sub> to 0V to enable it again.

### Truth Table

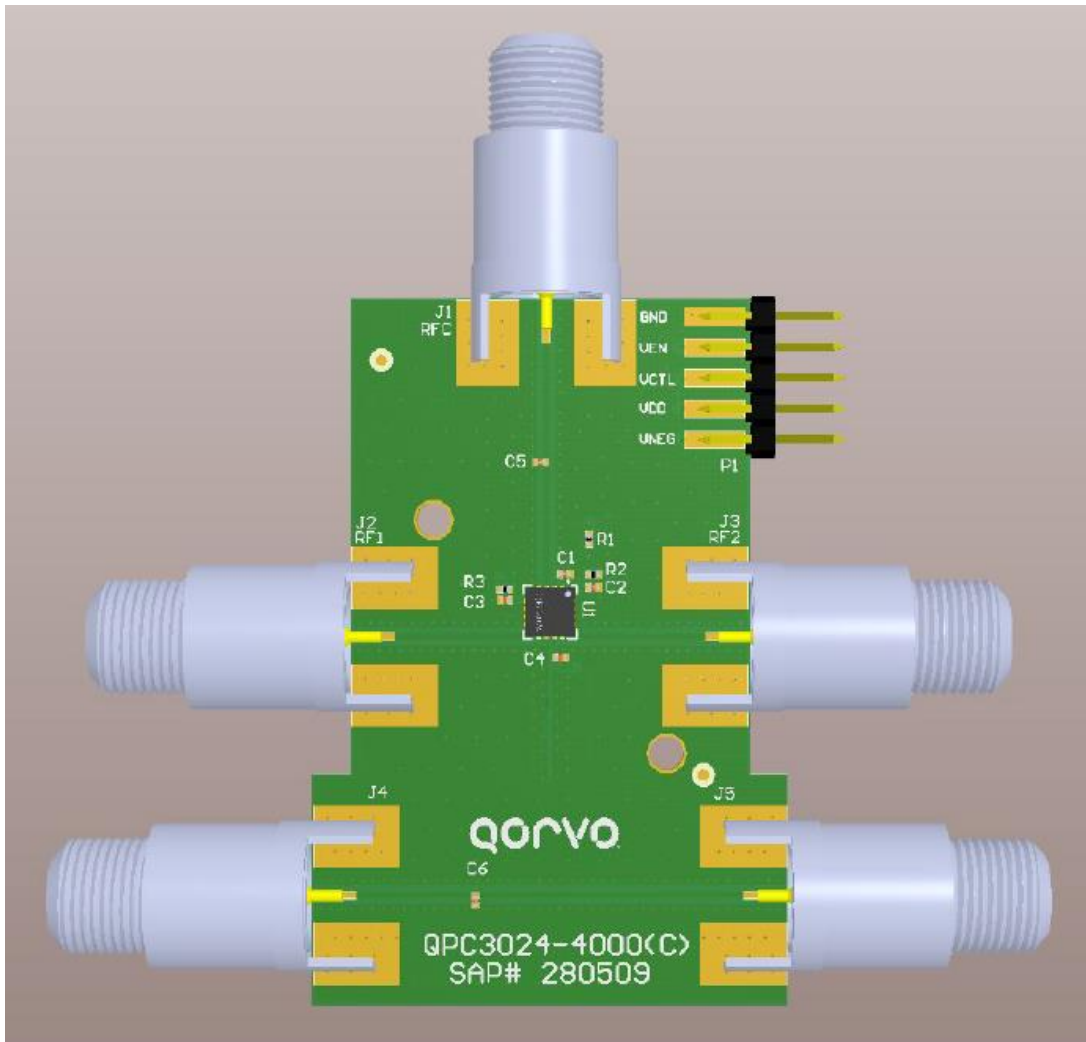
Control Input		Signal Path State	
V <sub>CTL</sub>	V <sub>EN</sub>	RFC-RF1	RFC-RF2
0	0	On	Off
1	0	Off	On
0	1	Off	Off
1	1	Off	Off

### 5-3000 MHz Evaluation Board Schematic (QPC3024PCK)



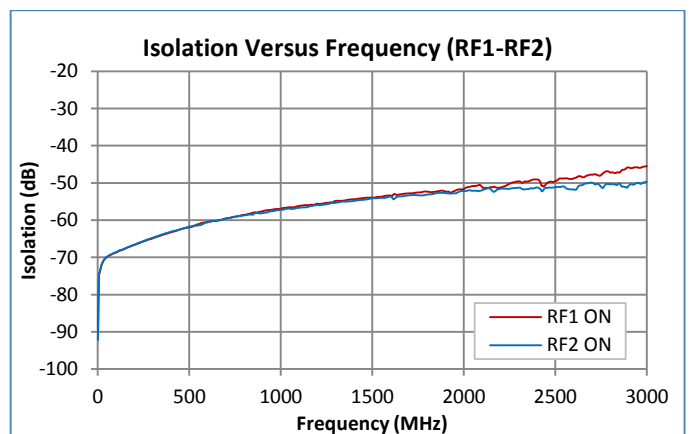
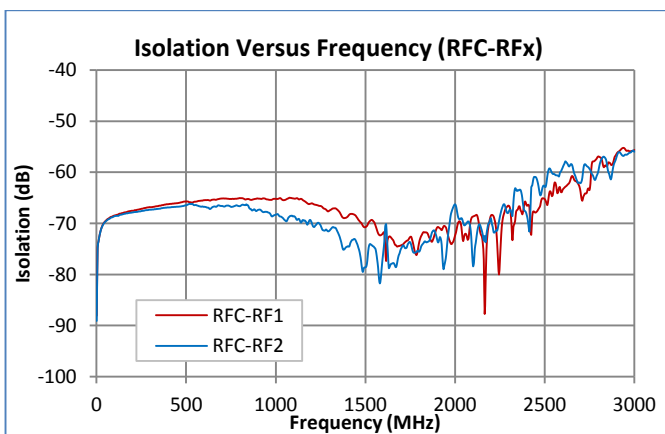
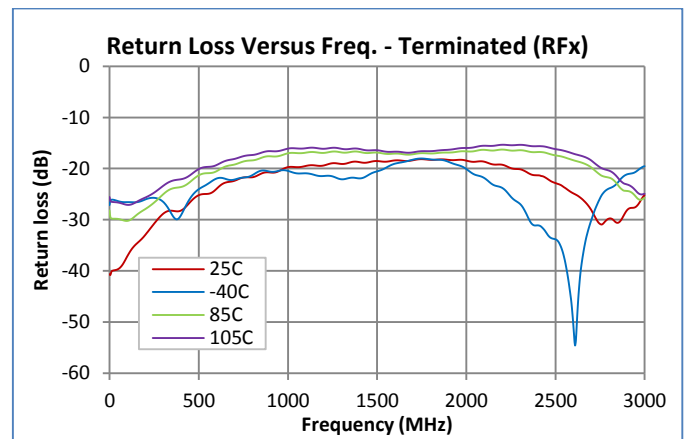
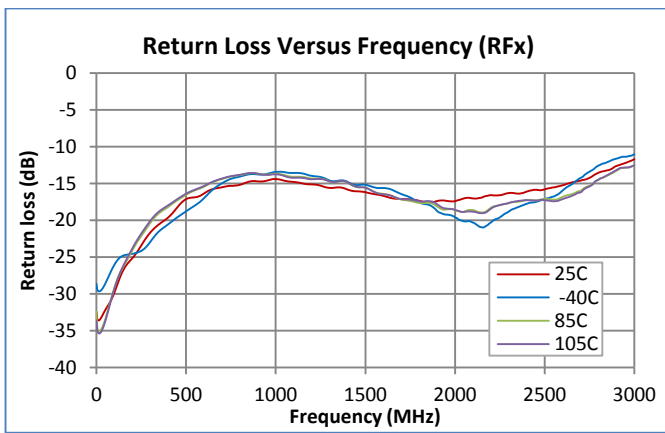
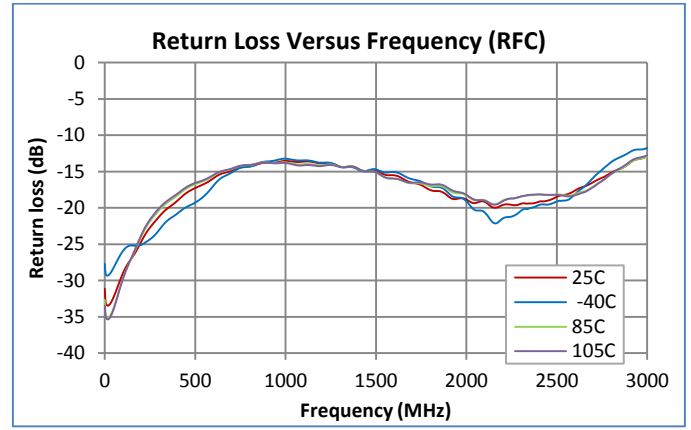
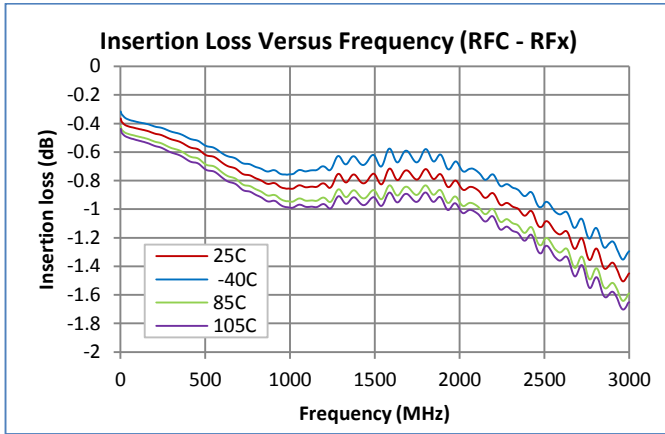
Ref. Designator	Description	Manufacturer	Part Number
PCB	Evaluation Board PCB	Viasystems	QPC3024-4000
U1	75ohm High Isolation Switch	Qorvo	QPC3024SB
J1, J2, J3, J4, J5	Conn, Type F, Edge Mount, 75 Ω, 0.065"	Genesis Technology	GT20-300204
R1, R2, R3	0 Ω RES, 0402	Panasonic	ERJ-2GE0R00X
P1	Conn, HDR, ST, 5-Pin, T/H	Molex	22-28-4053
C2, C4	100nF 10% X7R 16V CAP, 0402	Murata	GJM1555C1HR20RB12D
C5, C6	0.2pF +/- 0.03pF COG 50V CAP, 0402	Murata	GRM155R71C104KA88D
C1, C3	DNP	N/A	N/A

### Evaluation Board Assembly Drawing



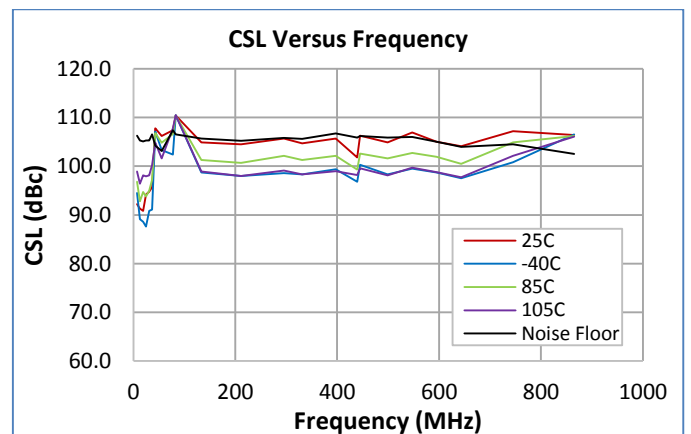
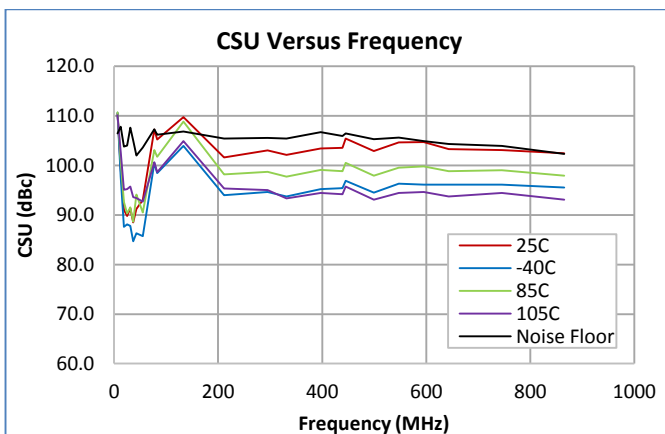
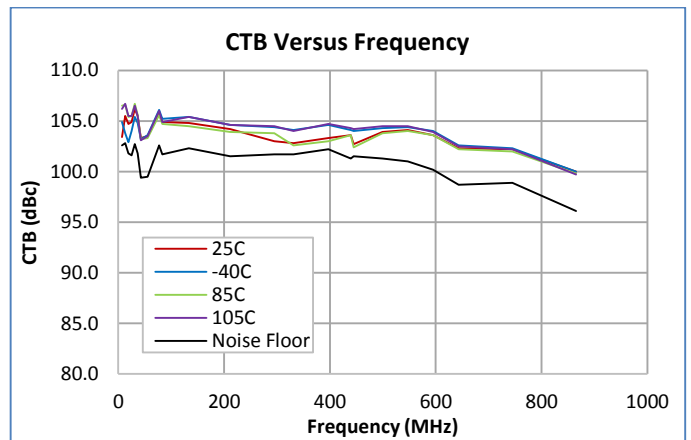
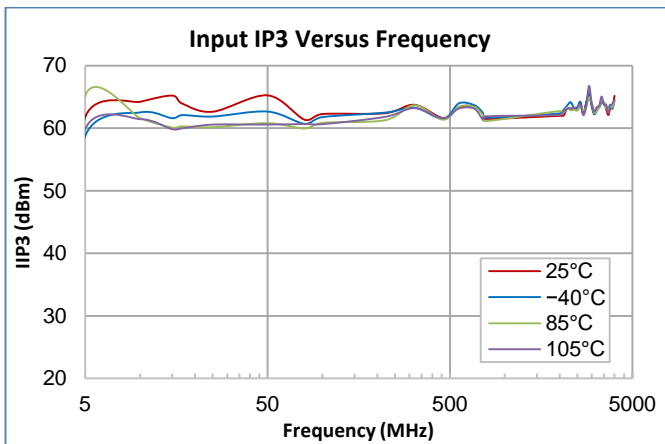
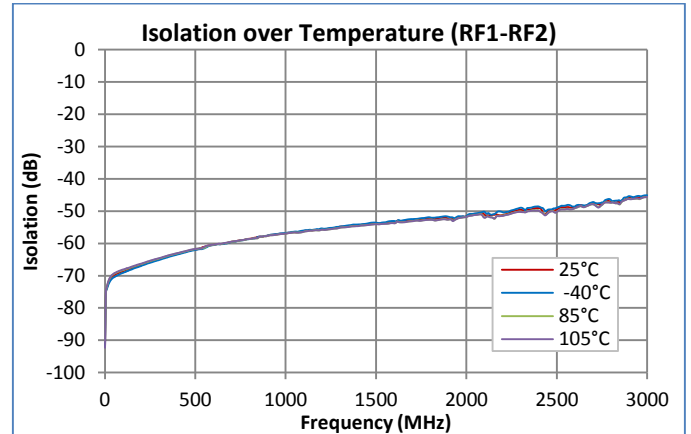
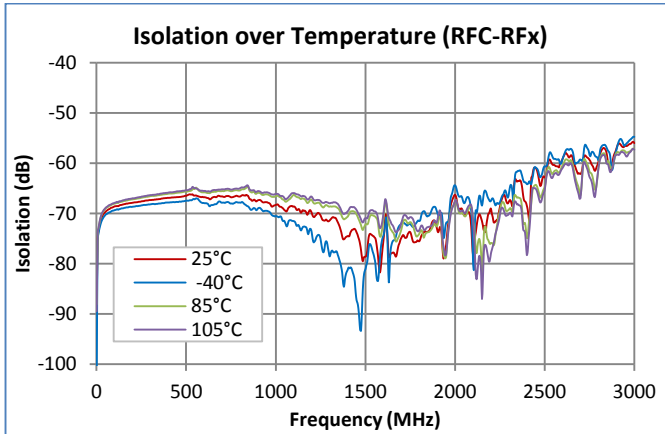
Performance Plots

Test conditions unless otherwise noted:  $V_{DD} = +5V$ ,  $V_{NEG} = -5V$ ,  $Temp = +25^{\circ}C$ ,  $Z_o = 75\Omega$



### Performance Plots (cont'd.)

Test conditions unless otherwise noted:  $V_{DD} = +5V$ ,  $V_{NEG} = -5V$  Temp =  $+25^\circ C$ ,  $Z_o = 75\Omega$



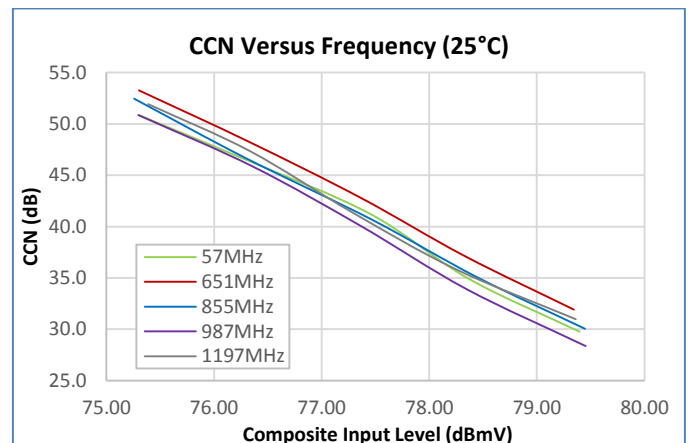
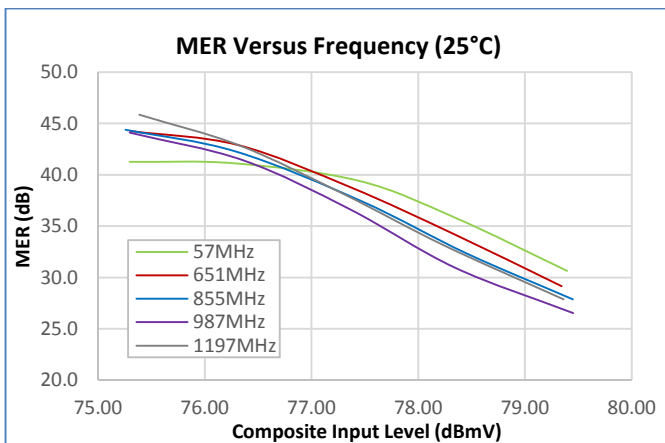
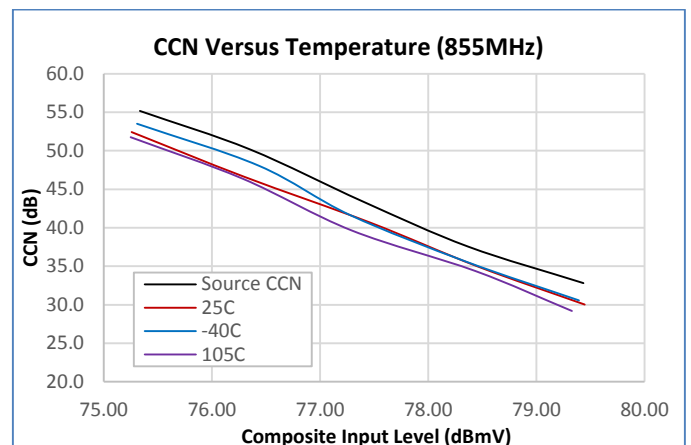
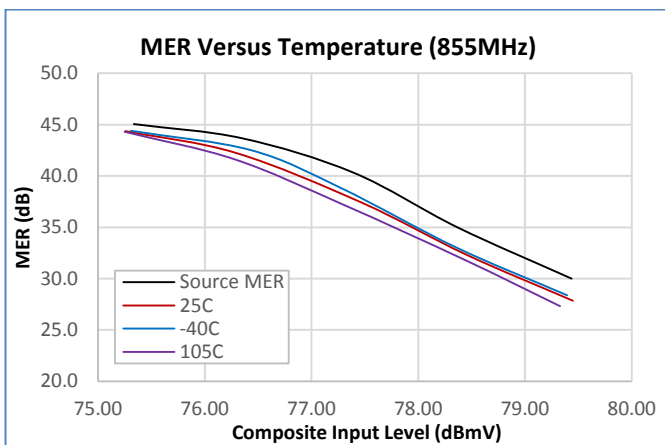
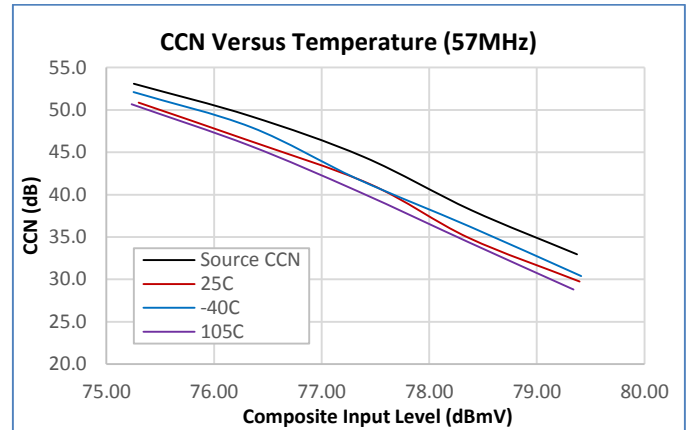
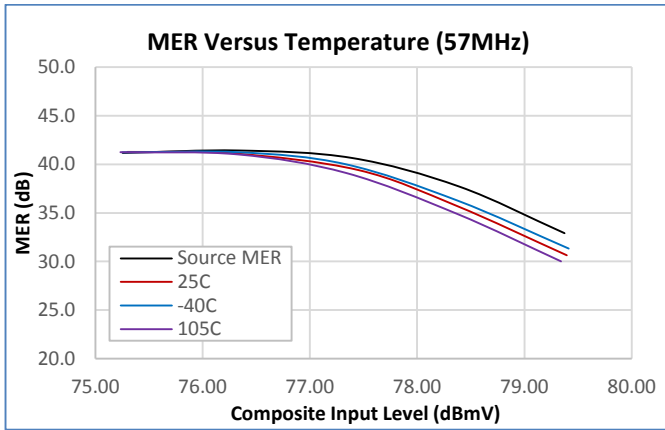
**Test Conditions:**

1. IIP3: Two tone, 50Ω, +12dBm per Tone.
2. CSO/CTB: 130 Channels, 42dBmV per Channel, Flat Tilt.



### Performance Plots (cont'd.)

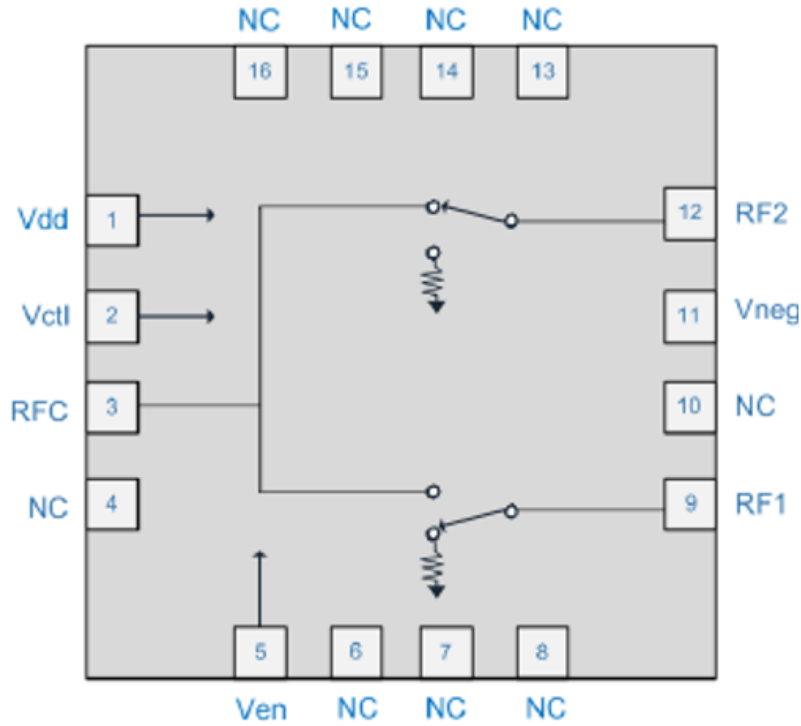
Test conditions unless otherwise noted:  $V_{DD} = +5V$ ,  $V_{NEG} = -5V$ , Temp =  $+25^{\circ}C$ ,  $Z_o = 75\Omega$



MER/CCN Test Conditions:

1. 190 QAM256 Channels, 57-1215MHz, ITU-T J.83, Annex B
2. CCN test procedure according to ANSI/SCTE 17. System BW 5.36MHz.

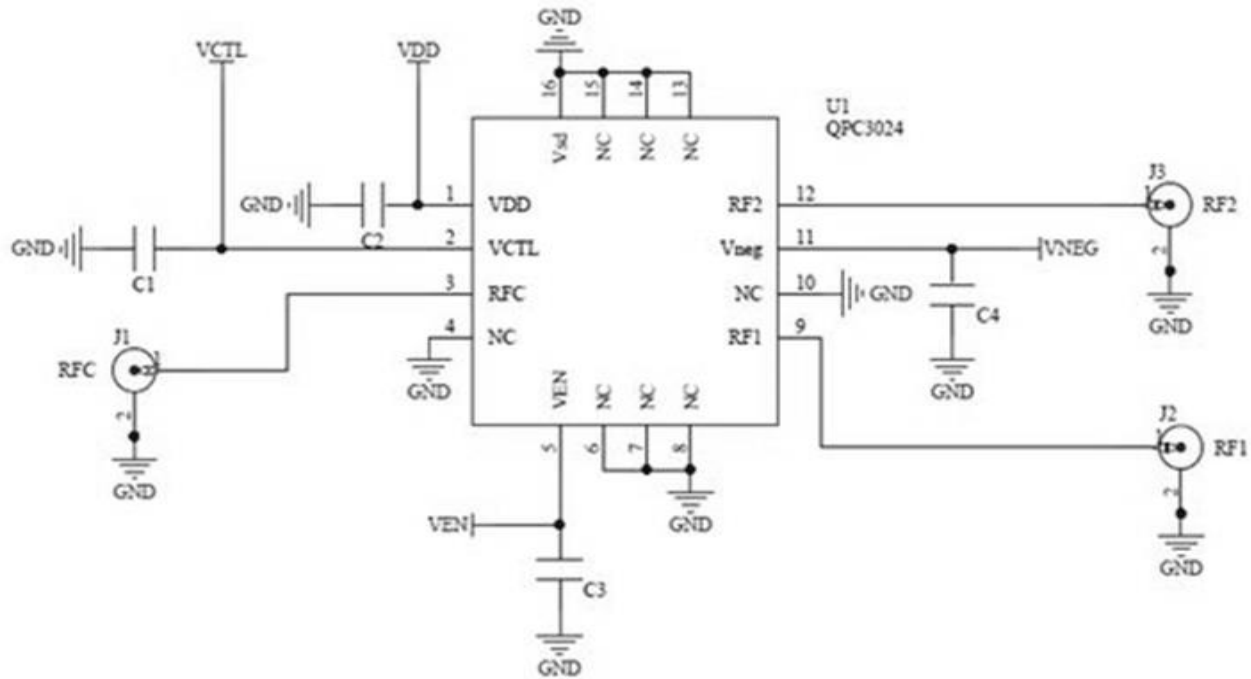
### Pad Configuration and Description



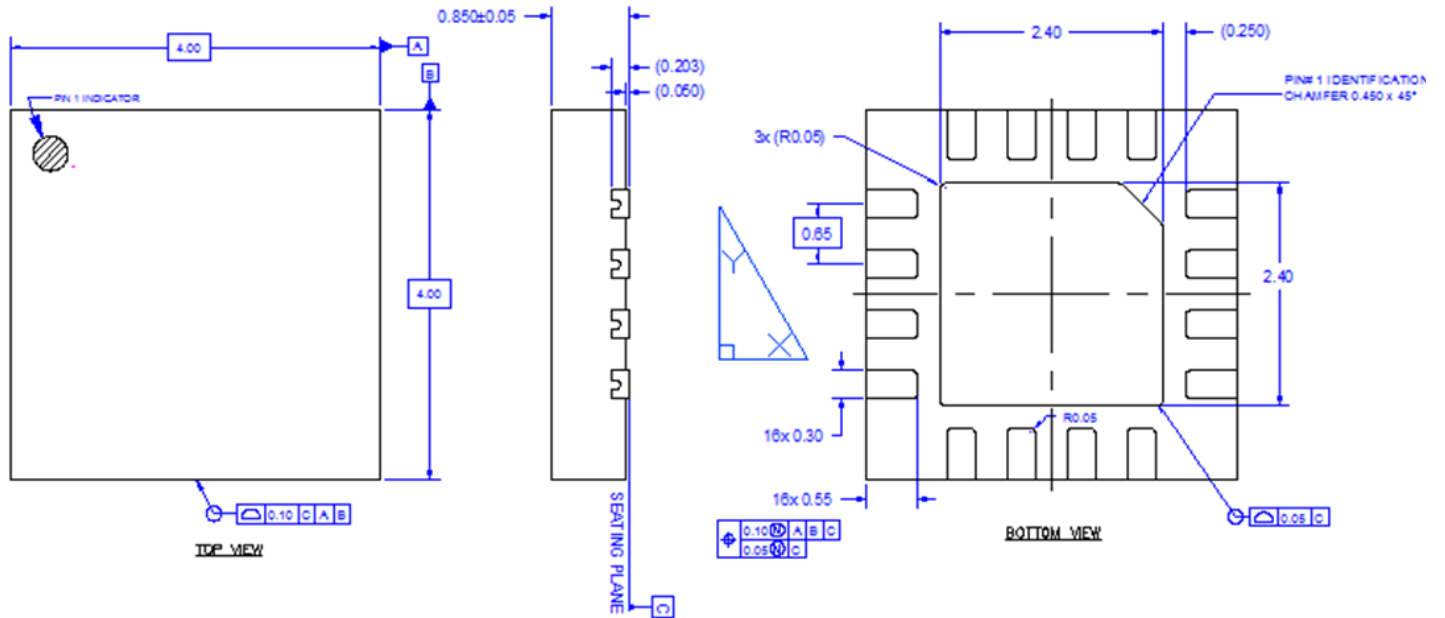
Top View

Pad No.	Label	Description
1	VDD	Supply Voltage
2	VCTL	Logic Control Input
3	RFC	RF Common Port
4	NC	Grounding this pin is recommended for performance
5	VEN	Logic input for putting switch in "all-off state". Logic high for "all-off state".
6, 7, 8, 13, 14, 15, 16	NC	Grounding this pin is recommended to maximize isolation
9	RF1	RF Port 1
10	NC	Grounding this pin is recommended for performance
11	VNEG	Negative Voltage Generator (NVG) control pin. Supply GND (Low inductive path to ground) to enable internal NVG or supply -2.7 V to -5 V to disable internal NVG. Once disabled, internal NVG cannot be enabled without cycling V <sub>DD</sub> .
12	RF2	RF Port 2
EPAD	GND	RF and DC Ground: Must be soldered to EVB ground plane.

### Applications Schematic; 5-1200MHz



### Package Dimensions

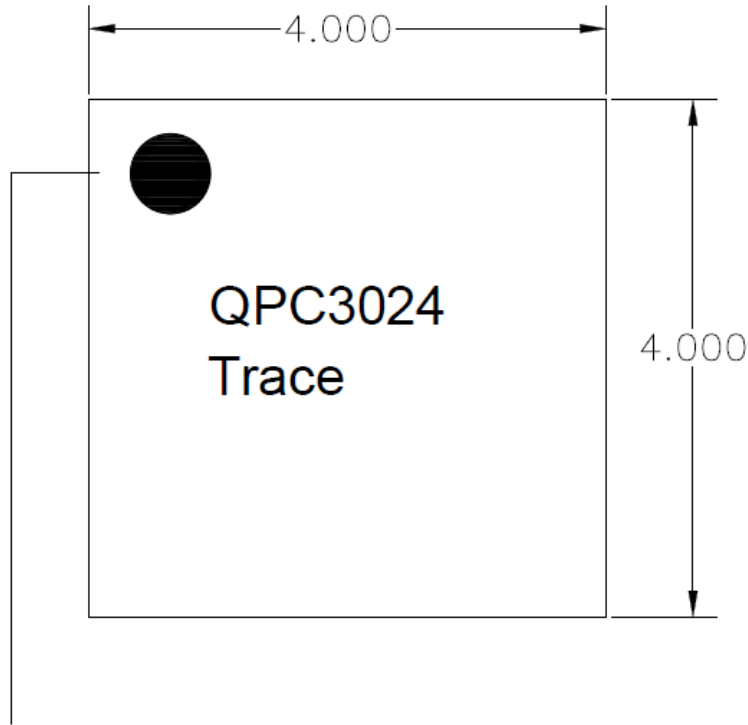


**Notes:**

1. All dimensions are in millimeters. Angles are in degrees.
2. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
3. Contact plating: NiPdAu

Package Marking

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Pin 1 Indicator

Trace Code to be assigned by SubCon

---

### Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1000V, Class C3	ANSI/ESDA/JEDEC JS-002-2014
ESD – Charged Device Model (CDM)	2000V, Class 2	ANSI/ESDA/JEDEC JS-002-2014
MSL – Moisture Sensitivity Level	Level 2	IPC/JEDEC J-STD-020



Caution!  
ESD-Sensitive Device

### Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.

Solder profiles available upon request.

Contact plating: NiPdAu

### RoHS Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment). This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C<sub>15</sub>H<sub>12</sub>Br<sub>4</sub>O<sub>2</sub>) Free
- PFOS Free
- SVHC Free
- Qorvo Green



### Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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Web: [www.qorvo.com](http://www.qorvo.com)

Email: [customer.support@qorvo.com](mailto:customer.support@qorvo.com)

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