



**SANYO Semiconductors**

**DATA SHEET**

An ON Semiconductor Company

Bi-CMOS LSI

**LV8413GP** — **For DSC, and Cell Phone Camera Modules**  
**H-Bridge × 2-channel Motor Driver**

## Overview

The LV8413GP is an H-bridge × 2-channel motor driver IC and is able to control 4 modes of forward, reverse, brake, and standby.

This IC housed in a miniature package is optimum for use in a stepping motor driving system for DSC or a camera module of cell phones.

## Features

- Saturation drive H-bridge : 2-channels
- Built-in thermal protection circuit
- Built-in low voltage malfunction prevention circuit
- Incorporates a transistor for driving photosensors

## Specifications

### Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage 1	VM max		6	V
Power supply voltage 2	V <sub>CC</sub> max		6	V
Output peak current	I <sub>O</sub> peak	Outs 1 to 4, t ≤ 10msec, ON-duty ≤ 20%	600	mA
Output continuous current 1	I <sub>O</sub> max1	Outs 1 to 4	400	mA
Output continuous current 2	I <sub>O</sub> max2	PI	15	mA
Allowable power dissipation	P <sub>d</sub> max	Mounted on a circuit board*	0.7	W
Operating temperature	T <sub>opr</sub>		-30 to +85	°C
Storage temperature	T <sub>stg</sub>		-55 to +150	°C

\* Specified circuit board : 50.0mm × 40.0mm × 0.8mm : glass epoxy four-layer board (2S2P)

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# LV8413GP

## Recommended Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings		Unit
Power supply voltage range 1	$\text{VM}$		2.5 to 5.5		V
Power supply voltage range 2	$\text{V}_{\text{CC}}$		2.5 to 5.5		V
Logic input voltage range	$\text{V}_{\text{IN}}$		0 to $\text{V}_{\text{CC}} + 0.3$		V
Input frequency	$f_{\text{IN}}$	IN1 to 4, INA	to 100		kHz

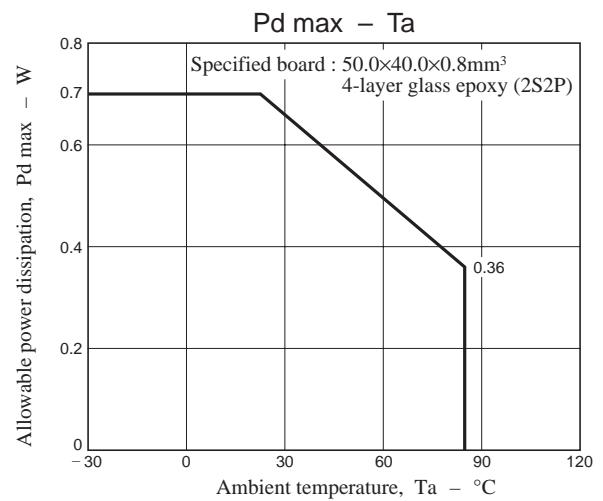
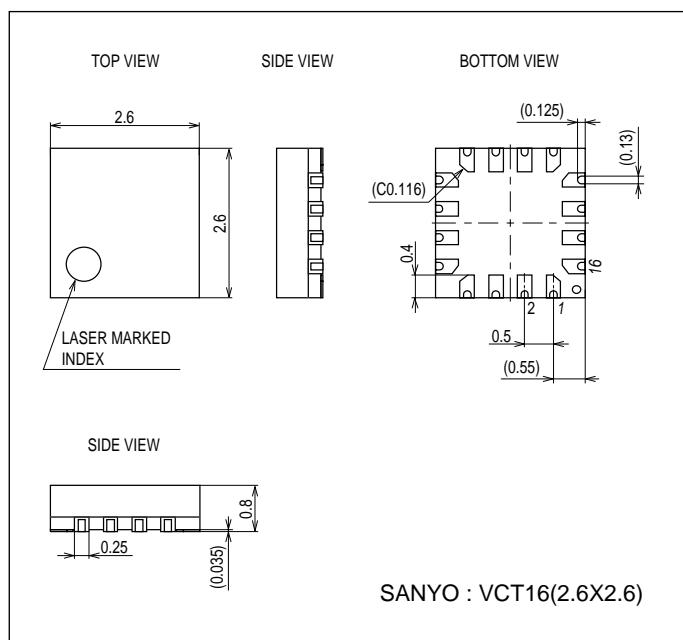
## Electrical Characteristics at $T_a = 25^\circ\text{C}$ , $\text{VM} = 5\text{V}$ , $\text{V}_{\text{CC}} = 3.3\text{V}$ , unless otherwise specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Standby mode current drain	$\text{I}_{\text{STN}}$	IN1 to 4 = "L"			1.0	$\mu\text{A}$
VM current drain	$\text{I}_{\text{M}}$	Any one of IN1 to 4 = "H", with no load		70	150	$\mu\text{A}$
$\text{V}_{\text{CC}}$ current drain	$\text{I}_{\text{CC}}$	Any one of IN1 to 4 = "H"		0.6	1.2	mA
$\text{V}_{\text{CC}}$ low-voltage cutoff voltage	$\text{V}_{\text{thV}_{\text{CC}}}$		1.85	2.10	2.35	V
Low-voltage hysteresis voltage	$\text{V}_{\text{thHYS}}$		100	150	200	mV
Thermal shutdown temperature	$\text{T}_{\text{SD}}$	Design guarantee value *	160	180	200	$^\circ\text{C}$
Thermal hysteresis width	$\Delta\text{T}_{\text{SD}}$	Design guarantee value *	10	30	50	$^\circ\text{C}$
<b>OUT1 to 4</b>						
Logic pin internal pull-down resistance	$\text{R}_{\text{IN}}$	IN1 to 4	50	100	200	$\text{k}\Omega$
Logic pin input current	$\text{I}_{\text{INL}}$	$\text{V}_{\text{IN}} = 0$ , IN1 to 4			1.0	$\mu\text{A}$
	$\text{I}_{\text{INH}}$	$\text{V}_{\text{IN}} = 3.3\text{V}$ , IN1 to 4	20	33	60	$\mu\text{A}$
Logic input high-level voltage	$\text{V}_{\text{INH}}$	IN1 to 4	2.5			V
Logic input low-level voltage	$\text{V}_{\text{INL}}$	IN1 to 4			1.0	V
Output on-resistance	$\text{R}_{\text{ONU}}$	$\text{I}_{\text{O}} = 400\text{mA}$ , upper ON resistance			0.5	$\Omega$
	$\text{R}_{\text{OND}}$	$\text{I}_{\text{O}} = 400\text{mA}$ , lower ON resistance			0.3	$\Omega$
Output leakage current	$\text{I}_{\text{OLeak}}$				1	$\mu\text{A}$
Diode forward voltage	$\text{V}_{\text{D}}$	$\text{I}_{\text{D}} = -400\text{mA}$		1.0		V
<b>PI</b>						
Logic pin internal pull-down resistance	$\text{R}_{\text{IN}}$	INA	50	100	200	$\text{k}\Omega$
Logic pin input current	$\text{I}_{\text{INL}}$	$\text{V}_{\text{IN}} = 0$ , INA			1.0	$\mu\text{A}$
	$\text{I}_{\text{INH}}$	$\text{V}_{\text{IN}} = 3.3\text{V}$ , INA	20	33	50	$\mu\text{A}$
Logic input high-level voltage	$\text{V}_{\text{INH}}$	INA	2.5			V
Logic input low-level voltage	$\text{V}_{\text{INL}}$	INA			1.0	V
Output on-resistance	$\text{R}_{\text{ON}}$	$\text{I}_{\text{O}} = 10\text{mA}$		4	6	$\Omega$
Output leakage current	$\text{I}_{\text{OLeak}}$				1	$\mu\text{A}$

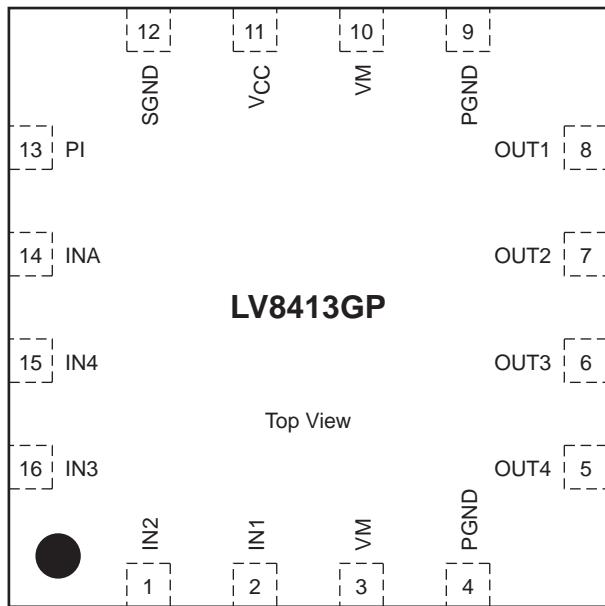
## Package Dimensions

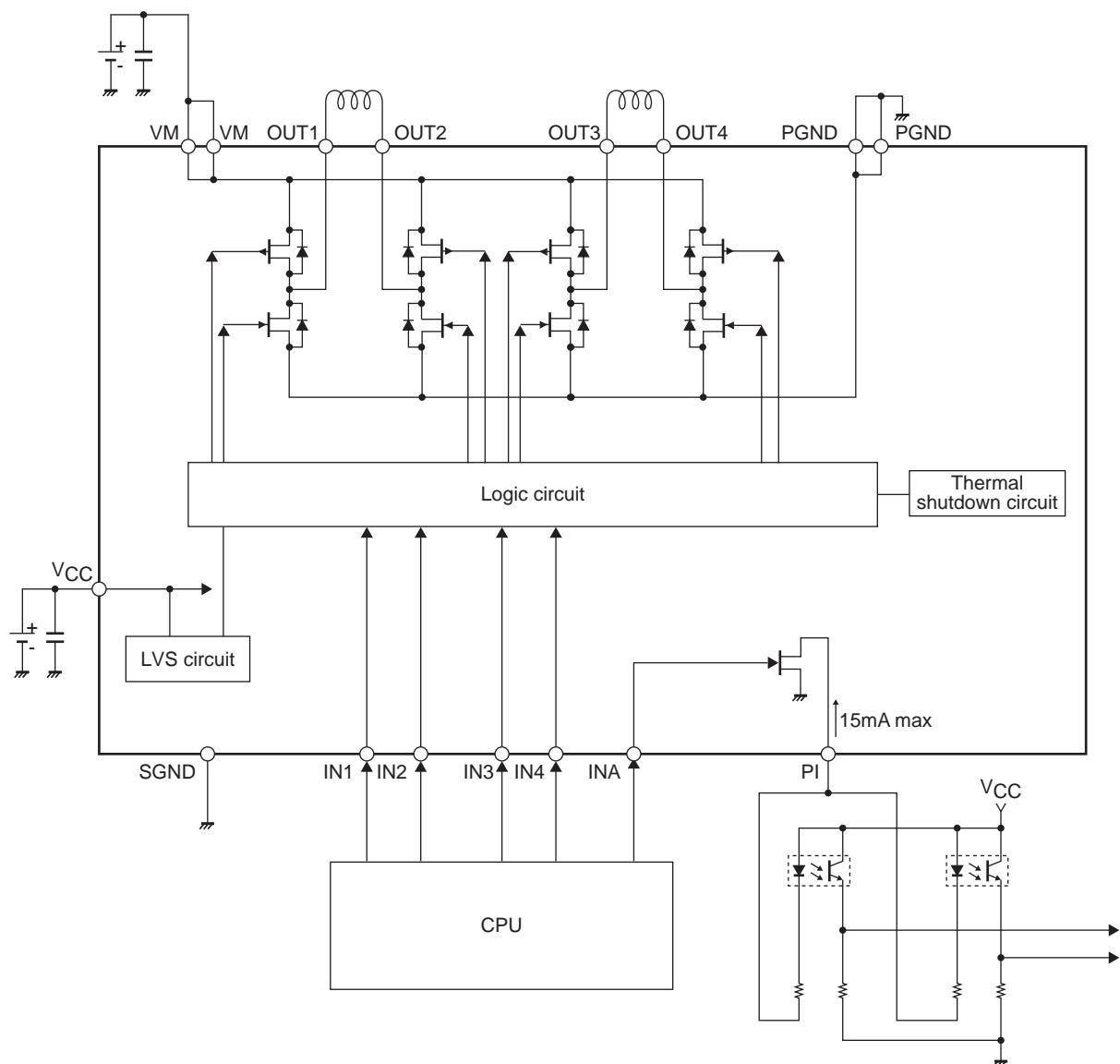
unit : mm (typ)

3318

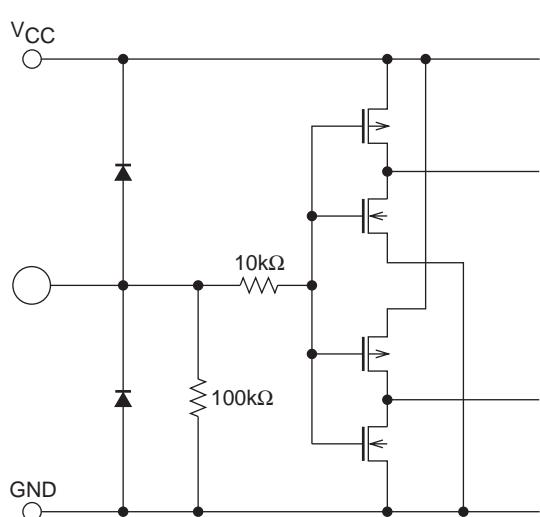
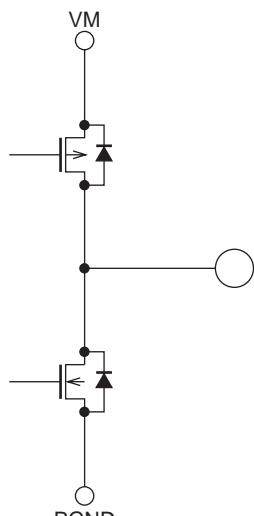
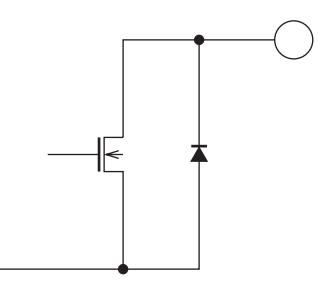


## Pin Assignment



**Block Diagram**

## Pin Functions

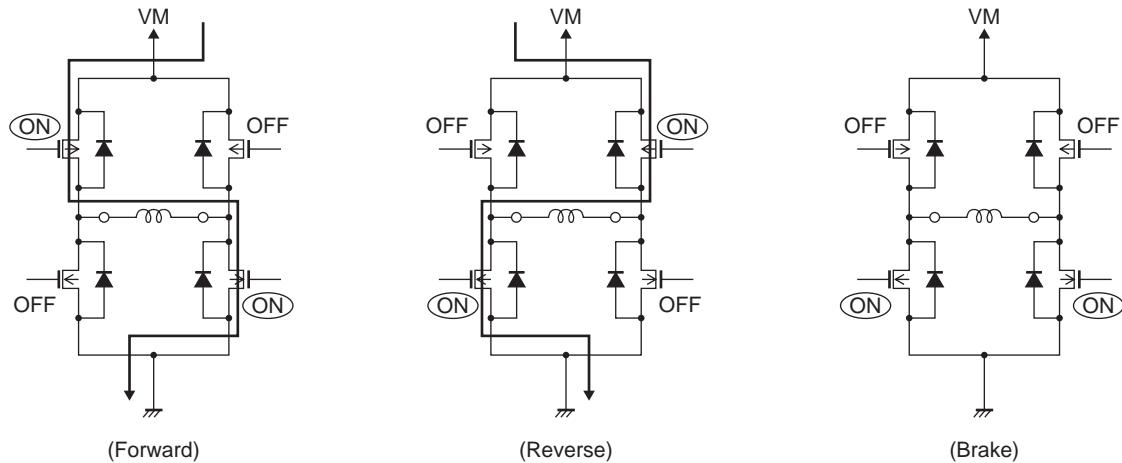
Pin No.	Pin name	Pin Function	Equivalent Circuit
2 1 16 15 14	IN1 IN2 IN3 IN4 INA	Control signal input pin Control signal input pin Control signal input pin Control signal input pin Control signal input pin	
8 7 6 5	OUT1 OUT2 OUT3 OUT4	Outpin Outpin Outpin Outpin	
13	PI	Outpin	
11	VCC	Logic system power supply connection pin	
3 10	VM	Motor power supply connection pin Motor power supply connection pin	
12	SGND	Signal ground	
4 9	PGND	Power ground Power ground	

## Logic input specifications

- Common channels 1 to 2  
ch1 : IN1 to IN2, OUT1 to OUT2  
ch2 : IN3 to IN4, OUT3 to OUT4

Input		Output		Operation mode
IN1	IN2	OUT1	OUT2	
L	L	OFF	OFF	Standby
H	L	H	L	CW (forward)
L	H	L	H	CCW (reverse)
H	H	L	L	Brake

- Output stage transistor function



- Photo sensor driving transistor

When thermal shutdown and V<sub>CC</sub> low-voltage cut circuits are activated, OUT1 through OUT4 are turned OFF under control of the internal circuit. But the output (PI) of photo sensor driving transistor continues operation.

Input INA	Photo sensor driving PI
L	OFF
H	ON

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