Blackfin Embedded Processor

Preliminary Technical Data

ADSP-BF592

FEATURES

- Up to 400 MHz high-performance Blackfin processor
  - 2 16-bit MACs, two 40-bit ALUs, four 8-bit video ALUs, 40-bit shifter
  - RISC-like register and instruction model for ease of programming and compiler-friendly support
  - Advanced debug, trace, and performance monitoring
- Accepts a wide range of supply voltages for internal and I/O operations. See Operating Conditions on Page 18
- Off-chip voltage regulator interface
- 64-lead (9 mm × 9 mm) LFCSP package

MEMORY

- 68K bytes of core-accessible memory:
  - (See Table 1 on Page 3 for L1 and L3 memory size details)
- 64K byte L1 instruction ROM
- Flexible booting options from internal L1 ROM and SPI memory or from host devices including SPI, PPI, and UART
- Memory management unit providing memory protection

PERIPHERALS

- 4 32-bit timers/counters, three with PWM support
- 2 dual-channel, full-duplex synchronous serial ports (SPORT), supporting eight stereo I²S channels
- 2 Serial Peripheral Interface (SPI) compatible ports
- 1 UART with IrDA support
- Parallel peripheral interface (PPI), supporting ITU-R 656 video data formats
- Two-wire interface (TWI) controller
- 9 peripheral DMAs
- 2 memory-to-memory DMA channels
- Event handler with 28 interrupt inputs
- 32 general-purpose I/Os (GPIOs), with programmable hysteresis
- Debug/JTAG interface
- On-chip PLL capable of frequency multiplication

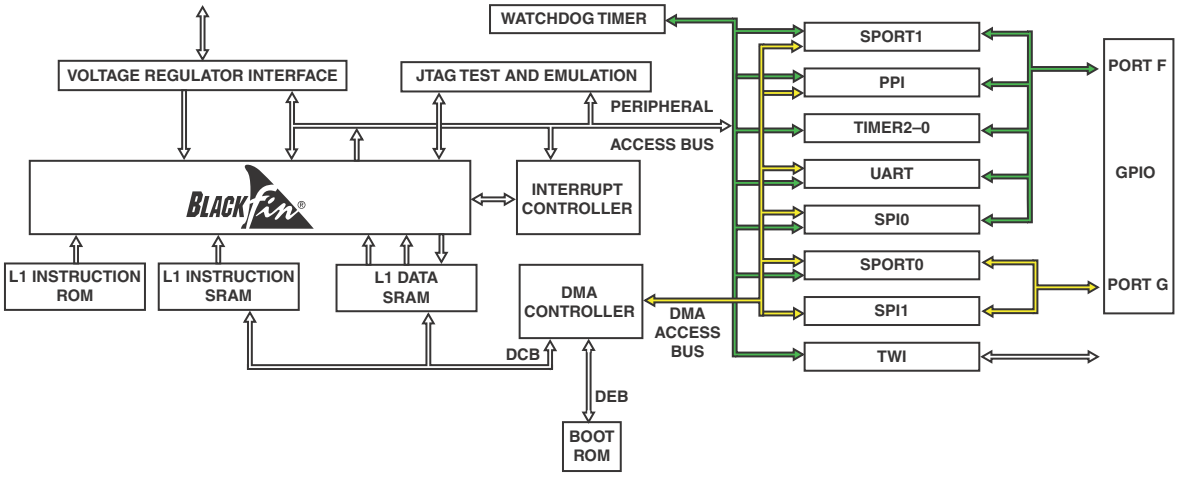


Figure 1. Processor Block Diagram

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Rev. PrC

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REVISION HISTORY

08/10—Rev. PrB to Rev. PrC:

Numerous small corrections and additions to document.

Updated Processor Features 3

Revised Core Clock (CCLK) Requirements 19

Revised Electrical Characteristics 20

Revised Absolute Maximum Ratings 22

Added 2.5 V/3.3 V specifications for most interfaces in Timing Specifications 23

Updated Output Drive Currents 37

Updated Capacitive Loading 39

Added Planned Models 44

GENERAL DESCRIPTION

The ADSP-BF592 processor is a member of the Blackfin® family of products, incorporating the Analog Devices/Intel Micro Signal Architecture (MSA). Blackfin processors combine a dual-MAC state-of-the-art signal processing engine, the advantages of a clean, orthogonal RISC-like microprocessor instruction set, and single-instruction, multiple-data (SIMD) multimedia capabilities into a single instruction-set architecture.

The ADSP-BF592 processor is completely code compatible with other Blackfin processors. ADSP-BF592 processors offer performance up to 400 MHz and reduced static power consumption. The processor features are shown in Table 1.

Table 1. Processor Features

Feature		ADSP-BF592
Timer/Counters with PWM		3
SPORTs		2
SPIs		2
UART		1
Parallel Peripheral Interface		1
TWI		1
GPIOs		32
Memory (bytes)	L1 Instruction SRAM	32K
	L1 Instruction ROM	64K
	L1 Data SRAM	32K
	L1 Scratchpad SRAM	4K
	L3 Boot ROM	4K
Maximum Instruction Rate[1]		400 MHz
Maximum System Clock Speed		100 MHz
Package Options		64-Lead LFCSP

[1] Maximum instruction rate is not available with every possible SCLK selection.

By integrating a rich set of industry-leading system peripherals and memory, Blackfin processors are the platform of choice for next-generation applications that require RISC-like programmability, multimedia support, and leading-edge signal processing in one integrated package.

PORTABLE LOW-POWER ARCHITECTURE

Blackfin processors provide world-class power management and performance. They are produced with a low-power and low-voltage design methodology and feature on-chip dynamic power management, which provides the ability to vary both the voltage and frequency of operation to significantly lower overall power consumption. This capability can result in a substantial reduction in power consumption, compared with just varying the frequency of operation. This allows longer battery life for portable appliances.

SYSTEM INTEGRATION

The ADSP-BF592 processor is a highly integrated system-on-a-chip solution for the next generation of digital communication and consumer multimedia applications. By combining industry-standard interfaces with a high-performance signal processing core, cost-effective applications can be developed quickly, without the need for costly external components. The system peripherals include a watchdog timer; three 32-bit timers/counters with PWM support; two dual-channel, full-duplex synchronous serial ports (SPORTs); two serial peripheral interface (SPI) compatible ports; one UART® with IrDA support; a parallel peripheral interface (PPI); and a two-wire interface (TWI) controller.

PROCESSOR PERIPHERALS

The ADSP-BF592 processor contains a rich set of peripherals connected to the core via several high-bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see Figure 1). The processor also contain dedicated communication modules and high-speed serial and parallel ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

The SPORTs, SPIs, UART, and PPI peripherals are supported by a flexible DMA structure. There are also separate memory DMA channels dedicated to data transfers between the processor's various memory spaces, including boot ROM. Multiple on-chip buses running at up to 100 MHz provide enough bandwidth to keep the processor core running along with activity on all of the on-chip and external peripherals.

The ADSP-BF592 processor includes an interface to an off-chip voltage regulator in support of the processor's dynamic power management capability.

BLACKFIN PROCESSOR CORE

As shown in Figure 2, the Blackfin processor core contains two 16-bit multipliers, two 40-bit accumulators, two 40-bit ALUs, four video ALUs, and a 40-bit shifter. The computation units process 8-, 16-, or 32-bit data from the register file.

The compute register file contains eight 32-bit registers. When performing compute operations on 16-bit operand data, the register file operates as 16 independent 16-bit registers. All operands for compute operations come from the multiported register file and instruction constant fields.

Each MAC can perform a 16-bit by 16-bit multiply in each cycle, accumulating the results into the 40-bit accumulators. Signed and unsigned formats, rounding, and saturation are supported.

The ALUs perform a traditional set of arithmetic and logical operations on 16-bit or 32-bit data. In addition, many special instructions are included to accelerate various signal processing tasks. These include bit operations such as field extract and

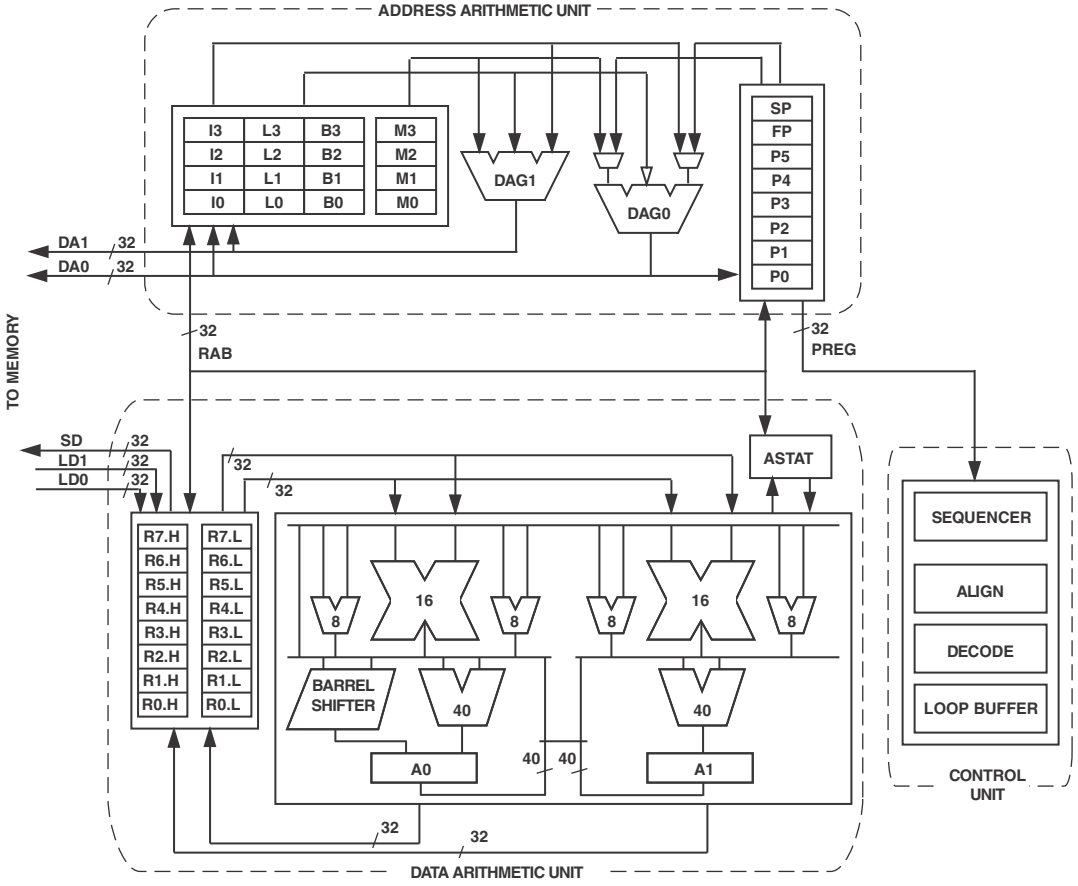


Figure 2. Blackfin Processor Core

population count, modulo 2^{32} multiply, divide primitives, saturation and rounding, and sign/exponent detection. The set of video instructions include byte alignment and packing operations, 16-bit and 8-bit adds with clipping, 8-bit average operations, and 8-bit subtract/absolute value/accumulate (SAA) operations. Also provided are the compare/select and vector search instructions.

For certain instructions, two 16-bit ALU operations can be performed simultaneously on register pairs (a 16-bit high half and 16-bit low half of a compute register). If the second ALU is used, quad 16-bit operations are possible.

The 40-bit shifter can perform shifts and rotates and is used to support normalization, field extract, and field deposit instructions.

The program sequencer controls the flow of instruction execution, including instruction alignment and decoding. For program flow control, the sequencer supports PC relative and indirect conditional jumps (with static branch prediction), and subroutine calls. Hardware is provided to support zero-overhead looping. The architecture is fully interlocked, meaning that the programmer need not manage the pipeline when executing instructions with data dependencies.

The address arithmetic unit provides two addresses for simultaneous dual fetches from memory. It contains a multiported register file consisting of four sets of 32-bit index, modify, length, and base registers (for circular buffering), and eight additional 32-bit pointer registers (for C-style indexed stack manipulation).

Blackfin processors support a modified Harvard architecture in combination with a hierarchical memory structure. Level 1 (L1) memories are those that typically operate at the full processor speed with little or no latency. At the L1 level, the instruction memory holds instructions only. Data memory holds data, and a dedicated scratchpad data memory stores stack and local variable information.

Multiple L1 memory blocks are provided. The memory management unit (MMU) provides memory protection for individual tasks that may be operating on the core and can protect system registers from unintended access.

The architecture provides three modes of operation: user mode, supervisor mode, and emulation mode. User mode has restricted access to certain system resources, thus providing a protected software environment, while supervisor mode has unrestricted access to the system and core resources.

The Blackfin processor instruction set has been optimized so that 16-bit opcodes represent the most frequently used instructions, resulting in excellent compiled code density. Complex DSP instructions are encoded into 32-bit opcodes, representing fully featured multifunction instructions. Blackfin processors support a limited multi-issue capability, where a 32-bit instruction can be issued in parallel with two 16-bit instructions, allowing the programmer to use many of the core resources in a single instruction cycle.

The Blackfin processor assembly language uses an algebraic syntax for ease of coding and readability. The architecture has been optimized for use in conjunction with the C/C++ compiler, resulting in fast and efficient software implementations.

MEMORY ARCHITECTURE

The Blackfin processor views memory as a single unified 4G byte address space, using 32-bit addresses. All resources, including internal memory and I/O control registers, occupy separate sections of this common address space. See Figure 3.

The core-accessible L1 memory system is high-performance internal memory that operates at the core clock frequency. The external bus interface unit (EBIU) provides access to the boot ROM.

The memory DMA controller provides high-bandwidth data-movement capability. It can perform block transfers of code or data between the L1 Instruction SRAM and L1 Data SRAM memory spaces.

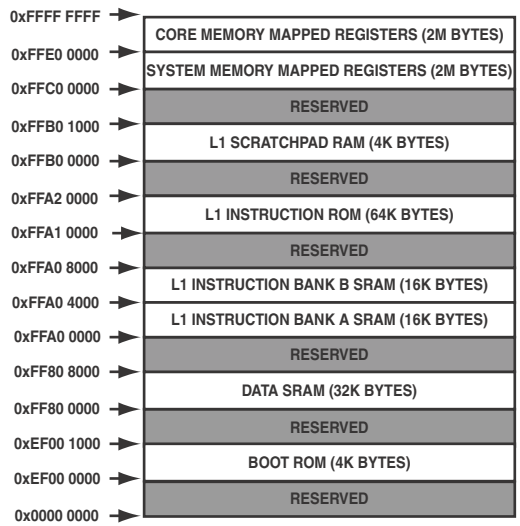


Figure 3. Internal/External Memory Map

Internal (Core-Accessible) Memory

The processor has three blocks of core-accessible memory, providing high-bandwidth access to the core.

The first block is the L1 instruction memory, consisting of 32K bytes SRAM. This memory is accessed at full processor speed.

The second core-accessible memory block is the L1 data memory, consisting of 32K bytes. This memory block is accessed at full processor speed.

The third memory block is a 4K byte L1 scratchpad SRAM which runs at the same speed as the other L1 memories.

L1 Utility ROM

The L1 instruction ROM contains utility ROM code. This includes the TMK (VDK core), C run-time libraries, and DSP libraries. See the VisualDSP++ documentation for more information.

Custom ROM (Optional)

The on chip L1 Instruction ROM on the ADSP-BF592 may be customized to contain user code with the following features:

- 64K bytes of L1 Instruction ROM available for custom code
- Ability to restrict access to all or specific segments of the on chip ROM

Customers wishing to customize the on chip ROM for their own application needs should contact ADI sales for more information on terms and conditions and details on the technical implementation.

I/O Memory Space

The processor does not define a separate I/O space. All resources are mapped through the flat 32-bit address space. On-chip I/O devices have their control registers mapped into memory-mapped registers (MMRs) at addresses near the top of the 4G byte address space. These are separated into two smaller blocks, one which contains the control MMRs for all core functions, and the other which contains the registers needed for setup and control of the on-chip peripherals outside of the core. The MMRs are accessible only in supervisor mode and appear as reserved space to on-chip peripherals.

Booting

The processor contains a small on-chip boot kernel, which configures the appropriate peripheral for booting. If the processor is configured to boot from boot ROM memory space, the processor starts executing from the on-chip boot ROM. For more information, see Booting Modes on Page 13.

Event Handling

The event controller on the processor handles all asynchronous and synchronous events to the processor. The processor provides event handling that supports both nesting and prioritization. Nesting allows multiple event service routines to be active simultaneously. Prioritization ensures that servicing of a higher-priority event takes precedence over servicing of a lower-priority event. The controller provides support for five different types of events:

- Emulation – An emulation event causes the processor to enter emulation mode, allowing command and control of the processor via the JTAG interface.
- $\overline{\text{RESET}}$ – This event resets the processor.

- Nonmaskable Interrupt (NMI) – The NMI event can be generated by the software watchdog timer or by the $\overline{\text{NMI}}$ input signal to the processor. The NMI event is frequently used as a power-down indicator to initiate an orderly shut-down of the system.
- Exceptions – Events that occur synchronously to program flow (in other words, the exception is taken before the instruction is allowed to complete). Conditions such as data alignment violations and undefined instructions cause exceptions.
- Interrupts – Events that occur asynchronously to program flow. They are caused by input signals, timers, and other peripherals, as well as by an explicit software instruction.

Each event type has an associated register to hold the return address and an associated return-from-event instruction. When an event is triggered, the state of the processor is saved on the supervisor stack.

The processor event controller consists of two stages: the core event controller (CEC) and the system interrupt controller (SIC). The core event controller works with the system interrupt controller to prioritize and control all system events. Conceptually, interrupts from the peripherals enter into the SIC and are then routed directly into the general-purpose interrupts of the CEC.

Core Event Controller (CEC)

The CEC supports nine general-purpose interrupts (IVG15–7), in addition to the dedicated interrupt and exception events. Of these general-purpose interrupts, the two lowest-priority interrupts (IVG15–14) are recommended to be reserved for software interrupt handlers, leaving seven prioritized interrupt inputs to support the peripherals of the processor. Table 2 describes the inputs to the CEC, identifies their names in the event vector table (EVT), and lists their priorities.

System Interrupt Controller (SIC)

The system interrupt controller provides the mapping and routing of events from the many peripheral interrupt sources to the prioritized general-purpose interrupt inputs of the CEC. Although the processor provides a default mapping, the user can alter the mappings and priorities of interrupt events by writing the appropriate values into the interrupt assignment registers (SIC_IARx). Table 3 describes the inputs into the SIC and the default mappings into the CEC.

Event Control

The processor provides a very flexible mechanism to control the processing of events. In the CEC, three registers are used to coordinate and control events. Each register is 16 bits wide.

- CEC interrupt latch register (ILAT) – Indicates when events have been latched. The appropriate bit is set when the processor has latched the event and is cleared when the event has been accepted into the system. This register is updated automatically by the controller, but it may be written only when its corresponding IMASK bit is cleared.
- CEC interrupt mask register (IMASK) – Controls the masking and unmasking of individual events. When a bit is set in the IMASK register, that event is unmasked and is processed by the CEC when asserted. A cleared bit in the IMASK register masks the event, preventing the processor from servicing the event even though the event may be latched in the ILAT register. This register may be read or written while in supervisor mode. (Note that general-purpose interrupts can be globally enabled and disabled with the STI and CLI instructions, respectively.)
- CEC interrupt pending register (IPEND) – The IPEND register keeps track of all nested events. A set bit in the IPEND register indicates the event is currently active or nested at some level. This register is updated automatically by the controller but may be read while in supervisor mode.

The SIC allows further control of event processing by providing three pairs of 32-bit interrupt control and status registers. Each register contains a bit, corresponding to each of the peripheral interrupt events shown in Table 3.

- SIC interrupt mask registers (SIC_IMASK) – Control the masking and unmasking of each peripheral interrupt event. When a bit is set in these registers, that peripheral event is unmasked and is processed by the system when asserted. A cleared bit in the register masks the peripheral event, preventing the processor from servicing the event.
- SIC interrupt status registers (SIC_ISR) – As multiple peripherals can be mapped to a single event, these registers allow the software to determine which peripheral event

Table 2. Core Event Controller (CEC)

Priority (0 is Highest)	Event Class	EVT Entry
0	Emulation/Test Control	EMU
1	$\overline{\text{RESET}}$	RST
2	Nonmaskable Interrupt	$\overline{\text{NMI}}$
3	Exception	EVX
4	Reserved	—
5	Hardware Error	IVHW
6	Core Timer	IVTMR
7	General-Purpose Interrupt 7	IVG7
8	General-Purpose Interrupt 8	IVG8
9	General-Purpose Interrupt 9	IVG9
10	General-Purpose Interrupt 10	IVG10
11	General-Purpose Interrupt 11	IVG11
12	General-Purpose Interrupt 12	IVG12
13	General-Purpose Interrupt 13	IVG13
14	General-Purpose Interrupt 14	IVG14
15	General-Purpose Interrupt 15	IVG15

source triggered the interrupt. A set bit indicates that the peripheral is asserting the interrupt, and a cleared bit indicates that the peripheral is not asserting the event.

- SIC interrupt wakeup enable registers (SIC_IWR) – By enabling the corresponding bit in these registers, a peripheral can be configured to wake up the processor, should the core be idled or in sleep mode when the event is generated. For more information, see Dynamic Power Management on Page 10.

Because multiple interrupt sources can map to a single general-purpose interrupt, multiple pulse assertions can occur simultaneously, before or during interrupt processing for an interrupt event already detected on this interrupt input. The IPEND register contents are monitored by the SIC as the interrupt acknowledgement.

The appropriate ILAT register bit is set when an interrupt rising edge is detected (detection requires two core clock cycles). The bit is cleared when the respective IPEND register bit is set. The IPEND bit indicates that the event has entered into the processor pipeline. At this point the CEC recognizes and queues the next rising edge event on the corresponding event input. The minimum latency from the rising edge transition of the general-purpose interrupt to the IPEND output asserted is three core clock cycles; however, the latency can be much higher, depending on the activity within and the state of the processor.

Table 3. System Interrupt Controller (SIC)

Peripheral Interrupt Source	General Purpose Interrupt (at Reset)	Peripheral Interrupt ID	Default Core Interrupt ID	SIC Interrupt Assignment
PLL Wakeup Interrupt	IVG7	0	0	IAR0
DMA Error (generic)	IVG7	1	0	IAR0
PPI0 Status	IVG7	2	0	IAR0
SPORT0 Status	IVG7	3	0	IAR0
SPORT1 Status	IVG7	4	0	IAR0
SPI0 Status	IVG7	5	0	IAR0
SPI1 Status	IVG7	6	0	IAR0
UART0 Status	IVG7	7	0	IAR0
DMA Channel 0 (PPI0)	IVG8	8	1	IAR1
DMA Channel 1 (SPORT0 RX)	IVG9	9	2	IAR1
DMA Channel 2 (SPORT0 TX)	IVG9	10	2	IAR1
DMA Channel 3 (SPORT1 RX)	IVG9	11	2	IAR1
DMA Channel 4 (SPORT1 TX)	IVG9	12	2	IAR1
DMA Channel 5 (SPI0 RX/TX)	IVG10	13	3	IAR1
DMA Channel 6 (SPI1 RX/TX)	IVG10	14	3	IAR1
DMA Channel 7 (UART0 RX)	IVG10	15	3	IAR1
DMA Channel 8 (UART0 TX)	IVG10	16	3	IAR2
Port F Interrupt A	IVG11	17	4	IAR2
Port F Interrupt B	IVG11	18	4	IAR2
Timer 0	IVG11	19	4	IAR2
Timer 1	IVG11	20	4	IAR2
Timer 2	IVG11	21	4	IAR2
Port G Interrupt A	IVG12	22	5	IAR2
Port G Interrupt B	IVG12	23	5	IAR2
TWI	IVG12	24	5	IAR3
Reserved	–	25	–	IAR3
Reserved	–	26	–	IAR3
Reserved	–	27	–	IAR3
Reserved	–	28	–	IAR3
DMA Channels 12 and 13 (Memory DMA Stream 0)	IVG13	29	6	IAR3
DMA Channels 14 and 15 (Memory DMA Stream 1)	IVG13	30	6	IAR3
Software Watchdog Timer	IVG13	31	6	IAR3

DMA CONTROLLERS

The processor has multiple, independent DMA channels that support automated data transfers with minimal overhead for the processor core. DMA transfers can occur between the processor's internal memories and any of its DMA-capable peripherals. DMA-capable peripherals include the SPORTs, SPI ports, UART, and PPI. Each individual DMA-capable peripheral has at least one dedicated DMA channel.

The processor DMA controller supports both one-dimensional (1-D) and two-dimensional (2-D) DMA transfers. DMA transfer initialization can be implemented from registers or from sets of parameters called descriptor blocks.

The 2-D DMA capability supports arbitrary row and column sizes up to 64K elements by 64K elements, and arbitrary row and column step sizes up to ±32K elements. Furthermore, the column step size can be less than the row step size, allowing implementation of interleaved data streams. This feature is especially useful in video applications where data can be de-interleaved on the fly.

Examples of DMA types supported by the processor DMA controller include:

- A single, linear buffer that stops upon completion
- A circular, auto-refreshing buffer that interrupts on each full or fractionally full buffer
- 1-D or 2-D DMA using a linked list of descriptors
- 2-D DMA using an array of descriptors, specifying only the base DMA address within a common page

In addition to the dedicated peripheral DMA channels, there are two memory DMA channels, which are provided for transfers between the various memories of the processor system with minimal processor intervention. Memory DMA transfers can be controlled by a very flexible descriptor-based methodology or by a standard register-based autobuffer mechanism.

WATCHDOG TIMER

The processor includes a 32-bit timer that can be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state through generation of a hardware reset, nonmaskable interrupt (NMI), or general-purpose interrupt, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error.

If configured to generate a hardware reset, the watchdog timer resets both the core and the processor peripherals. After a reset, software can determine whether the watchdog was the source of the hardware reset by interrogating a status bit in the watchdog timer control register.

The timer is clocked by the system clock (SCLK), at a maximum frequency of f_{SCLK}.

TIMERS

There are four general-purpose programmable timer units in the processors. Three timers have an external pin that can be configured either as a pulse width modulator (PWM) or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized: to an external clock input to the several other associated PF pins, to an external clock input to the PPI_CLK input pin, or to the internal SCLK.

The timer units can be used in conjunction with the UART to measure the width of the pulses in the data stream to provide a software auto-baud detect function for the respective serial channels.

The timers can generate interrupts to the processor core providing periodic events for synchronization, either to the system clock or to a count of external signals.

In addition to the three general-purpose programmable timers, a fourth timer is also provided. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generation of operating system periodic interrupts.

SERIAL PORTS

The processors incorporate two dual-channel synchronous serial ports (SPORT0 and SPORT1) for serial and multiprocessor communications. The SPORTs support the following features:

- I^2S capable operation.
- Bidirectional operation – Each SPORT has two sets of independent transmit and receive pins, enabling eight channels of I^2S stereo audio.
- Buffered (8-deep) transmit and receive ports – Each port has a data register for transferring data words to and from other processor components and shift registers for shifting data in and out of the data registers.
- Clocking – Each transmit and receive port can either use an external serial clock or generate its own, in frequencies ranging from (f_{SCLK}/131,070) Hz to (f_{SCLK}/2) Hz.
- Word length – Each SPORT supports serial data words from 3 to 32 bits in length, transferred most-significant-bit first or least-significant-bit first.
- Framing – Each transmit and receive port can run with or without frame sync signals for each data word. Frame sync signals can be generated internally or externally, active high or low, and with either of two pulse widths and early or late frame sync.
- Companding in hardware – Each SPORT can perform A-law or μ-law companding according to ITU recommendation G.711. Companding can be selected on the transmit and/or receive channel of the SPORT without additional latencies.

- DMA operations with single-cycle overhead – Each SPORT can automatically receive and transmit multiple buffers of memory data. The processor can link or chain sequences of DMA transfers between a SPORT and memory.
- Interrupts – Each transmit and receive port generates an interrupt upon completing the transfer of a data word or after transferring an entire data buffer, or buffers, through DMA.
- Multichannel capability – Each SPORT supports 128 channels out of a 1024-channel window and is compatible with the H.100, H.110, MVIP-90, and HMVIP standards.

SERIAL PERIPHERAL INTERFACE (SPI) PORTS

The processors have two SPI-compatible ports that enable the processor to communicate with multiple SPI-compatible devices.

The SPI interface uses three pins for transferring data: two data pins (Master Output-Slave Input, MOSI, and Master Input-Slave Output, MISO) and a clock pin (serial clock, SCK). An SPI chip select input pin ($\overline{\text{SPIx_SS}}$) lets other SPI devices select the processor, and many SPI chip select output pins ($\overline{\text{SPIx_SEL7–1}}$) let the processor select other SPI devices. The SPI select pins are reconfigured general-purpose I/O pins. Using these pins, the SPI port provides a full-duplex, synchronous serial interface, which supports both master/slave modes and multimaster environments.

UART PORT

The ADSP-BF592 processor provides a full-duplex universal asynchronous receiver/transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART port includes support for five to eight data bits, one or two stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

PARALLEL PERIPHERAL INTERFACE (PPI)

The processor provides a parallel peripheral interface (PPI) that can connect directly to parallel A/D and D/A converters, video encoders and decoders, and other general-purpose peripherals. The PPI consists of a dedicated input clock pin, up to three frame synchronization pins, and up to 16 data pins. The input clock supports parallel data rates up to half the system clock rate and the synchronization signals can be configured as either inputs or outputs.

The PPI supports a variety of general-purpose and ITU-R 656 modes of operation. In general-purpose mode, the PPI provides half-duplex, bidirectional data transfer with up to 16 bits of data. Up to three frame synchronization signals are also provided. In ITU-R 656 mode, the PPI provides half-duplex bidirectional transfer of 8- or 10-bit video data. Additionally, on-chip decode of embedded start-of-line (SOL) and start-of-field (SOF) preamble packets is supported.

General-Purpose Mode Descriptions

The general-purpose modes of the PPI are intended to suit a wide variety of data capture and transmission applications. Three distinct submodes are supported:

- Input mode – Frame syncs and data are inputs into the PPI.
- Frame capture mode – Frame syncs are outputs from the PPI, but data are inputs.
- Output mode – Frame syncs and data are outputs from the PPI.

Input Mode

Input mode is intended for ADC applications, as well as video communication with hardware signaling. In its simplest form, PPI_FS1 is an external frame sync input that controls when to read data. The PPI_DELAY MMR allows for a delay (in PPI_CLK cycles) between reception of this frame sync and the initiation of data reads. The number of input data samples is user programmable and defined by the contents of the PPI_COUNT register. The PPI supports 8-bit and 10-bit through 16-bit data, programmable in the PPI_CONTROL register.

Frame Capture Mode

Frame capture mode allows the video source(s) to act as a slave (for frame capture for example). The ADSP-BF592 processor controls when to read from the video source(s). PPI_FS1 is an HSYNC output and PPI_FS2 is a VSYNC output.

Output Mode

Output mode is used for transmitting video or other data with up to three output frame syncs. Typically, a single frame sync is appropriate for data converter applications, whereas two or three frame syncs could be used for sending video with hardware signaling.

ITU-R 656 Mode Descriptions

The ITU-R 656 modes of the PPI are intended to suit a wide variety of video capture, processing, and transmission applications. Three distinct submodes are supported:

- Active video only mode
- Vertical blanking only mode
- Entire field mode

Active Video Mode

Active video only mode is used when only the active video portion of a field is of interest and not any of the blanking intervals. The PPI does not read in any data between the end of active

video (EAV) and start of active video (SAV) preamble symbols, or any data present during the vertical blanking intervals. In this mode, the control byte sequences are not stored to memory; they are filtered by the PPI. After synchronizing to the start of Field 1, the PPI ignores incoming samples until it sees an SAV code. The user specifies the number of active video lines per frame (in PPI_COUNT register).

Vertical Blanking Interval Mode

In this mode, the PPI only transfers vertical blanking interval (VBI) data.

Entire Field Mode

In this mode, the entire incoming bit stream is read in through the PPI. This includes active video, control preamble sequences, and ancillary data that may be embedded in horizontal and vertical blanking intervals. Data transfer starts immediately after synchronization to Field 1. Data is transferred to or from the synchronous channels through eight DMA engines that work autonomously from the processor core.

TWI CONTROLLER INTERFACE

The processors include a two-wire interface (TWI) module for providing a simple exchange method of control data between multiple devices. The TWI is functionally compatible with the widely used I²C® bus standard. The TWI module offers the capabilities of simultaneous master and slave operation, support for both 7-bit addressing and multimedia data arbitration. The TWI interface utilizes two pins for transferring clock (SCL) and data (SDA) and supports the protocol at speeds up to 400K bits/sec.

The TWI module is compatible with serial camera control bus (SCCB) functionality for easier control of various CMOS camera sensor devices.

PORTS

The processor groups the many peripheral signals to two ports—Port F and Port G. Most of the associated pins are shared by multiple signals. The ports function as multiplexer controls.

General-Purpose I/O (GPIO)

The processor has 32 bidirectional, general-purpose I/O (GPIO) pins allocated across two separate GPIO modules—PORTFIO and PORTGIO, associated with Port F and Port G respectively. Each GPIO-capable pin shares functionality with other processor peripherals via a multiplexing scheme; however, the GPIO functionality is the default state of the device upon power-up. Neither GPIO output nor input drivers are active by default. Each general-purpose port pin can be individually controlled by manipulation of the port control, status, and interrupt registers:

- GPIO direction control register – Specifies the direction of each individual GPIO pin as input or output.
- GPIO control and status registers – The processor employs a “write one to modify” mechanism that allows any combination of individual GPIO pins to be modified in a single instruction, without affecting the level of any other GPIO pins. Four control registers are provided. One register is written in order to set pin values, one register is written in order to clear pin values, one register is written in order to toggle pin values, and one register is written in order to specify a pin value. Reading the GPIO status register allows software to interrogate the sense of the pins.
- GPIO interrupt mask registers – The two GPIO interrupt mask registers allow each individual GPIO pin to function as an interrupt to the processor. Similar to the two GPIO control registers that are used to set and clear individual pin values, one GPIO interrupt mask register sets bits to enable interrupt function, and the other GPIO interrupt mask register clears bits to disable interrupt function. GPIO pins defined as inputs can be configured to generate hardware interrupts, while output pins can be triggered by software interrupts.
- GPIO interrupt sensitivity registers – The two GPIO interrupt sensitivity registers specify whether individual pins are level- or edge-sensitive and specify—if edge-sensitive—whether just the rising edge or both the rising and falling edges of the signal are significant. One register selects the type of sensitivity, and one register selects which edges are significant for edge-sensitivity.

DYNAMIC POWER MANAGEMENT

The processor provides five operating modes, each with a different performance/power profile. In addition, dynamic power management provides the control functions to dynamically alter the processor core supply voltage, further reducing power dissipation. When configured for a 0 volt core supply voltage, the processor enters the hibernate state. Control of clocking to each of the processor peripherals also reduces power consumption. See Table 4 for a summary of the power settings for each mode.

Full-On Operating Mode—Maximum Performance

In the full-on mode, the PLL is enabled and is not bypassed, providing capability for maximum operational frequency. This is the power-up default execution state in which maximum performance can be achieved. The processor core and all enabled peripherals run at full speed.

Active Operating Mode—Moderate Dynamic Power Savings

In the active mode, the PLL is enabled but bypassed. Because the PLL is bypassed, the processor’s core clock (CCLK) and system clock (SCLK) run at the input clock (CLKIN) frequency. DMA access is available to appropriately configured L1 memories.

In the active mode, it is possible to disable the control input to the PLL by setting the PLL_OFF bit in the PLL control register. This register can be accessed with a user-callable routine in the on-chip ROM called bfrom_SysControl(). If disabled, the PLL control input must be re-enabled before transitioning to the full-on or sleep modes.

Table 4. Power Settings

Mode/State	PLL	PLL Bypassed	Core Clock (CCLK)	System Clock (SCLK)	Core Power
Full On	Enabled	No	Enabled	Enabled	On
Active	Enabled/ Disabled	Yes	Enabled	Enabled	On
Sleep	Enabled	—	Disabled	Enabled	On
Deep Sleep	Disabled	—	Disabled	Disabled	On
Hibernate	Disabled	—	Disabled	Disabled	Off

For more information about PLL controls, see the "Dynamic Power Management" chapter in the *ADSP-BF59x Blackfin Processor Hardware Reference*.

Sleep Operating Mode—High Dynamic Power Savings

The sleep mode reduces dynamic power dissipation by disabling the clock to the processor core (CCLK). The PLL and system clock (SCLK), however, continue to operate in this mode. Typically, an external event wakes up the processor. When in the sleep mode, asserting a wakeup enabled in the SIC_IWR0 registers causes the processor to sense the value of the BYPASS bit in the PLL control register (PLL_CTL). If BYPASS is disabled, the processor transitions to the full on mode. If BYPASS is enabled, the processor transitions to the active mode.

System DMA access to L1 memory is not supported in sleep mode.

Deep Sleep Operating Mode—Maximum Dynamic Power Savings

The deep sleep mode maximizes dynamic power savings by disabling the clocks to the processor core (CCLK) and to all synchronous peripherals (SCLK). Asynchronous peripherals may still be running but cannot access internal resources or external memory. This powered-down mode can only be exited by assertion of the reset interrupt ($\overline{\text{RESET}}$) or by an asynchronous interrupt generated by a GPIO pin. Assertion of $\overline{\text{RESET}}$ while in deep sleep mode causes the processor to transition to the full on mode. Assertion of a GPIO pin configured for wakeup (in the VR_CTL register) causes the processor to transition to active mode, and execution resumes from where the program counter was when deep sleep mode was entered.

Note that when a GPIO pin is used to trigger wake from deep sleep, the programmed wake level must linger for at least 10ns to guarantee detection.

Hibernate State—Maximum Static Power Savings

The hibernate state maximizes static power savings by disabling clocks to the processor core (CCLK) and to all of the peripherals (SCLK) as well as signaling an external voltage regulator that V_{DDINT} can be shut off. Any critical information stored internally (for example, memory contents, register contents, and other information) must be written to a non-volatile storage device prior to removing power if the processor state is to be preserved. Writing b#0 to the $\overline{\text{HIBERNATE}}$ bit causes EXT_WAKE to transition low, which can be used to signal an external voltage regulator to shut down.

Since V_{DDEXT} can still be supplied in this mode, all of the external pins three-state, unless otherwise specified. This allows other devices that may be connected to the processor to still have power applied without drawing unwanted current.

The processor can be woken up by asserting the $\overline{\text{RESET}}$ pin or by a general-purpose flag wake up event. All hibernate wakeup events initiate the hardware reset sequence. Individual sources are enabled by the VR_CTL register. The EXT_WAKE signal indicates the occurrence of a wakeup event.

As long as V_{DDEXT} is applied, the VR_CTL register maintains its state during hibernation. All other internal registers and memories, however, lose their content in the hibernate state.

Power Savings

As shown in Table 5, the processor supports two different power domains, which maximizes flexibility while maintaining compliance with industry standards and conventions. By isolating the internal logic of the processor into its own power domain, separate from other I/O, the processor can take advantage of dynamic power management without affecting the other I/O devices. There are no sequencing requirements for the various power domains, but all domains must be powered according to the appropriate Specifications table for processor operating conditions; even if the feature/peripheral is not used.

Table 5. Power Domains

Power Domain	V_{DD} Range
All internal logic and memories	V_{DDINT}
All other I/O	V_{DDEXT}

The dynamic power management feature of the processor allows both the processor's input voltage (V_{DDINT}) and clock frequency (f_{CCLK}) to be dynamically controlled.

The power dissipated by a processor is largely a function of its clock frequency and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation, while reducing the voltage by 25% reduces dynamic power dissipation by more than 40%. Further, these power savings are additive, in that if the clock frequency and supply voltage are both reduced, the power savings can be dramatic, as shown in the following equations.

$$\text{Power Savings Factor} = \frac{f_{CCLKRED}}{f_{CCLKNOM}} \times \left(\frac{V_{DDINTRED}}{V_{DDINTNOM}}\right)^2 \times \left(\frac{T_{RED}}{T_{NOM}}\right)$$

$$\%\ \text{Power Savings} = (1 - \text{Power Savings Factor}) \times 100\%$$

where the variables in the equations are:

$f_{CCLKNOM}$ is the nominal core clock frequency

$f_{CCLKRED}$ is the reduced core clock frequency

$V_{DDINTNOM}$ is the nominal internal supply voltage

$V_{DDINTRED}$ is the reduced internal supply voltage

T_{NOM} is the duration running at $f_{CCLKNOM}$

T_{RED} is the duration running at $f_{CCLKRED}$

VOLTAGE REGULATION

The ADSP-BF592 processor requires an external voltage regulator to power the V_{DDINT} domain. To reduce standby power consumption, the external voltage regulator can be signaled through EXT_WAKE to remove power from the processor core. This signal is high-true for power-up and may be connected directly to the low-true shut-down input of many common regulators.

While in the hibernate state, the external supply, V_{DDEXT}, can still be applied, eliminating the need for external buffers. The external voltage regulator can be activated from this power down state by asserting the $\overline{\text{RESET}}$ pin, which then initiates a boot sequence. EXT_WAKE indicates a wakeup to the external voltage regulator.

The power good ($\overline{\text{PG}}$) input signal allows the processor to start only after the internal voltage has reached a chosen level. In this way, the startup time of the external regulator is detected after hibernation. For a complete description of the power good functionality, refer to the *ADSP-BF59x Blackfin Processor Hardware Reference*.

CLOCK SIGNALS

The processor can be clocked by an external crystal, a sine wave input, or a buffered, shaped clock derived from an external clock oscillator.

If an external clock is used, it should be a TTL-compatible signal and must not be halted, changed, or operated below the specified frequency during normal operation. This signal is connected to the processor's CLKIN pin. When an external clock is used, the XTAL pin must be left unconnected.

Alternatively, because the processor includes an on-chip oscillator circuit, an external crystal may be used. For fundamental frequency operation, use the circuit shown in Figure 4. A parallel-resonant, fundamental frequency, microprocessor-grade crystal is connected across the CLKIN and XTAL pins. The on-chip resistance between CLKIN and the XTAL pin is in the 500 kΩ range. Further parallel resistors are typically not recommended. The two capacitors and the series resistor shown in Figure 4 fine tune phase and amplitude of the sine frequency.

The capacitor and resistor values shown in Figure 4 are typical values only. The capacitor values are dependent upon the crystal manufacturers' load capacitance recommendations and the PCB physical layout. The resistor value depends on the drive level specified by the crystal manufacturer. The user should verify the customized values based on careful investigations on multiple devices over temperature range.

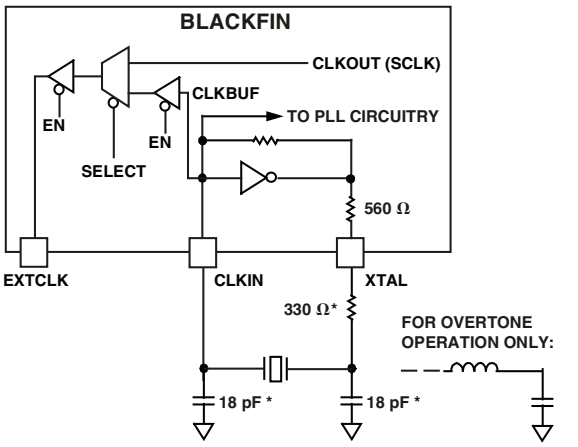


Figure 4. External Crystal Connections

A third-overtone crystal can be used for frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone, by adding a tuned inductor circuit as shown in Figure 4. A design procedure for third-overtone operation is discussed in detail in application note *(EE-168) Using Third Overtone Crystals with the ADSP-218x DSP* on the Analog Devices website (www.analog.com)—use site search on "EE-168."

The Blackfin core runs at a different clock rate than the on-chip peripherals. As shown in Figure 5, the core clock (CCLK) and system peripheral clock (SCLK) are derived from the input clock (CLKIN) signal. An on-chip PLL is capable of multiplying the CLKIN signal by a programmable 5× to 64× multiplication factor (bounded by specified minimum and maximum VCO frequencies). The default multiplier is 6×, but it can be modified by a software instruction sequence.

On-the-fly frequency changes can be effected by simply writing to the PLL_DIV register. The maximum allowed CCLK and SCLK rates depend on the applied voltages V_{DDINT} and V_{DDEXT}; the VCO is always permitted to run up to the frequency specified by the part's instruction rate. The CLKOUT pin reflects the SCLK frequency to the off-chip world. The pin functions as a reference signal in many timing specifications. While three-stated by default, it can be enabled using the VRCTL register.

All on-chip peripherals are clocked by the system clock (SCLK). The system clock frequency is programmable by means of the SSEL3–0 bits of the PLL_DIV register. The values programmed into the SSEL fields define a divide ratio between the PLL output (VCO) and the system clock. SCLK divider values are 1 through 15. Table 6 illustrates typical system clock ratios.

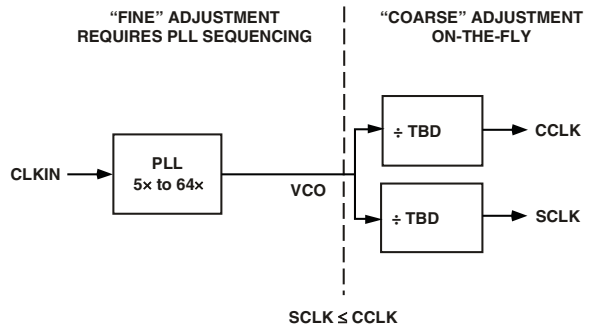


Figure 5. Frequency Modification Methods

Note that the divisor ratio must be chosen to limit the system clock frequency to its maximum of f_{SCLK}. The SSEL value can be changed dynamically without any PLL lock latencies by writing the appropriate values to the PLL divisor register (PLL_DIV).

The core clock (CCLK) frequency can also be dynamically changed by means of the CSEL1–0 bits of the PLL_DIV register. Supported CCLK divider ratios are 1, 2, 4, and 8, as shown in Table 7. This programmable core clock capability is useful for fast core frequency modifications.

Table 7. Core Clock Ratios

Signal Name CSEL1–0	Divider Ratio VCO/CCLK	Example Frequency Ratios (MHz)	
		VCO	CCLK
00	1:1	300	300
01	2:1	300	150
10	4:1	400	100
11	8:1	200	25

Table 6. Example System Clock Ratios

Signal Name SSEL3–0	Divider Ratio VCO/SCLK	Example Frequency Ratios (MHz)	
		VCO	SCLK
0010	2:1	100	50
0110	6:1	300	50
1010	10:1	400	40

The maximum CCLK frequency *both* depends on the part's instruction rate (see Page 45) *and* depends on the applied V_{DDINT} voltage. See Table 10 for details. The maximal system clock rate (SCLK) depends on the chip package and the applied V_{DDINT} and V_{DDEXT} voltages (see Table 12).

BOOTING MODES

The processor has several mechanisms (listed in Table 8) for automatically loading internal and external memory after a reset. The boot mode is defined by the BMODE input pins dedicated to this purpose. There are two categories of boot modes.

In master boot modes, the processor actively loads data from parallel or serial memories. In slave boot modes, the processor receives data from external host devices.

Table 8. Booting Modes

BMODE2–0	Description
000	Idle/No Boot
001	Reserved
010	SPI1 master boot from Flash, using $\overline{\text{SPI1_SSEL5}}$ on PG11
011	SPI1 slave boot from external master
100	SPI0 master boot from Flash, using $\overline{\text{SPI0_SSEL2}}$ on PF8
101	Boot from PPI port
110	Boot from UART host device
111	Execute from Internal L1 ROM

The boot modes listed in Table 8 provide a number of mechanisms for automatically loading the processor's internal and external memories after a reset. By default, all boot modes use the slowest meaningful configuration settings. Default settings can be altered via the initialization code feature at boot time. The BMODE pins of the reset configuration register, sampled during power-on resets and software-initiated resets, implement the modes shown in Table 8.

- IDLE State / No Boot (BMODE - 0x0) — In this mode, the boot kernel transitions the processor into Idle state. The processor can then be controlled through JTAG for recovery, debug, or other functions.
- SPI1 master boot from flash (BMODE = 0x2) — In this mode SPI1 is configured to operate in master mode and to connect to 8-, 16-, 24-, or 32-bit addressable devices. The processor uses the PG11/$\overline{\text{SPI1_SSEL5}}$ to select a single SPI EEPROM/flash device, submits a read command and successive address bytes (0×00) until a valid 8-, 16-, 24-, or 32-bit addressable device is detected, and begins clocking data into the processor. Pull-up resistors are required on the SSEL and MISO pins. By default, a value of 0×85 is written to the SPI_BAUD register.
- SPI1 slave boot from external master (BMODE = 0x3) — In this mode SPI1 is configured to operate in slave mode and to receive the bytes of the .LDR file from a SPI host (master) agent. To hold off the host device from transmitting while the boot ROM is busy, the Blackfin processor asserts a GPIO pin, called host wait (HWAIT), to signal to the host device not to send any more bytes until the pin is deasserted. The host must interrogate the HWAIT signal, available on PF4, before transmitting every data unit to the processor. A pull-up resistor is required on the $\overline{\text{SPI1_SS}}$ input. A pull-down on the serial clock may improve signal quality and booting robustness.
- SPI0 master boot from flash (BMODE = 0x4) — In this mode SPI0 is configured to operate in master mode and to connect to 8-, 16-, 24-, or 32-bit addressable devices. The processor uses the PF8/$\overline{\text{SPI0_SSEL2}}$ to select a single SPI EEPROM/flash device, submits a read command and successive address bytes (0×00) until a valid 8-, 16-, 24-, or 32-

bit addressable device is detected, and begins clocking data into the processor. Pull-up resistors are required on the SSEL and MISO pins. By default, a value of 0×85 is written to the SPI_BAUD register.

- Boot from PPI host device (BMODE = 0x5) — The processor operates in PPI slave mode and is configured to receive the bytes of the LDR file from a PPI host (master) agent.
- Boot from UART host device (BMODE = 0x6) — In this mode UART0 is used as the booting source. Using an autobaud handshake sequence, a boot-stream formatted program is downloaded by the host. The host selects a bit rate within the UART clocking capabilities. When performing the autobaud, the UART expects a "@" (0×40) character (eight bits data, one start bit, one stop bit, no parity bit) on the RXD pin to determine the bit rate. The UART then replies with an acknowledgment which is composed of 4 bytes (0xBF—the value of UART_DLL) and (0×00—the value of UART_DLH). The host can then download the boot stream. To hold off the host the processor signals the host with the boot host wait (HWAIT) signal. Therefore, the host must monitor the HWAIT, (on PF4), before every transmitted byte.
- Execute from internal L1 ROM (BMODE = 0x7) — In this mode the processor begins execution from the on-chip 64k Byte L1 instruction ROM starting at address 0xFFA1 0000.

For each of the boot modes (except Execute from internal L1 ROM), a 16 byte header is first brought in from an external device. The header specifies the number of bytes to be transferred and the memory destination address. Multiple memory blocks may be loaded by any boot sequence. Once all blocks are loaded, program execution commences from the start of L1 instruction SRAM.

The boot kernel differentiates between a regular hardware reset and a wakeup-from-hibernate event to speed up booting in the latter case. Bits 7–4 in the system reset configuration (SYSCR) register can be used to bypass the boot kernel or simulate a wakeup-from-hibernate boot in case of a software reset.

The boot process can be further customized by "initialization code." This is a piece of code that is loaded and executed prior to the regular application boot. Typically, this is used to speed up booting by managing the PLL, clock frequencies, or serial bit rates.

The boot ROM also features C-callable functions that can be called by the user application at run time. This enables second stage boot or boot management schemes to be implemented with ease.

INSTRUCTION SET DESCRIPTION

The Blackfin processor family assembly language instruction set employs an algebraic syntax designed for ease of coding and readability. The instructions have been specifically tuned to provide a flexible, densely encoded instruction set that compiles to a very small final memory size. The instruction set also provides fully featured multifunction instructions that allow the programmer to use many of the processor core resources in a single instruction. Coupled with many features more often seen on microcontrollers, this instruction set is very efficient when compiling C and C++ source code. In addition, the architecture supports both user (algorithm/application code) and supervisor (O/S kernel, device drivers, debuggers, ISRs) modes of operation, allowing multiple levels of access to core processor resources.

The assembly language, which takes advantage of the processor's unique architecture, offers the following advantages:

- Seamlessly integrated DSP/MCU features are optimized for both 8-bit and 16-bit operations.
- A multi-issue load/store modified-Harvard architecture, which supports two 16-bit MAC or four 8-bit ALU + two load/store + two pointer updates per cycle.
- All registers, I/O, and memory are mapped into a unified 4G byte memory space, providing a simplified programming model.
- Microcontroller features, such as arbitrary bit and bit-field manipulation, insertion, and extraction; integer operations on 8-, 16-, and 32-bit data-types; and separate user and supervisor stack pointers.
- Code density enhancements, which include intermixing of 16-bit and 32-bit instructions (no mode switching, no code segregation). Frequently used instructions are encoded in 16 bits.

DEVELOPMENT TOOLS

The processor is supported with a complete set of CROSSCORE® software and hardware development tools, including Analog Devices emulators and VisualDSP++® development environment. The same emulator hardware that supports other Blackfin processors also fully emulates the ADSP-BF592 processor.

EZ-KIT Lite® Evaluation Board

For evaluation of the ADSP-BF592 processor, use the EZ-KIT Lite boards *soon to be* available from Analog Devices. *When these evaluation kits are available,* order using part number ADZS-BF592-EZLITE. The boards come with on-chip emulation capabilities and are equipped to enable software development. Multiple daughter cards *will be* available.

DESIGNING AN EMULATOR-COMPATIBLE PROCESSOR BOARD (TARGET)

The Analog Devices family of emulators are tools that every system developer needs in order to test and debug hardware and software systems. Analog Devices has supplied an IEEE 1149.1 JTAG Test Access Port (TAP) on each JTAG processor. The emulator uses the TAP to access the internal features of the processor, allowing the developer to load code, set breakpoints, observe variables, observe memory, and examine registers. The processor must be halted to send data and commands, but once an operation has been completed by the emulator, the processor system is set running at full speed with no impact on system timing.

To use these emulators, the target board must include a header that connects the processor's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, multiprocessor scan chains, signal buffering, signal termination, and emulator pod logic, see *(EE-68) Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

RELATED DOCUMENTS

The following publications that describe the ADSP-BF592 processor (and related processors) can be ordered from any Analog Devices sales office or accessed electronically on our website:

- *Getting Started With Blackfin Processors*
- *ADSP-BF59x Blackfin Processor Hardware Reference*
- *Blackfin Processor Programming Reference*
- *ADSP-BF592 Blackfin Processor Anomaly List*

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab™ site (http:\\www.analog.com\signalchains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

SIGNAL DESCRIPTIONS

Signal definitions for the ADSP-BF592 processor are listed in Table 9. In order to maintain maximum function and reduce package size and pin count, some pins have dual, multiplexed functions. In cases where pin function is reconfigurable, the default state is shown in plain text, while the alternate function is shown in italics.

All pins are three-stated during and immediately after reset, with the exception of EXT_CLK, which toggles at the system clock rate.

All I/O pins have their input buffers disabled with the exception of the pins that need pull-ups or pull-downs, as noted in Table 9.

Adding a parallel termination to EXT_CLK may prove useful in further enhancing signal integrity. Be sure to verify overshoot/undershoot and signal integrity specifications on actual hardware.

Table 9. Signal Descriptions

Signal Name	Type	Function	Driver Type
Port F: *GPIO and Multiplexed Peripherals*			
PF0–GPIO/*DR1SEC/PPI_D8/WAKEN1*	I/O	GPIO/*SPORT1 Receive Data Secondary/PPI Data 8/Wake Enable 1*	A
PF1–GPIO/*DR1PRI/PPI_D9*	I/O	GPIO/*SPORT1 Receive Data Primary/PPI Data 9*	A
PF2–GPIO/*RSCLK1/PPI_D10*	I/O	GPIO/*SPORT1 Receive Serial Clock/PPI Data 10*	A
PF3–GPIO/*RFS1/PPI_D11*	I/O	GPIO/*SPORT1 Receive Frame Sync/PPI Data 11*	A
PF4–GPIO/*DT1SEC/PPI_D12*	I/O	GPIO/*SPORT1 Transmit Data Secondary/PPI Data 12*	A
PF5–GPIO/*DT1PRI/PPI_D13*	I/O	GPIO/*SPORT1 Transmit Data Primary/PPI Data 13*	A
PF6–GPIO/*TSCLK1/PPI_D14*	I/O	GPIO/*SPORT1 Transmit Serial Clock/PPI Data 14*	A
PF7–GPIO/*TFS1/PPI_D15*	I/O	GPIO/*SPORT1 Transmit Frame Sync/PPI Data 15*	A
PF8–GPIO/*TMR2/$\overline{\text{SPI0_SSEL2}}$/WAKEN0*	I/O	GPIO/*Timer 2/SPI0 Slave Select Enable 2/Wake Enable 0*	A
PF9–GPIO/*TMR0/PPI_FS1/*$\overline{\text{SPI0_SSEL3}}$	I/O	GPIO/*Timer 0/PPI Frame Sync 1/SPI0 Slave Select Enable 3*	A
PF10–GPIO/*TMR1/PPI_FS2*	I/O	GPIO/*Timer 1/PPI Frame Sync 2*	A
PF11–GPIO/*UA_TX/$\overline{\text{SPI0_SSEL4}}$*	I/O	GPIO/*UART Transmit/SPI0 Slave Select Enable 4*	A
PF12–GPIO/*UA_RX/$\overline{\text{SPI0_SSEL7}}$/TACI2–0*	I/O	GPIO/*UART Receive/SPI0 Slave Select Enable 7/Timers 2–0 Alternate Input Capture*	A
PF13–GPIO/*SPI0_MOSI/$\overline{\text{SPI1_SSEL3}}$*	I/O	GPIO/*SPI0 Master Out Slave In/SPI1 Slave Select Enable 3*	A
PF14–GPIO/*SPI0_MISO/$\overline{\text{SPI1_SSEL4}}$*	I/O	GPIO/*SPI0 Master In Slave Out/SPI1 Slave Select Enable 4* (This pin should always be pulled high through a 4.7 kΩ resistor, if booting via the SPI port.)	A
PF15–GPIO/*SPI0_SCK/$\overline{\text{SPI1_SSEL5}}$*	I/O	GPIO/*SPI0 Clock/SPI1 Slave Select Enable 5*	A
Port G: *GPIO and Multiplexed Peripherals*			
PG0–GPIO/*DR0SEC/$\overline{\text{SPI0_SSEL1}}$/$\overline{\text{SPI0_SS}}$*	I/O	GPIO/*SPORT0 Receive Data Secondary/SPI0 Slave Select Enable 1/SPI0 Slave Select Input*	A
PG1–GPIO/*DR0PRI/$\overline{\text{SPI1_SSEL1}}$/WAKEN3*	I/O	GPIO/*SPORT0 Receive Data Primary/SPI1 Slave Select Enable 1/Wake Enable 3*	A
PG2–GPIO/*RSCLK0/$\overline{\text{SPI0_SSEL5}}$*	I/O	GPIO/*SPORT0 Receive Serial Clock/SPI0 Slave Select Enable 5*	A
PG3–GPIO/*RFS0/PPI_FS3*	I/O	GPIO/*SPORT0 Receive Frame Sync/PPI Frame Sync 3*	A
PG4–GPIO(HWAIT)/*DT0SEC/$\overline{\text{SPI0_SSEL6}}$*	I/O	GPIO (HWAIT output for Slave Boot Modes)/*SPORT0 Transmit Data Secondary/SPI0 Slave Select Enable 6*	A
PG5–GPIO/*DT0PRI/$\overline{\text{SPI1_SSEL6}}$*	I/O	GPIO/*SPORT0 Transmit Data Primary/SPI1 Slave Select Enable 6*	A
PG6–GPIO/*TSCLK0*	I/O	GPIO/*SPORT0 Transmit Serial Clock*	A
PG7–GPIO/*TFS0/$\overline{\text{SPI1_SSEL7}}$*	I/O	GPIO/*SPORT0 Transmit Frame Sync/SPI1 Slave Select Enable 7*	A
PG8–GPIO/*SPI1_SCK/PPI_D0*	I/O	GPIO/*SPI1 Clock/PPI Data 0*	A
PG9–GPIO/*SPI1_MOSI/PPI_D1*	I/O	GPIO/*SPI1 Master Out Slave In/PPI Data 1*	A
PG10–GPIO/*SPI1_MISO/PPI_D2*	I/O	GPIO/*SPI1 Master In Slave Out/PPI Data 2* (This pin should always be pulled high through a 4.7 kΩ resistor if booting via the SPI port.)	A

Table 9. Signal Descriptions (Continued)

Signal Name	Type	Function	Driver Type
PG11–GPIO/*SPI1_SSEL5*/*PPI_D3*	I/O	GPIO/*SPI1 Slave Select Enable 5*/*PPI Data 3*	A
PG12–GPIO/*SPI1_SSEL2*/*PPI_D4*/*WAKEN2*	I/O	GPIO/*SPI1 Slave Select Enable 2 Output*/*PPI Data 4*/*Wake Enable 2*	A
PG13–GPIO/*SPI1_SSEL1*/*SPI1_SS*/*PPI_D5*	I/O	GPIO/*SPI1 Slave Select Enable 1 Output*/*PPI Data 5*/*SPI1 Slave Select Input*	A
PG14–GPIO/*SPI1_SSEL4*/*PPI_D6*/*TACLK1*	I/O	GPIO/*SPI1 Slave Select Enable 4*/*PPI Data 6*/*Timer 1 Auxiliary Clock Input*	A
PG15–GPIO/*SPI1_SSEL6*/*PPI_D7*/*TACLK2*	I/O	GPIO/*SPI1 Slave Select Enable 6*/*PPI Data 7*/*Timer 2 Auxiliary Clock Input*	A
TWI			
SCL	I/O	TWI Serial Clock (This signal is an open-drain output and requires a pull-up resistor. Consult version 2.1 of the I^2C specification for the proper resistor value.)	B
SDA	I/O	TWI Serial Data (This signal is an open-drain output and requires a pull-up resistor. Consult version 2.1 of the I^2C specification for the proper resistor value.)	B
JTAG Port			
TCK	I	JTAG CLK	
TDO	O	JTAG Serial Data Out	A
TDI	I	JTAG Serial Data In	
TMS	I	JTAG Mode Select	
$\overline{\text{TRST}}$	I	JTAG Reset (This lead should be pulled low if the JTAG port is not used.)	
$\overline{\text{EMU}}$	O	Emulation Output	A
Clock			
CLKIN	I	CLK/Crystal In	
XTAL	O	Crystal Output	
EXT_CLK	O	External Clock Output pin/System Clock Output	C
Mode Controls			
$\overline{\text{RESET}}$	I	Reset	
$\overline{\text{NMI}}$	I	Nonmaskable Interrupt (This lead should be pulled high when not used.)	
BMODE2–0	I	Boot Mode Strap 2–0	
PPI_CLK	I	PPI Clock Input	
External Regulator Control			
$\overline{\text{PG}}$	I	Power Good indication	
EXT_WAKE	O	Wake up Indication	A
Power Supplies		**ALL SUPPLIES MUST BE POWERED** See Operating Conditions on Page 18.	
V_{DDEXT}	P	I/O Power Supply	
V_{DDINT}	P	Internal Power Supply	
GND	G	Ground for All Supplies (Back Side of LFCSP Package.)	

SPECIFICATIONS

Specifications are subject to change without notice.

OPERATING CONDITIONS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DDINT}	Internal Supply Voltage		1.16		1.47	V
V_{DDEXT}[1]	External Supply Voltage		1.7	1.8/2.5/3.3	3.6	V
V_{IH}	High Level Input Voltage[2, 3]	V_{DDEXT} = 1.9 V	1.1			V
$V_{IHCLKIN}$	High Level Input Voltage[2, 3]	V_{DDEXT} = 1.9 V	1.2			V
V_{IH}	High Level Input Voltage[2, 3]	V_{DDEXT} = 2.75 V	1.7			V
V_{IH}	High Level Input Voltage[2, 3]	V_{DDEXT} = 3.6 V	2.0			V
$V_{IHCLKIN}$	High Level Input Voltage[2, 3]	V_{DDEXT} = 3.6 V	2.2			V
V_{IHTWI}	High Level Input Voltage[4]	V_{DDEXT} = 1.90 V/2.75 V/3.6 V	0.7 × V_{VDDEXT}		5.5	V
V_{IL}	Low Level Input Voltage[2, 3]	V_{DDEXT} = 1.7 V			0.6	V
V_{IL}	Low Level Input Voltage[2, 3]	V_{DDEXT} = 2.25 V			0.7	V
V_{IL}	Low Level Input Voltage[2, 3]	V_{DDEXT} = 3.0 V			0.8	V
V_{ILTWI}	Low Level Input Voltage[4]	V_{DDEXT} = Minimum			0.3 × V_{VDDEXT}	V
T_J	Junction Temperature	64-Lead LFCSP @ $T_{AMBIENT}$ = 0°C to +70°C	0		80	°C
T_J	Junction Temperature	64-Lead LFCSP @ $T_{AMBIENT}$ = –40°C to +85°C	–40		95	°C

[1] Must remain powered (even if the associated function is not used).

[2] Bidirectional leads (PF15–0, PG15–0) and input leads (TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, $\overline{NMI}$, and BMODE2–0) of the ADSP-BF592 processor are 3.3 V tolerant (always accept up to 3.6 V maximum V_{IH}). Voltage compliance (on outputs, V_{OH}) is limited by the V_{DDEXT} supply voltage.

[3] Parameter value applies to all input and bidirectional leads, except SDA and SCL.

[4] Parameter applies to SDA and SCL.

ADSP-BF592 Clock Related Operating Conditions

Table 10 describes the core clock timing requirements for the ADSP-BF592 processor. Take care in selecting MSEL, SSEL, and CSEL ratios so as not to exceed the maximum core clock and system clock (see Table 12). Table 11 describes phase-locked loop operating conditions.

Table 10. Core Clock (CCLK) Requirements[1]

Parameter		Nominal Voltage Setting	Max	Unit
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.33 V Minimum)[2]	1.400 V	400	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.16 V Minimum)	1.225 V	300	MHz

[1] See the Ordering Guide on Page 45.
[2] Applies only to 400 MHz instruction rates. See the Ordering Guide on Page 45.

Table 11. Phase-Locked Loop Operating Conditions

Parameter		Minimum	Maximum	Unit
f_{VCO}	Voltage Controlled Oscillator (VCO) Frequency	70	Instruction Rate[1]	MHz

[1] See the Ordering Guide on Page 45.

Table 12. SCLK Conditions

Parameter[1]		Maximum	Unit
f_{SCLK}	CLKOUT/SCLK Frequency (V_{DDINT} ≥ 1.16 V Minimum)	100	MHz

[1] f_{SCLK} must be less than or equal to f_{CCLK} and is subject to additional restrictions for SDRAM interface operation. See Table 32 on Page 35.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	Min	Typical	Max	Unit
V_{OH}	High Level Output Voltage	V_{DDEXT} = 1.7 V, I_{OH} = –0.5 mA	1.35			V
V_{OH}	High Level Output Voltage	V_{DDEXT} = 2.25 V, I_{OH} = –0.5 mA	2.0			V
V_{OH}	High Level Output Voltage	V_{DDEXT} = 3.0 V, I_{OH} = –0.5 mA	2.4			V
V_{OL}	Low Level Output Voltage	V_{DDEXT} = 1.7 V/2.25 V/3.0 V, I_{OL} = 2.0 mA			0.4	V
V_{OLTWI}	Low Level Output Voltage	V_{DDEXT} = 1.7 V/2.25 V/3.0 V, I_{OL} = 2.0 mA			0.4	V V
I_{IH}	High Level Input Current[1]	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V			10	µA
I_{IL}	Low Level Input Current[1]	V_{DDEXT} = 3.6 V, V_{IN} = 0 V			10	µA
I_{IHP}	High Level Input Current JTAG[2]	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V	10		50	µA
I_{OZH}	Three-State Leakage Current[3]	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V			10	µA
I_{OZHTWI}	Three-State Leakage Current[4]	V_{DDEXT} = 3.0 V, V_{IN} = 5.5 V			10	µA
I_{OZL}	Three-State Leakage Current[3]	V_{DDEXT} = 3.6 V, V_{IN} = 0 V			10	µA
C_{IN}	Input Capacitance[5]	f_{IN} = 1 MHz, $T_{AMBIENT}$ = 25°C, V_{IN} = 2.5 V		4	8[6]	pF
$I_{DDDEEPSLEEP}$[7]	V_{DDINT} Current in Deep Sleep Mode	V_{DDINT} = 1.2 V, f_{CCLK} = 0 MHz, f_{SCLK} = 0 MHz, T_J = 25°C, ASF = 0.00		0.8		mA
$I_{DDSLEEP}$	V_{DDINT} Current in Sleep Mode	V_{DDINT} = 1.2 V, f_{SCLK} = 25 MHz, T_J = 25°C		4		mA
$I_{DD-IDLE}$	V_{DDINT} Current in Idle	V_{DDINT} = 1.2 V, f_{CCLK} = 50 MHz, T_J = 25°C, ASF = 0.35		6		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.3 V, f_{CCLK} = 300 MHz, T_J = 25°C, ASF = 1.00		66		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.4 V, f_{CCLK} = 400 MHz, T_J = 25°C, ASF = 1.00		91		mA
$I_{DDHIBERNATE}$[7]	Hibernate State Current	V_{DDEXT} = 3.3 V, T_J = 25°C, CLKIN = 0 MHz with voltage regulator off (V_{DDINT} = 0 V)		20		µA
$I_{DDDEEPSLEEP}$[7]	V_{DDINT} Current in Deep Sleep Mode	f_{CCLK} = 0 MHz, f_{SCLK} = 0 MHz			Table 14	mA
I_{DDINT}[8]	V_{DDINT} Current	f_{CCLK} > 0 MHz, f_{SCLK} ≥ 0 MHz			Table 14 + (Table 15 × ASF)	mA

[1] Applies to input pins.
[2] Applies to JTAG input pins (TCK, TDI, TMS, $\overline{\text{TRST}}$).
[3] Applies to three-statable pins.
[4] Applies to bidirectional pins SCL and SDA.
[5] Applies to all signal pins.
[6] Guaranteed, but not tested.
[7] See the *ADSP-BF52x Blackfin Processor Hardware Reference Manual* for definition of sleep, deep sleep, and hibernate operating modes.
[8] See Table 13 for the list of I_{DDINT} power vectors covered.

Total Power Dissipation

Total power dissipation has two components:

1. Static, including leakage current
2. Dynamic, due to transistor switching characteristics

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. Electrical Characteristics on Page 20 shows the current dissipation for internal circuitry (V_{DDINT}). $I_{DDDEEPSLEEP}$ specifies static power dissipation as a function of voltage (V_{DDINT}) and temperature (see Table 14), and I_{DDINT} specifies the total power specification for the listed test conditions, including the dynamic component as a function of voltage (V_{DDINT}) and frequency (Table 15).

There are two parts to the dynamic component. The first part is due to transistor switching in the core clock (CCLK) domain. This part is subject to an Activity Scaling Factor (ASF) which represents application code running on the processor core and L1 memories (Table 13).

The ASF is combined with the CCLK Frequency and V_{DDINT} dependent data in Table 15 to calculate this part. The second part is due to transistor switching in the system clock (SCLK) domain, which is included in the I_{DDINT} specification equation.

Table 13. Activity Scaling Factors (ASF)[1]

I_{DDINT} Power Vector	Activity Scaling Factor (ASF)
$I_{DD-PEAK}$	1.29
$I_{DD-HIGH}$	1.26
I_{DD-TYP}	1.00
I_{DD-APP}	0.83
I_{DD-NOP}	0.66
$I_{DD-IDLE}$	0.33

[1] See *Estimating Power for ASDP-BF534/BF536/BF537 Blackfin Processors (EE-297)*. The power vector information also applies to the ADSP-BF592 processor.

Table 14. Preliminary ADSP-BF592 Static Current - $I_{DD-DEEPSLEEP}$ (mA)[1]

T_J (°C)[2]	Voltage (V_{DDINT})[2]							
	1.15 V	1.20 V	1.25 V	1.30 V	1.35 V	1.40 V	1.45 V	1.50 V
25	0.85	0.98	1.13	1.29	1.46	1.62	1.85	2.07
40	1.57	1.8	2.01	2.16	2.51	2.74	3.05	3.36
55	2.57	2.88	3.2	3.5	3.84	4.22	4.63	5.05
70	4.04	4.45	4.86	5.3	5.81	6.31	6.87	7.45
85	6.52	7.12	7.73	8.36	9.09	9.86	10.67	11.54
100	9.67	10.51	11.37	12.24	13.21	14.26	15.37	16.55
115	14.18	15.29	16.45	17.71	19.05	20.45	21.96	23.56

[1] All specifications and references to ADSP-BF592 Blackfin processor are preliminary and subject to change.
[2] Valid temperature and voltage ranges are model-specific. See Operating Conditions on Page 18.

Table 15. Preliminary ADSP-BF592 Dynamic Current in CCLK Domain (mA, with ASF = 1.0)[1, 2]

f_{CCLK} (MHz)[3]	Voltage (V_{DDINT})[3]							
	1.15 V	1.20 V	1.25 V	1.30 V	1.35 V	1.40 V	1.45 V	1.50 V
400	N/A	N/A	N/A	81.55	85.31	88.96	92.81	96.63
350	N/A	N/A	N/A	72.08	75.41	78.70	82.07	85.46
300	N/A	57.52	60.38	63.22	66.14	69.02	71.93	75.05
250	46.10	48.43	50.76	53.19	55.68	58.17	60.69	63.23
200	37.86	39.80	41.76	43.79	45.81	47.85	49.97	52.09
100	21.45	22.56	23.78	24.98	25.97	26.64	27.92	29.98

[1] All specifications and references to ADSP-BF592 Blackfin processor are preliminary and subject to change.
[2] The values are not guaranteed as stand-alone maximum specifications. They must be combined with static current per the equations of Electrical Characteristics on Page 20.
[3] Valid frequency and voltage ranges are model-specific. See Operating Conditions on Page 18.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 16 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 16. Absolute Maximum Ratings

Parameter	Rating
Internal Supply Voltage (V_{DDINT})	1.16 V to +1.47 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +3.8 V
Input Voltage[1, 2]	–0.5 V to +3.6 V
Output Voltage Swing	–0.5 V to V_{DDEXT}+0.5 V
I_{OH}/I_{OL} Current per Pin Group	55 mA (Max)
I_{OH}/I_{OL} Current per Individual Pin	25 mA (Max)
Storage Temperature Range	–65°C to +150°C
Junction Temperature While Biased	+110°C

[1] Applies to 100% transient duty cycle. For other duty cycles see Table 17.
[2] Applies only when V_{DDEXT} is within specifications. When V_{DDEXT} is outside specifications, the range is V_{DDEXT} ± 0.2 Volts.

Table 17. Maximum Duty Cycle for Input Transient Voltage[1]

V_{IN} Min (V)[2]	V_{IN} Max (V)[2]	Maximum Duty Cycle[3]
–0.5	+3.8	100%
–0.7	+4.0	40%
–0.8	+4.1	25%
–0.9	+4.2	15%
–1.0	+4.3	10%

[1] Applies to all signal pins with the exception of CLKIN, XTAL, EXT_WAKE.
[2] The individual values cannot be combined for analysis of a single instance of overshoot or undershoot. The worst case observed value must fall within one of the voltages specified and the total duration of the overshoot or undershoot (exceeding the 100% case) must be less than or equal to the corresponding duty cycle.
[3] Duty cycle refers to the percentage of time the signal exceeds the value for the 100% case. The is equivalent to the measured duration of a single instance of overshoot or undershoot as a percentage of the period of occurrence.

Table 16 specifies the maximum total source/sink (I_{OH}/I_{OL}) current for a group of pins and for individual pins. Permanent damage can occur if this value is exceeded. To understand this specification, if pins PF0 and PF1 from Group 1 in the Total Current Pin Groups-Vddext Groups table were sourcing or sinking 10 mA each, the total current for those pins would be 20 mA. This would allow up to 35 mA total that could be sourced or sunk by the remaining pins in the group without damaging the device. It should also be noted that the maximum source or sink current for an individual pin can not exceed 25 mA. For a list of all groups and their pins, see Table 18. Note that the V_{OH} and V_{OL} specifications have separate per-pin maximum current requirements, see the Electrical Characteristics table.

Table 18. Total Current Pin Groups–V_{DDEXT} Groups

Group	Pins in Group
1	PF0, PF1, PF2, PF3
2	PF4, PF5, PF6, PF7
3	PF8, PF9, PF10, PF11
4	PF12, PF13, PF14, PF15
5	PG3, PG2, PG1, PG0
6	PG7, PG6, PG5, PG4
7	PG11, PG10, PG9, PG8
8	PG15, PG14, PG13, PG12
9	TDI, TDO, EMU, TCK, $\overline{TRST}$, TMS
10	BMODE2, BMODE1, BMODE0
11	EXT_WAKE, $\overline{PG}$, $\overline{RESET}$, $\overline{NMI}$, PPI_CLK, CLKBUF
12	SDA, SCL, CLKIN, XTAL

ESD SENSITIVITY



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

The information presented in Figure 6 and Table 19 provides details about the package branding for the ADSP-BF592 processor. For a complete listing of product availability, see Ordering Guide on Page 45.

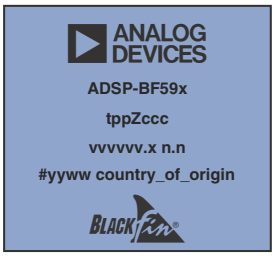


Figure 6. Product Information on Package

Table 19. Package Brand Information

Brand Key	Field Description
ADSP-BF592	Product Name
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Designation
ccc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliance Designator
yyww	Date Code

TIMING SPECIFICATIONS

Specifications are subject to change without notice.

Clock and Reset Timing

Table 20 and Figure 7 describe clock and reset operations. Per the CCLK and SCLK timing specifications in Table 10 to Table 12, combinations of CLKIN and clock multipliers must not select core/peripheral clocks in excess of the processor's instruction rate.

Table 20. Clock and Reset Timing

Parameter		V_{DDEXT} 1.8 V Nominal Min	V_{DDEXT} 1.8 V Nominal Max	V_{DDEXT} 2.5/3.3 V Nominal Min	V_{DDEXT} 2.5/3.3 V Nominal Max	Unit
Timing Requirements						
f_{CKIN}	CLKIN Period[1, 2, 3, 4]	12	50	12	50	MHz
t_{CKINL}	CLKIN Low Pulse[1]	10		10		ns
t_{CKINH}	CLKIN High Pulse[1]	10		10		ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulse Width Low[5]	$11 \times t_{CKIN}$		$11 \times t_{CKIN}$		ns
Switching Characteristic						
$t_{BUFDLAY}$	CLKIN to CLKBUF Delay		TBD		10	ns

[1] Applies to PLL bypass mode and PLL non bypass mode.
[2] Combinations of the CLKIN frequency and the PLL clock multiplier must not exceed the allowed f_{VCO}, f_{CCLK}, and f_{SCLK} settings discussed in Table 10 on Page 19 through Table 12 on Page 19.
[3] The t_{CKIN} period (see Figure 7) equals $1/f_{CKIN}$.
[4] If the DF bit in the PLL_CTL register is set, the minimum f_{CKIN} specification is 24 MHz.
[5] Applies after power-up sequence is complete. See Table 21 and Figure 8 for power-up reset timing.

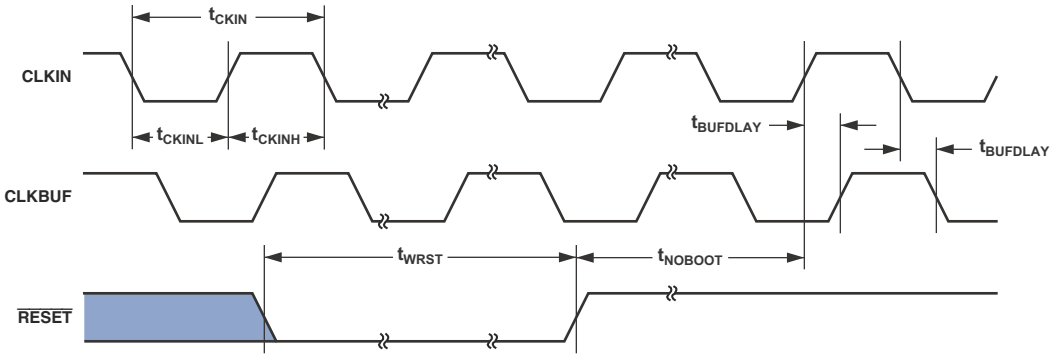


Figure 7. Clock and Reset Timing

Table 21. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
$t_{RST_IN_PWR}$	$\overline{\text{RESET}}$ Deasserted after the V_{DDINT}, V_{DDEXT}, and CLKIN Pins are Stable and Within Specification	$3500 \times t_{CKIN}$		µs

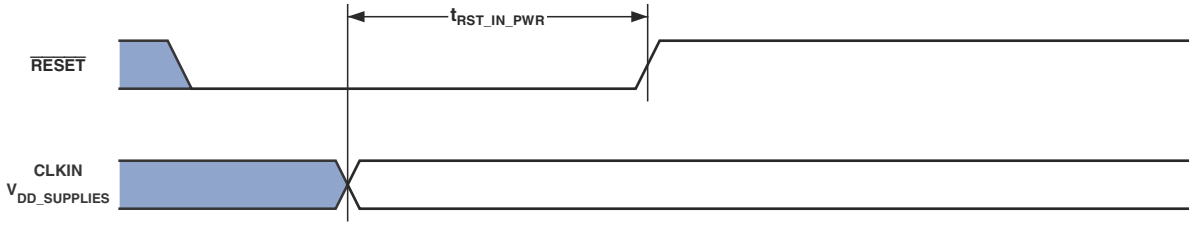


Figure 8. Power-Up Reset Timing

Parallel Peripheral Interface Timing

Table 22 and Figure 9 on Page 25, Figure 13 on Page 28, and Figure 15 on Page 29 describe parallel peripheral interface operations.

Table 22. Parallel Peripheral Interface Timing

Parameter		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5/3.3 V Nominal		Unit
		Min	Max	Min	Max	
Timing Requirements						
t_{PCLKW}	PPI_CLK Width[1]	TBD		TBD		ns
t_{PCLK}	PPI_CLK Period[1]	TBD		TBD		ns
Timing Requirements - GP Input and Frame Capture Modes						
t_{SFSPE}	External Frame Sync Setup Before PPI_CLK (Nonsampling Edge for Rx, Sampling Edge for Tx)	TBD		TBD		ns
t_{HFSPE}	External Frame Sync Hold After PPI_CLK	TBD		TBD		ns
t_{SDRPE}	Receive Data Setup Before PPI_CLK	TBD		TBD		ns
t_{HDRPE}	Receive Data Hold After PPI_CLK	TBD		TBD		ns
Switching Characteristics - GP Output and Frame Capture Modes						
t_{DFSPE}	Internal Frame Sync Delay After PPI_CLK		TBD		TBD	ns
t_{HOFSPE}	Internal Frame Sync Hold After PPI_CLK	TBD		TBD		ns
t_{DDTPE}	Transmit Data Delay After PPI_CLK		TBD		TBD	ns
t_{HDTPE}	Transmit Data Hold After PPI_CLK	TBD		TBD		ns

[1] PPI_CLK frequency cannot exceed $f_{SCLK}/2$

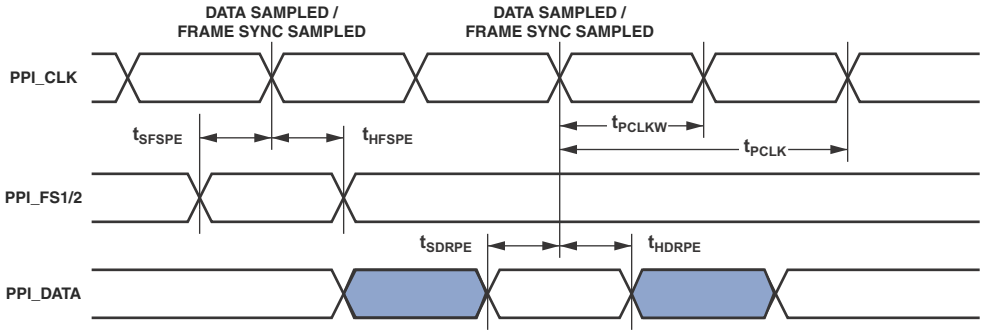


Figure 9. PPI GP Rx Mode with External Frame Sync Timing

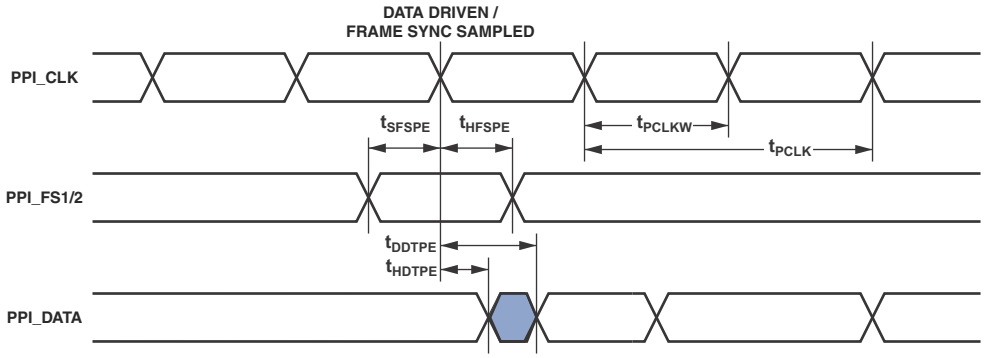


Figure 10. PPI GP Tx Mode with External Frame Sync Timing

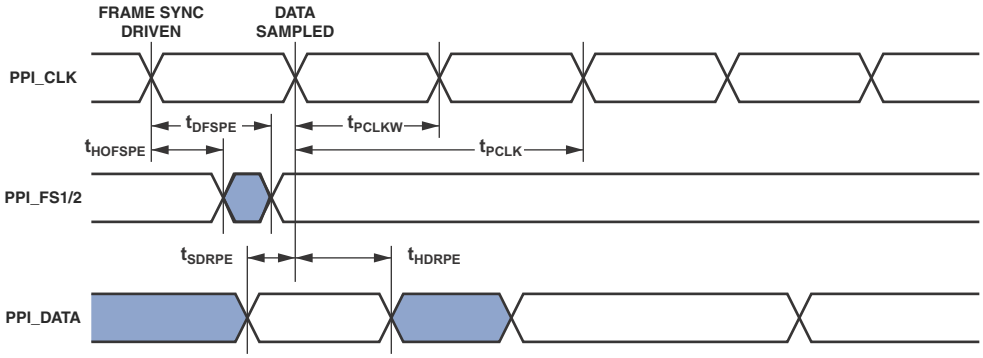


Figure 11. PPI GP Rx Mode with Internal Frame Sync Timing

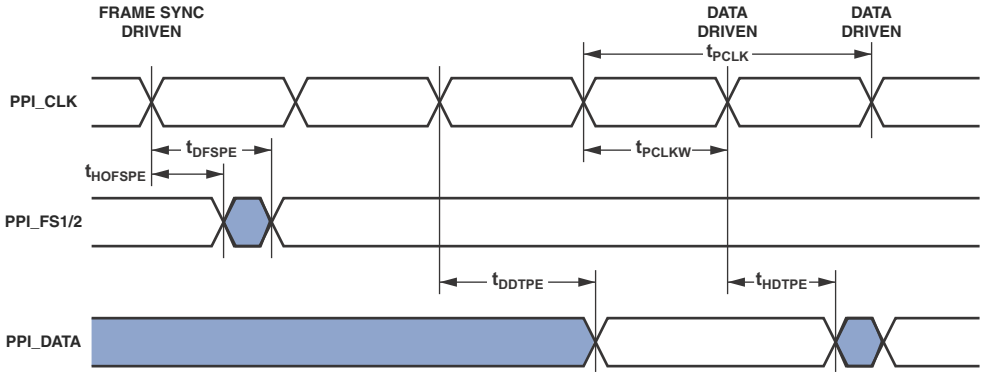


Figure 12. PPI GP Tx Mode with Internal Frame Sync Timing

Serial Ports

Table 23 through Table 26 on Page 29 and Figure 13 on Page 28 through Figure 15 on Page 29 describe serial port operations.

Table 23. Serial Ports—External Clock

Parameter		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5/3.3 V Nominal		Unit
		Min	Max	Min	Max	
Timing Requirements						
t_{SFSE}	TFSx/RFSx Setup Before TSCLKx/RSCLKx[1]	TBD		3		ns
t_{HFSE}	TFSx/RFSx Hold After TSCLKx/RSCLKx[1]	TBD		3		ns
t_{SDRE}	Receive Data Setup Before RSCLKx[1]	TBD		3		ns
t_{HDRE}	Receive Data Hold After RSCLKx[1]	TBD		3.6		ns
t_{SCLKEW}	TSCLKx/RSCLKx Width	TBD		5.4		ns
t_{SCLKE}	TSCLKx/RSCLKx Period	TBD		$2 \times t_{SCLK}$		ns
t_{SUDTE}	Start-Up Delay From SPORT Enable To First External TFSx[2]	$4 \times t_{TSCLKE}$		$4 \times t_{TSCLKE}$		ns
t_{SUDRE}	Start-Up Delay From SPORT Enable To First External RFSx[2]	$4 \times t_{RSCLKE}$		$4 \times t_{RSCLKE}$		ns
Switching Characteristics						
t_{DFSE}	TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[3]		TBD		12	ns
t_{HOFSE}	TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[1]	TBD		0		ns
t_{DDTE}	Transmit Data Delay After TSCLKx[1]		TBD		12	ns
t_{HDTE}	Transmit Data Hold After TSCLKx[1]	TBD		0		ns

[1] Referenced to sample edge.
[2] Verified in design but untested.
[3] Referenced to drive edge.

Table 24. Serial Ports—Internal Clock

Parameter		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5/3.3 V Nominal		Unit
		Min	Max	Min	Max	
Timing Requirements						
t_{SFSI}	TFSx/RFSx Setup Before TSCLKx/RSCLKx[1]	TBD		11.3		ns
t_{HFSI}	TFSx/RFSx Hold After TSCLKx/RSCLKx[1]	TBD		–1.5		ns
t_{SDRI}	Receive Data Setup Before RSCLKx[1]	TBD		11.3		ns
t_{HDRI}	Receive Data Hold After RSCLKx[1]	TBD		–1.5		ns
Switching Characteristics						
t_{SCLKIW}	TSCLKx/RSCLKx Width	TBD		5.4		ns
t_{SCLKI}	TSCLKx/RSCLKx Period	TBD		18		ns
t_{DFSI}	TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[2]		TBD		3	ns
t_{HOFSI}	TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[1]	TBD		–1		ns
t_{DDTI}	Transmit Data Delay After TSCLKx[1]		TBD		3	ns
t_{HDTI}	Transmit Data Hold After TSCLKx[1]	TBD		–1.8		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

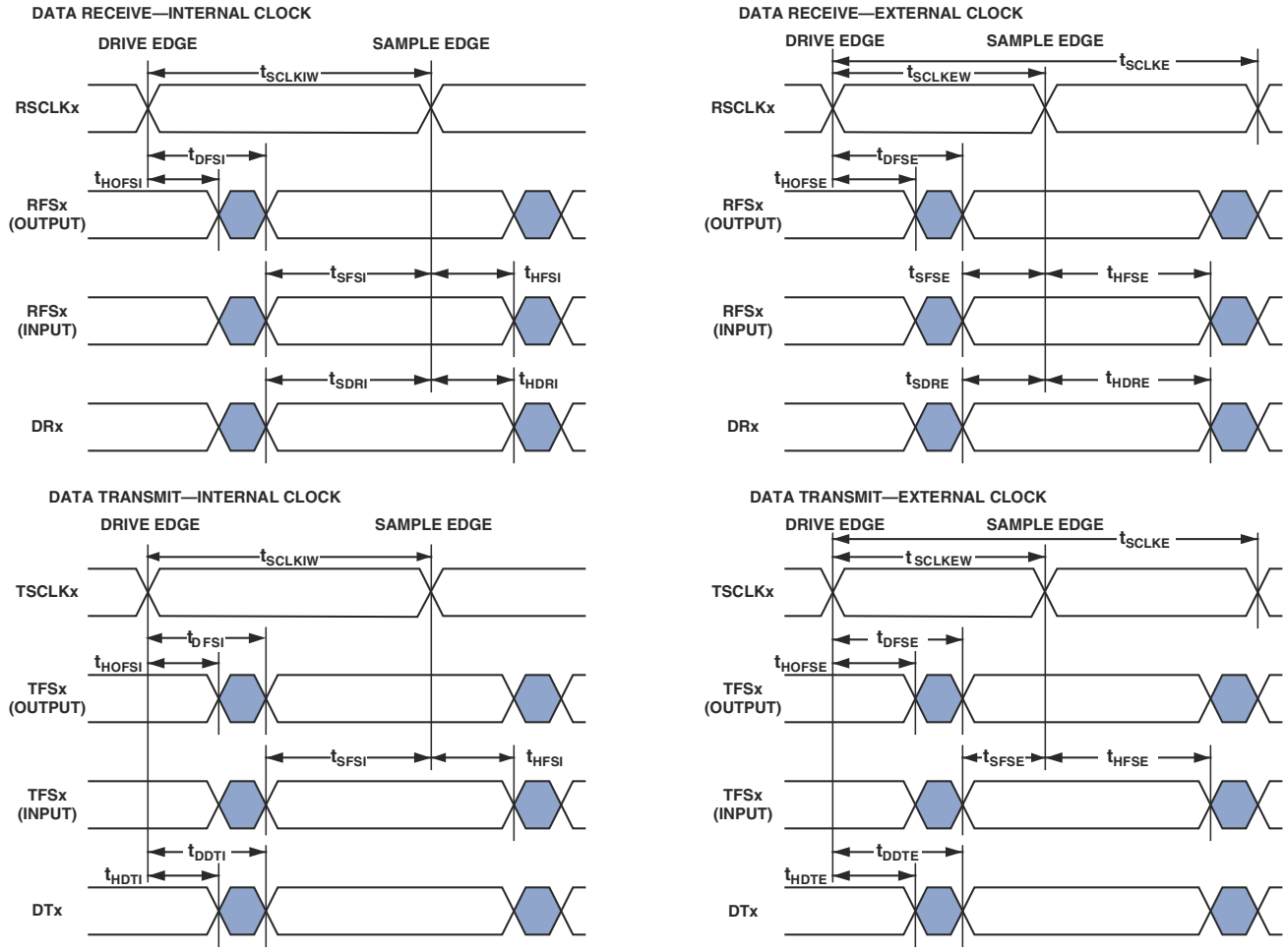


Figure 13. Serial Ports

Table 25. Serial Ports—Enable and Three-State

Parameter		V_{DDEXT} 1.8 V Nominal Min	V_{DDEXT} 1.8 V Nominal Max	V_{DDEXT} 2.5/3.3 V Nominal Min	V_{DDEXT} 2.5/3.3 V Nominal Max	Unit
Switching Characteristics						
t_{DTENE}	Data Enable Delay from External TSCLKx[1]	TBD		0		ns
t_{DDTTE}	Data Disable Delay from External TSCLKx[1]		TBD		t_{SCLK} + 1	ns
t_{DTENI}	Data Enable Delay from Internal TSCLKx[1]	TBD		–2		ns
t_{DDTTI}	Data Disable Delay from Internal TSCLKx[1]		TBD		t_{SCLK} + 1	ns

[1] Referenced to drive edge.

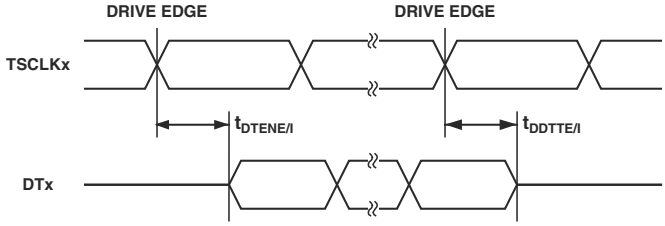


Figure 14. Serial Ports — Enable and Three-State

Table 26. Serial Ports — External Late Frame Sync

Parameter		V_{DDEXT} 1.8 V Nominal Min	V_{DDEXT} 1.8 V Nominal Max	V_{DDEXT} 2.5/3.3 V Nominal Min	V_{DDEXT} 2.5/3.3 V Nominal Max	Unit
Switching Characteristics						
$t_{DDTLFSE}$	Data Delay from Late External TFSx or External RFSx in multi-channel mode with MFD = 0[1, 2]		TBD		10	ns
$t_{DTENLFSE}$	Data Enable from External RFSx in multi-channel mode with MFD = 0[1, 2]	TBD		0		ns

[1] When in multi-channel mode, TFSx enable and TFSx valid follow $t_{DTENLFSE}$ and $t_{DDTLFSE}$.
[2] If external RFSx/TFSx setup to RSCLKx/TSCLKx > $t_{SCLKE}/2$ then $t_{DDTTE/I}$ and $t_{DTENE/I}$ apply, otherwise $t_{DDTLFSE}$ and $t_{DTENLFSE}$ apply.

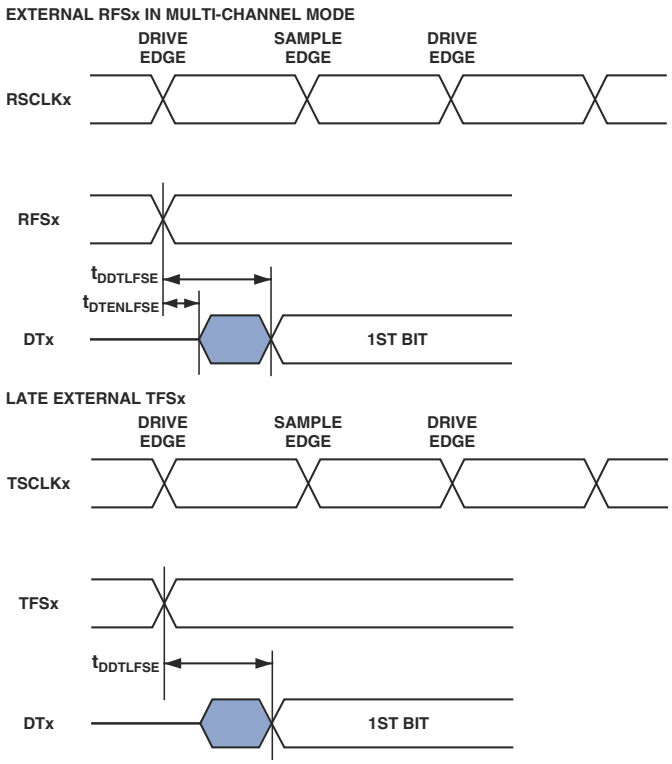


Figure 15. Serial Ports — External Late Frame Sync

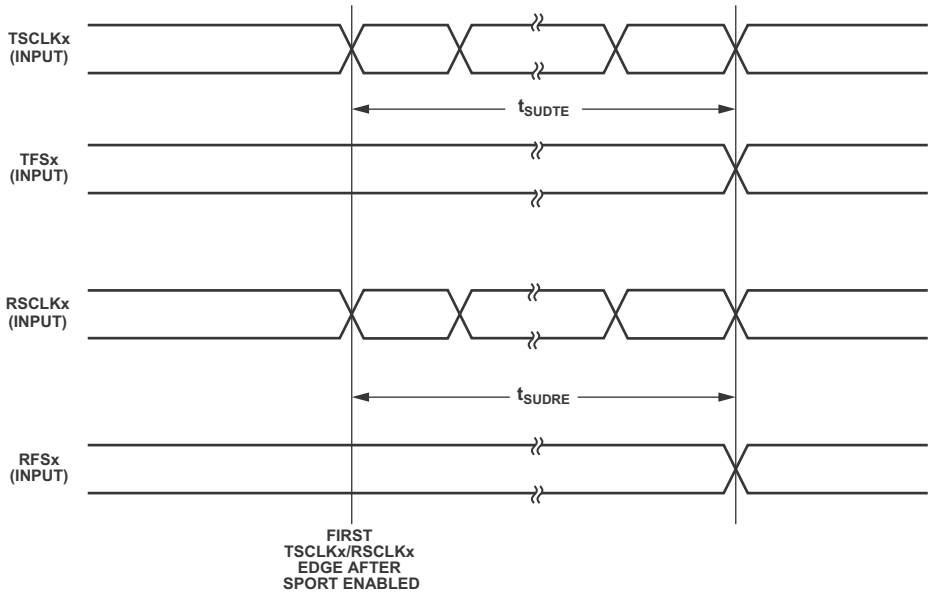


Figure 16. Serial Port Start Up with External Clock and Frame Sync

Table 27. Serial Ports—Gated Clock Mode

		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5 V/3.3 V Nominal		
Parameter		**Min**	**Max**	**Min**	**Max**	**Unit**
Timing Requirements						
t_{SDRI}	Receive Data Setup Before TSCLKx	TBD		11.3		ns
t_{HDRI}	Receive Hold After TSCLKx	TBD		0		ns
Switching Characteristics						
t_{DDTI}	Transmit Data Delay After TSCLKx		TBD		3	ns
t_{HDTI}	Transmit Data Hold After TSCLKx	TBD		–1.8		ns
$t_{DFTSCLKCNV}$	First TSCLKx edge delay after TFSx/TMR1 Low	TBD		$0.5 \times t_{TSCLK} - 3$		ns
$t_{DCNVLTSCLK}$	TFSx/TMR1 High Delay After Last TSCLKx Edge	TBD		$t_{TSCLK} - 3$		ns

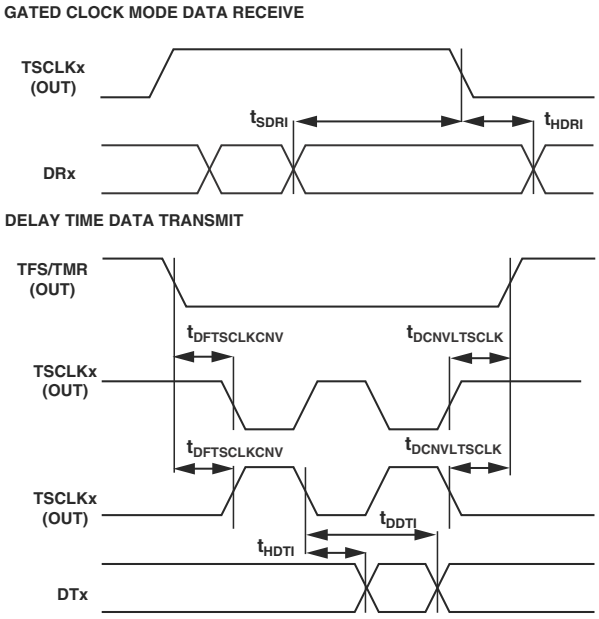


Figure 17. Serial Port Gated Clock Mode

Serial Peripheral Interface (SPI) Port—Master Timing

Table 28 and Figure 18 describe SPI port master operations.

Table 28. Serial Peripheral Interface (SPI) Port—Master Timing

Parameter		V_{DDEXT} 1.8 V Nominal Min	V_{DDEXT} 1.8 V Nominal Max	V_{DDEXT} 2.5/3.3 V Nominal Min	V_{DDEXT} 2.5/3.3 V Nominal Max	Unit
Timing Requirements						
t_{SSPIDM}	Data Input Valid to SCK Edge (Data Input Setup)	TBD		12.0		ns
t_{HSPIDM}	SCK Sampling Edge to Data Input Invalid	TBD		–1.5		ns
Switching Characteristics						
t_{SDSCIM}	$\overline{SPI_SELx}$ low to First SCK Edge	TBD		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICHM}	Serial Clock High Period	TBD		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLM}	Serial Clock Low Period	TBD		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	TBD		$4 \times t_{SCLK} - 1.5$		ns
t_{HDSM}	Last SCK Edge to $\overline{SPI_SELx}$ High	TBD		$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDM}	Sequential Transfer Delay	TBD		$2 \times t_{SCLK} - 1.5$		ns
$t_{DDSPIDM}$	SCK Edge to Data Out Valid (Data Out Delay)		TBD	0	6	ns
$t_{HDSPIDM}$	SCK Edge to Data Out Invalid (Data Out Hold)	TBD		–1		ns

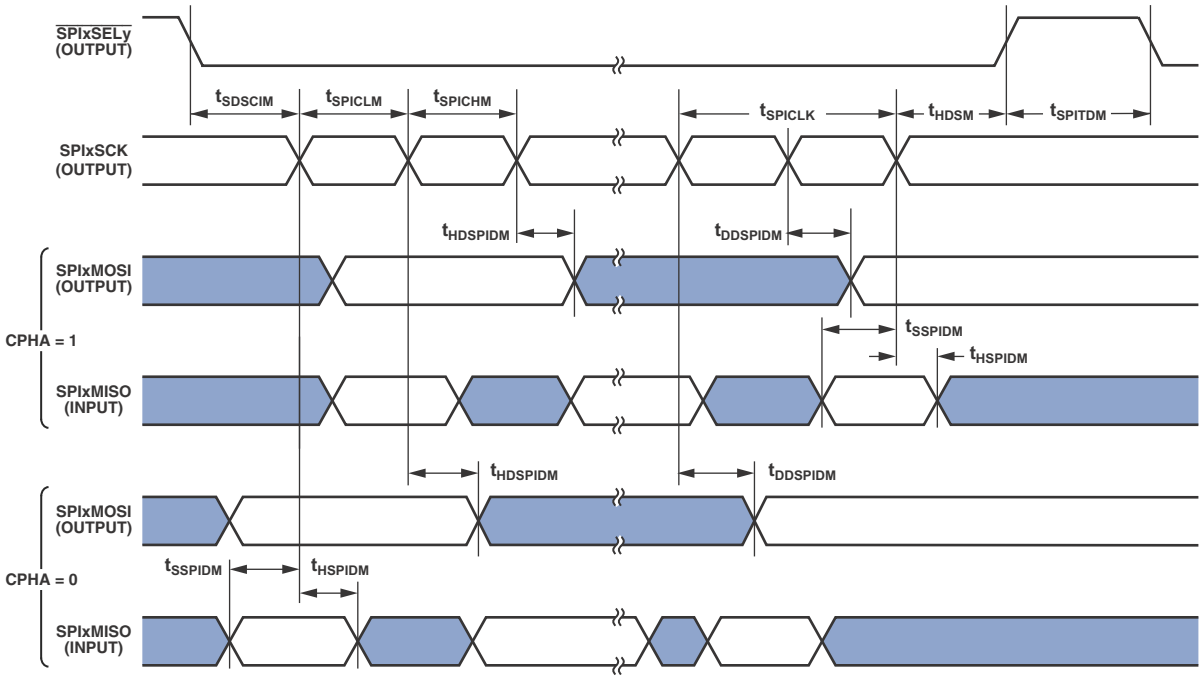


Figure 18. Serial Peripheral Interface (SPI) Port—Master Timing

Serial Peripheral Interface (SPI) Port—Slave Timing

Table 29 and Figure 19 describe SPI port slave operations.

Table 29. Serial Peripheral Interface (SPI) Port—Slave Timing

Parameter		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5/3.3 V Nominal		Unit
		Min	Max	Min	Max	
Timing Requirements						
t_{SPICHS}	Serial Clock High Period	TBD		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLS}	Serial Clock Low Period	TBD		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	TBD		$4 \times t_{SCLK}$		ns
t_{HDS}	Last SCK Edge to $\overline{SPI_SS}$ Not Asserted	TBD		$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDS}	Sequential Transfer Delay	TBD		$2 \times t_{SCLK} - 1.5$		ns
t_{SDSCI}	$\overline{SPI_SS}$ Assertion to First SCK Edge	TBD		$2 \times t_{SCLK} - 1.5$		ns
t_{SSPID}	Data Input Valid to SCK Edge (Data Input Setup)	TBD		1.6		ns
t_{HSPID}	SCK Sampling Edge to Data Input Invalid	TBD		1.6		ns
Switching Characteristics						
t_{DSOE}	$\overline{SPI_SS}$ Assertion to Data Out Active	TBD	TBD	0	12	ns
t_{DSDHI}	$\overline{SPI_SS}$ Deassertion to Data High Impedance	TBD	TBD	0	11	ns
t_{DDSPID}	SCK Edge to Data Out Valid (Data Out Delay)		TBD		10	ns
t_{HDSPID}	SCK Edge to Data Out Invalid (Data Out Hold)	TBD		0		ns

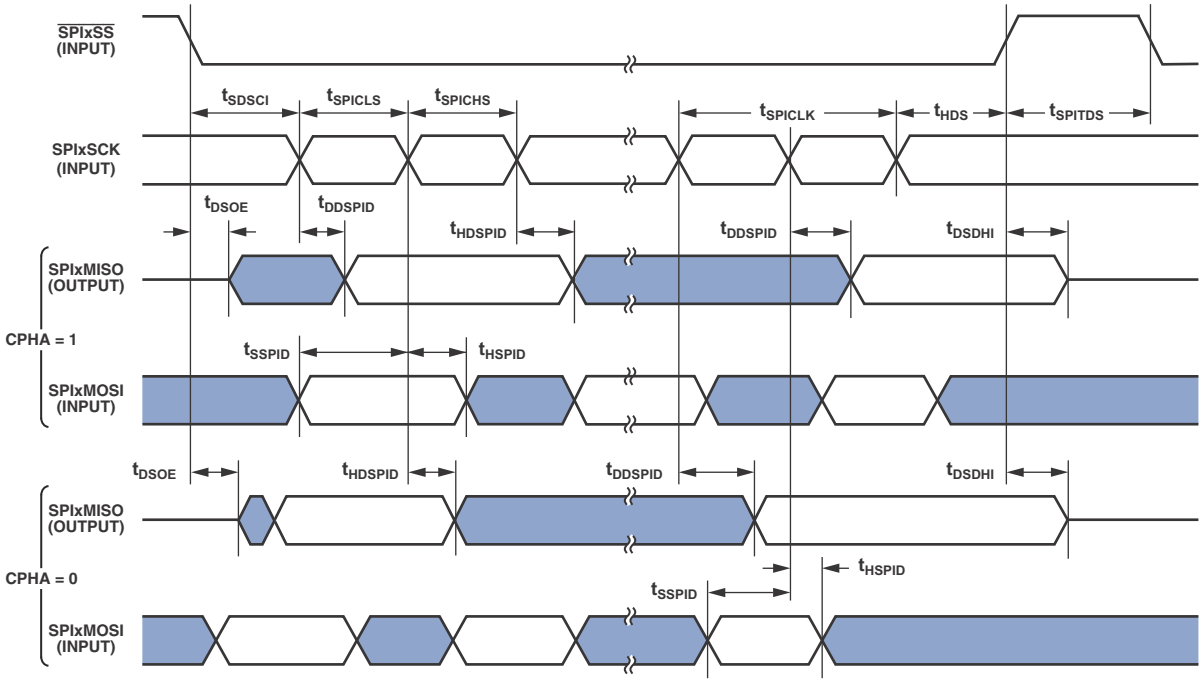


Figure 19. Serial Peripheral Interface (SPI) Port—Slave Timing

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

The UART ports receive and transmit operations are described in the *ADSP-BF59x Hardware Reference Manual*.

General-Purpose Port Timing

Table 30 and Figure 20 describe general-purpose port operations.

Table 30. General-Purpose Port Timing

Parameter		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5/3.3 V Nominal		Unit
		Min	Max	Min	Max	
Timing Requirement						
t_{WFI}	General-Purpose Port Pin Input Pulse Width	TBD		t_{SCLK} + 1		ns
Switching Characteristics						
t_{GPOD}	General-Purpose Port Pin Output Delay from CLKOUT Low	TBD	TBD	0	10	ns

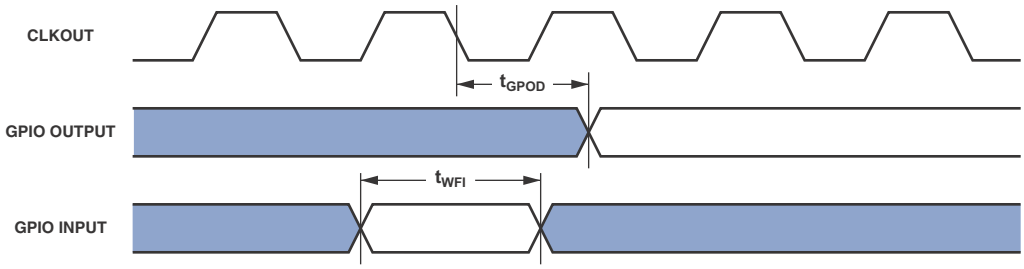


Figure 20. General-Purpose Port Timing

Timer Cycle Timing

Table 31 and Figure 21 describe timer expired operations. The input signal is asynchronous in "width capture mode" and "external clock mode" and has an absolute maximum input frequency of (f_{SCLK}/2) MHz.

Table 31. Timer Cycle Timing

Parameter		V_{DDEXT} 1.8 V Nominal Min	V_{DDEXT} 1.8 V Nominal Max	V_{DDEXT} 2.5/3.3 V Nominal Min	V_{DDEXT} 2.5/3.3 V Nominal Max	Unit
Timing Requirements						
t_{WL}	Timer Pulse Width Input Low (Measured In SCLK Cycles)[1]	TBD		t_{SCLK} + 1		ns
t_{WH}	Timer Pulse Width Input High (Measured In SCLK Cycles)[1]	TBD		t_{SCLK} + 1		ns
t_{TIS}	Timer Input Setup Time Before CLKOUT Low[2]	TBD		8		ns
t_{TIH}	Timer Input Hold Time After CLKOUT Low[2]	TBD		–2		ns
Switching Characteristics						
t_{HTO}	Timer Pulse Width Output (Measured In SCLK Cycles)	TBD	TBD	t_{SCLK} – 1.5	$(2^{32} – 1) \times t_{SCLK}$	ns
t_{TOD}	Timer Output Update Delay After CLKOUT High		TBD		8.1	ns

[1] The minimum pulse widths apply for TMRx signals in width capture and external clock modes. They also apply to the PG0 or PPI_CLK signals in PWM output mode.
[2] Either a valid setup and hold time or a valid pulse width is sufficient. There is no need to resynchronize programmable flag inputs.

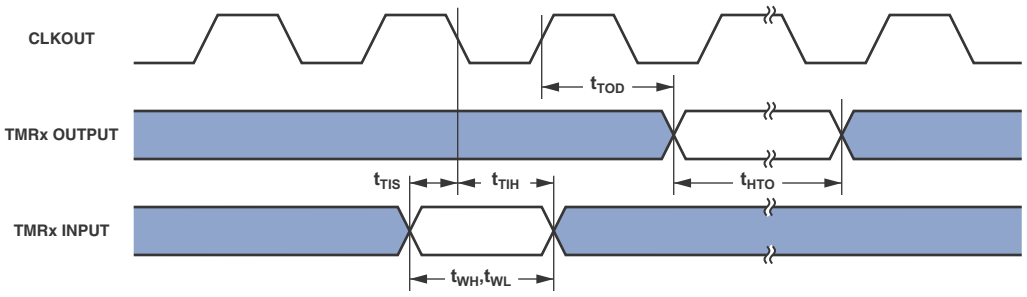


Figure 21. Timer Cycle Timing

Timer Clock Timing

Table 32 and Figure 22 describe timer clock timing.

Table 32. Timer Clock Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5/3.3 V Min	V_{DDEXT} = 2.5/3.3 V Max	Unit
Switching Characteristic						
t_{TODP}	Timer Output Update Delay After PPI_CLK High		TBD		12.64	ns

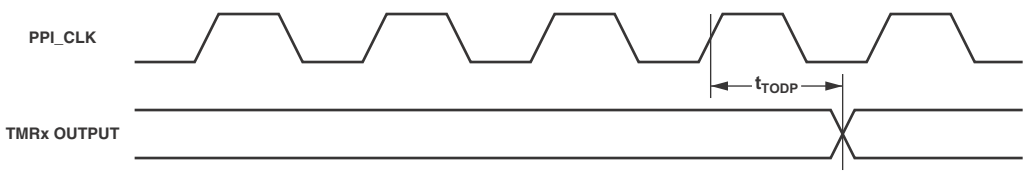


Figure 22. Timer Clock Timing

JTAG Test And Emulation Port Timing

Table 33 and Figure 23 describe JTAG port operations.

Table 33. JTAG Port Timing

Parameter		V_{DDEXT} 1.8 V Nominal Min	V_{DDEXT} 1.8 V Nominal Max	V_{DDEXT} 2.5/3.3 V Nominal Min	V_{DDEXT} 2.5/3.3 V Nominal Max	Unit
Timing Requirements						
t_{TCK}	TCK Period	TBD		20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	TBD		4		ns
t_{HTAP}	TDI, TMS Hold After TCK High	TBD		4		ns
t_{SSYS}	System Inputs Setup Before TCK High[1]	TBD		5		ns
t_{HSYS}	System Inputs Hold After TCK High[1]	TBD		5		ns
t_{TRSTW}	$\overline{TRST}$ Pulse Width[2] (measured in TCK cycles)	TBD		4		TCK
Switching Characteristics						
t_{DTDO}	TDO Delay from TCK Low		TBD		10	ns
t_{DSYS}	System Outputs Delay After TCK Low[3]		TBD		13	ns

[1] System Inputs = SCL, SDA, PF15–0, PG15–0, PH2–0, TCK, $\overline{NMI}$, BMODE3–0, $\overline{PG}$.
[2] 50 MHz Maximum
[3] System Outputs = CLKOUT, SCL, SDA, PF15–0, PG15–0, PH2–0, TDO, $\overline{EMU}$, EXT_WAKE.

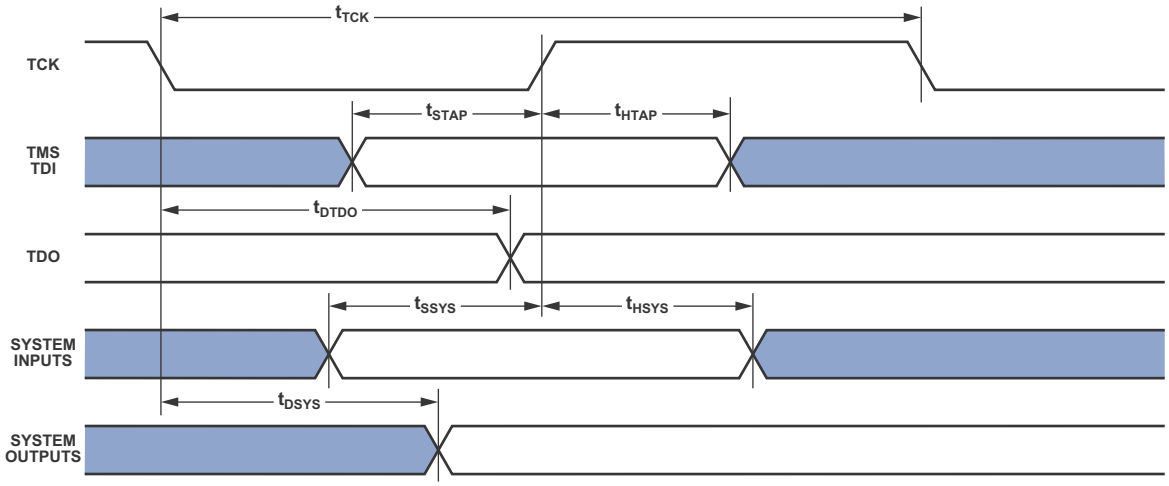


Figure 23. JTAG Port Timing

OUTPUT DRIVE CURRENTS

Figure 30 through Figure 29 show typical current-voltage characteristics for the output drivers of the ADSP-BF592 processor.

The curves represent the current drive capability of the output drivers. See Table 9 on Page 16 for information about which driver type corresponds to a particular pin.

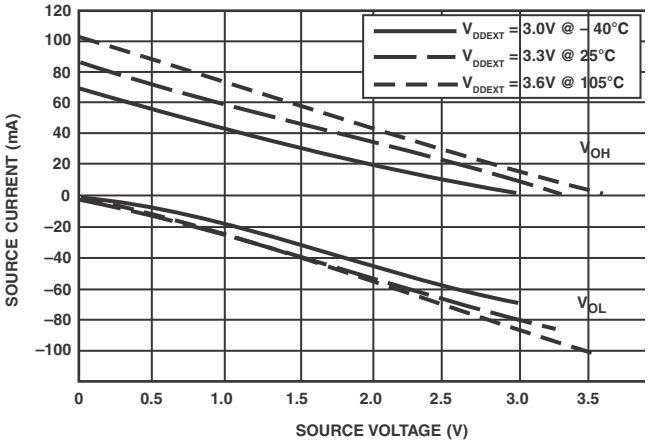


Figure 24. Driver Type A Current (3.3V V_{DDEXT})

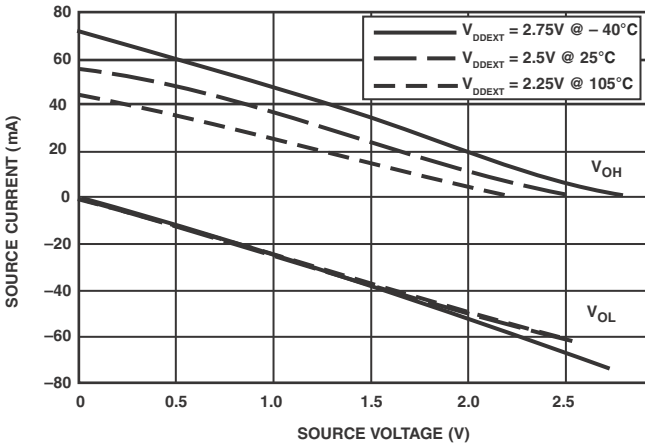


Figure 25. Drive Type A Current (2.5V V_{DDEXT})

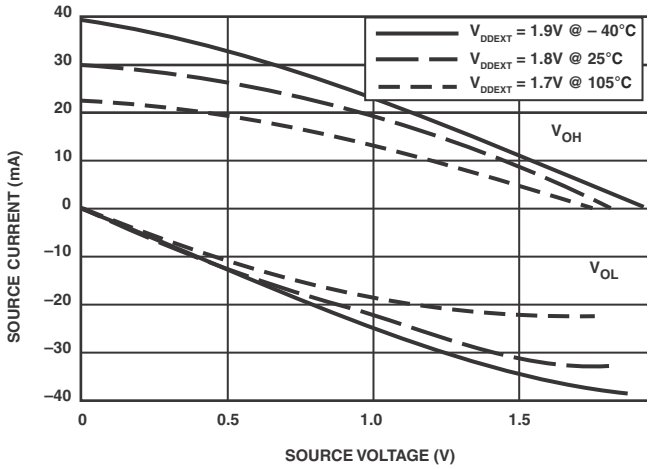


Figure 26. Driver Type A Current (1.8V V_{DDEXT})

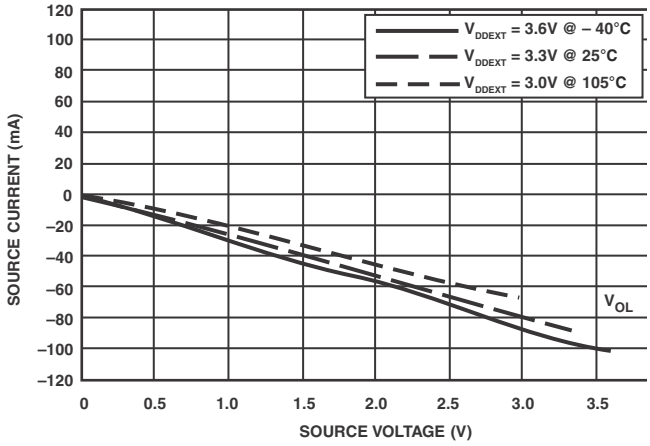


Figure 27. Driver Type B Current (3.3V V_{DDEXT})

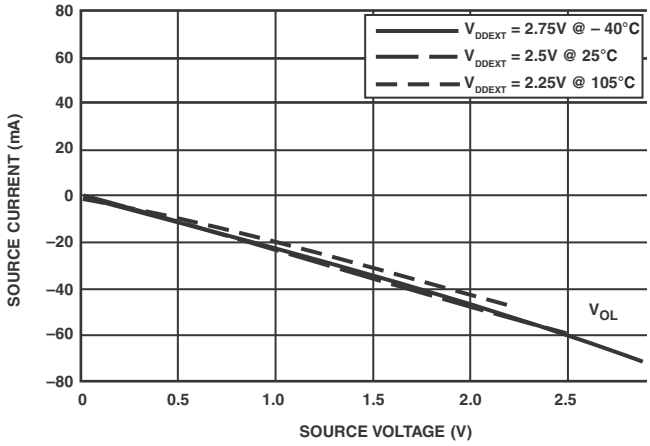


Figure 28. Driver Type B Current (2.5V V_{DDEXT})

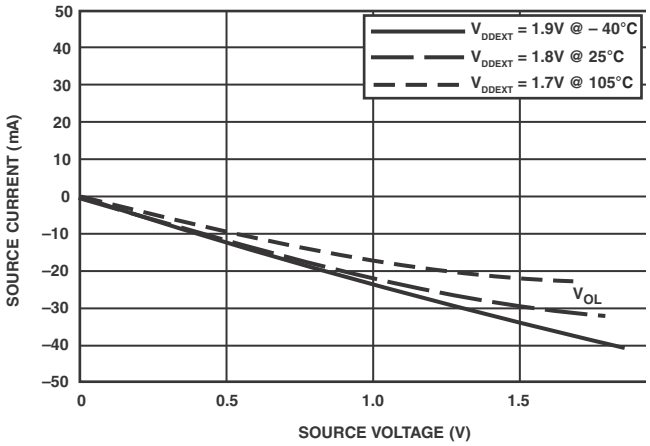


Figure 29. Driver Type B Current (1.8V V_{DDEXT})

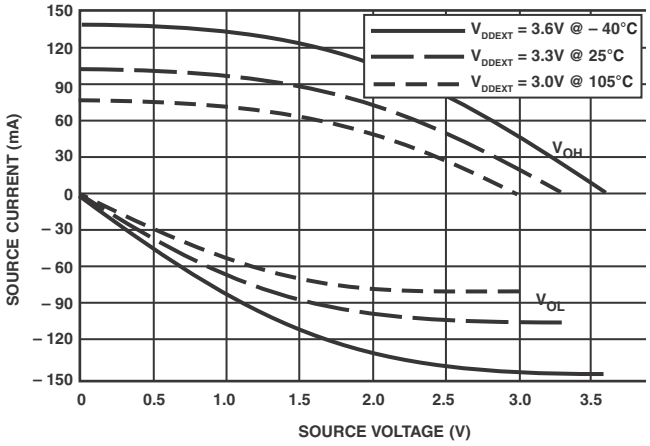


Figure 30. Driver Type C Current (3.3V V_{DDEXT})

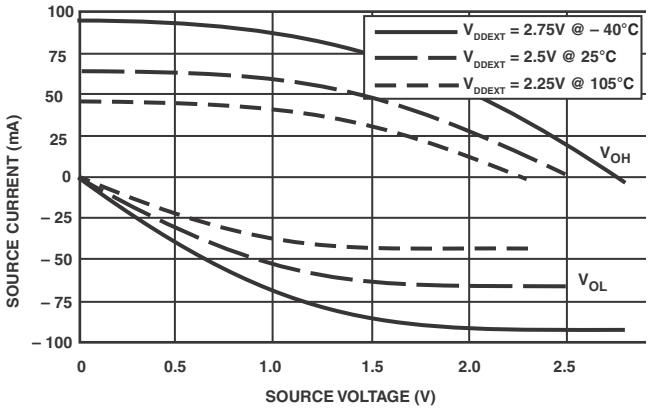


Figure 31. Driver Type C Current (2.5V V_{DDEXT})

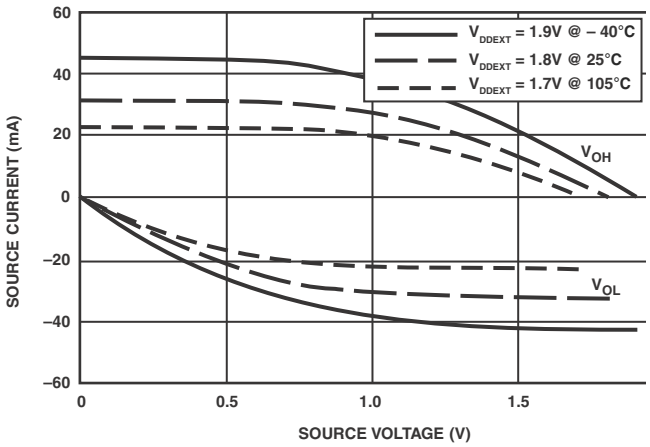


Figure 32. Driver Type C Current (1.8V V_{DDEXT})

TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 33 shows the measurement point for AC measurements (except output enable/disable). The measurement point V_{MEAS} is $V_{DDEXT}/2$ for V_{DDEXT} (nominal) = 1.8 V/2.5 V/3.3 V.

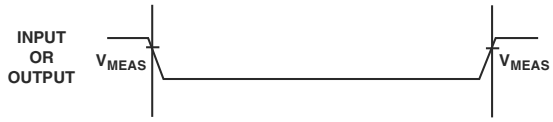


Figure 33. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time Measurement

Output pins are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving.

The output enable time t_{ENA} is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving as shown on the right side of Figure 34.

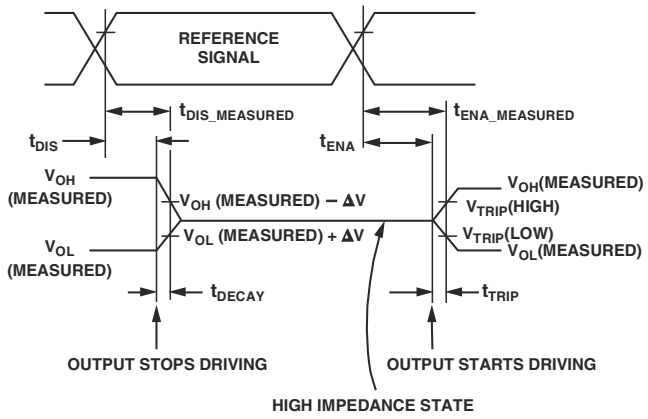


Figure 34. Output Enable/Disable

The time $t_{ENA_MEASURED}$ is the interval, from when the reference signal switches, to when the output voltage reaches V_{TRIP}(high) or V_{TRIP}(low). For V_{DDEXT} (nominal) = 1.8V, V_{TRIP} (high) is 1.05V, and V_{TRIP} (low) is 0.75V. For V_{DDEXT} (nominal) = 2.5V, V_{TRIP} (high) is 1.5V and V_{TRIP} (low) is 1.0V. For V_{DDEXT} (nominal) = 3.3V, V_{TRIP} (high) is 1.9V, and V_{TRIP} (low) is 1.4V. Time t_{TRIP} is the interval from when the output starts driving to when the output reaches the V_{TRIP}(high) or V_{TRIP}(low) trip voltage.

Time t_{ENA} is calculated as shown in the equation:

$$t_{ENA} = t_{ENA_MEASURED} - t_{TRIP}$$

If multiple pins are enabled, the measurement value is that of the first lead to start driving.

Output Disable Time Measurement

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The output disable time t_{DIS} is the difference between $t_{DIS_MEASURED}$ and t_{DECAY} as shown on the left side of Figure 34.

$$t_{DIS} = t_{DIS_MEASURED} - t_{DECAY}$$

The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load C_L and the load current I_L. This decay time can be approximated by the equation:

$$t_{DECAY} = (C_L \Delta V)/I_L$$

The time t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.25 V for V_{DDEXT} (nominal) = 2.5 V/3.3 V and 0.15 V for V_{DDEXT} (nominal) = 1.8V.

The time $t_{DIS_MEASURED}$ is the interval from when the reference signal switches, to when the output voltage decays ΔV from the measured output high or output low voltage.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the processor's output voltage and the input threshold for the device requiring the hold time. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the various output disable times as specified in the Timing Specifications on Page 23.

Capacitive Loading

Output delays and holds are based on standard capacitive loads of an average of 6 pF on all pins (see Figure 35). V_{LOAD} is equal to (V_{DDEXT}) /2.

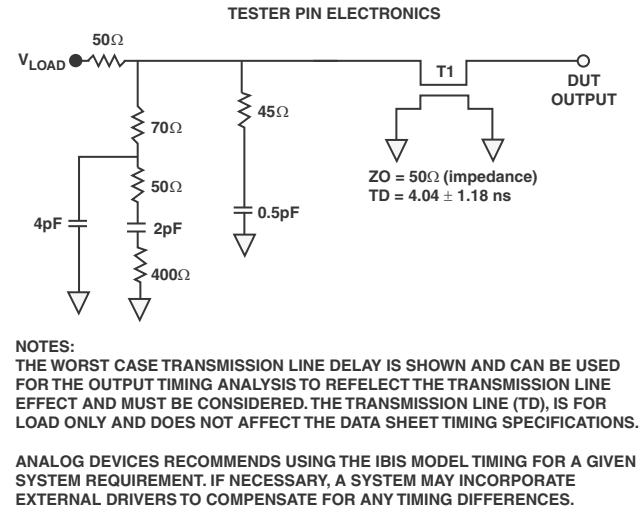


Figure 35. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

The graphs of Figure 39 through Figure 38 show how output rise time varies with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.

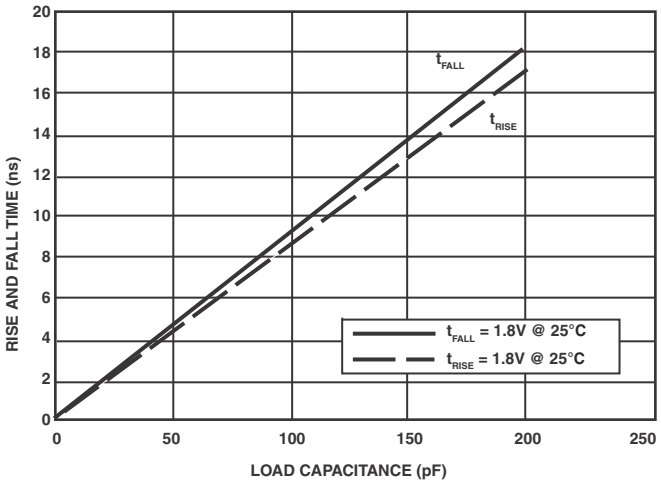


Figure 36. Driver Type A Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (1.8V V_{DDEXT})

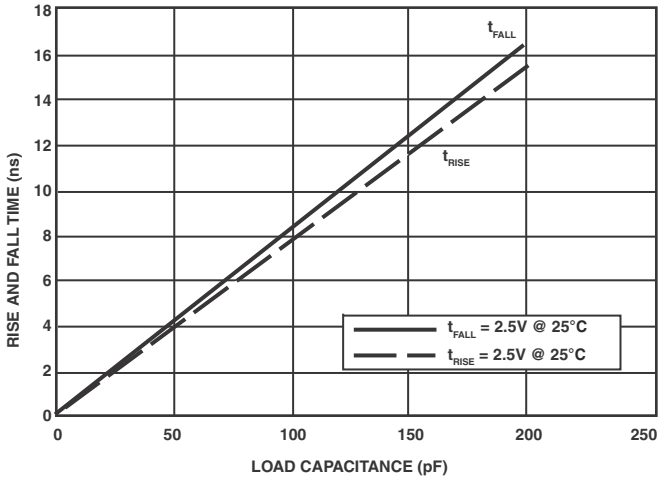


Figure 37. Driver Type A Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5V V_{DDEXT})

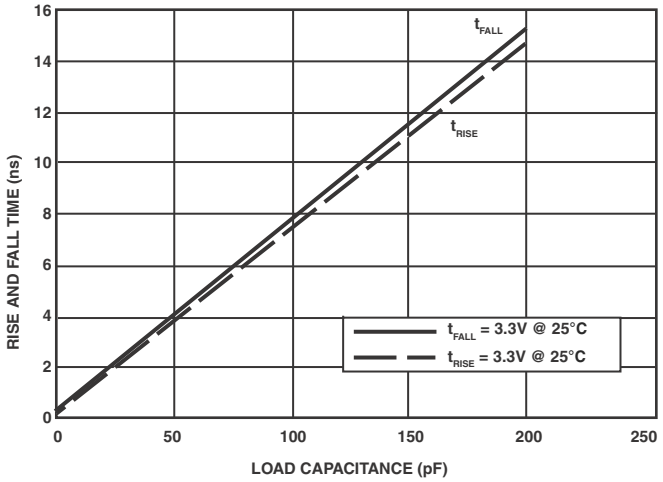


Figure 38. Driver Type A Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3V V_{DDEXT})

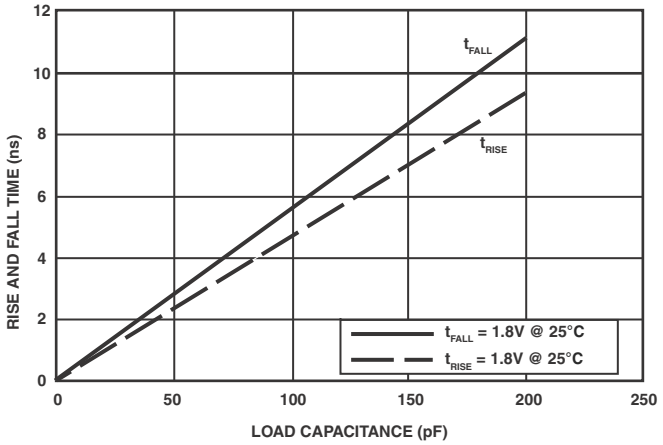


Figure 39. Driver Type C Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (1.8V V_{DDEXT})

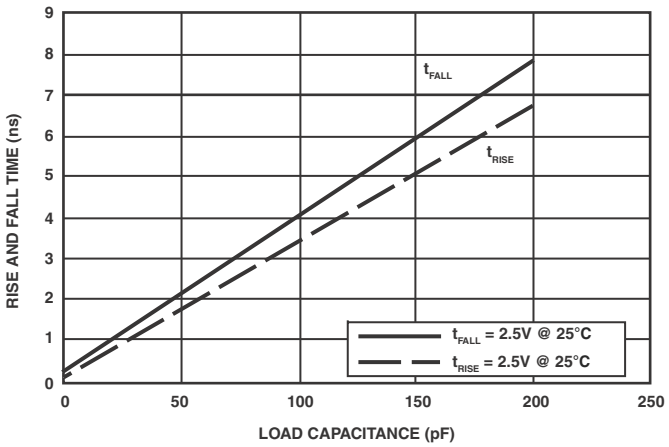


Figure 40. Driver Type C Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5V V_{DDEXT})

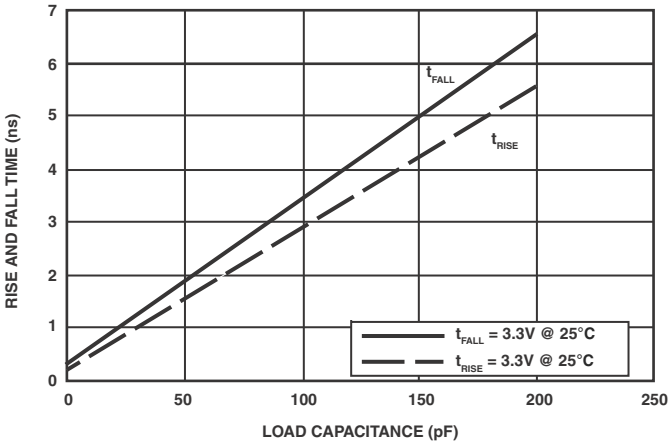


Figure 41. Driver Type C Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3V V_{DDEXT})

ENVIRONMENTAL CONDITIONS

To determine the junction temperature on the application printed circuit board use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = Junction temperature (°C)

T_{CASE} = Case temperature (°C) measured by customer at top center of package.

Ψ_{JT} = From Table 34

P_D = Power dissipation (see Total Power Dissipation on Page 21 for the method to calculate P_D)

Table 34. Thermal Characteristics

Parameter	Condition	Typical	Unit
θ_{JA}	0 linear m/s air flow	23.5	°C/W
θ_{JMA}	1 linear m/s air flow	20.9	°C/W
θ_{JMA}	2 linear m/s air flow	20.2	°C/W
θ_{JB}		11.2	°C/W
θ_{JC}		9.5	°C/W
Ψ_{JT}	0 linear m/s air flow	0.21	°C/W
Ψ_{JT}	1 linear m/s air flow	0.36	°C/W
Ψ_{JT}	2 linear m/s air flow	0.43	°C/W

Values of θ_{JA} are provided for package comparison and printed circuit board design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = Ambient temperature (°C)

Values of θ_{JC} are provided for package comparison and printed circuit board design considerations when an external heat sink is required.

Values of θ_{JB} are provided for package comparison and printed circuit board design considerations.

In Table 34, airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6, and the junction-to-board measurement complies with JESD51-8. The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

64-LEAD LFCSP PIN ASSIGNMENT

Table 35 lists the LFCSP pins by signal mnemonic. Table 36 lists the LFCSP by pin number.

Table 35. 64-Lead LFCSP Pin Assignment (Alphabetically by Signal)

Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.
BMODE0	29	PF7	7	PG6	38	TDO	23
BMODE1	28	PF8	10	PG7	39	TMS	21
BMODE2	27	PF9	11	PG8	42	$\overline{\text{TRST}}$	20
CLKBUF/SCLK	57	PF10	12	PG9	43	V_{DDEXT}	3
CLKIN	61	PF11	13	PG10	44	V_{DDEXT}	14
$\overline{\text{EMU}}$	19	PF12	15	PG11	45	V_{DDEXT}	25
EXT_WAKE	51	PF13	16	PG12	47	V_{DDEXT}	35
GND	30	PF14	17	PG13	48	V_{DDEXT}	46
$\overline{\text{NMI}}$	54	PF15	18	PG14	49	V_{DDEXT}	58
PF0	63	$\overline{\text{PG}}$	52	PG15	50	V_{DDINT}	8
PF1	64	PG0	31	PPI_CLK	56	V_{DDINT}	9
PF2	1	PG1	32	$\overline{\text{RESET}}$	53	V_{DDINT}	26
PF3	2	PG2	33	SCL	60	V_{DDINT}	40
PF4	4	PG3	34	SDA	59	V_{DDINT}	41
PF5	5	PG4	36	TCK	24	V_{DDINT}	55
PF6	6	PG5	37	TDI	22	XTAL	62
						GND*	65

* Pin no. 65 is the GND supply (see Figure 42 and Figure 43) for the processor (6.2mm × 6.2mm); this pad **must** connect to GND.

Table 36. 64-Lead LFCSP Pin Assignment (Numerically by Pin Number)

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
1	PF2	17	PF14	33	PG2	49	PG14
2	PF3	18	PF15	34	PG3	50	PG15
3	V_{DDEXT}	19	$\overline{\text{EMU}}$	35	V_{DDEXT}	51	EXT_WAKE
4	PF4	20	$\overline{\text{TRST}}$	36	PG4	52	$\overline{\text{PG}}$
5	PF5	21	TMS	37	PG5	53	$\overline{\text{RESET}}$
6	PF6	22	TDI	38	PG6	54	$\overline{\text{NMI}}$
7	PF7	23	TDO	39	PG7	55	V_{DDINT}
8	V_{DDINT}	24	TCK	40	V_{DDINT}	56	PPI_CLK
9	V_{DDINT}	25	V_{DDEXT}	41	V_{DDINT}	57	CLKBUF/SCLK
10	PF8	26	V_{DDINT}	42	PG8	58	V_{DDEXT}
11	PF9	27	BMODE2	43	PG9	59	SDA
12	PF10	28	BMODE1	44	PG10	60	SCL
13	PF11	29	BMODE0	45	PG11	61	CLKIN
14	V_{DDEXT}	30	GND	46	V_{DDEXT}	62	XTAL
15	PF12	31	PG0	47	PG12	63	PF0
16	PF13	32	PG1	48	PG13	64	PF1
						65	GND*

* Pin no. 65 is the GND supply (see Figure 42 and Figure 43) for the processor (6.2mm × 6.2mm); this pad **must** connect to GND.

Figure 42 shows the top view of the LFCSP pin configuration. Figure 43 shows the bottom view of the LFCSP pin configuration.

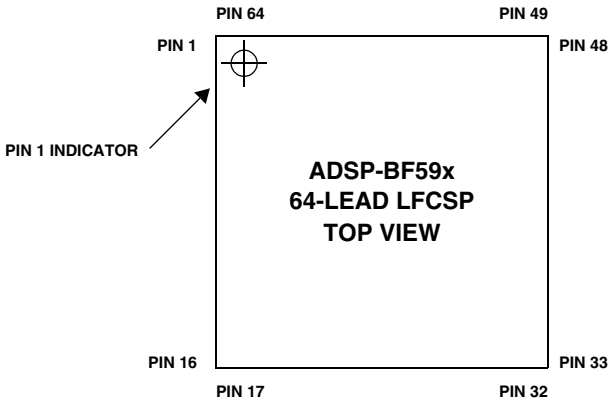


Figure 42. 64-Lead LFCSP Lead Configuration (Top View)

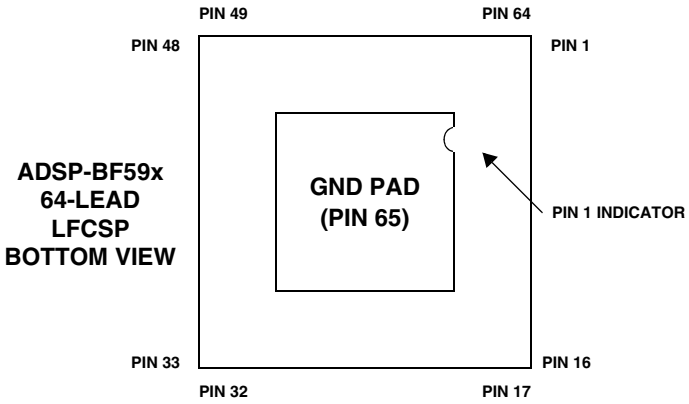


Figure 43. 64-Lead LFCSP Lead Configuration (Bottom View)

OUTLINE DIMENSIONS

Dimensions in Figure 44, are shown in millimeters.

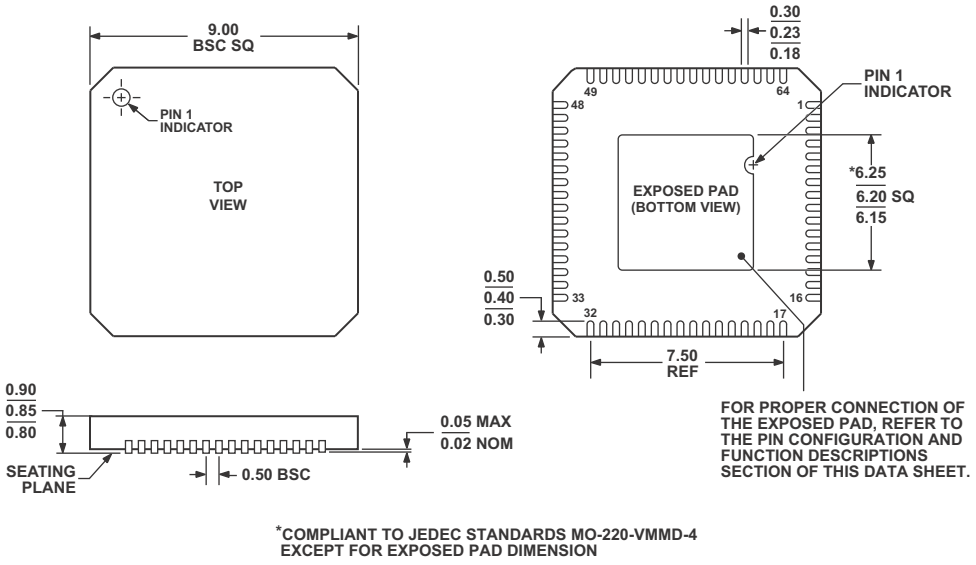


Figure 44. 64-Lead LFCSP (CP-64-1)

SURFACE MOUNT DESIGN

Table 37 is provided as an aide to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface Mount Design and Land Pattern Standard*.

Table 37. Surface Mount Design Supplement

Package	Package Lead Attach Type	Package Solder Mask Opening	Package Lead Pad Size
64-Lead LFCSP	Solder Mask Defined	TBD mm diameter	TBD mm diameter

PLANNED MODELS

The products listed in the table below are planned for production.

Model	Temperature Range[1]	Instruction Rate (Max)	Package Description	Package Option
ADSP-BF592KCPZ[2, 3]	0°C to +70°C	400 MHz	64-Lead LFCSP	CP-64-4
ADSP-BF592BCPZ[2, 3]	–40°C to +85°C	400 MHz	64-Lead LFCSP	CP-64-4

[1] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 18 for junction temperature (T_J) specification which is the only temperature specification.
[2] Z = RoHS Compliant part.
[3] Available with a wide variety of audio algorithm combinations sold as part of a chipset and bundled with necessary software. For a complete list, visit our website at www.analog.com/Blackfin.

ORDERING GUIDE

The products listed in the table below are planned for sampling.

Model	Temperature Range[1]	Instruction Rate (Max)	Package Description	Package Option
ADSP-BF592KCPZ-X[2, 3]	0°C to +70°C	400 MHz	64-Lead LFCSP	CP-64-1

[1] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 18 for junction temperature (T_J) specification which is the only temperature specification.

[2] Z = RoHS Compliant part.

[3] Available with a wide variety of audio algorithm combinations sold as part of a chipset and bundled with necessary software. For a complete list, visit our website at www.analog.com/Blackfin.

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