

BUK7607-55B

N-channel TrenchMOS standard level FET Rev. 2 — 26 July 2011

Product data sheet

1. **Product profile**

1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Q101 compliant

- Suitable for standard level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V and 24 V loads
- Automotive systems

- General purpose power switching
- Motors, lamps and solenoids

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DS}	drain-source voltage	$T_j \ge 25 \text{ °C}; T_j \le 175 \text{ °C}$	-	-	55	V
I _D	drain current	$V_{GS} = 10 \text{ V}; T_{mb} = 25 \text{ °C};$ see <u>Figure 1</u> ; see <u>Figure 3</u>	<u>[1]</u> _	-	75	А
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	-	203	W
Static char	acteristics					
R _{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; see <u>Figure 11</u> ; see <u>Figure 12</u>	-	5.8	7.1	mΩ
Avalanche	ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 75 A; $V_{sup} \le$ 55 V; R_{GS} = 50 Ω ; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped	-	-	351	mJ
Dynamic cl	Dynamic characteristics					
Q _{GD}	gate-drain charge	$V_{GS} = 10 \text{ V; } I_D = 25 \text{ A;}$ $V_{DS} = 44 \text{ V; } T_j = 25 \text{ °C;}$ see <u>Figure 13</u>	-	17	-	nC

^[1] Continuous current is limited by package.



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		_
2	D	drain[1]	mb	D
3	S	source		
mb	D	mounting base; connected to drain		mbb076 S
			SOT404 (D2PAK)	

^[1] It is not possible to make connection to pin 2.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7607-55B	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

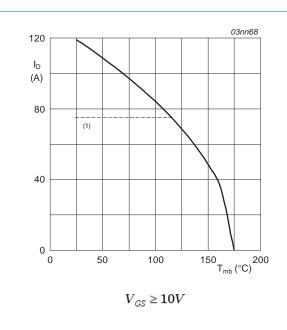
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	55	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	55	V
V_{GS}	gate-source voltage		-20	20	V
I _D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; see <u>Figure 1</u> ; see <u>Figure 3</u>	<u>[1]</u> -	75	Α
		T_{mb} = 100 °C; V_{GS} = 10 V; see <u>Figure 1</u>	<u>[1]</u> -	75	Α
		T_{mb} = 25 °C; V_{GS} = 10 V; see <u>Figure 1</u> ; see <u>Figure 3</u>	[2] -	119	Α
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \le 10 \mu s$; see Figure 3	-	478	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	203	W
T _{stg}	storage temperature		-55	175	°C
Tj	junction temperature		-55	175	°C
Source-drai	n diode				
Is	source current	T _{mb} = 25 °C	[2] _	119	Α
			<u>[1]</u> _	75	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$	-	478	Α
Avalanche i	ruggedness				
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 75 A; $V_{sup} \le$ 55 V; R_{GS} = 50 Ω ; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped	-	351	mJ
-					

^[1] Continuous current is limited by package.

^[2] Current is limited by power dissipation chip rating.



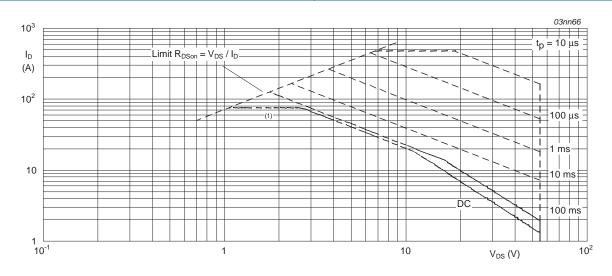
Pder (%)

80

40 $P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$

Fig 1. Normalized continuous drain current as a function of mounting base temperature

Fig 2. Normalized total power dissipation as a function of mounting base temperature



 $T_{mb} = 25$ °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <u>Figure 4</u>	-	-	0.74	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board	-	50	-	K/W

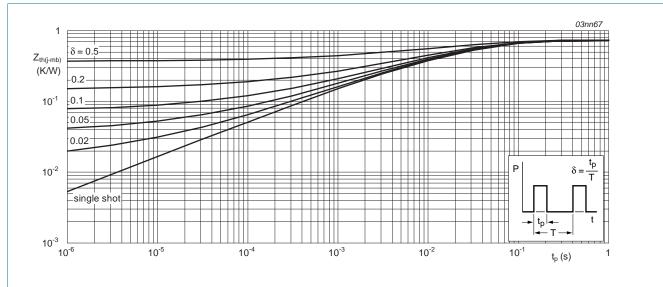


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Table 0.	-					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
	nracteristics					
$V_{(BR)DSS}$	drain-source	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	55	-	-	V
	breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ °C}$	50	-	-	V
V _{GS(th)}	gate-source threshold voltage	$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ °C}$; see <u>Figure 10</u>	2	3	4	V
		I_D = 1 mA; V_{DS} = V_{GS} ; T_j = 175 °C; see <u>Figure 10</u>	1	-	-	V
		$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = -55 \text{ °C}$; see <u>Figure 10</u>	-	-	4.4	V
I _{DSS}	drain leakage current	$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.02	1	μA
		V _{DS} = 55 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
I _{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; see <u>Figure 11</u> ; see <u>Figure 12</u>	-	-	14.2	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; see <u>Figure 11</u> ; see <u>Figure 12</u>	-	5.8	7.1	mΩ
Dynamic	characteristics					
Q _{G(tot)}	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 44 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ °C}; \text{ see } \frac{\text{Figure } 13}{\text{Figure } 13}$	-	53	-	nC
Q _{GS}	gate-source charge		-	12	-	nC
Q_{GD}	gate-drain charge		-	17	-	nC
C _{iss}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$	-	2820	3760	pF
C _{oss}	output capacitance	T _j = 25 °C; see <u>Figure 14</u>	-	554	665	pF
C _{rss}	reverse transfer capacitance		-	200	274	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \Omega; V_{GS} = 10 \text{ V};$	-	24	-	ns
t _r	rise time	$R_{G(ext)} = 10 \Omega$; $T_j = 25 °C$	-	52	-	ns
t _{d(off)}	turn-off delay time		-	77	-	ns
t _f	fall time		-	41	-	ns
L _D	internal drain inductance	from drain lead 6 mm from package to center of die; T _i = 25 °C	-	4.5	-	nΗ
		from upper edge of drain mounting base to centre of die; T _j = 25 °C	-	2.5	-	nΗ
L _S	internal source inductance	from source lead to source bond pad; $T_j = 25 ^{\circ}\text{C}$	-	7.5	-	nΗ
Source-d	rain diode					
V_{SD}	source-drain voltage	$I_S = 40 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C};$ see <u>Figure 15</u>	-	0.85	1.2	V
t _{rr}	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s};$	-	62	-	ns
Q _r	recovered charge	$V_{GS} = -10 \text{ V}; V_{DS} = 30 \text{ V}; T_j = 25 \text{ °C}$	-	60	-	nC

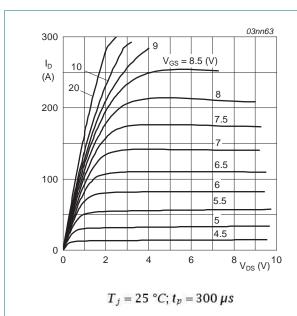


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

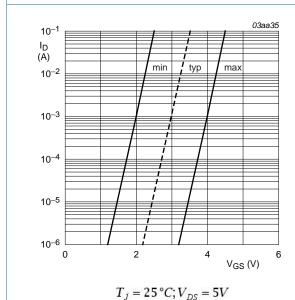
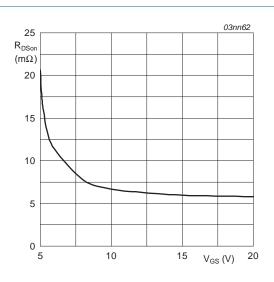
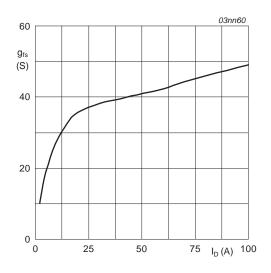


Fig 7. Sub-threshold drain current as a function of gate-source voltage



 $T_j=25^{\circ}C; I_D=25A$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values



 $T_j = 25^{\circ}C; V_{DS} = 25V$

Fig 8. Forward transconductance as a function of drain current; typical values

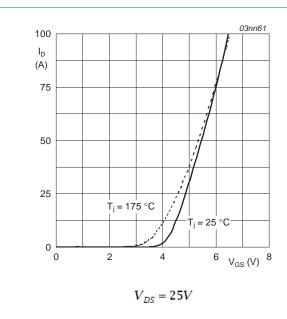


Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

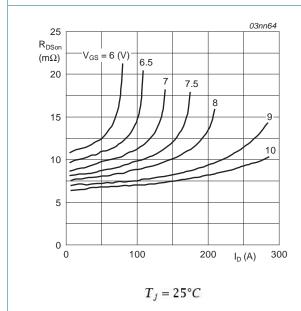
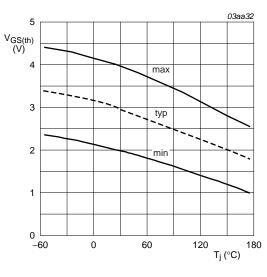


Fig 11. Drain-source on-state resistance as a function of drain current; typical values



 $I_D = 1 mA; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature

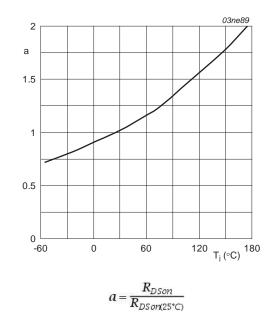
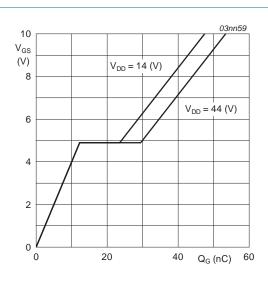
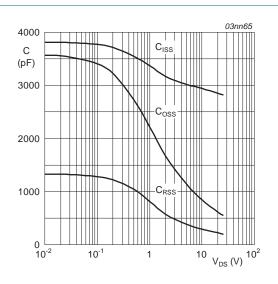


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



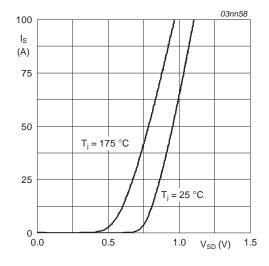
 $T_j=25^{\circ}C; I_D=25A$

Fig 13. Gate-source voltage as a function of gate charge; typical values



$$V_{GS} = 0V; f = 1MHz$$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



 $V_{GS} = 0V$

Fig 15. Source current as a function of source-drain voltage; typical values

7. Package outline

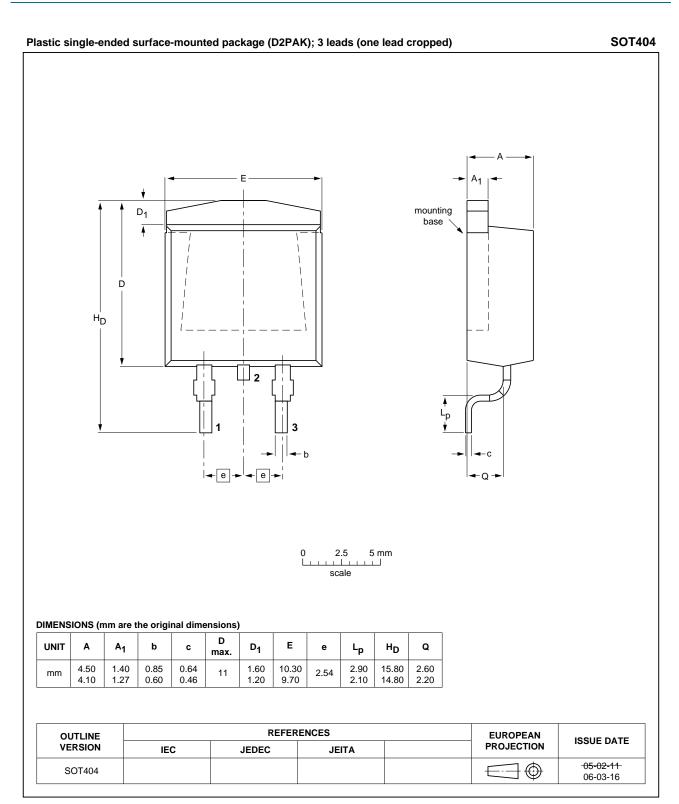


Fig 16. Package outline SOT404 (D2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
BUK7607-55B v.2	20110726	Product data sheet	-	BUK75_7607_55B_1	
Modifications:	 Type number BL 	JK7607-55B separated fro	m data sheet BUK75_7	607_55B_1.	
	 The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. 				
 Legal texts have been adapted to the new company name where appropriate. 					
BUK75_7607_55B_1 (9397 750 11235)	20030515	Product data	-	-	

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N-channel TrenchMOS standard level FET

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105318, г. Москва, ул. Щербаковская д. 3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

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