KSZ8893MQL/MBL

Integrated 3-Port 10/100 Managed Switch with PHYs

Rev. 1.6

General Description

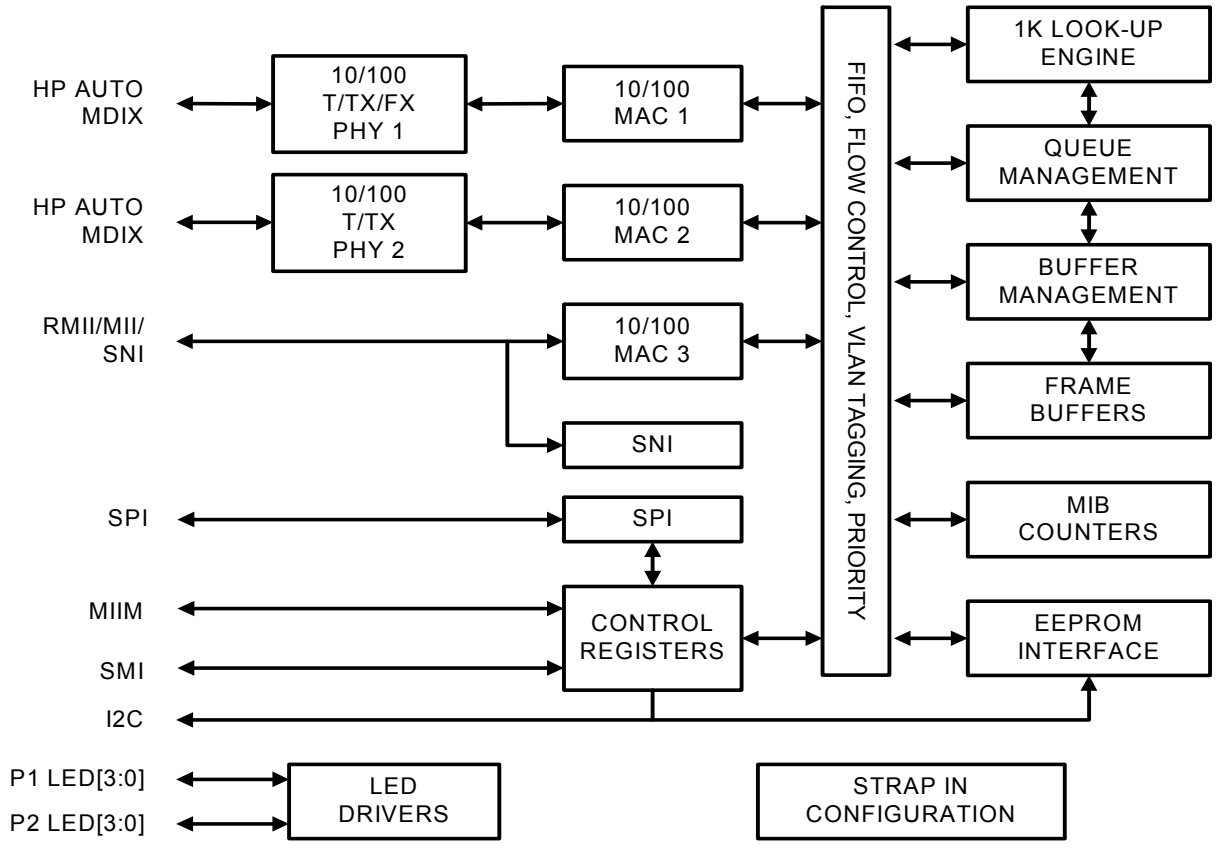
The KSZ8893MQL/MBL, a highly integrated layer 2 managed switch, is designed for low port count, cost-sensitive 10/100 Mbps switch systems. It offers an extensive feature set that includes rate limiting, tag/port-based VLAN, QoS priority, management, management information base (MIB) counters, RMII/MII/SNI, and CPU control/data interfaces to effectively address both current and emerging Fast Ethernet applications.

The KSZ8893MQL/MBL contains two 10/100 transceivers with patented mixed-signal low-power technology, three media access control (MAC) units, a high-speed non-blocking switch fabric, a dedicated address lookup engine, and an on-chip frame buffer memory.

Both PHY units support 10BASE-T and 100BASE-TX. In addition, one PHY unit supports 100BASE-FX.

The KSZ8893MQL/MBL comes in a lead-free package, and is also available in industrial temperature-grade KS8893MQLI/MBLI and Automotive-grade KSZ8893 MQL AM. (See Ordering Information).

Functional Diagram



Features

- **Proven Integrated 3-Port 10/100 Ethernet Switch**
  – 3rd generation switch with three MACs and two PHYs fully compliant with IEEE 802.3u standard
  – Non-blocking switch fabric assures fast packet delivery by utilizing an 1K MAC address lookup table and a store-and-forward architecture
  – Full duplex IEEE 802.3x flow control (PAUSE) with force mode option
  – Half-duplex back pressure flow control
  – HP Auto MDI-X for reliable detection of and correction for straight-through and crossover cables with disable and enable option
  – Micrel LinkMD™ TDR-based cable diagnostics permit identification of faulty copper cabling
  – 100BASE-FX support on port 1
  – MII interface supports both MAC mode and PHY mode
  – RMII interface support with external 50MHz system clock
  – 7-wire serial network interface (SNI) support for legacy MAC
  – Comprehensive LED Indicator support for link, activity, full/half duplex and 10/100 speed
- **Comprehensive Configuration Register Access**
  – Serial management interface (SMI) to all internal registers
  – MII management (MIIM) interface to PHY registers
  – SPI and I^2C Interface to all internal registers
  – I/0 pins strapping and EEPROM to program selective registers in unmanaged switch mode
  – Control registers configurable on the fly (port-priority, 802.1p/d/q, AN…)
- **QoS/CoS Packet Prioritization Support**
  – Per port, 802.1p and DiffServ-based
  – Re-mapping of 802.1p priority field per port basis
  – Four priority levels
- **Advanced Switch Features**
  – IEEE 802.1q VLAN support for up to 16 groups (full-range of VLAN IDs)
  – VLAN ID tag/untag options, per port basis
  – IEEE 802.1p/q tag insertion or removal on a per port basis (egress)
  – Programmable rate limiting at the ingress and egress on a per port basis
  – Broadcast storm protection with % control (global and per port basis)
  – IEEE 802.1d spanning tree protocol support
  – Special tagging mode to inform the processor which ingress port receives the packet
  – IGMP snooping (Ipv4) and MLD snooping (Ipv6) support for multicast packet filtering
  – MAC filtering function to forward unknown unicast packets to specified port
  – Double-tagging support
  – Support IEEE 802.1w, 802.1t spanning tree
- **Low Latency Support**
  – Repeater mode
- **Switch Monitoring Features**
  – Port mirroring/monitoring/sniffing: ingress and/or egress traffic to any port or MII
  – MIB counters for fully compliant statistics gathering, 34 MIB counters per port
  – Loopback modes for remote diagnostic of failure
- **Low Power Dissipation**:
  – Full-chip hardware power-down (register configuration not saved)
  – Per port based software power-save on PHY (idle link detection, register configuration preserved)
  – Voltages: Single power supply: 3.3V
- Industrial Temperature Range: –40°C to +85°C
- Available in 128-Pin PQFP and 100-ball LFBGA, Lead- free package

Applications

- **Typical**
  – Media Converter
  – FTTx customer premises equipment
  – VoIP Phone
  – SOHO Residential Gateway
  – Broadband Gateway / Firewall / VPN
  – Integrated DSL/Cable Modem
  – Wireless LAN access point + gateway
  – Set-top/Game Box
  – Standalone 10/100 switch
- **Upgradeable**(1)
  – Unmanaged switch with future option to migrate to a managed solution
  – Single PHY alternative with future expansion option for two ports
- **Industrial**
  – Applications requiring port redundancy and port monitoring
  – Sensor devices in redundant ring topology

Note:
1. Reduces cost and time of PCB re-spin.

Ordering Information

Part Number	Operation Temp. Range	Package	Grade
KSZ8893MQL	0°C to 70°C	128-Pin PQFP, Lead-free	Commercial
KSZ8893MQLI	–40°C to +85°C	128-Pin PQFP, Lead-free	Industrial
KSZ8893MQL AM	-40°C to +85°C	128-Pin PQFP, Lead-free	Automotive grade
KSZ8893MBL	0°C to 70°C	100-Ball LFBGA	Commercial
KSZ8893MBLI	–40°C to +85°C	100-Ball LFBGA	Industrial

Revision History

Revision	Date	Summary of Changes
1.0	6/30/05	Initial release
1.1	11/17/05	Updated ordering information Updated package information Updated default register values Updated current consumption description Changed device reference in datasheet from KS8893M to KSZ8893MQL Added repeater mode description
1.2	02/08/07	Modify Table 5. RMII Signal Connections Add TLA-6T718 to Table 16. Qualified Single Port Magnetics
1.3	06/19/07	Add Thermal Resistance (θ_{JC}) to Operating Rating
1.4	10/16/07	Recommend connecting a 100ohm resistor between VDDC and 3.3V power rail.
1.5	11/05/07 11/26/07 12/10/07 07/30/08 09/16/08 02/12/09	Add the KSZ8893MBL BGA device information. Modify the Hold time, Output valid in table 25, 26 and Figure 25,26 of MII interface timing. Add the I2C timing diagram and parameters in Figure 24 to 27 and Table 28. Add MBLI to order information Modify the paragraph “Unicast MAC Address Filtering” Modify the Table 5 (RMII Signal Connections)

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Pin Description and I/O Assignment of KSZ8893MQL

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type (1)</th><th>Description</th></tr>
<tr><td>1</td><td>P1LED2</td><td>Ipu/O</td><td rowspan="3">Port 1 LED Indicators
(apply to all modes of operation, except Repeater Mode)

<table>
<tr><th></th><th colspan="2">[LEDSEL1, LEDSEL0]</th></tr>
<tr><th></th><th>[0, 0]</th><th>[0, 1]</th></tr>
<tr><td>P1LED3</td><td>—</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link/Act</td><td>100Link/Act</td></tr>
<tr><td>P1LED1</td><td>Full duplex/Col</td><td>10Link/Act</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>Full duplex</td></tr>
</table>

<table>
<tr><th></th><th colspan="2">[LEDSEL1, LEDSEL0]</th></tr>
<tr><th></th><th>[1, 0]</th><th>[1, 1]</th></tr>
<tr><td>P1LED3</td><td>Act</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P1LED1</td><td>Full duplex/Col</td><td>—</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>—</td></tr>
</table>
Link/Act, 100Link/Act, 10Link/Act : Low (link), High (no link), Toggle (transmit / receive activity)
Full duplex/Col : Low (full duplex), High (half duplex), Toggles (collision)
Speed : Low (100BASE-TX), High (10BASE-T)
Full duplex : Low (full duplex), High (half duplex)
Act : Toggle (transmit / receive activity)
Link : Low (link), High (no link)

Repeater Mode (only)
<table>
<tr><th></th><th>[LEDSEL1, LEDSEL0]</th></tr>
<tr><th></th><th>[0, 0]</th></tr>
<tr><td>P1LED3</td><td>RPT_COL</td></tr>
<tr><td>P1LED2</td><td>RPT_LINK3/RX</td></tr>
<tr><td>P1LED1</td><td>RPT_LINK2/RX</td></tr>
<tr><td>P1LED0</td><td>RPT_LINK1/RX</td></tr>
</table>
RPT_COL : Low (collision)
RPT_LINK#/RX (# = port) : Low (link), High (no link), Toggles (receive activity)

Notes:
LEDSEL0 is external strap-in pin 70.
LEDSEL1 is external strap-in pin 23.
P1LED3 is pin 25.
During reset, P1LED[2:0] are inputs for internal testing.</td></tr>
<tr><td>2</td><td>P1LED1</td><td>Ipu/O</td></tr>
<tr><td>3</td><td>P1LED0</td><td>Ipu/O</td></tr>
</table>

Note:

1. Ipu/O = Input with internal pull-up during reset, output pin otherwise.

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type (1)</th><th>Description</th></tr>
<tr><td>4</td><td>P2LED2</td><td>Ipu/O</td><td rowspan="3">Port 2 LED Indicators
(apply to all modes of operation, except Repeater Mode)

<table>
<tr><td></td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[0, 0]</td><td>[0, 1]</td></tr>
<tr><td>P2LED3</td><td>—</td><td>—</td></tr>
<tr><td>P2LED2</td><td>Link/Act</td><td>100Link/Act</td></tr>
<tr><td>P2LED1</td><td>Full duplex/Col</td><td>10Link/Act</td></tr>
<tr><td>P2LED0</td><td>Speed</td><td>Full duplex</td></tr>
</table>

<table>
<tr><td></td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[1, 0]</td><td>[1, 1]</td></tr>
<tr><td>P2LED3</td><td>Act</td><td>—</td></tr>
<tr><td>P2LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P2LED1</td><td>Full duplex/Col</td><td>—</td></tr>
<tr><td>P2LED0</td><td>Speed</td><td>—</td></tr>
</table>
Link/Act, 100Link/Act, 10Link/Act : Low (link), High (no link), Toggle (transmit / receive activity)
Full duplex/Col : Low (full duplex), High (half duplex), Toggles (collision)
Speed : Low (100BASE-TX), High (10BASE-T)
Full duplex : Low (full duplex), High (half duplex)
Act : Toggle (transmit / receive activity)
Link : Low (link), High (no link)

Repeater Mode (only)
<table>
<tr><td></td><td>[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[0, 0]</td></tr>
<tr><td>P2LED3</td><td>RPT_ACT</td></tr>
<tr><td>P2LED2</td><td>RPT_ERR3</td></tr>
<tr><td>P2LED1</td><td>RPT_ERR2</td></tr>
<tr><td>P2LED0</td><td>RPT_ERR1</td></tr>
</table>
RPT_ACT : Low (activity)
RPT_ERR# (# = port) : Low (error status due to either isolation, partition, jabber, or JK error)
Notes:
LEDSEL0 is external strap-in pin 70.
LEDSEL1 is external strap-in pin 23.
P2LED3 is pin 20.
During reset, P2LED[2:0] are inputs for internal testing.</td></tr>
<tr><td>5</td><td>P2LED1</td><td>Ipu/O</td></tr>
<tr><td>6</td><td>P2LED0</td><td>Ipu/O</td></tr>
<tr><td>7</td><td>DGND</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>8</td><td>VDDIO</td><td>P</td><td>3.3V digital V_{DD}</td></tr>
</table>

Note:
1. P = Power supply.
   Gnd = Ground.
   Ipu/O = Input with internal pull-up during reset, output pin otherwise.

Pin Number	Pin Name	Type (1)	Description
9	NC	Ipd	No connect
10	NC	Ipd	No connect
11	NC	Ipu	No connect
12	ADVFC	Ipu	1 = advertise the switch's flow control capability via auto-negotiation. 0 = will not advertise the switch's flow control capability via auto-negotiation.
13	P2ANEN	Ipu	1 = enable auto-negotiation on port 2 0 = disable auto-negotiation on port 2
14	P2SPD	Ipd	1 = force port 2 to 100BT if P2ANEN = 0 0 = force port 2 to 10BT if P2ANEN = 0
15	P2DPX	Ipd	1 = port 2 default to full duplex mode if P2ANEN = 1 and auto-negotiation fails. Force port 2 in full duplex mode if P2ANEN = 0. 0 = port 2 default to half duplex mode if P2ANEN = 1 and auto-negotiation fails. Force port 2 in half duplex mode if P2ANEN = 0.
16	P2FFC	Ipd	1 = always enable (force) port 2 flow control feature 0 = port 2 flow control feature enable is determined by auto-negotiation result.
17	NC	Opu	No connect
18	NC	Ipd	No connect
19	NC	Ipd	No connect
20	P2LED3	Opd	Port 2 LED indicator Note: Internal pull-down is weak; it will not turn ON the LED. See description in pin 4.
21	DGND	Gnd	Digital ground
22	VDDCO	P	1.2V digital VDD Provides V_{OUT_1V2} to KSZ8893MQL's input power pins: V_{DDAP} (pin 63), V_{DDC} (pins 91 and 123), and V_{DDA} (pins 38, 43, and 57). It is recommended the pin should be connected to 3.3V power rail by a 100ohm resistor for the internal LDO application.
23	LEDSEL1	Ipd	LED display mode select See description in pins 1 and 4.
24	NC	O	No connect
25	P1LED3	Opd	Port 1 LED indicator Note: An external 1K pull-down is needed on this pin if it is connected to a LED. The 1K resistor will not turn ON the LED. See description in pin 1.

Note:

1. P = Power supply.
   Gnd = Ground.
   O = Output.
   Ipu = Input w/ internal pull-up.
   Ipd = Input w/ internal pull-down.
   Opu = Output w/ internal pull-up.
   Opd = Output w/ internal pull-down.

Pin Number	Pin Name	Type (1)	Description
26	RMII_EN	Opd	Strap pin for RMII Mode 0 = Disable 1 = Enable After reset, this pin has no meaning and is a no connect.
27	HWPOVR	Ipd	Hardware pin overwrite 0 = Disable. All strap-in pins configurations are overwritten by the EEPROM configuration data 1 = Enable. All strap-in pins configurations are overwritten by the EEPROM configuration data, except for register 0x2C bits [7:5], (port 2: auto-negotiation enable, force speed, force duplex).
28	P2MDIXDIS	Ipd	Port 2 Auto MDI/MDI-X PD (default) = enable PU = disable
29	P2MDIX	Ipd	Port 2 MDI/MDI-X setting when auto MDI/MDI-X is disabled. PD (default) = MDI-X (transmit on TXP2 / TXM2 pins) PU = MDI, (transmit on RXP2 / RXM2 pins)
30	P1ANEN	Ipu	1 = enable auto-negotiation on port 1 0 = disable auto-negotiation on port 1
31	P1SPD	Ipd	1 = force port 1 to 100BT if P1ANEN = 0 0 = force port 1 to 10BT if P1ANEN = 0
32	P1DPX	Ipd	1 = port 1 default to full duplex mode if P1ANEN = 1 and auto-negotiation fails. Force port 1 in full-duplex mode if P1ANEN = 0. 0 = port 1 default to half duplex mode if P1ANEN = 1 and auto- negotiation fails. Force port 1 in half duplex mode if P1ANEN = 0.
33	P1FFC	Ipd	1 = always enable (force) port 1 flow control feature 0 = port 1 flow control feature enable is determined by auto negotiation result.
34	NC	Ipd	No connect
35	NC	Ipd	No connect
36	PWRDN	Ipu	Chip power down input (active low)
37	AGND	Gnd	Analog ground
38	VDDA	P	1.2V analog V_{DD}
39	AGND	Gnd	Analog ground
40	MUX1	I	Factory test pin - float for normal operation
41	MUX2	I	Factory test pin - float for normal operation

Note:

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   Ipu = Input w/ internal pull-up.
   Ipd = Input w/ internal pull-down.
   Opd = Output w/ internal pull-down.

Pin Number	Pin Name	Type (1)	Description
42	AGND	Gnd	Analog ground
43	VDDA	P	1.2V analog V_{DD}
44	FXSD1	I	Fiber signal detect / factory test pin
45	RXP1	I/O	Physical receive or transmit signal (+ differential)
46	RXM1	I/O	Physical receive or transmit signal (– differential)
47	AGND	Gnd	Analog ground
48	TXP1	I/O	Physical transmit or receive signal (+ differential)
49	TXM1	I/O	Physical transmit or receive signal (– differential)
50	VDDATX	P	3.3V analog V_{DD}
51	VDDARX	P	3.3V analog V_{DD}
52	RXM2	I/O	Physical receive or transmit signal (– differential)
53	RXP2	I/O	Physical receive or transmit signal (+ differential)
54	AGND	Gnd	Analog ground.
55	TXM2	I/O	Physical transmit or receive signal (– differential)
56	TXP2	I/O	Physical transmit or receive signal (+ differential)
57	VDDA	P	1.2V analog V_{DD}
58	AGND	Gnd	Analog ground
59	TEST1	I	Factory test pin - float for normal operation
60	TEST2	I	Factory test pin - float for normal operation
61	ISET	O	Set physical transmit output current. Pull-down this pin with a 3.01K 1% resistor to ground.
62	AGND	Gnd	Analog ground
63	VDDAP	P	1.2V analog V_{DD} for PLL
64	AGND	Gnd	Analog ground.
65	X1	I	25MHz crystal/oscillator clock connections Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect. Note: Clock is +/- 50ppm for both crystal and oscillator.
66	X2	O	
67	RST_N	Ipu	Hardware reset pin (active low)
68	UNUSED	I	Unused pin – externally pull down for normal operation
69	UNUSED	I	Unused pin – externally pull down for normal operation

Note:

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.
   Ipu = Input w/ internal pull-up.

Pin Number	Pin Name	Type [1]	Description
70	LEDSEL0	I	LED display mode select See description in pins 1 and 4.
71	SMTXEN	I	Switch MII transmit enable
72	SMTXD3	I	Switch MII transmit data bit 3
73	SMTXD2	I	Switch MII transmit data bit 2
74	SMTXD1	I	Switch MII transmit data bit 1
75	SMTXD0	I	Switch MII transmit data bit 0
76	SMTXER	I	Switch MII transmit error
77	SMTXC / REFCLK	I/O	Switch MII transmit clock (MII and SNI modes only) Output in PHY MII mode and SNI mode Input in MAC MII mode Reference Clock (RMII mode only) Input for 50MHz +/- 50ppm system clock Note: In RMII mode, pin X1 is pulled up to VDDIO supply with a 10K resistor and pin X2 is a no connect.
78	DGND	Gnd	Digital ground
79	VDDIO	P	3.3V digital V_{DD}
80	SMRXC	I/O	Switch MII receive clock. Output in PHY MII mode Input in MAC MII mode
81	SMRXDV	O	Switch MII receive data valid
82	SMRXD3	Ipd/O	Switch MII receive data bit 3 Strap option: switch MII full-duplex flow control PD (default) = disable PU = enable
83	SMRXD2	Ipd/O	Switch MII receive data bit 2 Strap option: switch MII is in PD (default) = full-duplex mode PU = half-duplex mode
84	SMRXD1	Ipd/O	Switch MII receive data bit 1 Strap option: Switch MII is in PD (default) = 100Mbps mode PU = 10Mbps mode
85	SMRXD0	I/O	Switch MII receive data bit 0 Strap option: switch will accept packet size up to PD = 1536 bytes (inclusive) PU = 1522 bytes (tagged), 1518 bytes (untagged)
86	SCOL	I/O	Switch MII collision detect
87	SCRS	I/O	Switch MII carrier sense

Note:
1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise.
   I/O = Bi-directional.

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type (1)</th><th>Description</th></tr>
<tr><td>88</td><td>SCONF1</td><td>I</td><td rowspan="2">Switch MII interface configuration<table><tr><th>(SCONF1, SCONF0)</th><th>Description</th></tr><tr><td>(0,0)</td><td>disable, outputs tri-stated</td></tr><tr><td>(0,1)</td><td>PHY mode MII</td></tr><tr><td>(1,0)</td><td>MAC mode MII</td></tr><tr><td>(1,1)</td><td>PHY mode SNI</td></tr></table></td></tr>
<tr><td>89</td><td>SCONF0</td><td>I</td></tr>
<tr><td>90</td><td>DGND</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>91</td><td>VDDC</td><td>P</td><td>1.2V digital VDD</td></tr>
<tr><td>92</td><td>UNUSED</td><td>I</td><td rowspan="2">Unused pins – externally pull down for normal operation</td></tr>
<tr><td>93</td><td>UNUSED</td><td>I</td></tr>
<tr><td>94</td><td>MDC</td><td>I</td><td>MII management interface: clock input</td></tr>
<tr><td>95</td><td>MDIO</td><td>I/O</td><td>MII management interface: data input/output
Note: an external pull-up is needed on this pin when it is in use.</td></tr>
<tr><td>96</td><td>SPIQ</td><td>O</td><td>SPI slave mode: serial data output
See description in pins 100 and 101.
Note: an external pull-up is needed on this pin when it is in use.</td></tr>
<tr><td>97</td><td>SCL</td><td>I/O</td><td>SPI slave mode / I^2C slave mode: clock input
I^2C master mode: clock output
See description in pins 100 and 101.</td></tr>
<tr><td>98</td><td>SDA</td><td>I/O</td><td>SPI slave mode: serial data input
I^2C master/slave mode: serial data input/output
See description in pins 100 and 101.
Note: an external pull-up is needed on this pin when it is in use.</td></tr>
<tr><td>99</td><td>SPIS_N</td><td>I</td><td>SPI slave mode: chip select (active low)
When SPIS_N is high, the KSZ8893MQL is deselected and SPIQ is held in high impedance state.
A high-to-low transition is used to initiate SPI data transfer.
See description in pins 100 and 101.
Note: an external pull-up is needed on this pin when it is in use.</td></tr>
</table>

Note:

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type (1)</th><th>Description</th></tr>
<tr><td>100</td><td>PS1</td><td>I</td><td rowspan="2">Serial bus configuration pins to select mode of access to KSZ8893MQL internal registers.

[PS1, PS0] = [0, 0] — I²C master (EEPROM) mode
(If EEPROM is not detected, the KSZ8893MQL will be configured with the default values of its internal registers and the values of its strap-in pins.)
<table><tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr><tr><td>SPIQ</td><td>O</td><td>Not used (tri-stated)</td></tr><tr><td>SCL</td><td>O</td><td>I²C clock</td></tr><tr><td>SDA</td><td>I/O</td><td>I²C data I/O</td></tr><tr><td>SPIS_N</td><td>I</td><td>Not used</td></tr></table>[PS1, PS0] = [0, 1] — I²C slave mode
The external I²C master will drive the SCL clock.
The KSZ8893MQL device addresses are:
1011_1111 <read>
1011_1110 <write>
<table><tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr><tr><td>SPIQ</td><td>O</td><td>Not used (tri-stated)</td></tr><tr><td>SCL</td><td>I</td><td>I²C clock</td></tr><tr><td>SDA</td><td>I/O</td><td>I²C data I/O</td></tr><tr><td>SPIS_N</td><td>I</td><td>Not used</td></tr></table>[PS1, PS0] = [1, 0] — SPI slave mode
<table><tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr><tr><td>SPIQ</td><td>O</td><td>SPI data out</td></tr><tr><td>SCL</td><td>I</td><td>SPI clock</td></tr><tr><td>SDA</td><td>I</td><td>SPI data In</td></tr><tr><td>SPIS_N</td><td>I</td><td>SPI chip select</td></tr></table>[PS1, PS0] = [1, 1] – SMI-mode
In this mode, the KSZ8893MQL provides access to all its internal 8-bit registers through its MDC and MDIO pins.

Note:
When (PS1, PS0) ≠ (1,1), the KSZ8893MQL provides access to its 16-bit MIIM registers through its MDC and MDIO pins.</td></tr>
<tr><td>101</td><td>PS0</td><td>I</td></tr>
<tr><td>102</td><td>UNUSED</td><td>I</td><td rowspan="2">Unused pins – externally pull up for normal operation</td></tr>
<tr><td>103</td><td>UNUSED</td><td>I</td></tr>
</table>

Note:

1. I = Input.

Pin Number	Pin Name	Type [1]	Description
104	UNUSED	I	Unused pins – externally pull up for normal operation
105	UNUSED	I	
106	DGND	Gnd	Digital ground
107	VDDIO	P	3.3V digital V_{DD}
108	UNUSED	I	Unused pins – externally pull up for normal operation
109	UNUSED	I	
110	UNUSED	I	Unused pin – externally pull down for normal operation
111	UNUSED	I	Unused pin – externally pull down for normal operation
112	UNUSED	I	Unused pin – externally pull down for normal operation
113	UNUSED	I	Unused pin – externally pull down for normal operation
114	UNUSED	I	Unused pin – externally pull down for normal operation
115	UNUSED	I	Unused pin – externally pull down for normal operation
116	UNUSED	I	Unused pin – externally pull down for normal operation
117	UNUSED	I	Unused pin – externally pull down for normal operation
118	UNUSED	I	Unused pin – externally pull down for normal operation
119	UNUSED	I	Unused pin – externally pull down for normal operation
120	UNUSED	I	Unused pin – externally pull down for normal operation
121	UNUSED	I	Unused pin – externally pull down for normal operation
122	DGND	Gnd	Digital ground
123	VDDC	P	1.2V digital V_{DD}
124	UNUSED	I	Unused pin – externally pull down for normal operation
125	UNUSED	I	Unused pin – externally pull down for normal operation
126	UNUSED	I	Unused pin – externally pull down for normal operation
127	TESTEN	Ipd	Scan Test Enable For normal operation, pull-down this pin to ground.
128	SCANEN	Ipd	Scan Test Scan Mux Enable For normal operation, pull-down this pin to ground.

Note:

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   Ipd = Input w/ internal pull-down.

Ball Description and I/O Assignment of KSZ8893MBL

<table>
<tr><th>Ball Number</th><th>Ball Name</th><th>Type (1)</th><th>Ball Function Description</th></tr>
<tr><td>C10</td><td>P1LED2</td><td>Ipu/O</td><td rowspan="3">Port 1 LED Indicators
(apply to all modes of operation, except Repeater Mode)

<table>
<tr><th></th><th colspan="2">[LEDSEL1, LEDSEL0]</th></tr>
<tr><th></th><th>[0, 0]</th><th>[0, 1]</th></tr>
<tr><td>P1LED3</td><td>—</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link/Act</td><td>100Link/Act</td></tr>
<tr><td>P1LED1</td><td>Full duplex/Col</td><td>10Link/Act</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>Full duplex</td></tr>
</table>

<table>
<tr><th></th><th colspan="2">[LEDSEL1, LEDSEL0]</th></tr>
<tr><th></th><th>[1, 0]</th><th>[1, 1]</th></tr>
<tr><td>P1LED3</td><td>Act</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P1LED1</td><td>Full duplex/Col</td><td>—</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>—</td></tr>
</table>
Link/Act, 100Link/Act, 10Link/Act : Low (link), High (no link), Toggle (transmit / receive activity)
Full duplex/Col : Low (full duplex), High (half duplex), Toggles (collision)
Speed : Low (100BASE-TX), High (10BASE-T)
Full duplex : Low (full duplex), High (half duplex)
Act : Toggle (transmit / receive activity)
Link : Low (link), High (no link)

Repeater Mode (only)
<table>
<tr><th></th><th>[LEDSEL1, LEDSEL0]</th></tr>
<tr><th></th><th>[0, 0]</th></tr>
<tr><td>P1LED3</td><td>RPT_COL</td></tr>
<tr><td>P1LED2</td><td>RPT_LINK3/RX</td></tr>
<tr><td>P1LED1</td><td>RPT_LINK2/RX</td></tr>
<tr><td>P1LED0</td><td>RPT_LINK1/RX</td></tr>
</table>
RPT_COL : Low (collision)
RPT_LINK#/RX (# = port) : Low (link), High (no link), Toggles (receive activity)

Notes:
LEDSEL0 is external strap-in pin 70.
LEDSEL1 is external strap-in pin 23.
P1LED3 is pin 25.
During reset, P1LED[2:0] are inputs for internal testing.</td></tr>
<tr><td>B10</td><td>P1LED1</td><td>Ipu/O</td></tr>
<tr><td>A10</td><td>P1LED0</td><td>Ipu/O</td></tr>
</table>

Note:

1. Ipu/O = Input with internal pull-up during reset, output pin otherwise.

<table>
<tr><th>Ball Number</th><th>Ball Name</th><th>Type (1)</th><th>Ball Function Description</th></tr>
<tr><td>C9</td><td>P2LED2</td><td>Ipu/O</td><td rowspan="3">Port 2 LED Indicators
(apply to all modes of operation, except Repeater Mode)

<table>
<tr><td></td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[0, 0]</td><td>[0, 1]</td></tr>
<tr><td>P2LED3</td><td>—</td><td>—</td></tr>
<tr><td>P2LED2</td><td>Link/Act</td><td>100Link/Act</td></tr>
<tr><td>P2LED1</td><td>Full duplex/Col</td><td>10Link/Act</td></tr>
<tr><td>P2LED0</td><td>Speed</td><td>Full duplex</td></tr>
</table>
<table>
<tr><td></td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[1, 0]</td><td>[1, 1]</td></tr>
<tr><td>P2LED3</td><td>Act</td><td>—</td></tr>
<tr><td>P2LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P2LED1</td><td>Full duplex/Col</td><td>—</td></tr>
<tr><td>P2LED0</td><td>Speed</td><td>—</td></tr>
</table>
Link/Act, 100Link/Act, 10Link/Act : Low (link), High (no link), Toggle (transmit / receive activity)
Full duplex/Col : Low (full duplex), High (half duplex), Toggles (collision)
Speed : Low (100BASE-TX), High (10BASE-T)
Full duplex : Low (full duplex), High (half duplex)
Act : Toggle (transmit / receive activity)
Link : Low (link), High (no link)

Repeater Mode (only)
<table>
<tr><td></td><td>[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[0, 0]</td></tr>
<tr><td>P2LED3</td><td>RPT_ACT</td></tr>
<tr><td>P2LED2</td><td>RPT_ERR3</td></tr>
<tr><td>P2LED1</td><td>RPT_ERR2</td></tr>
<tr><td>P2LED0</td><td>RPT_ERR1</td></tr>
</table>
RPT_ACT : Low (activity)
RPT_ERR# (# = port) : Low (error status due to either isolation, partition, jabber, or JK error)
Notes:
LEDSEL0 is external strap-in pin 70.
LEDSEL1 is external strap-in pin 23.
P2LED3 is pin 20.
During reset, P2LED[2:0] are inputs for internal testing.</td></tr>
<tr><td>B9</td><td>P2LED1</td><td>Ipu/O</td></tr>
<tr><td>A9</td><td>P2LED0</td><td>Ipu/O</td></tr>
<tr><td>C8</td><td>ADVFC</td><td>Ipu</td><td>1 = advertise the switch’s flow control capability via auto-negotiation.
0 = will not advertise the switch’s flow control capability via auto-negotiation.</td></tr>
<tr><td>B8</td><td>P2ANEN</td><td>Ipu</td><td>1 = enable auto-negotiation on port 2
0 = disable auto-negotiation on port 2</td></tr>
</table>

Ball Number	Ball Name	Type [1]	Ball Function Description
A8	P2SPD	Ipd	1 = force port 2 to 100BT if P2ANEN = 0 0 = force port 2 to 10BT if P2ANEN = 0
B7	P2DPX	Ipd	1 = port 2 default to full duplex mode if P2ANEN = 1 and auto-negotiation fails. Force port 2 in full duplex mode if P2ANEN = 0. 0 = port 2 default to half duplex mode if P2ANEN = 1 and auto-negotiation fails. Force port 2 in half duplex mode if P2ANEN = 0.
A7	P2FFC	Ipd	1 = always enable (force) port 2 flow control feature 0 = port 2 flow control feature enable is determined by auto-negotiation result.
B6	P2LED3	Opd	Port 2 LED indicator Note: Internal pull-down is weak; it will not turn ON the LED. See description in pin 4.
A6	LEDSEL1	Ipd	LED display mode select See description in pins 1 and 4.
B5	P1LED3	Opd	Port 1 LED indicator Note: An external 1K pull-down is needed on this pin if it is connected to a LED. The 1K resistor will not turn ON the LED. See description in pin 1.
A5	RMII_EN	Opd	Strap pin for RMII Mode 0 = Disable 1 = Enable After reset, this pin has no meaning and is a no connect.
B4	HWPOVR	Ipd	Hardware pin overwrite 0 = Disable. All strap-in pins configurations are overwritten by the EEPROM configuration data 1 = Enable. All strap-in pins configurations are overwritten by the EEPROM configuration data, except for register 0x2C bits [7:5], (port 2: auto-negotiation enable, force speed, force duplex).
A4	P2MDIXDIS	Ipd	Port 2 Auto MDI/MDI-X PD (default) = enable PU = disable
B3	P2MDIX	Ipd	Port 2 MDI/MDI-X setting when auto MDI/MDI-X is disabled. PD (default) = MDI-X (transmit on TXP2 / TXM2 pins) PU = MDI, (transmit on RXP2 / RXM2 pins)
A3	P1ANEN	Ipu	1 = enable auto-negotiation on port 1 0 = disable auto-negotiation on port 1
B2	P1SPD	Ipd	1 = force port 1 to 100BT if P1ANEN = 0 0 = force port 1 to 10BT if P1ANEN = 0
A2	P1DPX	Ipd	1 = port 1 default to full duplex mode if P1ANEN = 1 and auto- negotiation fails. Force port 1 in full-duplex mode if P1ANEN = 0. 0 = port 1 default to half duplex mode if P1ANEN = 1 and auto- negotiation fails. Force port 1 in half duplex mode if P1ANEN = 0.

Ball Number	Ball Name	Type (1)	Ball Function Description
A1	P1FFC	Ipd	1 = always enable (force) port 1 flow control feature 0 = port 1 flow control feature enable is determined by auto negotiation result.
B1	PWRDN	Ipu	Chip power down input (active low)
C3	FXSD1	I	Fiber signal detect / factory test pin
C1	RXP1	I/O	Physical receive or transmit signal (+ differential)
C2	RXM1	I/O	Physical receive or transmit signal (– differential)
D1	TXP1	I/O	Physical transmit or receive signal (+ differential)
D2	TXM1	I/O	Physical transmit or receive signal (– differential)
F2	RXM2	I/O	Physical receive or transmit signal (– differential)
F1	RXP2	I/O	Physical receive or transmit signal (+ differential)
G2	TXM2	I/O	Physical transmit or receive signal (– differential)
G1	TXP2	I/O	Physical transmit or receive signal (+ differential)
H2	ISET	O	Set physical transmit output current. Pull-down this pin with a 3.01K 1% resistor to ground.
H1	X1	I	25MHz crystal/oscillator clock connections
J1	X2	O	Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect. Note: Clock is +/- 50ppm for both crystal and oscillator.
K1	RST_N	Ipu	Hardware reset pin (active low)
J2	LEDSEL0	I	LED display mode select See description in pins 1 and 4.
K2	SMTXEN	I	Switch MII transmit enable
J3	SMTXD3	I	Switch MII transmit data bit 3
K3	SMTXD2	I	Switch MII transmit data bit 2
J4	SMTXD1	I	Switch MII transmit data bit 1
K4	SMTXD0	I	Switch MII transmit data bit 0
J5	SMTXER	I	Switch MII transmit error
K5	SMTXC / REFCLK	I/O	Switch MII transmit clock (MII and SNI modes only) Output in PHY MII mode and SNI mode Input in MAC MII mode Reference Clock (RMII mode only) Input for 50MHz +/- 50ppm system clock Note: In RMII mode, pin X1 is pulled up to VDDIO supply with a 10K resistor and pin X2 is a no connect.
K6	SMRXC	I/O	Switch MII receive clock. Output in PHY MII mode Input in MAC MII mode
J6	SMRXDV	O	Switch MII receive data valid
J7	SMRXD3	Ipd/O	Switch MII receive data bit 3 Strap option: switch MII full-duplex flow control PD (default) = disable PU = enable

<table>
<tr><th>Ball Number</th><th>Ball Name</th><th>Type (1)</th><th>Ball Function Description</th></tr>
<tr><td>K7</td><td>SMRXD2</td><td>Ipd/O</td><td>Switch MII receive data bit 2
Strap option: switch MII is in
PD (default) = full-duplex mode
PU = half-duplex mode</td></tr>
<tr><td>J8</td><td>SMRXD1</td><td>Ipd/O</td><td>Switch MII receive data bit 1
Strap option: Switch MII is in
PD (default) = 100Mbps mode
PU = 10Mbps mode</td></tr>
<tr><td>K8</td><td>SMRXD0</td><td>I/O</td><td>Switch MII receive data bit 0
Strap option: switch will accept packet size up to
PD = 1536 bytes (inclusive)
PU = 1522 bytes (tagged), 1518 bytes (untagged)</td></tr>
<tr><td>J9</td><td>SCOL</td><td>I/O</td><td>Switch MII collision detect</td></tr>
<tr><td>K9</td><td>SCRS</td><td>I/O</td><td>Switch MII carrier sense</td></tr>
<tr><td>J10</td><td>SCONF1</td><td>I</td><td rowspan="2">Switch MII interface configuration<table><tr><th>(SCONF1, SCONF0)</th><th>Description</th></tr><tr><td>(0,0)</td><td>disable, outputs tri-stated</td></tr><tr><td>(0,1)</td><td>PHY mode MII</td></tr><tr><td>(1,0)</td><td>MAC mode MII</td></tr><tr><td>(1,1)</td><td>PHY mode SNI</td></tr></table></td></tr>
<tr><td>K10</td><td>SCONF0</td><td>I</td></tr>
<tr><td>H10</td><td>MDC</td><td>I</td><td>MII management interface: clock input</td></tr>
<tr><td>H9</td><td>MDIO</td><td>I/O</td><td>MII management interface: data input/output
Note: an external pull-up is needed on this pin when it is in use.</td></tr>
<tr><td>G9</td><td>SPIQ</td><td>O</td><td>SPI slave mode: serial data output
See description in pins 100 and 101.
Note: an external pull-up is needed on this pin when it is in use.</td></tr>
<tr><td>G10</td><td>SCL</td><td>I/O</td><td>SPI slave mode / I^2C slave mode: clock input
I^2C master mode: clock output
See description in pins 100 and 101.</td></tr>
<tr><td>F9</td><td>SDA</td><td>I/O</td><td>SPI slave mode: serial data input
I^2C master/slave mode: serial data input/output
See description in pins 100 and 101.
Note: an external pull-up is needed on this pin when it is in use.</td></tr>
<tr><td>F10</td><td>SPIS_N</td><td>I</td><td>SPI slave mode: chip select (active low)
When SPIS_N is high, the KSZ8893MBL is deselected and SPIQ is held in high impedance state.
A high-to-low transition is used to initiate SPI data transfer.
See description in pins 100 and 101.
Note: an external pull-up is needed on this pin when it is in use.</td></tr>
</table>

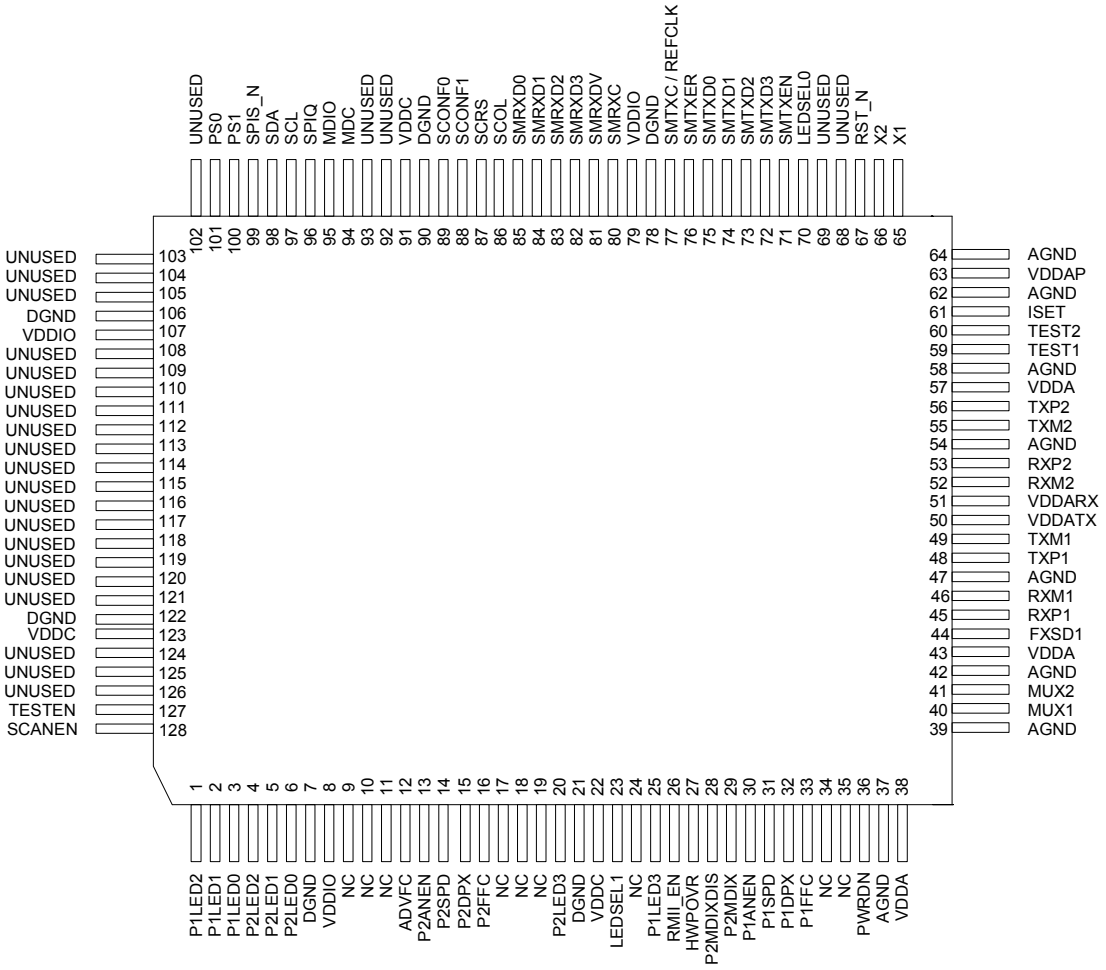
<table>
<tr><th>Ball Number</th><th>Ball Name</th><th>Type (1)</th><th>Ball Function Description</th></tr>
<tr><td>E9</td><td>PS1</td><td>I</td><td rowspan="2">Serial bus configuration pins to select mode of access to KSZ8893MBL internal registers.
[PS1, PS0] = [0, 0] — I²C master (EEPROM) mode
(If EEPROM is not detected, the KSZ8893MBL will be configured with the default values of its internal registers and the values of its strap-in pins.)
<table><tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr><tr><td>SPIQ</td><td>O</td><td>Not used (tri-stated)</td></tr><tr><td>SCL</td><td>O</td><td>I²C clock</td></tr><tr><td>SDA</td><td>I/O</td><td>I²C data I/O</td></tr><tr><td>SPIS_N</td><td>I</td><td>Not used</td></tr></table>[PS1, PS0] = [0, 1] — I²C slave mode
The external I²C master will drive the SCL clock.
The KSZ8893MBL device addresses are:
1011_1111 <read>
1011_1110 <write>
<table><tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr><tr><td>SPIQ</td><td>O</td><td>Not used (tri-stated)</td></tr><tr><td>SCL</td><td>I</td><td>I²C clock</td></tr><tr><td>SDA</td><td>I/O</td><td>I²C data I/O</td></tr><tr><td>SPIS_N</td><td>I</td><td>Not used</td></tr></table>[PS1, PS0] = [1, 0] — SPI slave mode
<table><tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr><tr><td>SPIQ</td><td>O</td><td>SPI data out</td></tr><tr><td>SCL</td><td>I</td><td>SPI clock</td></tr><tr><td>SDA</td><td>I</td><td>SPI data In</td></tr><tr><td>SPIS_N</td><td>I</td><td>SPI chip select</td></tr></table>[PS1, PS0] = [1, 1] – SMI-mode
In this mode, the KSZ8893MBL provides access to all its internal 8-bit registers through its MDC and MDIO pins.
Note:
When (PS1, PS0) ≠ (1,1), the KSZ8893MBL provides access to its 16-bit MIIM registers through its MDC and MDIO pins.</td></tr>
<tr><td>E10</td><td>PS0</td><td>I</td></tr>
<tr><td>D9</td><td>TESTEN</td><td>Ipd</td><td>Scan Test Enable
For normal operation, pull-down this pin to ground.</td></tr>
<tr><td>D10</td><td>SCANEN</td><td>Ipd</td><td>Scan Test Scan Mux Enable
For normal operation, pull-down this pin to ground.</td></tr>
<tr><td>C5, D8, E8, H6, H7</td><td>VDDC</td><td>P</td><td>1.2V digital V_{DD}</td></tr>
<tr><td>C4</td><td>VDDCO</td><td>P</td><td>1.2V digital V_{DD}
Provides V_{OUT_1V2} to KSZ8893MBL’s input power pins: V_{DDA} (pin E3, F3 and G3), V_{DDC} (pins C5, D8, E8, H6 and H7). It is recommended the pin should be connected to 3.3V power rail by a 100ohm resistor for the internal LDO application.</td></tr>
<tr><th>Ball Number</th><th>Ball Name</th><th>Type (1)</th><th>Ball Function Description</th></tr>
</table>

E3, F3, G3	VDDA	P	1.2V analog V_{DD}
C6, C7, F8, G8, H4, H5	VDDIO	P	3.3V digital V_{DD}
E1	VDDATX	P	3.3V analog V_{DD}
E2	VDDARX	P	3.3V analog V_{DD}
D4, D5, D6, D7, E4, E5, E6, E7, F4, F5, F6, F7, G4, G5, G6, G7	GND	Gnd	Ground
D3, H3, H8	NC	NC	No connect

Note:

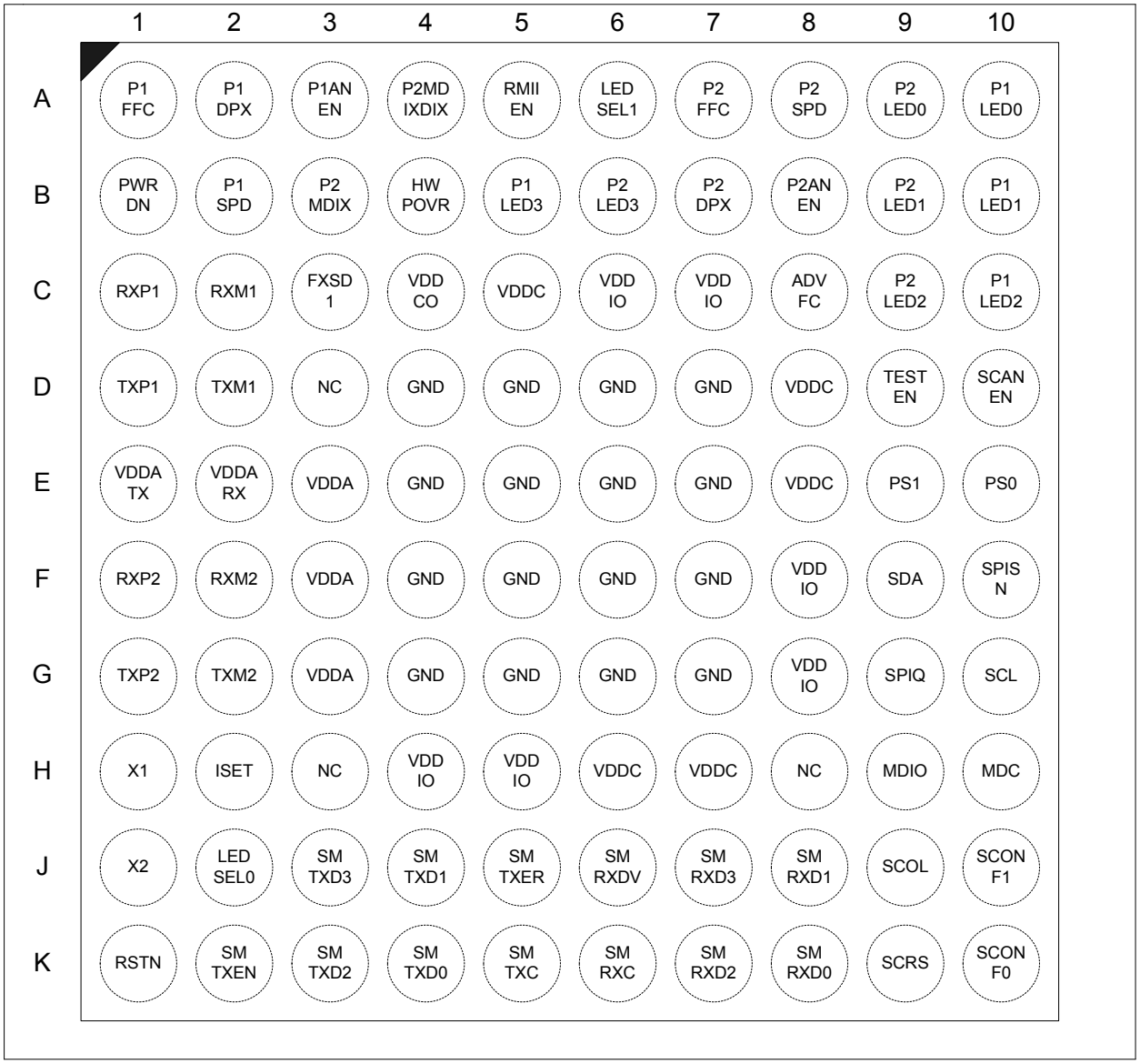
1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.
   Ipu = Input w/ internal pull-up.

Pin Configuration



KSZ8893 128-Pin PQFP (Top View)

Ball Configuration



KSZ8893MBL 100-Ball LFBGA (Top View)

Functional Description

The KSZ8893MQL/MBL contains two 10/100 physical layer transceivers and three MAC units with an integrated Layer 2 managed switch.

The KSZ8893MQL/MBL has the flexibility to reside in either a managed or unmanaged design. In a managed design, the host processor has complete control of the KSZ8893MQL/MBL via the SMI interface, MIIM interface, SPI bus, or I^2C bus. An unmanaged design is achieved through I/O strapping and/or EEPROM programming at system reset time.

On the media side, the KSZ8893MQL/MBL supports IEEE 802.3 10BASE-T and 100BASE-TX on both PHY ports, and also 100BASE-FX on PHY port 1, which allows the KSZ8893MQL/MBL to be used as a media converter.

Physical signal transmission and reception are enhanced through the use of patented analog circuitries that make the design more efficient and allow for lower power consumption and smaller chip die size.

Functional Overview: Physical Layer Transceiver

100BASE-TX Transmit

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by an external1% 3.01KΩ resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

100BASE-TX Receive

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

PLL Clock Synthesizer

The KSZ8893MQL/MBL generates 125MHz, 31.25MHz, 25MHz, and 10MHz clocks for system timing. Internal clocks are generated from an external 25MHz crystal or oscillator. In RMII mode, these internal clocks are generated from an external 50MHz oscillator or system clock.

Scrambler/De-scrambler (100BASE-TX Only)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander. Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence, and the receiver then de-scrambles the incoming data stream using the same sequence as at the transmitter.

100BASE-FX Operation

100BASE-FX operation is similar to 100BASE-TX operation with the differences being that the scrambler/de-scrambler and MLT3 encoder/decoder are bypassed on transmission and reception. In addition, auto-negotiation is bypassed and auto MDI/MDI-X is disabled.

100BASE-FX Signal Detection

In 100BASE-FX operation, FXSD1 (fiber signal detect), input pin 44, is usually connected to the fiber transceiver SD (signal detect) output pin. 100BASE-FX mode is activated when the FXSD1 input pin is greater than 1V. When FXSD1 is between 1V and 1.8V, no fiber signal is detected and a far-end fault (FEF) is generated. When FXSD1 is over 2.2V, the fiber signal is detected.

Alternatively, the designer may choose not to implement the FEF feature. In this case, the FXSD1 input pin is tied high to force 100BASE-FX mode.

100BASE-FX signal detection is summarized in the following table:

FXSD1 Input Voltage	Mode
Less than 0.2V	TX mode
Greater than 1V, but less than 1.8V	FX mode No signal detected. Far-end fault generated
Greater than 2.2V	FX mode Signal detected

Table 1. FX and TX Mode Selection

To ensure proper operation, a resistive voltage divider is recommended to adjust the fiber transceiver SD output voltage swing to match the FXSD1 pin's input voltage threshold.

100BASE-FX Far-End Fault

A far-end fault (FEF) occurs when the signal detection is logically false on the receive side of the fiber transceiver. The KSZ8893MQL/MBL detects a FEF when its FXSD1 input is between 1V and 1.8V. When a FEF is detected, the KSZ8893MQL/MBL signals its fiber link partner that a FEF has occurred by sending 84 1's followed by a zero in the idle period between frames.

By default, FEF is enabled. FEF can be disabled through register setting.

10BASE-T Transmit

The 10BASE-T driver is incorporated with the 100BASE-TX driver to allow for transmission using the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with a typical 2.3V amplitude. The harmonic contents are at least 27dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

10BASE-T Receive

On the receive side, input buffers and level detecting squelch circuits are employed. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400mV or with short pulse widths to prevent noise at the RXP-or-RXM input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8893MQL/MBL decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

Power Management

The KSZ8893MQL/MBL features a per-port power down mode. To save power, a PHY port that is not in use can be powered down via port control register, or MIIM PHY register.

In addition, there is a full chip power down mode. When activated, the entire chip is powered down.

MDI/MDI-X Auto Crossover

To eliminate the need for crossover cables between similar devices, the KSZ8893MQL/MBL supports HP Auto MDI/MDI-X and IEEE 802.3u standard MDI/MDI-X auto crossover. HP Auto MDI/MDI-X is the default.

The auto-sense function detects remote transmit and receive pairs and correctly assigns transmit and receive pairs for the KSZ8893MQL/MBL device. This feature is extremely useful when end users are unaware of cable types, and also, saves on an additional uplink configuration connection. The auto-crossover feature can be disabled through the port control registers, or MIIM PHY registers.

The IEEE 802.3u standard MDI and MDI-X definitions are:

MDI		MDI-X	
RJ-45 Pins	**Signals**	**RJ-45 Pins**	**Signals**
1	TD+	1	RD+
2	TD-	2	RD-
3	RD+	3	TD+
6	RD-	6	TD-

Table 2. MDI/MDI-X Pin Definitions

Straight Cable

A straight cable connects an MDI device to an MDI-X device, or an MDI-X device to an MDI device. The following diagram depicts a typical straight cable connection between a NIC card (MDI) and a switch, or hub (MDI-X).

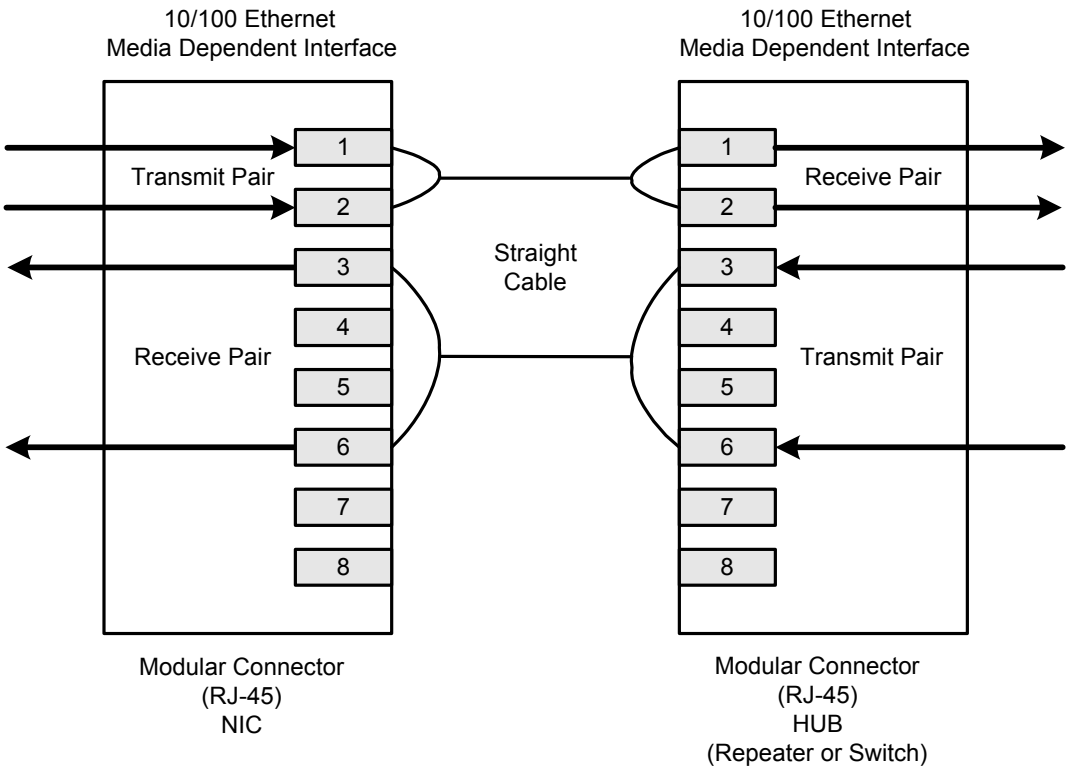


Figure 1. Typical Straight Cable Connection

Crossover Cable

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. The following diagram shows a typical crossover cable connection between two switches or hubs (two MDI-X devices).

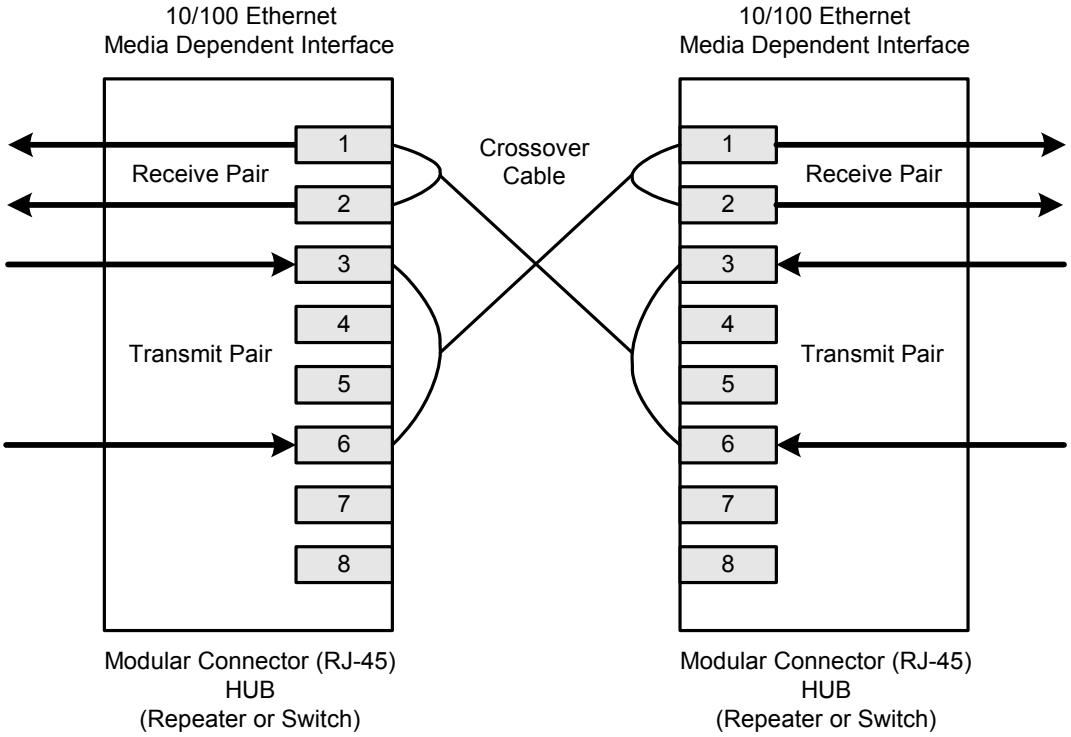


Figure 2. Typical Crossover Cable Connection

Auto-Negotiation

The KSZ8893MQL/MBL conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3u specification.

Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the best common mode of operation. In auto-negotiation, link partners advertise their capabilities across the link to each other. If auto-negotiation is not supported or the KSZ8893MQL/MBL link partner is forced to bypass auto-negotiation, the KSZ8893MQL/MBL sets its operating mode by observing the signal at its receiver. This is known as parallel detection, and allows the KSZ8893MQL/MBL to establish link by listening for a fixed signal protocol in the absence of auto-negotiation advertisement protocol.

The link up process is shown in the following flow diagram.

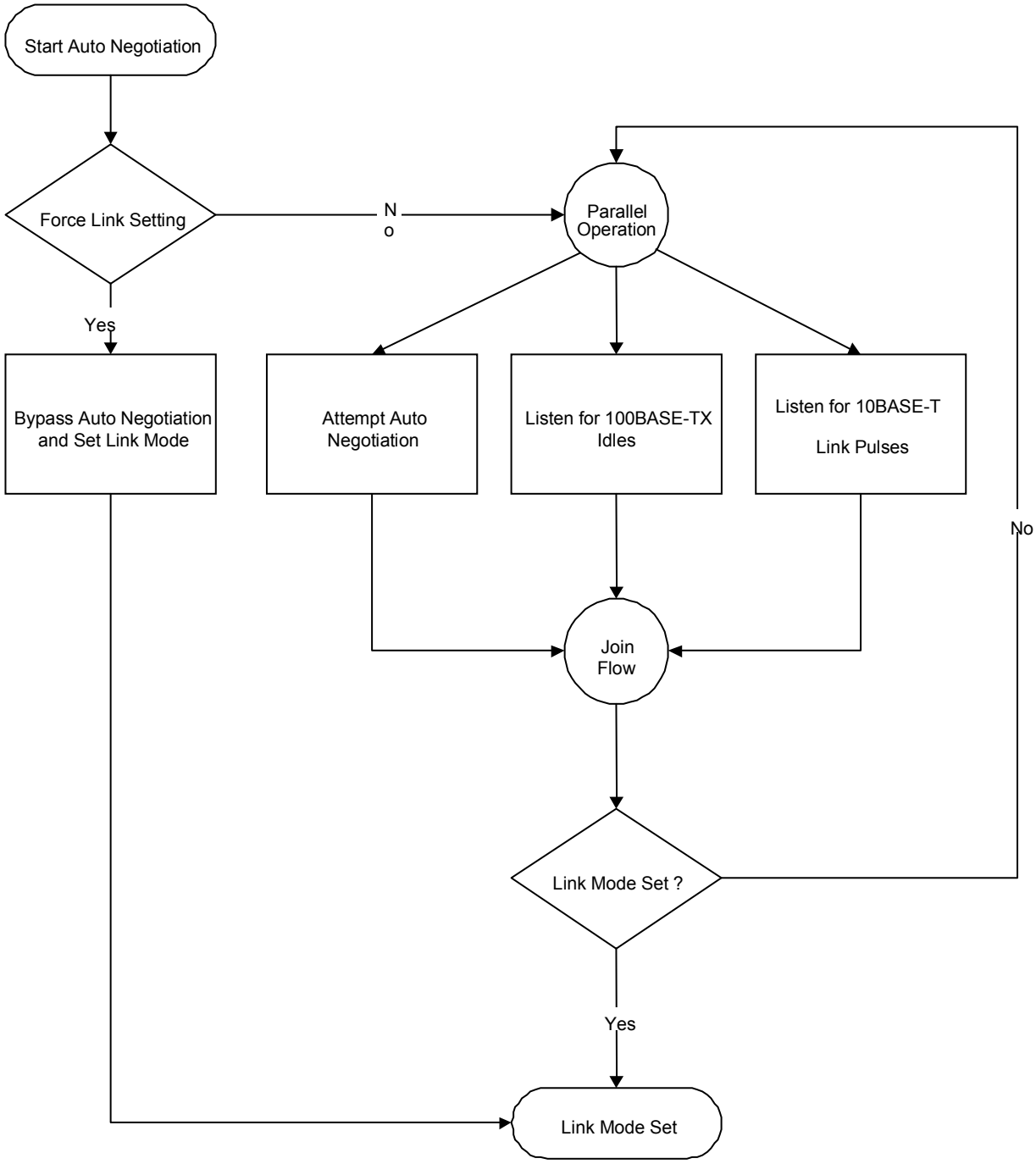


Figure 3. Auto-Negotiation and Parallel Operation

LinkMD Cable Diagnostics

The LinkMD feature utilizes time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems such as open circuits, short circuits and impedance mismatches.

LinkMD works by sending a pulse of known amplitude and duration down the MDI and MDI-X pairs and then analyzes the shape of the reflected signal. Timing the pulse duration gives an indication of the distance to the cabling fault with maximum distance of 200m and accuracy of +/- 2m. Internal circuitry displays the TDR information in a user-readable digital format.

Note: Cable diagnostics are only valid for copper connections and do not support fiber optic operation.

Access

LinkMD is initiated by accessing registers {26,27} and {42,43}, the LinkMD Control/Status registers, for ports 1 and 2, respectively; and in conjunction with registers 29 and 45, Port Control Register 13, for ports 1 and 2, respectively.

Alternatively, the MIIM PHY registers 0 and 29 can be used for LinkMD access.

Usage

The following is a sample procedure for using LinkMD with registers {26,27,29} on port 1.

1. Disable auto MDI/MDI-X by writing a '1' to register 29, bit [2] to enable manual control over the differential pair used to transmit the LinkMD pulse.
2. Start cable diagnostic test by writing a '1' to register 26, bit [4]. This enable bit is self-clearing.
3. Wait (poll) for register 26, bit [4] to return a '0', indicating cable diagnostic test is completed.
4. Read cable diagnostic test results in register 26, bits [6:5]. The results are as follows:

   00 = normal condition (valid test)
   01 = open condition detected in cable (valid test)
   10 = short condition detected in cable (valid test)
   11 = cable diagnostic test failed (invalid test)

   The '11' case, invalid test, occurs when the KSZ8893MQL/MBL is unable to shut down the link partner. In this instance, the test is not run, since it would be impossible for the KSZ8893MQL/MBL to determine if the detected signal is a reflection of the signal generated or a signal from another source.
5. Get distance to fault by concatenating register 26, bit [0] and register 27, bits [7:0]; and multiplying the result by a constant of 0.4. The distance to the cable fault can be determined by the following formula:

   D (distance to cable fault) = 0.4 x {(register 26, bit [0]),(register 27, bits [7:0])}

   D (distance to cable fault) is expressed in meters.

   Concatenated value of registers 26 and 27 is converted to decimal before multiplying by 0.4.

   The constant (0.4) may be calibrated for different cabling conditions, including cables with a velocity of propagation that varies significantly from the norm.

For port 2 and for the MIIM PHY registers, LinkMD usage is similar.

Functional Overview: MAC and Switch

Address Lookup

The internal lookup table stores MAC addresses and their associated information. It contains a 1K unicast address table plus switching information.

The KSZ8893MQL/MBL is guaranteed to learn 1K addresses and distinguishes itself from hash-based lookup tables, which depending on the operating environment and probabilities, may not guarantee the absolute number of addresses it can learn.

Learning

The internal lookup engine updates its table with a new entry if the following conditions are met:

1. The received packet's Source Address (SA) does not exist in the lookup table.
2. The received packet is good; the packet has no receiving errors, and is of legal length.

The lookup engine inserts the qualified SA into the table, along with the port number and time stamp. If the table is full, the last entry of the table is deleted to make room for the new entry.

Migration

The internal lookup engine also monitors whether a station has moved. If a station has moved, it will update the table accordingly. Migration happens when the following conditions are met:

1. The received packet's SA is in the table but the associated source port information is different.
2. The received packet is good; the packet has no receiving errors, and is of legal length.

The lookup engine will update the existing record in the table with the new source port information.

Aging

The lookup engine updates the time stamp information of a record whenever the corresponding SA appears. The time stamp is used in the aging process. If a record is not updated for a period of time, the lookup engine removes the record from the table. The lookup engine constantly performs the aging process and will continuously remove aging records. The aging period is about 200 seconds. This feature can be enabled or disabled through register 3 (0x03) bit [2].

Forwarding

The KSZ8893MQL/MBL forwards packets using the algorithm that is depicted in the following flowcharts. Figure 4 shows stage one of the forwarding algorithm where the search engine looks up the VLAN ID, static table, and dynamic table for the destination address, and comes up with “port to forward 1” (PTF1). PTF1 is then further modified by spanning tree, IGMP snooping, port mirroring, and port VLAN processes to come up with “port to forward 2” (PTF2), as shown in Figure 5. The packet is sent to PTF2.

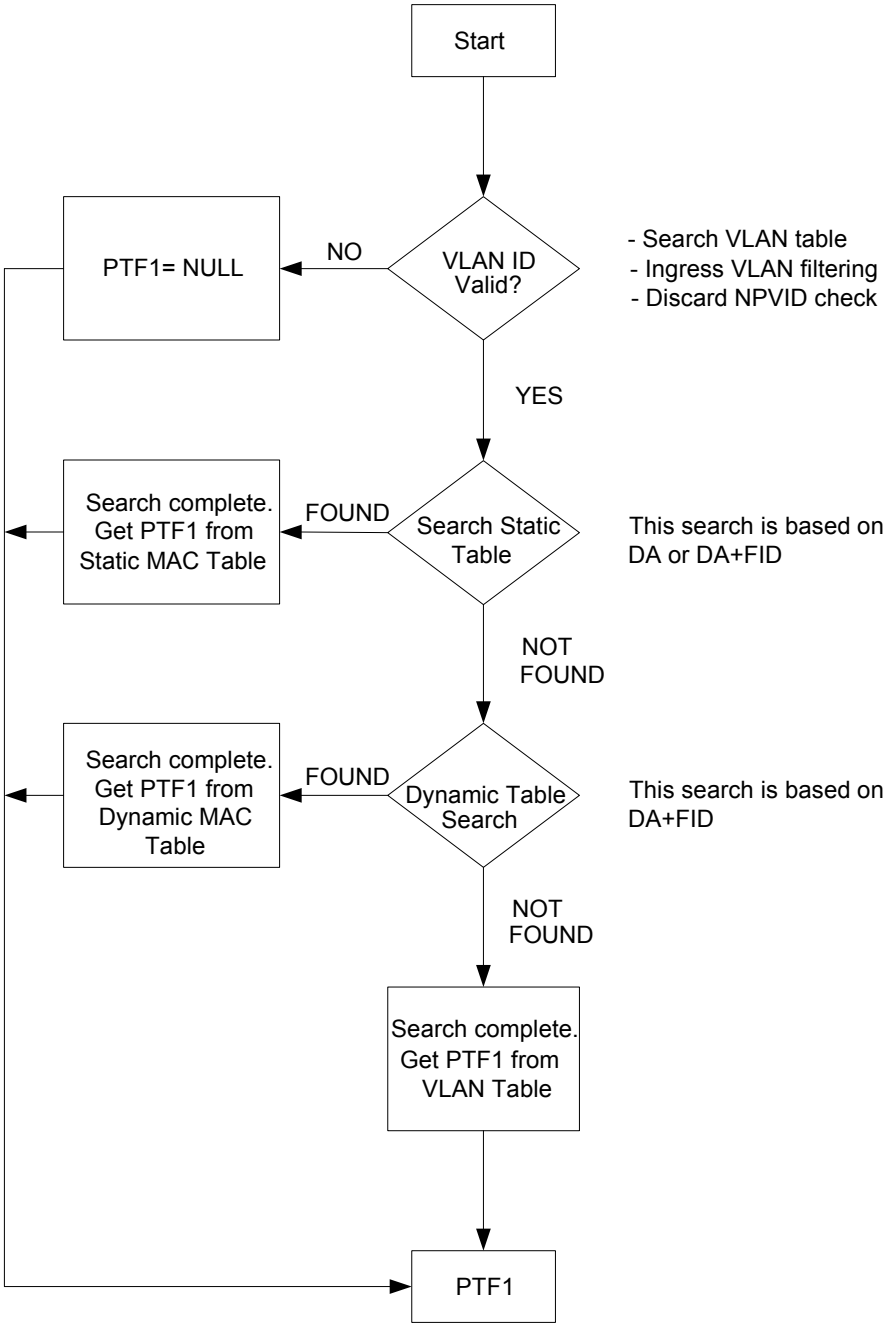


Figure 4. Destination Address Lookup Flow Chart, Stage 1

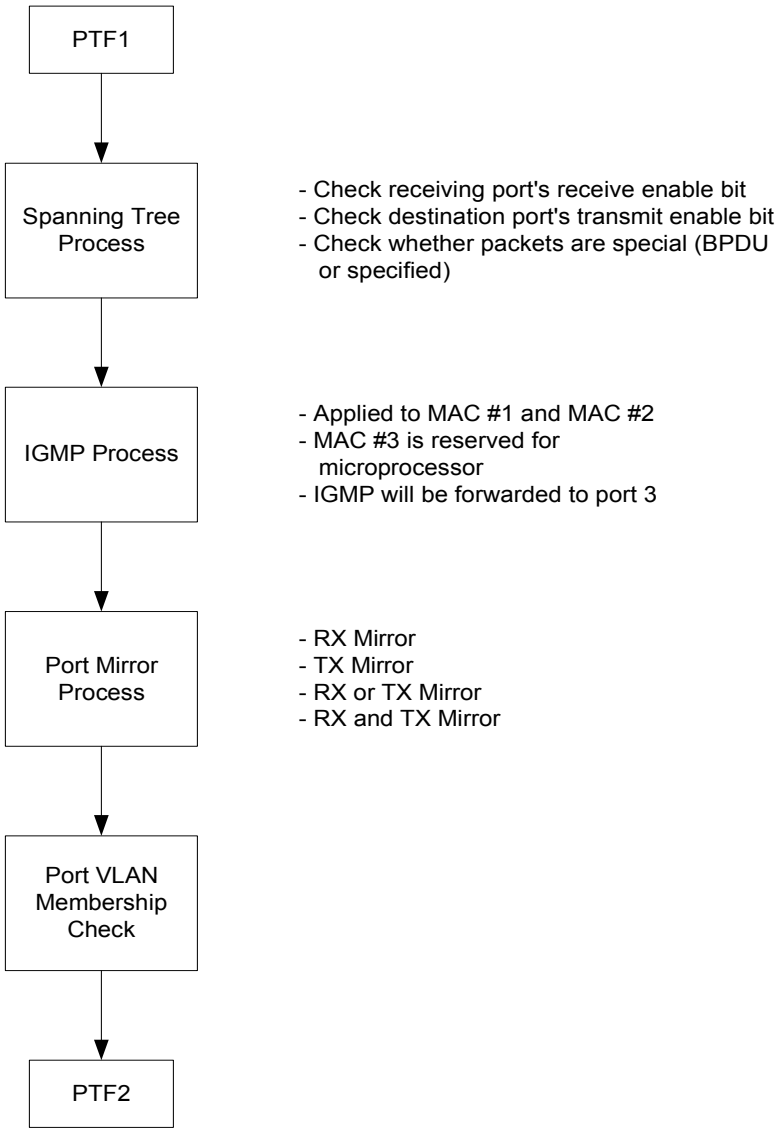


Figure 5. Destination Address Resolution Flow Chart, Stage 2

The KSZ8893MQL/MBL will not forward the following packets:

1. Error packets
   These include framing errors, Frame Check Sequence (FCS) errors, alignment errors, and illegal size packet errors.
2. IEEE802.3x PAUSE frames
   KSZ8893MQL/MBL intercepts these packets and performs full duplex flow control accordingly.
3. "Local" packets
   Based on destination address (DA) lookup. If the destination port from the lookup table matches the port from which the packet originated, the packet is defined as "local."

Switching Engine

The KSZ8893MQL/MBL features a high-performance switching engine to move data to and from the MACs' packet buffers. It operates in store and forward mode, while the efficient switching mechanism reduces overall latency.

The switching engine has a 32kB internal frame buffer. This buffer pool is shared between all three ports. There are a total of 256 buffers available. Each buffer is sized at 128 bytes.

MAC Operation

The KSZ8893MQL/MBL strictly abides by IEEE 802.3 standards to maximize compatibility.

Inter Packet Gap (IPG)

If a frame is successfully transmitted, the 96 bits time IPG is measured between the two consecutive MTXEN. If the current packet is experiencing collision, the 96 bits time IPG is measured from MCRS and the next MTXEN.

Back-Off Algorithm

The KSZ8893MQL/MBL implements the IEEE 802.3 standard for the binary exponential back-off algorithm, and optional "aggressive mode" back-off. After 16 collisions, the packet is optionally dropped depending on the switch configuration for register 4 (0x04) bit [3].

Late Collision

If a transmit packet experiences collisions after 512 bit times of the transmission, the packet is dropped.

Illegal Frames

The KSZ8893MQL/MBL discards frames less than 64 bytes, and can be programmed to accept frames up to1518 bytes, 1536 bytes or 1916 bytes. These maximum frame size settings are programmed in register 4 (0x04). Since the KSZ8893MQL/MBL supports VLAN tags, the maximum sizing is adjusted when these tags are present.

Full Duplex Flow Control

The KSZ8893MQL/MBL supports standard IEEE 802.3x flow control frames on both transmit and receive sides.

On the receive side, if the KSZ8893MQL/MBL receives a pause control frame, the KSZ8893MQL/MBL will not transmit the next normal frame until the timer, specified in the pause control frame, expires. If another pause frame is received before the current timer expires, the timer will be updated with the new value in the second pause frame. During this period (while it is flow controlled), only flow control packets from the KSZ8893MQL/MBL are transmitted.

On the transmit side, the KSZ8893MQL/MBL has intelligent and efficient ways to determine when to invoke flow control. The flow control is based on availability of the system resources, including available buffers, available transmit queues and available receive queues.

The KSZ8893MQL/MBL will flow control a port that has just received a packet if the destination port resource is busy. The KSZ8893MQL/MBL issues a flow control frame (XOFF), containing the maximum pause time defined by the IEEE 802.3x standard. Once the resource is freed up, the KSZ8893MQL/MBL sends out the other flow control frame (XON) with zero pause time to turn off the flow control (turn on transmission to the port). A hysteresis feature is provided to prevent the flow control mechanism from being constantly activated and deactivated.

The KSZ8893MQL/MBL flow controls all ports if the receive queue becomes full.

Half-Duplex Backpressure

A half-duplex backpressure option (not in IEEE 802.3 standards) is also provided. The activation and deactivation conditions are the same as full duplex flow control. If backpressure is required, the KSZ8893MQL/MBL sends preambles to defer the other stations' transmission (carrier sense deference).

To avoid jabber and excessive deference (as defined in the 802.3 standard), after a certain time, the KSZ8893MQL/MBL discontinues the carrier sense and then raises it again quickly. This short silent time (no carrier sense) prevents other stations from sending out packets thus keeping other stations in a carrier sense

deferred state. If the port has packets to send during a backpressure situation, the carrier sense type backpressure is interrupted and those packets are transmitted instead. If there are no additional packets to send, carrier sense type backpressure is reactivated again until switch resources free up. If a collision occurs, the binary exponential back-off algorithm is skipped and carrier sense is generated immediately, thus reducing the chance of further collisions and carrier sense is maintained to prevent packet reception.

To ensure no packet loss in 10 BASE-T or 100 BASE-TX half duplex modes, the user must enable the following:

1. Aggressive back-off (register 3 (0x03), bit [0])
2. No excessive collision drop (register 4 (0x04), bit [3])

Note: These bits are not set as defaults, as this is not the IEEE standard.

Broadcast Storm Protection

The KSZ8893MQL/MBL has an intelligent option to protect the switch system from receiving too many broadcast packets. As the broadcast packets are forwarded to all ports except the source port, an excessive number of switch resources (bandwidth and available space in transmit queues) may be utilized. The KSZ8893MQL/MBL has the option to include “multicast packets” for storm control. The broadcast storm rate parameters are programmed globally, and can be enabled or disabled on a per port basis. The rate is based on a 67ms interval for 100BT and a 500ms interval for 10BT. At the beginning of each interval, the counter is cleared to zero, and the rate limit mechanism starts to count the number of bytes during the interval. The rate definition is described in register 6 (0x06) and 7 (0x07). The default setting is 0x63 (99 decimal). This is equal to a rate of 1%, calculated as follows:

148,800 frames/sec * 67ms/interval * 1% = 99 frames/interval (approx.) = 0x63

Note: 148,800 frames/sec is based on 64-byte block of packets in 100BASE-TX with 12 bytes of IPG and 8 bytes of preamble between two packets.

MII Interface Operation

The Media Independent Interface (MII) is specified in Clause 22 of the IEEE 802.3u Standard. It provides a common interface between physical layer and MAC layer devices. The MII provided by the KSZ8893MQL/MBL is connected to the device’s third MAC. The interface contains two distinct groups of signals: one for transmission and the other for reception. The following table describes the signals used by the MII bus.

PHY-Mode Connections			**MAC-Mode Connections**	
External MAC Controller Signals	**KSZ8893MQL/MBL PHY Signals**	**Pin Descriptions**	**External PHY Signals**	**KSZ8893MQL/MBL MAC Signals**
MTXEN	SMTXEN	Transmit enable	MTXEN	SMRXDV
MTXER	SMTXER	Transmit error	MTXER	(not used)
MTXD3	SMTXD[3]	Transmit data bit 3	MTXD3	SMRXD[3]
MTXD2	SMTXD[2]	Transmit data bit 2	MTXD2	SMRXD[2]
MTXD1	SMTXD[1]	Transmit data bit 1	MTXD1	SMRXD[1]
MTXD0	SMTXD[0]	Transmit data bit 0	MTXD0	SMRXD[0]
MTXC	SMTXC	Transmit clock	MTXC	SMRXC
MCOL	SCOL	Collision detection	MCOL	SCOL
MCRS	SCRS	Carrier sense	MCRS	SCRS
MRXDV	SMRXDV	Receive data valid	MRXDV	SMTXEN
MRXER	(not used)	Receive error	MRXER	SMTXER
MRXD3	SMRXD[3]	Receive data bit 3	MRXD3	SMTXD[3]
MRXD2	SMRXD[2]	Receive data bit 2	MRXD2	SMTXD[2]
MRXD1	SMRXD[1]	Receive data bit 1	MRXD1	SMTXD[1]
MRXD0	SMRXD[0]	Receive data bit 0	MRXD0	SMTXD[0]
MRXC	SMRXC	Receive clock	MRXC	SMTXC

Table 3. MII Signals

The MII operates in either PHY mode or MAC mode. The data interface is a nibble wide and runs at ¼ the network bit rate (not encoded). Additional signals on the transmit side indicate when data is valid or when an error occurs during transmission. Similarly, the receive side has signals that convey when the data is valid and without physical layer errors. For half duplex operation, the SCOL signal indicates if a collision has occurred during transmission.

The KSZ8893MBL does not provide the MRXER signal for PHY mode operation and the MTXER signal for MAC mode operation. Normally, MRXER indicates a receive error coming from the physical layer device and MTXER indicates a transmit error from the MAC device. Since the switch filters error frames, these MII error signals are not used by the KSZ8893MBL. So, for PHY mode operation, if the device interfacing with the KSZ8893MBL has an MRXER input pin, it needs to be tied low. And, for MAC mode operation, if the device interfacing with the KSZ8893MQL/MBL has an MTXER input pin, it also needs to be tied low.

RMII Interface Operation

The Reduced Media Independent Interface (RMII) specifies a low pin count Media Independent Interface (MII). RMII provides a common interface between physical layer and MAC layer devices, and has the following key characteristics:

1. Supports 10Mbps and 100Mbps data rates.
2. Uses a single 50 MHz clock reference (provided externally).
3. Provides independent 2-bit wide (di-bit) transmit and receive data paths.
4. Contains two distinct groups of signals: one for transmission and the other for reception

The RMII provided by the KSZ8893MQL/MBL is connected to the device's third MAC. It complies with the RMII Specification. The following table describes the signals used by the RMII bus. Refer to RMII Specification for full detail on the signal description.

RMII Signal Name	Direction (with respect to the PHY)	Direction (with respect to the MAC)	RMII Signal Description	KSZ8893MQL/MBL RMII Signal (direction)
REF_CLK	Input	Input or Output	Synchronous 50 MHz clock reference for receive, transmit and control interface	REFCLK (input)
CRS_DV	Output	Input	Carrier sense/ Receive data valid	SMRXDV (output)
RXD1	Output	Input	Receive data bit 1	SMRXD[1] (output)
RXD0	Output	Input	Receive data bit 0	SMRXD[0] (output)
TX_EN	Input	Output	Transmit enable	SMTXEN (input)
TXD1	Input	Output	Transmit data bit 1	SMTXD[1] (input)
TXD0	Input	Output	Transmit data bit 0	SMTXD[0] (input)
RX_ER	Output	Input (not required)	Receive error	(not used)
---	---	---	---	SMTXER* (input) *** Connects to RX_ER signal of RMII PHY device**

Table 4: RMII Signal Description

The KSZ8893MQL/MBL filters error frames, and thus does not implement the RX_ER output signal. To detect error frames from RMII PHY devices, the SMTXER input signal of the KSZ8893MQL/MBL is connected to the RXER output signal of the RMII PHY device.

Collision detection is implemented in accordance with the RMII Specification.

In RMII mode, tie MII signals, SMTXD[3:2] and SMTXER, to ground if they are not used.

The KSZ8893MQL/MBL RMII can interface with RMII PHY and RMII MAC devices. The latter allows two KSZ8893MQL/MBL devices to be connected back-to-back. The following table shows the KSZ8893MQL/MBL RMII pin connections with an external RMII PHY and an external RMII MAC, such as another KSZ8893MQL/MBL device.

KSZ8893MQL/MBL PHY-MAC Connections			**KSZ8893MQL/MBL MAC-MAC Connections**	
External PHY Signals	**KSZ8893MQL/MBL MAC Signals**	**Pin Descriptions**	**KSZ8893MQL/MBL MAC Signals**	**External MAC Signals**
REF_CLK	REFCLK	Reference Clock	REFCLK	REF_CLK
TX_EN	SMRXDV	Carrier sense/ Receive data valid	SMRXDV	CRS_DV
TXD1	SMRXD[1]	Receive data bit 1	SMRXD[1]	RXD1
TXD0	SMRXD[0]	Receive data bit 0	SMRXD[0]	RXD0
CRS_DV	SMTXEN	Transmit enable	SMTXEN	TX_EN
RXD1	SMTXD[1]	Transmit data bit 1	SMTXD[1]	TXD1
RXD0	SMTXD[0]	Transmit data bit 0	SMTXD[0]	TXD0
RX_ER	SMTXER	Receive error	(not used)	(not used)

Table 5: RMII Signal Connections

SNI (7-Wire) Operation

The serial network interface (SNI) or 7-wire is compatible with some controllers used for network layer protocol processing. In SNI mode, the KSZ8893MQL/MBL acts like a PHY and the external controller functions as the MAC. The KSZ8893MQL/MBL can interface directly with external controllers using the 7-wire interface. These signals are divided into two groups, one for transmission and the other for reception. The signals involved are described in the following table.

Pin Descriptions	**External MAC Controller Signals**	**KSZ8893MQL/MBL PHY Signals**
Transmit enable	TXEN	SMTXEN
Serial transmit data	TXD	SMTXD[0]
Transmit clock	TXC	SMTXC
Collision detection	COL	SCOL
Carrier sense	CRS	SMRXDV
Serial receive data	RXD	SMRXD[0]
Receive clock	RXC	SMRXC

Table 6. SNI Signals

The SNI interface is a bit wide data interface and therefore runs at the network bit rate (not encoded). An additional signal on the transmit side indicates when data is valid. Similarly, the receive side has an indicator that conveys when the data is valid.

For half duplex operation, the SCOL signal is used to indicate that a collision has occurred during transmission.

MII Management (MIIM) Interface

The KSZ8893MQL/MBL supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input/Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the states of the KSZ8893MQL/MBL. An external device with MDC/MDIO capability is used to read the PHY status or configure the PHY settings. Further detail on the MIIM interface is found in Clause 22.2.4.5 of the IEEE 802.3u Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the data line (MDIO) and the clock line (MDC).
- A specific protocol that operates across the aforementioned physical connection that allows an external controller to communicate with the KSZ8893MQL/MBL device.
- Access to a set of eight 16-bit registers, consisting of six standard MIIM registers [0:5] and two custom MIIM registers [29, 31].

The MIIM Interface can operate up to a maximum clock speed of 5 MHz.

The following table depicts the MII Management Interface frame format.

	Preamble	Start of Frame	Read/Write OP Code	PHY Address Bits [4:0]	REG Address Bits [4:0]	TA	Data Bits [15:0]	Idle
Read	32 1's	01	10	AAAAA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	AAAAA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

Table 7. MII Management Interface Frame Format

Serial Management Interface (SMI)

The SMI is the KSZ8893MQL/MBL non-standard MIIM interface that provides access to all KSZ8893MQL/MBL configuration registers. This interface allows an external device to completely monitor and control the states of the KSZ8893MQL/MBL.

The SMI interface consists of the following:

- A physical connection that incorporates the data line (MDIO) and the clock line (MDC).
- A specific protocol that operates across the aforementioned physical connection that allows an external controller to communicate with the KSZ8893MQL/MBL device.
- Access to all KSZ8893MQL/MBL configuration registers. Register access includes the Global, Port and Advanced Control Registers 0-141 (0x00 – 0x8D), and indirect access to the standard MIIM registers [0:5] and custom MIIM registers [29, 31].

The following table depicts the SMI frame format.

	Preamble	Start of Frame	Read/Write OP Code	PHY Address Bits [4:0]	REG Address Bits [4:0]	TA	Data Bits [15:0]	Idle
Read	32 1's	01	00	1xRRR	RRRRR	Z0	0000_0000_DDDD_DDDD	Z
Write	32 1's	01	00	0xRRR	RRRRR	10	xxxx_xxxx_DDDD_DDDD	Z

Table 8. Serial Management Interface (SMI) Frame Format

SMI register read access is selected when OP Code is set to "00" and bit 4 of the PHY address is set to '1'. SMI register write access is selected when OP Code is set to "00" and bit 4 of the PHY address is set to '0'. PHY address bit[3] is undefined for SMI register access, and hence can be set to either '0' or '1' in read/write operations.

To access the KSZ8893MQL/MBL registers 0-141 (0x00 – 0x8D), the following applies:

- PHYAD[2:0] and REGAD[4:0] are concatenated to form the 8-bit address;
  that is, {PHYAD[2:0], REGAD[4:0]} = bits [7:0] of the 8-bit address.
- Registers are 8 data bits wide.
  For read operation, data bits [15:8] are read back as 0's.
  For write operation, data bits [15:8] are not defined, and hence can be set to either '0' or '1'.

SMI register access is the same as the MIIM register access, except for the register access requirements presented in this section.

Repeater Mode

The KSZ8893MQL/MBL supports repeater mode in 100BASE-TX Half Duplex mode. In repeater mode, all ingress packets are broadcast to the other two ports. MAC address checking and learning are disabled.

Repeater mode is enabled by setting register 6 bit[7] to '1'. Prior to setting this bit, all three ports need to be configured to 100BASE-TX Half Duplex mode. Additionally, both PHY ports need to have auto-negotiation disabled.

The latency between the two PHY ports is 270 ns (minimum) and 310 ns (maximum). The 40 ns difference is one clock skew (one 25 MHz clock period) between reception and transmission. Latency is defined as the time from the first bit of the Destination Address (DA) entering the ingress port to the first bit of the DA exiting the egress port.

Advanced Switch Functions

Spanning Tree Support

To support spanning tree, port 3 is designated as the processor port.

The other ports (port 1 and port 2) can be configured in one of the five spanning tree states via “transmit enable”, “receive enable” and “learning disable” register settings in registers 18 and 34 for ports 1 and 2, respectively. The following table shows the port setting and software actions taken for each of the five spanning tree states.

Disable State	**Port Setting**	**Software Action**
The port should not forward or receive any packets. Learning is disabled.	“transmit enable = 0, receive enable = 0, learning disable =1”	The processor should not send any packets to the port. The switch may still send specific packets to the processor (packets that match some entries in the “static MAC table” with “overriding bit” set) and the processor should discard those packets. Address learning is disabled on the port in this state.
Blocking State	**Port Setting**	**Software Action**
Only packets to the processor are forwarded. Learning is disabled.	“transmit enable = 0, receive enable = 0, learning disable =1”	The processor should not send any packets to the port(s) in this state. The processor should program the “Static MAC table” with the entries that it needs to receive (for example, BPDU packets). The “overriding” bit should also be set so that the switch will forward those specific packets to the processor. Address learning is disabled on the port in this state.
Listening State	**Port Setting**	**Software Action**
Only packets to and from the processor are forwarded. Learning is disabled.	“transmit enable = 0, receive enable = 0, learning disable =1”	The processor should program the “Static MAC table” with the entries that it needs to receive (for example, BPDU packets). The “overriding” bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state. See “Special Tagging Mode” for details. Address learning is disabled on the port in this state.
Learning State	**Port Setting**	**Software Action**
Only packets to and from the processor are forwarded. Learning is enabled.	“transmit enable = 0, receive enable = 0, learning disable = 0”	The processor should program the “Static MAC table” with the entries that it needs to receive (for example, BPDU packets). The “overriding” bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state. See “Special Tagging Mode” for details. Address learning is enabled on the port in this state.
Forwarding State	**Port Setting**	**Software Action**
Packets are forwarded and received normally. Learning is enabled.	“transmit enable = 1, receive enable = 1, learning disable = 0”	The processor programs the “Static MAC table” with the entries that it needs to receive (for example, BPDU packets). The “overriding” bit is set so that the switch forwards those specific packets to the processor. The processor can send packets to the port(s) in this state. See “Special Tagging Mode” for details. Address learning is enabled on the port in this state.

Table 9: Spanning Tree States

Special Tagging Mode

Special Tagging Mode is designed for spanning tree protocol IGMP snooping and is flexible for use in other applications. Special Tagging, similar to 802.1Q Tagging, requires software to change network drivers to insert/modify/strip/interpret the special tag. This mode is enabled by setting both register 11 bit [0] and register 48 bit [2] to '1'.

802.1Q Tag Format	Special Tag Format
TPID (tag protocol identifier, 0x8100) + TCI.	STPID (special tag identifier, 0x810 + 4 bit for "port mask") + TCI

Table 10. Special Tagging Mode Format

The STPID is only seen and used by the port 3 interface, which should be connected to a processor. Packets from the processor to the switch's port 3 should be tagged with the STPID and the port mask, defined as follows:

"0001", forward packet to port 1 only
"0010", forward packet to port 2 only
"0011", broadcast packet to port 1 and port 2

Packets with normal tags ("0000" port masks) will use KSZ8893MQL/MBL internal MAC table lookup to determine the forwarding port(s). Also, if packets from the processor are not tagged, the KSZ8893MQL/MBL will treat them as normal packets and use internal MAC table lookup to determine the forwarding port(s).

The KSZ8893MQL/MBL uses a non-zero "port mask" to bypass the internal MAC table lookup result, and override any port setting, regardless of port states (disable, blocking, listening, learning). The table below shows the processor to switch egress rules when dealing with STPID.

Ingress Tag Field	TX port "tag insertion"	TX port "tag removal"	Egress Action to Tag Field
(0x810+ port mask)	0	0	- Modify tag field to 0x8100 - Recalculate CRC - No change to TCI if not null VID - Replace VID with ingress (port 3) port VID if null VID
(0x810+ port mask)	0	1	- (STPID + TCI) will be removed - Padding to 64 bytes if necessary - Recalculate CRC
(0x810+ port mask)	1	0	- Modify tag field to 0x8100 - Recalculate CRC - No change to TCI if not null VID - Replace VID with ingress (port 3) port VID if null VID
(0x810+ port mask)	1	1	- Modify tag field to 0x8100 - Recalculate CRC - No change to TCI if not null VID - Replace VID with ingress (port 3) port VID if null VID
Not Tagged	Don't care	Don't care	- Determined by the Dynamic MAC Address Table

Table 11. STPID Egress Rules (Processor to Switch Port 3)

For packets from regular ports (port 1 & port 2) to port 3, the port mask is used to tell the processor which port the packets were received on, defined as follows:

"0001", packet from port 1
"0010", packet from port 2

No port mask values, other than the previous two defined ones, should be received in this direction in Special Tagging Mode. The switch to processor egress rules are defined as follows:

Ingress Packets	Egress Action to Tag Field
Tagged with 0x8100 + TCI	- Modify TPID to 0x810 + "port mask", which indicates source port. - No change to TCI if VID is not null - Replace null VID with ingress port VID - Recalculate CRC
Not tagged.	- Insert TPID to 0x810 + "port mask", which indicates source port - Insert TCI with ingress port VID - Recalculate CRC

Table 12. STPID Egress Rules (Switch Port 3 to Processor)

IGMP Support

For Internet Group Management Protocol (IGMP) support in layer 2, the KSZ8893MQL/MBL provides two components:

IGMP Snooping

The KSZ8893MQL/MBL traps IGMP packets and forwards them only to the processor (port 3). The IGMP packets are identified as IP packets (either Ethernet IP packets, or IEEE 802.3 SNAP IP packets) with IP version = 0x4 and protocol version number = 0x2.

Multicast Address Insertion in the Static MAC Table

Once the multicast address is programmed in the Static MAC Table, the multicast session is trimmed to the subscribed ports, instead of broadcasting to all ports.

To enable IGMP support, set register 5 bit [6] to '1'. Also, Special Tagging Mode needs to be enabled, so that the processor knows which port the IGMP packet was received on. This is achieved by setting both register 11 bit [0] and register 48 bit [2] to '1'.

IPv6 MLD Snooping

The KSZ8893MQL/MBL traps IPv6 Multicast Listener Discovery (MLD) packets and forwards them only to processor (port 3). MLD snooping is controlled by register 5 bit 5 (MLD snooping enable) and register 5 bit 4 (MLD option).

With MLD snooping enabled, the KSZ8893MQL/MBL traps packets that meet all of the following conditions:

- IPv6 multicast packets
- Hop count limit = 1
- IPv6 next header = 1 or 58 (or = 0 with hop-by-hop next header = 1 or 58)

If the MLD option bit is set to "1", the KSZ8893MQL/MBL traps packets with the following additional condition:

- IPv6 next header = 43, 44, 50, 51, or 60 (or = 0 with hop-by-hop next header = 43, 44, 50, 51, or 60)

For MLD snooping, Special Tagging Mode also needs to be enabled, so that the processor knows which port the MLD packet was received on. This is achieved by setting both register 11 bit [0] and register 48 bit [2] to '1'.

Port Mirroring Support

KSZ8893MQL/MBL supports “Port Mirroring” comprehensively as:

“receive only” mirror on a port

All the packets received on the port are mirrored on the sniffer port. For example, port 1 is programmed to be “receive sniff” and port 3 is programmed to be the “sniffer port”. A packet received on port 1 is destined to port 2 after the internal lookup. The KSZ8893MQL/MBL forwards the packet to both port 2 and port 3. The KSZ8893MQL/MBL can optionally even forward “bad” received packets to the “sniffer port”.

“transmit only” mirror on a port

All the packets transmitted on the port are mirrored on the sniffer port. For example, port 1 is programmed to be “transmit sniff” and port 3 is programmed to be the “sniffer port”. A packet received on port 2 is destined to port 1 after the internal lookup. The KSZ8893MQL/MBL forwards the packet to both port 1 and port 3.

“receive and transmit” mirror on two ports

All the packets received on port A and transmitted on port B are mirrored on the sniffer port. To turn on the “AND” feature, set register 5 bit [0] to ‘1’. For example, port 1 is programmed to be “receive sniff”, port 2 is programmed to be “transmit sniff”, and port 3 is programmed to be the “sniffer port”. A packet received on port 1 is destined to port 2 after the internal lookup. The KSZ8893MQL/MBL forwards the packet to both port 2 and port 3.

Multiple ports can be selected as “receive sniff” or “transmit sniff”. In addition, any port can be selected as the “sniffer port”. All these per port features can be selected through registers 17, 33 and 49 for ports 1, 2 and 3, respectively.

IEEE 802.1Q VLAN Support

The KSZ8893MQL/MBL supports 16 active VLANs out of the 4096 possible VLANs specified in the IEEE 802.1Q specification. KSZ8893MQL/MBL provides a 16-entries VLAN Table, which converts the 12-bits VLAN ID (VID) to the 4-bits Filter ID (FID) for address lookup. If a non-tagged or null-VID-tagged packet is received, the ingress port default VID is used for lookup. In VLAN mode, the lookup process starts with VLAN Table lookup to determine whether the VID is valid. If the VID is not valid, the packet is dropped and its address is not learned. If the VID is valid, the FID is retrieved for further lookup. The FID + Destination Address (FID+DA) are used to determine the destination port. The FID + Source Address (FID+SA) are used for address learning.

DA found in Static MAC Table?	Use FID flag?	FID match?	DA+FID found in Dynamic MAC Table?	Action
No	Don’t care	Don’t care	No	Broadcast to the membership ports defined in the *VLAN Table* bits [18:16]
No	Don’t care	Don’t care	Yes	Send to the destination port defined in the *Dynamic MAC Address Table* bits [53:52]
Yes	0	Don’t care	Don’t care	Send to the destination port(s) defined in the *Static MAC Address Table* bits [50:48]
Yes	1	No	No	Broadcast to the membership ports defined in the *VLAN Table* bits [18:16]
Yes	1	No	Yes	Send to the destination port defined in the *Dynamic MAC Address Table* bits [53:52]
Yes	1	Yes	Don’t care	Send to the destination port(s) defined in the *Static MAC Address Table* bits [50:48]

Table 13. FID+DA Lookup in VLAN Mode

FID+SA found in Dynamic MAC Table?	Action
No	Learn and add FID+SA to the Dynamic MAC Address Table
Yes	Update time stamp

Table 14. FID+SA Lookup in VLAN Mode

Advanced VLAN features, such as “Ingress VLAN filtering” and “Discard Non PVID packets” are also supported by the KSZ8893MQL/MBL. These features can be set on a per port basis, and are defined in register 18, 34 and 50 for ports 1, 2 and 3, respectively.

QoS Priority Support

The KSZ8893MQL/MBL provides Quality of Service (QoS) for applications such as VoIP and video conferencing. Offering four priority queues per port, the per-port transmit queue can be split into four priority queues: Queue 3 is the highest priority queue and Queue 0 is the lowest priority queue. Bit [0] of registers 16, 32 and 48 is used to enable split transmit queues for ports 1, 2 and 3, respectively. If a port's transmit queue is not split, high priority and low priority packets have equal priority in the transmit queue.

There is an additional option to either always deliver high priority packets first or use weighted fair queuing for the four priority queues. This global option is set and explained in bit [3] of register 5.

Port-Based Priority

With port-based priority, each ingress port is individually classified as a high priority receiving port. All packets received at the high priority receiving port are marked as high priority and are sent to the high-priority transmit queue if the corresponding transmit queue is split. Bits [4:3] of registers 16, 32 and 48 are used to enable port-based priority for ports 1, 2 and 3, respectively.

802.1p-Based Priority

For 802.1p-based priority, the KSZ8893MQL/MBL examines the ingress (incoming) packets to determine whether they are tagged. If tagged, the 3-bit priority field in the VLAN tag is retrieved and compared against the “priority mapping” value, as specified by the registers 12 and 13. The “priority mapping” value is programmable.

The following figure illustrates how the 802.1p priority field is embedded in the 802.1Q VLAN tag.

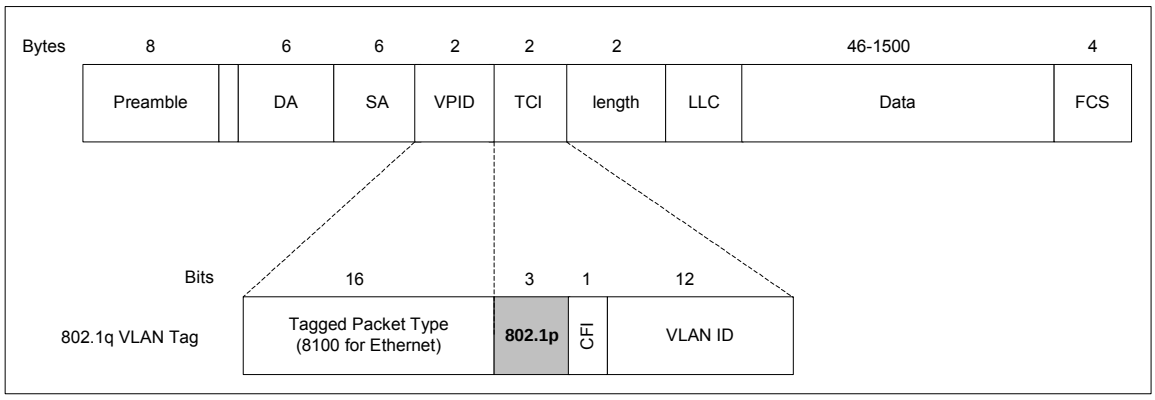


Figure 6. 802.1p Priority Field Format

802.1p-based priority is enabled by bit [5] of registers 16, 32 and 48 for ports 1, 2 and 3, respectively.

The KSZ8893MQL/MBL provides the option to insert or remove the priority tagged frame's header at each individual egress port. This header, consisting of the 2 bytes VLAN Protocol ID (VPID) and the 2-byte Tag Control Information field (TCI), is also referred to as the IEEE 802.1Q VLAN tag.

Tag Insertion is enabled by bit [2] of registers 16, 32 and 48 for ports 1, 2 and 3, respectively. At the egress port, untagged packets are tagged with the ingress port's default tag. The default tags are programmed in register sets {19,20}, {35,36} and {51,52} for ports 1, 2 and 3, respectively. The KSZ8893MQL/MBL will not add tags to already tagged packets.

Tag Removal is enabled by bit [1] of registers 16, 32 and 48 for ports 1, 2 and 3, respectively. At the egress port, tagged packets will have their 802.1Q VLAN Tags removed. The KSZ8893MQL/MBL will not modify untagged packets.

The CRC is recalculated for both tag insertion and tag removal.

802.1p Priority Field Re-mapping is a QoS feature that allows the KSZ8893MQL/MBL to set the "User Priority Ceiling" at any ingress port. If the ingress packet's priority field has a higher priority value than the default tag's priority field of the ingress port, the packet's priority field is replaced with the default tag's priority field. The "User Priority Ceiling" is enabled by bit [3] of registers 17, 33 and 49 for ports 1, 2 and 3, respectively.

DiffServ-Based Priority

DiffServ-based priority uses the ToS registers (registers 96 to 111) in the Advanced Control Registers section. The ToS priority control registers implement a fully decoded, 64-bit Differentiated Services Code Point (DSCP) register to determine packet priority from the 6-bit ToS field in the IP header. When the most significant 6 bits of the ToS field are fully decoded, the resultant of the 64 possibilities is compared with the corresponding bits in the DSCP register to determine priority.

Rate Limiting Support

The KSZ8893MQL/MBL supports hardware rate limiting from 64 Kbps to 88 Mbps, independently on the "receive side" and on the "transmit side" on a per port basis. For 10BASE-T, a rate setting above 10 Mbps means the rate is not limited. On the receive side, the data receive rate for each priority at each port can be limited by setting up Ingress Rate Control Registers. On the transmit side, the data transmit rate for each priority queue at each port can be limited by setting up Egress Rate Control Registers. The size of each frame has options to include minimum IFG (Inter Frame Gap) or Preamble byte, in addition to the data field (from packet DA to FCS).

For ingress rate limiting, KSZ8893MQL/MBL provides options to selectively choose frames from all types, multicast, broadcast, and flooded unicast frames. The KSZ8893MQL/MBL counts the data rate from those selected type of frames. Packets are dropped at the ingress port when the data rate exceeds the specified rate limit.

For egress rate limiting, the Leaky Bucket algorithm is applied to each output priority queue for shaping output traffic. Inter frame gap is stretched on a per frame base to generate smooth, non-burst egress traffic. The throughput of each output priority queue is limited by the egress rate specified.

If any egress queue receives more traffic than the specified egress rate throughput, packets may be accumulated in the output queue and packet memory. After the memory of the queue or the port is used up, packet dropping or flow control will be triggered. As a result of congestion, the actual egress rate may be dominated by flow control/dropping at the ingress end, and may be therefore slightly less than the specified egress rate.

To reduce congestion, it is a good practice to make sure the egress bandwidth exceeds the ingress bandwidth.

Unknown Unicast MAC Address Filtering

The unicast MAC address filtering function works in conjunction with the static MAC address table. First, the static MAC address table is used to assign a dedicated MAC address to a specific port. If a unicast MAC address is not recorded in the static table, and also not learned in the dynamic MAC table, KSZ8893MQL/MBL is then configured with the option to either filter or forward unicast packets for an unknown MAC address. This option is enabled and configured in register 14.

This function is useful in preventing the broadcast of unicast packets that could degrade the quality of the port in applications such as voice over Internet Protocol (VoIP).

Configuration Interface

The KSZ8893MQL/MBL can operate as both a managed switch and an unmanaged switch.

In unmanaged mode, the KSZ8893MQL/MBL is typically programmed using an EEPROM. If no EEPROM is present, the KSZ8893MQL/MBL is configured using its default register settings. Some default settings are configured via strap-in pin options. The strap-in pins are indicated in the "KSZ8893MQL/MBL Pin Description and I/O Assignment" table.

I^2C Master Serial Bus Configuration

With an additional I^2C ("2-wire") EEPROM, the KSZ8893MQL/MBL can perform more advanced switch features like "broadcast storm protection" and "rate control" without the need of an external processor.

For KSZ8893MQL/MBL I^2C Master configuration, the EEPROM stores the configuration data for register 0 to register 120 (as defined in the KSZ8893MQL/MBL register map) with the exception of the "Read Only" status registers. After the de-assertion of reset, the KSZ8893MQL/MBL sequentially reads in the configuration data for all 121 registers, starting from register 0. The configuration access time (t_{prgm}) is less than 15 ms, as depicted in the following figure.

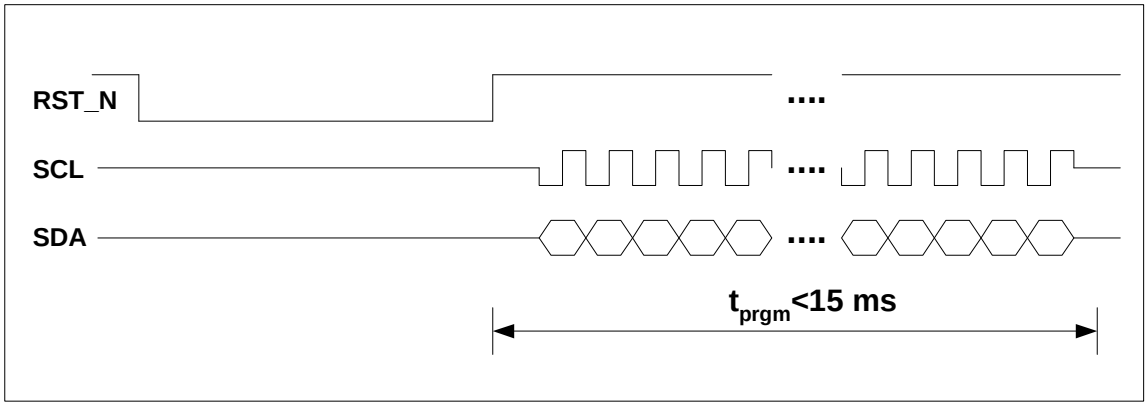


Figure 7. KSZ8893MQL/MBL EEPROM Configuration Timing Diagram

The following is a sample procedure for programming the KSZ8893MQL/MBL with a pre-configured EEPROM:

1. Connect the KSZ8893MQL/MBL to the EEPROM by joining the SCL and SDA signals of the respective devices. For the KSZ8893MQL/MBL, SCL is pin 97 and SDA is pin 98.
2. Enable I^2C master mode by setting the KSZ8893MQL/MBL strap-in pins, PS[1:0] (pins 100 and 101, respectively) to "00".
3. Check to ensure that the KSZ8893MQL/MBL reset signal input, RST_N (pin 67), is properly connected to the external reset source at the board level.
4. Program the desired configuration data into the EEPROM.
5. Place the EEPROM on the board and power up the board.
6. Assert an active-low reset to the RST_N pin of the KSZ8893MQL/MBL. After reset is de-asserted, the KSZ8893MQL/MBL begins reading the configuration data from the EEPROM. The KSZ8893MQL/MBL checks that the first byte read from the EEPROM is "88". If this value is correct, EEPROM configuration continues. If not, EEPROM configuration access is denied and all other data sent from the EEPROM is ignored by the KSZ8893MQL/MBL. The configuration access time (t_{prgm}) is less than 15ms.

Note: For proper operation, check to ensure that the KSZ8893MQL/MBL PWRDN input signal (pin 36) is not asserted during the reset operation. The PWRDN input is active low.

I^2C Slave Serial Bus Configuration

In managed mode, the KSZ8893MQL/MBL can be configured as an I^2C slave device. In this mode, an I^2C master device (external controller/CPU) has complete programming access to the KSZ8893MQL/MBL's 142 registers. Programming access includes the Global Registers, Port Registers, Advanced Control Registers and indirect access to the "Static MAC Table", "VLAN Table", "Dynamic MAC Table," and "MIB Counters." The tables and counters are indirectly accessed via registers 121 to 131.

In I^2C slave mode, the KSZ8893MQL/MBL operates like other I^2C slave devices. Addressing the KSZ8893MQL/MBL's 8-bit registers is similar to addressing Atmel's AT24C02 EEPROM's memory locations. Details of I^2C read/write operations and related timing information can be found in the AT24C02 Datasheet.

Two fixed 8-bit device addresses are used to address the KSZ8893MQL/MBL in I^2C slave mode. One is for read; the other is for write. The addresses are as follow:

1011_1111 <read>

1011_1110 <write>

The following is a sample procedure for programming the KSZ8893MQL/MBL using the I^2C slave serial bus:

1. Enable I^2C slave mode by setting the KSZ8893MQL/MBL strap-in pins PS[1:0] (pins 100 and 101, respectively) to "01".
2. Power up the board and assert reset to the KSZ8893MQL/MBL. After reset, the "Start Switch" bit (register 1 bit [0]) is set to '0'.
3. Configure the desired register settings in the KSZ8893MQL/MBL, using the I^2C write operation.
4. Read back and verify the register settings in the KSZ8893MQL/MBL, using the I^2C read operation.
5. Write a '1' to the "Start Switch" bit to start the KSZ8893MQL/MBL with the programmed settings.

Note: The "Start Switch" bit cannot be set to '0' to stop the switch after an '1' is written to this bit. Thus, it is recommended that all switch configuration settings are programmed before the "Start Switch" bit is set to '1'.

Some of the configuration settings, such as "Aging enable", "Auto Negotiation Enable", "Force Speed" and "Power down" can be programmed after the switch has been started.

SPI Slave Serial Bus Configuration

In managed mode, the KSZ8893MQL/MBL can be configured as a SPI slave device. In this mode, a SPI master device (external controller/CPU) has complete programming access to the KSZ8893MQL/MBL's 142 registers. Programming access includes the Global Registers, Port Registers, Advanced Control Registers and indirect access to the "Static MAC Table", "VLAN Table", "Dynamic MAC Table" and "MIB Counters". The tables and counters are indirectly accessed via registers 121 to 131.

The KSZ8893MQL/MBL supports two standard SPI commands: '0000_0011' for data read and '0000_0010' for data write. SPI multiple read and multiple write are also supported by the KSZ8893MQL/MBL to expedite register read back and register configuration, respectively.

SPI multiple read is initiated when the master device continues to drive the KSZ8893MQL/MBL SPIS_N input pin (SPI Slave Select signal) low after a byte (a register) is read. The KSZ8893MQL/MBL internal address counter increments automatically to the next byte (next register) after the read. The next byte at the next register address is shifted out onto the KSZ8893MQL/MBL SPIQ output pin. SPI multiple read continues until the SPI master device terminates it by de-asserting the SPIS_N signal to the KSZ8893MQL/MBL.

Similarly, SPI multiple write is initiated when the master device continues to drive the KSZ8893MQL/MBL SPIS_N input pin low after a byte (a register) is written. The KSZ8893MQL/MBL internal address counter increments automatically to the next byte (next register) after the write. The next byte that is sent from the master device to the KSZ8893MQL/MBL SDA input pin is written to the next register address. SPI multiple write continues until the SPI master device terminates it by de-asserting the SPIS_N signal to the KSZ8893MQL/MBL.

For both SPI multiple read and multiple write, the KSZ8893MQL/MBL internal address counter wraps back to register address zero once the highest register address is reached. This feature allows all 142 KSZ8893MQL/MBL registers to be read, or written with a single SPI command from any initial register address.

The KSZ8893MQL/MBL is capable of supporting a 5MHz SPI bus.

The following is a sample procedure for programming the KSZ8893MQL/MBL using the SPI bus:

1. At the board level, connect the KSZ8893MQL/MBL pins as follows:

KSZ8893MQL/MBL Pin #	KSZ8893MQL/MBL Signal Name	External Processor Signal Description
99	SPIS_N	SPI Slave Select
97	SCL (SPIC)	SPI Clock
98	SDA (SPID)	SPI Data (Master output; Slave input)
96	SPIQ	SPI Data (Master input; Slave output)

Table 15. KSZ8893MQL/MBL SPI Connections

2. Enable SPI slave mode by setting the KSZ8893MQL/MBL strap-in pins PS[1:0] (pins 100 and 101, respectively) to "10".
3. Power up the board and assert reset to the KSZ8893MQL/MBL.
   After reset, the "Start Switch" bit (register 1 bit [0]) is set to '0'.
4. Configure the desired register settings in the KSZ8893MQL/MBL, using the SPI write or multiple write command.
5. Read back and verify the register settings in the KSZ8893MQL/MBL, using the SPI read or multiple read command.
6. Write a '1' to the "Start Switch" bit to start the KSZ8893MQL/MBL with the programmed settings.

Note: The "Start Switch" bit cannot be set to '0' to stop the switch after an '1' is written to this bit. Thus, it is recommended that all switch configuration settings are programmed before the "Start Switch" bit is set to '1'.

Some of the configuration settings, such as "Aging enable", "Auto Negotiation Enable", "Force Speed" and "Power down" can be programmed after the switch has been started.

The following four figures illustrate the SPI data cycles for "Write", "Read", "Multiple Write" and "Multiple Read". The read data is registered out of SPIQ on the falling edge of SPIC, and the data input on SPID is registered on the rising edge of SPIC.

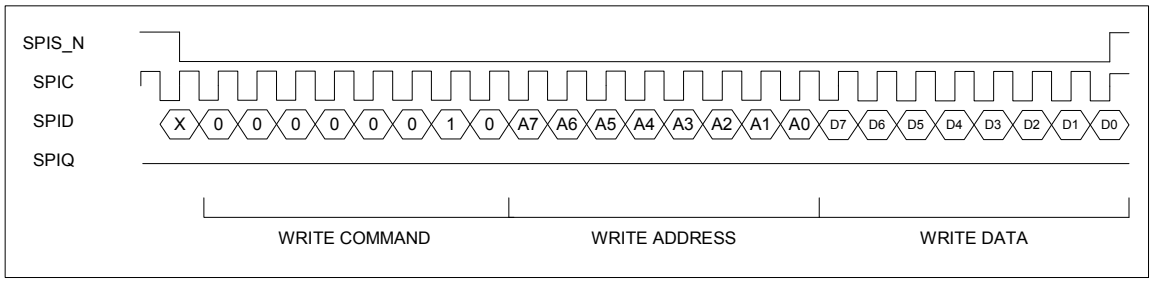


Figure 8. SPI Write Data Cycle

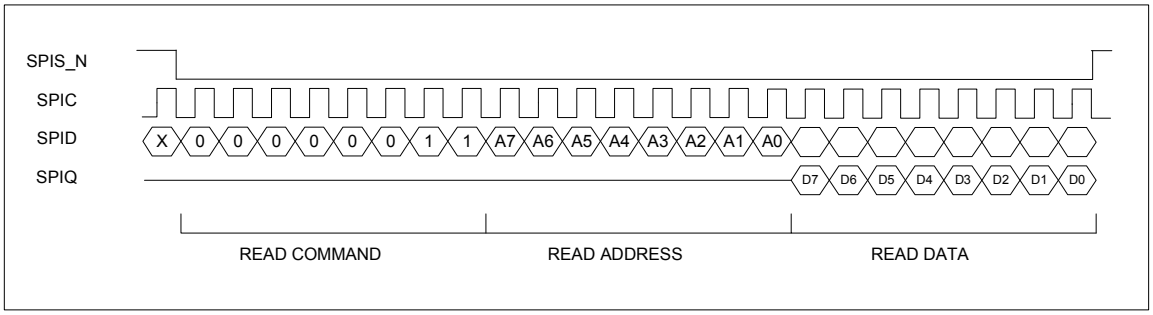


Figure 9. SPI Read Data Cycle

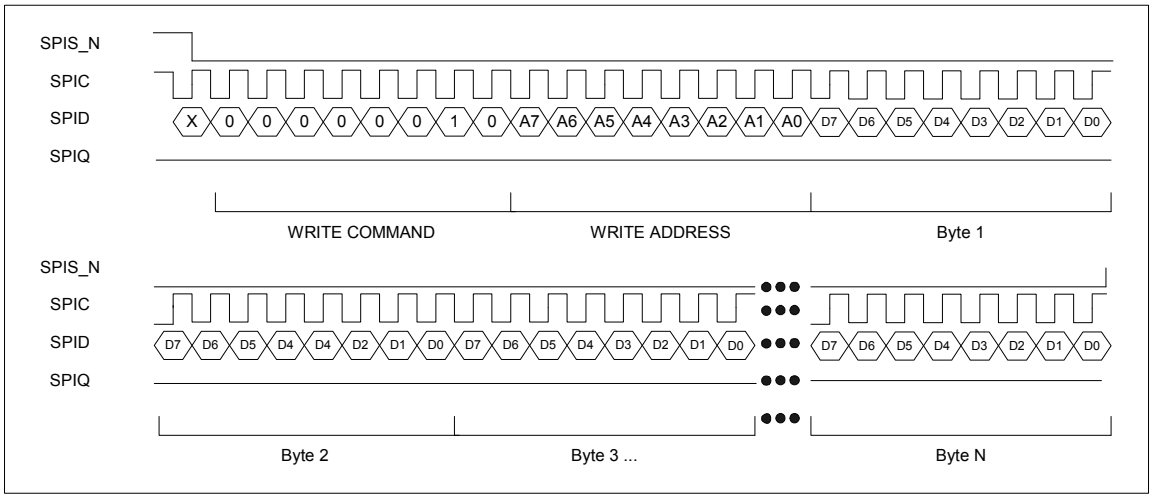


Figure 10. SPI Multiple Write

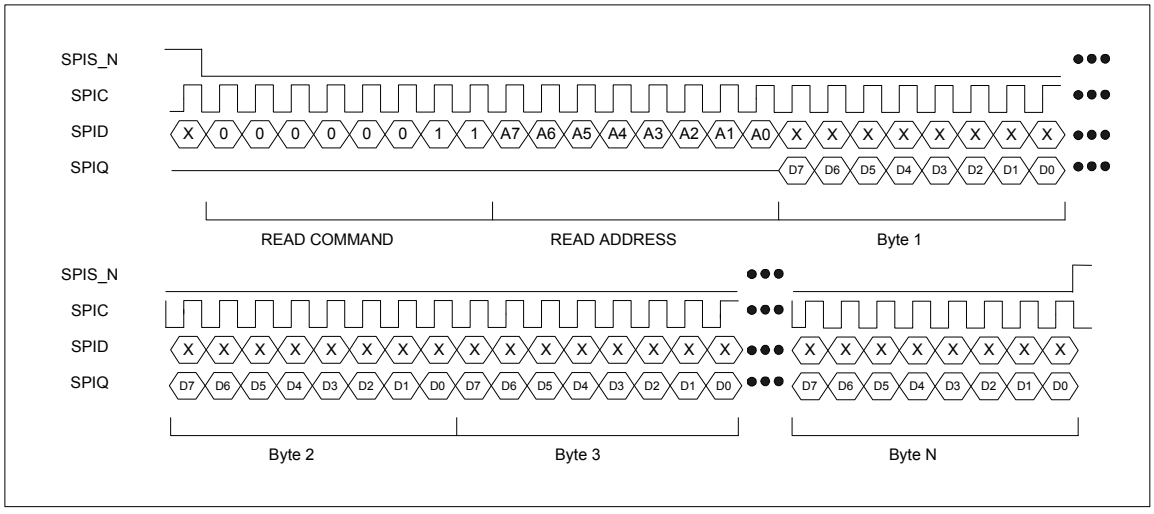


Figure 11. SPI Multiple Read

Loopback Support

The KSZ8893MQL/MBL provides loopback support for remote diagnostic of failure. In loopback mode, the speed at both PHY ports needs to be set to 100BASE-TX. Two types of loopback are supported: Far-end Loopback and Near-end (Remote) Loopback.

Far-end Loopback

Far-end loopback is conducted between the KSZ8893MQL/MBL's two PHY ports. The loopback path starts at the "Originating." PHY port's receive inputs (RXP/RXM), wraps around at the "loopback" PHY port's PMD/PMA, and ends at the "Originating" PHY port's transmit outputs (TXP/TXM).

Bit [0] of registers 29 and 45 is used to enable far-end loopback for ports 1 and 2, respectively. Alternatively, the MII Management register 0, bit [14] can be used to enable far-end loopback.

The far-end loopback path is illustrated in the following figure.

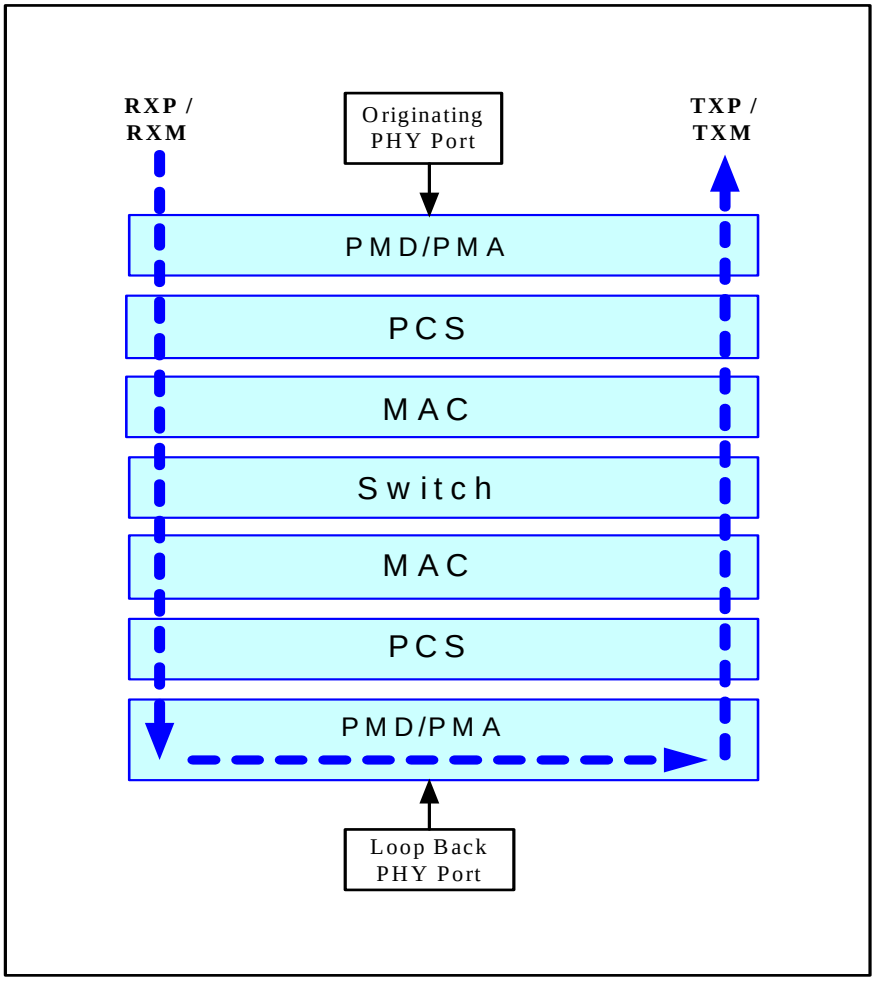


Figure 12: Far-End Loopback Path

Near-end (Remote) Loopback

Near-end (Remote) loopback is conducted at either PHY port 1 or PHY port 2.of the KSZ8893MQL/MBL. The loopback path starts at the PHY port's receive inputs (RXPx/RXMx), wraps around at the same PHY port's PMD/PMA, and ends at the PHY port's transmit outputs (TXPx/TXMx).

Bit [1] of registers 26 and 42 is used to enable near-end loopback for ports 1 and 2, respectively. Alternatively, the MII Management register 31, bit [1] can be used to enable near-end loopback.

The near-end loopback paths are illustrated in the following figure.

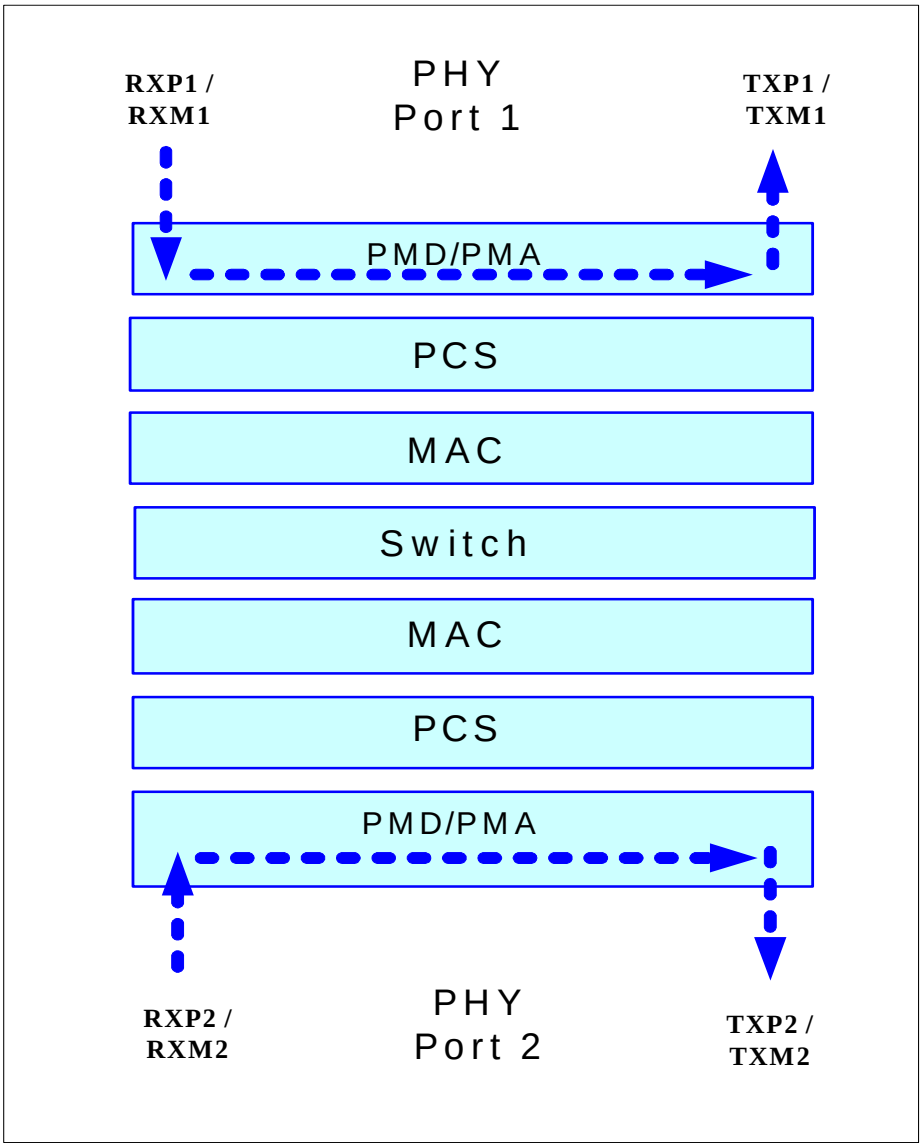


Figure 13. Near-end (Remote) Loopback Path

MII Management (MIIM) Registers

The MIIM interface is used to access the MII PHY registers defined in this section. The SPI, I^2C, and SMI interfaces can also be used to access some of these registers. The latter three interfaces use a different mapping mechanism than the MIIM interface.

The “PHYADs” by defaults are assigned “0x1” for PHY1 (port 1) and “0x2” for PHY2 (port 2). Additionally, these “PHYADs” can be programmed to the PHY addresses specified in bits[7:3] of Register 15 (0x0F): Global Control 13.

The “REGAD” supported are 0x0-0x5, 0x1D and 0x1F.

Register Number	Description
PHYAD = 0x1, REGAD = 0x0	PHY1 Basic Control Register
PHYAD = 0x1, REGAD = 0x1	PHY1 Basic Status Register
PHYAD = 0x1, REGAD = 0x2	PHY1 Physical Identifier I
PHYAD = 0x1, REGAD = 0x3	PHY1 Physical Identifier II
PHYAD = 0x1, REGAD = 0x4	PHY1 Auto-Negotiation Advertisement Register
PHYAD = 0x1, REGAD = 0x5	PHY1 Auto-Negotiation Link Partner Ability Register
PHYAD = 0x1, 0x6 – 0x1C	PHY1 Not supported
PHYAD = 0x1, 0x1D	PHY1 LinkMD Control/Status
PHYAD = 0x1, 0x1E	PHY1 Not supported
PHYAD = 0x1, 0x1F	PHY1 Special Control/Status
PHYAD = 0x2, REGAD = 0x0	PHY2 Basic Control Register
PHYAD = 0x2, REGAD = 0x1	PHY2 Basic Status Register
PHYAD = 0x2, REGAD = 0x2	PHY2 Physical Identifier I
PHYAD = 0x2, REGAD = 0x3	PHY2 Physical Identifier II
PHYAD = 0x2, REGAD = 0x4	PHY2 Auto-Negotiation Advertisement Register
PHYAD = 0x2, REGAD = 0x5	PHY2 Auto-Negotiation Link Partner Ability Register
PHYAD = 0x2, 0x6 – 0x1C	PHY2 Not supported
PHYAD = 0x2, 0x1D	PHY2 LinkMD Control/Status
PHYAD = 0x2, 0x1E	PHY2 Not supported
PHYAD = 0x2, 0x1F	PHY2 Special Control/Status

PHY1 Register 0 (PHYAD = 0x1, REGAD = 0x0): MII Basic Control

PHY2 Register 0 (PHYAD = 0x2, REGAD = 0x0): MII Basic Control

Bit	Name	R/W	Description	Default	Reference
15	Soft reset	RO	NOT SUPPORTED	0	
14	Loopback	R/W	= 1, Perform loopback, as indicated: **Port 1 Loopback (reg. 29, bit 0 = '1')** Start: RXP2/RXM2 (port 2) Loopback: PMD/PMA of port 1's PHY End: TXP2/TXM2 (port 2) **Port 2 Loopback (reg. 45, bit 0 = '1')** Start: RXP1/RXM1 (port 1) Loopback: PMD/PMA of port 2's PHY End: TXP1/TXM1 (port 1) =0, Normal operation	0	Reg. 29, bit 0 Reg. 45, bit 0
13	Force 100	R/W	=1, 100 Mbps =0, 10 Mbps	0	Reg. 28, bit 6 Reg. 44, bit 6
12	AN enable	R/W	=1, Auto-negotiation enabled =0, Auto-negotiation disabled	1	Reg. 28, bit 7 Reg. 44, bit 7
11	Power down	R/W	=1, Power down =0, Normal operation	0	Reg. 29, bit 3 Reg. 45, bit 3
10	Isolate	RO	NOT SUPPORTED	0	
9	Restart AN	R/W	=1, Restart auto-negotiation =0, Normal operation	0	Reg. 29, bit 5 Reg. 45, bit 5
8	Force full duplex	R/W	=1, Full duplex =0, Half duplex	0	Reg. 28, bit 5 Reg. 44, bit 5
7	Collision test	RO	NOT SUPPORTED	0	
6	Reserved	RO		0	
5	Hp_mdix	R/W	1 = HP Auto MDI/MDI-X mode 0 = Micrel Auto MDI/MDI-X mode	1	Reg. 31, bit 7 Reg. 47, bit 7
4	Force MDI	R/W	=1, Force MDI (transmit on RXP / RXM pins) =0, Normal operation (transmit on TXP / TXM pins)	0	Reg. 29, bit 1 Reg. 45, bit 1
3	Disable MDIX	R/W	=1, Disable auto MDI-X =0, Enable auto MDI-X	0	Reg. 29, bit 2 Reg. 45, bit 2
2	Disable far-end fault	R/W	=1, Disable far-end fault detection =0, Normal operation	0	Reg. 29, bit 4
1	Disable transmit	R/W	=1, Disable transmit =0, Normal operation	0	Reg. 29, bit 6 Reg. 45, bit 6
0	Disable LED	R/W	=1, Disable LED =0, Normal operation	0	Reg. 29, bit 7 Reg. 45, bit 7

PHY1 Register 1 (PHYAD = 0x1, REGAD = 0x1): MII Basic Status

PHY2 Register 1 (PHYAD = 0x2, REGAD = 0x1): MII Basic Status

Bit	Name	R/W	Description	Default	Reference
15	T4 capable	RO	=0, Not 100 BASE-T4 capable	0	
14	100 Full capable	RO	=1, 100BASE-TX full duplex capable =0, Not capable of 100BASE-TX full duplex	1	Always 1
13	100 Half capable	RO	=1, 100BASE-TX half duplex capable =0, Not 100BASE-TX half duplex capable	1	Always 1
12	10 Full capable	RO	=1, 10BASE-T full duplex capable =0, Not 10BASE-T full duplex capable	1	Always 1
11	10 Half capable	RO	=1, 10BASE-T half duplex capable =0, Not 10BASE-T half duplex capable	1	Always 1
10-7	Reserved	RO		0000	
6	Preamble suppressed	RO	NOT SUPPORTED	0	
5	AN complete	RO	=1, Auto-negotiation complete =0, Auto-negotiation not completed	0	Reg. 30, bit 6 Reg. 46, bit 6
4	Far-end fault	RO	=1, Far-end fault detected =0, No far-end fault detected	0	Reg. 31, bit 0
3	AN capable	RO	=1, Auto-negotiation capable =0, Not auto-negotiation capable	1	Reg. 28, bit 7 Reg. 44, bit 7
2	Link status	RO	=1, Link is up =0, Link is down	0	Reg. 30, bit 5 Reg. 46, bit 5
1	Jabber test	RO	NOT SUPPORTED	0	
0	Extended capable	RO	=0, Not extended register capable	0	

PHY1 Register 2 (PHYAD = 0x1, REGAD = 0x2): PHYID High

PHY2 Register 2 (PHYAD = 0x2, REGAD = 0x2): PHYID High

Bit	Name	R/W	Description	Default
15-0	PHYID high	RO	High order PHYID bits	0x0022

PHY1 Register 3 (PHYAD = 0x1, REGAD = 0x3): PHYID Low

PHY2 Register 3 (PHYAD = 0x2, REGAD = 0x3): PHYID Low

Bit	Name	R/W	Description	Default
15-0	PHYID low	RO	Low order PHYID bits	0x1430

PHY1 Register 4 (PHYAD = 0x1, REGAD = 0x4): Auto-Negotiation Advertisement Ability

PHY2 Register 4 (PHYAD = 0x2, REGAD = 0x4): Auto-Negotiation Advertisement Ability

Bit	Name	R/W	Description	Default	Reference
15	Next page	RO	NOT SUPPORTED	0	
14	Reserved	RO		0	
13	Remote fault	RO	NOT SUPPORTED	0	
12-11	Reserved	RO		00	
10	Pause	R/W	=1, Advertise pause ability =0, Do not advertise pause ability	1	Reg. 28, bit 4 Reg. 44, bit 4
9	Reserved	R/W		0	
8	Adv 100 Full	R/W	=1, Advertise 100 full duplex ability =0, Do not advertise 100 full duplex ability	1	Reg. 28, bit 3 Reg. 44, bit 3
7	Adv 100 Half	R/W	=1, Advertise 100 half duplex ability =0, Do not advertise 100 half duplex ability	1	Reg. 28, bit 2 Reg. 44, bit 2
6	Adv 10 Full	R/W	=1, Advertise 10 full duplex ability =0, Do not advertise 10 full duplex ability	1	Reg. 28, bit 1 Reg. 44, bit 1
5	Adv 10 Half	R/W	=1, Advertise 10 half duplex ability =0, Do not advertise 10 half duplex ability	1	Reg. 28, bit 0 Reg. 44, bit 0
4-0	Selector field	RO	802.3	00001	

PHY1 Register 5 (PHYAD = 0x1, REGAD = 0x5): Auto-Negotiation Link Partner Ability

PHY2 Register 5 (PHYAD = 0x2, REGAD = 0x5): Auto-Negotiation Link Partner Ability

Bit	Name	R/W	Description	Default	Reference
15	Next page	RO	NOT SUPPORTED	0	
14	LP ACK	RO	NOT SUPPORTED	0	
13	Remote fault	RO	NOT SUPPORTED	0	
12-11	Reserved	RO		00	
10	Pause	RO	Link partner pause capability	0	Reg. 30, bit 4 Reg. 46, bit 4
9	Reserved	RO		0	
8	Adv 100 Full	RO	Link partner 100 full capability	0	Reg. 30, bit 3 Reg. 46, bit 3
7	Adv 100 Half	RO	Link partner 100 half capability	0	Reg. 30, bit 2 Reg. 46, bit 2
6	Adv 10 Full	RO	Link partner 10 full capability	0	Reg. 30, bit 1 Reg. 46, bit 1
5	Adv 10 Half	RO	Link partner 10 half capability	0	Reg. 30, bit 0 Reg. 46, bit 0
4-0	Reserved	RO		00000	

PHY1 Register 29 (PHYAD = 0x1, REGAD = 0x1D): LinkMD Control/Status

PHY2 Register 29 (PHYAD = 0x2, REGAD = 0x1D): LinkMD Control/Status

Bit	Name	R/W	Description	Default	Reference
15	Vct_enable	R/W (SC)	1 = enable cable diagnostic. After VCT test has completed, this bit will be self-cleared. 0 = indicate cable diagnostic test (if enabled) has completed and the status information is valid for read.	0	Reg. 26, bit 4 Reg. 42, bit 4
14-13	Vct_result	RO	00 = normal condition 01 = open condition detected in cable 10 = short condition detected in cable 11 = cable diagnostic test has failed	00	Reg 26, bit[6:5] Reg 42, bit[6:5]
12	Vct 10M Short	RO	1 = Less than 10 meter short	0	Reg. 26, bit 7 Reg. 42, bit 7
11-9	Reserved	RO	Reserved	000	
8-0	Vct_fault_count	RO	Distance to the fault. It's approximately 0.4m*vct_fault_count[8:0]	{0, (0x00)}	{(Reg. 26, bit 0), (Reg. 27, bit[7:0])} {(Reg. 42, bit 0), (Reg. 43, bit[7:0])}

PHY1 Register 31 (PHYAD = 0x1, REGAD = 0x1F): PHY Special Control/Status

PHY2 Register 31 (PHYAD = 0x2, REGAD = 0x1F): PHY Special Control/Status

Bit	Name	R/W	Description	Default	Reference
15-6	Reserved	RO	Reserved	{(0x00),00}	
5	Polrvs	RO	1 = polarity is reversed 0 = polarity is not reversed	0	Reg. 31, bit 5 Reg. 47, bit 5
4	MDI-X status	RO	1 = MDI-X 0 = MDI	0	Reg. 30, bit 7 Reg. 46, bit 7
3	Force_lnk	R/W	1 = Force link pass 0 = Normal Operation	0	Reg. 26, bit 3 Reg. 42, bit 3
2	Pwrsave	R/W	0 = Enable power saving 1 = Disable power saving	1	Reg. 26, bit 2 Reg. 42, bit 2
1	Remote Loopback	R/W	1 = Perform Remote loopback, as follows: **Port 1 (reg. 26, bit 1 = '1')** Start: RXP1/RXM1 (port 1) Loopback: PMD/PMA of port 1's PHY End: TXP1/TXM1 (port 1) **Port 2 (reg. 42, bit 1 = '1')** Start: RXP2/RXM2 (port 2) Loopback: PMD/PMA of port 2's PHY End: TXP2/TXM2 (port 2) 0 = Normal Operation	0	Reg. 26, bit 1 Reg. 42, bit 1
0	Reserved	R/W	Reserved Do not change the default value.	0	

Register Map: Switch & PHY (8-bit registers)

Global Registers

Register (Decimal)	Register (Hex)	Description
0-1	0x00-0x01	Chip ID Registers
2-15	0x02-0x0F	Global Control Registers

Port Registers

Register (Decimal)	Register (Hex)	Description
16-29	0x10-0x1D	Port 1 Control Registers, including MII PHY Registers
30-31	0x1E-0x1F	Port 1 Status Registers, including MII PHY Registers
32-45	0x20-0x2D	Port 2 Control Registers, including MII PHY Registers
46-47	0x2E-0x2F	Port 2 Status Registers, including MII PHY Registers
48-57	0x30-0x39	Port 3 Control Registers
58-62	0x3A-0x3E	Reserved
63	0x3F	Port 3 Status Register
64-95	0x40-0x5F	Reserved

Advanced Control Registers

Register (Decimal)	Register (Hex)	Description
96-111	0x60-0x6F	TOS Priority Control Registers
112-117	0x70-0x75	Switch Engine's MAC Address Registers
118-120	0x76-0x78	User Defined Registers
121-122	0x79-0x7A	Indirect Access Control Registers
123-131	0x7B-0x83	Indirect Data Registers
132	0x84	Digital Testing Status Register
133	0x85	Digital Testing Control Register
134-137	0x86-0x89	Analog Testing Control Registers
138	0x8A	Analog Testing Status Register
139	0x8B	Analog Testing Control Register
140-141	0x8C-0x8D	QM Debug Registers

Global Registers

Register 0 (0x00): Chip ID0

Bit	Name	R/W	Description	Default
7-0	Family ID	RO	Chip family	0x88

Register 1 (0x01): Chip ID1 / Start Switch

Bit	Name	R/W	Description	Default
7-4	Chip ID	RO	0x2 is assigned to M series. (93M)	0x2
3-1	Revision ID	RO	Revision ID	-
0	Start Switch	RW	= 1, start the chip when external pins (PS1, PS0) = (0,1) or (1,0) or (1,1). **Note:** In (PS1, PS0) = (0, 0) mode, the chip will start automatically after trying to read the external EEPROM. If EEPROM does not exist, the chip will use pin strapping and default values for all internal registers. If EEPROM is present, the contents in the EEPROM will be checked. The switch will check: (1) Register 0 = 0x88, (2) Register 1 bits [7:4] = 0x2. If this check is OK, the contents in the EEPROM will override chip registers' default values. = 0, chip will not start when external pins (PS1, PS0) = (0,1) or (1,0) or (1,1).	-

Register 2 (0x02): Global Control 0

Bit	Name	R/W	Description	Default
7	New Back-off Enable	R/W	New back-off algorithm designed for UNH 1 = Enable 0 = Disable	0
6-4	Reserved	R/W	Reserved Do not change the default value.	100
3	Pass Flow Control Packet	R/W	= 1, switch will not filter 802.1x "flow control" packets	0
2	Reserved	R/W	Reserved Do not change the default value.	1
1	Reserved	R/W	Reserved Do not change the default value.	0
0	Link Change Age	R/W	= 1, link change from "link" to "no link" will cause fast aging (<800us) to age address table faster. After an age cycle is complete, the age logic will return to normal aging (about 200 sec). **Note:** If any port is unplugged, all addresses will be automatically aged out.	0

Register 3 (0x03): Global Control 1

Bit	Name	R/W	Description	Default
7	Pass All Frames	R/W	= 1, switch all packets including bad ones. Used solely for debugging purposes. Works in conjunction with sniffer mode only.	0
6	Reserved	R/W	Reserved Do not change the default value.	0
5	IEEE 802.3x Transmit Direction Flow Control Enable	R/W	= 1, will enable transmit direction flow control feature. = 0, will not enable transmit direction flow control feature. Switch will not generate any flow control (PAUSE) frame.	1
4	IEEE 802.3x Receive Direction Flow Control Enable	R/W	= 1, will enable receive direction flow control feature. = 0, will not enable receive direction flow control feature. Switch will not react to any flow control (PAUSE) frame it receives.	1
3	Frame Length Field Check	R/W	1 = will check frame length field in the IEEE packets. If the actual length does not match, the packet will be dropped (for Length/Type field < 1500).	0
2	Aging Enable	R/W	1 = enable age function in the chip 0 = disable age function in the chip	0
1	Fast Age Enable	R/W	1 = turn on fast age (800us)	0
0	Aggressive Back-off Enable	R/W	1 = enable more aggressive back off algorithm in half duplex mode to enhance performance. This is not an IEEE standard.	0

Register 4 (0x04): Global Control 2

Bit	Name	R/W	Description	Default
7	Unicast Port-VLAN Mismatch Discard	R/W	This feature is used with port-VLAN (described in reg. 17, reg. 33, …) = 1, all packets can not cross VLAN boundary = 0, unicast packets (excluding unkown/multicast/ broadcast) can cross VLAN boundary Note: Port mirroring is not supported if this bit is set to “0”.	1
6	Multicast Storm Protection Disable	R/W	= 1, “Broadcast Storm Protection” does not include multicast packets. Only DA = FF-FF-FF-FF-FF-FF packets will be regulated. = 0, “Broadcast Storm Protection” includes DA = FF-FF-FF-FF-FF-FF and DA[40] = 1 packets.	1
5	Back Pressure Mode	R/W	= 1, carrier sense based backpressure is selected = 0, collision based backpressure is selected	1

Register 4 (0x04): Global Control 2 (continued)

Bit	Name	R/W	Description	Default
4	Flow Control and Back Pressure Fair Mode	R/W	= 1, fair mode is selected. In this mode, if a flow control port and a non-flow control port talk to the same destination port, packets from the non-flow control port may be dropped. This is to prevent the flow control port from being flow controlled for an extended period of time. = 0, in this mode, if a flow control port and a non-flow control port talk to the same destination port, the flow control port will be flow controlled. This may not be "fair" to the flow control port.	1
3	No Excessive Collision Drop	R/W	= 1, the switch will not drop packets when 16 or more collisions occur. = 0, the switch will drop packets when 16 or more collisions occur.	0
2	Huge Packet Support	R/W	= 1, will accept packet sizes up to 1916 bytes (inclusive). This bit setting will override setting from bit 1 of this register. = 0, the max packet size will be determined by bit 1 of this register.	0
1	Legal Maximum Packet Size Check Enable	R/W	= 0, will accept packet sizes up to 1536 bytes (inclusive). = 1, 1522 bytes for tagged packets, 1518 bytes for untagged packets. Any packets larger than the specified value will be dropped.	SMRXD0 (pin 85) value during reset
0	Priority Buffer Reserve	R/W	= 1, each port is pre-allocated 48 buffers for high priority (q3, q2, and q1) packets. This selection is effective only when the multiple queue feature is turned on. It is recommended to enable this bit for multiple queue. = 0, no reserved buffers for high priority packets. Each port is pre-allocated 48 buffers for all priority packets (q3, q2,q1, and q0).	1

Register 5 (0x05): Global Control 3

Bit	Name	R/W	Description	Default
7	802.1Q VLAN Enable	R/W	= 1, 802.1Q VLAN mode is turned on. VLAN table needs to set up before the operation. = 0, 802.1Q VLAN is disabled.	0
6	IGMP Snoop Enable on Switch MII Interface	R/W	=1, IGMP snoop is enabled. All IGMP packets will be forwarded to the Switch MII port. =0, IGMP snoop is disabled.	0
5	IPv6 MLD Snooping Enable	R/W	IPv6 MLD snooping 1 = enable 0 = disable	0
4	IPv6 MLD Snooping Option	R/W	IPv6 MLD snooping option 1 = enable 0 = disable	0

Register 5 (0x05): Global Control 3 (continued)

Bit	Name	R/W	Description	Default
3	Weighted Fair Queue Enable	R/W	0 = always transmit higher priority packets first 1 = Weighted Fair Queueing enabled. When all four queues have packets waiting to transmit, the bandwidth allocation is q3:q2:q1:q0 = 8:4:2:1. If any queues are empty, the highest non-empty queue gets one more weighting. For example, if q2 is empty, q3:q2:q1:q0 becomes (8+1):0:2:1.	0
2-1	Reserved	R/W	Reserved Do not change the default values.	00
0	Sniff Mode Select	R/W	= 1, will do RX AND TX sniff (both source port and destination port need to match) = 0, will do RX OR TX sniff (either source port or destination port needs to match). This is the mode used to implement RX only sniff.	0

Register 6 (0x06): Global Control 4

Bit	Name	R/W	Description	Default
7	Repeater Mode	R/W	=1, enable repeater mode =0, disable repeater mode **Note:** For repeater mode, all ports need to be set to 100BASE-TX and half duplex mode. PHY ports need to have auto-negotiation disabled.	0
6	Switch MII Half Duplex Mode	R/W	= 1, enable MII interface half-duplex mode. = 0, enable MII interface full-duplex mode.	Pin SMRXD2 strap option. Pull-down(0): Full-duplex mode Pull-up(1): Half-duplex mode Note: SMRXD2 has internal pull-down.
5	Switch MII Flow Control Enable	R/W	= 1, enable full duplex flow control on Switch MII interface. = 0, disable full duplex flow control on Switch MII interface.	Pin SMRXD3 strap option. Pull-down(0): Disable flow control Pull- up(1): Enable flow control Note: SMRXD3 has internal pull-down.

Register 6 (0x06): Global Control 4 (continued)

Bit	Name	R/W	Description	Default
4	Switch MII 10BT	R/W	= 1, the switch interface is in 10Mbps mode = 0, the switch interface is in 100Mbps mode	Pin SMRXD1 strap option. Pull-down(0): Enable 100Mbps Pull-up(1): Enable 10Mbps Note: SMRXD1 has internal pull-down.
3	Null VID Replacement	R/W	= 1, will replace NULL VID with port VID (12 bits) = 0, no replacement for NULL VID	0
2-0	Broadcast Storm Protection Rate[1] Bit [10:8]	R/W	This register along with the next register determines how many “64 byte blocks” of packet data are allowed on an input port in a preset period. The period is 67ms for 100BT or 500ms for 10BT. The default is 1%.	000

Register 7 (0x07): Global Control 5

Bit	Name	R/W	Description	Default
7-0	Broadcast Storm Protection Rate[1] Bit [7:0]	R/W	This register along with the previous register determines how many “64 byte blocks” of packet data are allowed on an input port in a preset period. The period is 67ms for 100BT or 500ms for 10BT. The default is 1%.	0x63

Note: [1] 100BT Rate: 148,800 frames/sec * 67 ms/interval * 1% = 99 frames/interval (approx.) = 0x63

Register 8 (0x08): Global Control 6

Bit	Name	R/W	Description	Default
7-0	Factory Testing	R/W	Reserved Do not change the default values.	0x00

Register 9 (0x09): Global Control 7

Bit	Name	R/W	Description	Default
7-0	Factory Testing	R/W	Reserved Do not change the default values.	0x24

Register 10 (0x0A): Global Control 8

Bit	Name	R/W	Description	Default
7-0	Factory Testing	R/W	Reserved Do not change the default values.	0x35

Register 11 (0x0B): Global Control 9

Bit	Name	R/W	Description	Default
7	LEDSEL1	R/W	LED mode select See description in bit 1 of this register.	LEDSEL1 (pin 23) value during reset
6-5	Reserved	R/W	Reserved Do not change the default values.	00
4	Reserved	R/W	Testing mode. Set to '0' for normal operation.	0
3-2	Reserved	R/W	Reserved Do not change the default values.	10
1	LEDSEL0	R/W	LED mode select This bit and bit 7 of this register select the LED mode. For LED definitions, see pins 1, 2, 3, 4, 5 and 6 of Pin Description and I/O Assignment listing. Notes: LEDSEL1 is also external strap-in pin #23. LEDSEL0 is also external strap-in pin #70.	LEDSEL0 (pin 70) value during reset
0	Special TPID mode	R/W	Used for direct mode forwarding from port 3. See description in spanning tree functional description. 0 = disable 1 = enable	0

Register 12 (0x0C): Global Control 10

Bit	Name	R/W	Description	Default
7-6	Tag_0x3	R/W	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x3.	01
5-4	Tag_0x2	R/W	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x2.	01
3-2	Tag_0x1	R/W	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x1.	00
1-0	Tag_0x0	R/W	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x0.	00

Register 13 (0x0D): Global Control 11

Bit	Name	R/W	Description	Default
7-6	Tag_0x7	R/W	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x7.	11
5-4	Tag_0x6	R/W	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x6.	11
3-2	Tag_0x5	R/W	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x5.	10
1-0	Tag_0x4	R/W	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x4.	10

Register 14 (0x0E): Global Control 12

Bit	Name	R/W	Description	Default
7	Unknown Packet Default Port Enable	R/W	Send packets with unknown destination MAC addresses to specified port(s) in bits [2:0] of this register. 0 = disable 1 = enable	0
6-3	Reserved	R/W	Reserved Do not change the default values.	0x0
2-0	Unknown Packet Default Port	R/W	Specify which port(s) to send packets with unknown destination MAC addresses. This feature is enabled by bit [7] of this register. Bit 2 stands for port 3. Bit 1 stands for port 2. Bit 0 stands for port 1. An '1' includes a port. An '0' excludes a port.	111

Register 15 (0x0F): Global Control 13

Bit	Name	R/W	Description	Default
7-3	PHY Address	R/W	00000 : N/A 00001 : Port 1 PHY address is 0x1 00010 : Port 1 PHY address is 0x2 … 11101 : Port 1 PHY address is 0x29 11110 : N/A 11111 : N/A Note: Port 2 PHY address = (Port 1 PHY address) + 1	00001
2-0	Reserved	RO	Reserved Do not change the default values.	000

Port Registers

The following registers are used to enable features that are assigned on a per port basis. The register bit

assignments are the same for all ports, but the address for each port is different, as indicated.

Register 16 (0x10): Port 1 Control 0

Register 32 (0x20): Port 2 Control 0

Register 48 (0x30): Port 3 Control 0

Bit	Name	R/W	Description	Default
7	Broadcast Storm Protection Enable	R/W	= 1, enable broadcast storm protection for ingress packets on port = 0, disable broadcast storm protection	0
6	DiffServ Priority Classification Enable	R/W	= 1, enable DiffServ priority classification for ingress packets (IPv4 and IPv6) on port = 0, disable DiffServ function	0
5	802.1p Priority Classification Enable	R/W	= 1, enable 802.1p priority classification for ingress packets on port = 0, disable 802.1p	0
4-3	Port-based Priority Classification	R/W	= 00, ingress packets on port will be classified as priority 0 queue if “Diffserv” or “802.1p” classification is not enabled or fails to classify. = 01, ingress packets on port will be classified as priority 1 queue if “Diffserv” or “802.1p” classification is not enabled or fails to classify. = 10, ingress packets on port will be classified as priority 2 queue if “Diffserv” or “802.1p” classification is not enabled or fails to classify. = 11, ingress packets on port will be classified as priority 3 queue if “Diffserv” or “802.1p” classification is not enabled or fails to classify. Note: “DiffServ”, “802.1p” and port priority can be enabled at the same time. The OR’ed result of 802.1p and DSCP overwrites the port priority.	00
2	Tag Insertion	R/W	= 1, when packets are output on the port, the switch will add 802.1p/q tags to packets without 802.1p/q tags when received. The switch will not add tags to packets already tagged. The tag inserted is the ingress port’s “port VID”. = 0, disable tag insertion	0
1	Tag Removal	R/W	= 1, when packets are output on the port, the switch will remove 802.1p/q tags from packets with 802.1p/q tags when received. The switch will not modify packets received without tags. = 0, disable tag removal	0
0	TX Multiple Queues Select Enable	R/W	= 1, the port output queue is split into four priority queues. = 0, single output queue on the port. There is no priority differentiation even though packets are classified into high or low priority.	0

Register 17 (0x11): Port 1 Control 1

Register 33 (0x21): Port 2 Control 1

Register 49 (0x31): Port 3 Control 1

Bit	Name	R/W	Description	Default
7	Sniffer Port	R/W	= 1, Port is designated as sniffer port and will transmit packets that are monitored. = 0, Port is a normal port	0
6	Receive Sniff	R/W	= 1, All packets received on the port will be marked as “monitored packets” and forwarded to the designated “sniffer port” = 0, no receive monitoring	0
5	Transmit Sniff	R/W	= 1, All packets transmitted on the port will be marked as “monitored packets” and forwarded to the designated “sniffer port” = 0, no transmit monitoring	0
4	Double Tag	R/W	= 1, All packets will be tagged with port default tag of ingress port regardless of the original packets are tagged or not = 0, do not double tagged on all packets	0
3	User Priority Ceiling	R/W	= 1, if the packet’s “user priority field” is greater than the “user priority field” in the port default tag register, replace the packet’s “user priority field” with the “user priority field” in the port default tag register. = 0, do not compare and replace the packet’s ‘user priority field”	0
2-0	Port VLAN membership	R/W	Define the port’s egress port VLAN membership. The port can only communicate within the membership. Bit 2 stands for port 3, bit 1 stands for port 2, bit 0 stands for port 1. An ‘1’ includes a port in the membership. An ‘0’ excludes a port from membership.	111

Register 18 (0x12): Port 1 Control 2

Register 34 (0x22): Port 2 Control 2

Register 50 (0x32): Port 3 Control 2

Bit	Name	R/W	Description	Default
7	Reserved	R/W	Reserved Do not change the default value.	0
6	Ingress VLAN Filtering	R/W	= 1, the switch will discard packets whose VID port membership in VLAN table bits [18:16] does not include the ingress port. = 0, no ingress VLAN filtering.	0
5	Discard non PVID Packets	R/W	= 1, the switch will discard packets whose VID does not match ingress port default VID. = 0, no packets will be discarded	0
4	Force Flow Control	R/W	= 1, will always enable full duplex flow control on the port, regardless of AN result. = 0, full duplex flow control is enabled based on AN result.	Pin value during reset: For port 1, P1FFC pin For port 2, P2FFC pin For port 3, this bit has no meaning. Flow control is set by Reg. 6, bit 5.
3	Back Pressure Enable	R/W	= 1, enable port's half duplex back pressure = 0, disable port's half duplex back pressure	0
2	Transmit Enable	R/W	= 1, enable packet transmission on the port = 0, disable packet transmission on the port	1
1	Receive Enable	R/W	= 1, enable packet reception on the port = 0, disable packet reception on the port	1
0	Learning Disable	R/W	= 1, disable switch address learning capability = 0, enable switch address learning	0

Note: Bits [2:0] are used for spanning tree support.

Register 19 (0x13): Port 1 Control 3

Register 35 (0x23): Port 2 Control 3

Register 51 (0x33): Port 3 Control 3

Bit	Name	R/W	Description	Default
7-0	Default Tag [15:8]	R/W	Port's default tag, containing 7-5 : User priority bits 4 : CFI bit 3-0 : VID[11:8]	0x00

Register 20 (0x14): Port 1 Control 4

Register 36 (0x24): Port 2 Control 4

Register 52 (0x34): Port 3 Control 4

Bit	Name	R/W	Description	Default
7-0	Default Tag [7:0]	R/W	Port's default tag, containing 7-0 : VID[7:0]	0x01

Note: Registers 19 and 20 (and those corresponding to other ports) serve two purposes:

1. Associated with the ingress untagged packets, and used for egress tagging.
2. Default VID for the ingress untagged or null-VID-tagged packets, and used for address lookup.

Register 21 (0x15): Port 1 Control 5

Register 37 (0x25): Port 2 Control 5

Register 53 (0x35): Port 3 Control 5

Bit	Name	R/W	Description	Default
7-4	Reserved	R/W	Reserved Do not change the default values.	0x0
3-2	Limit Mode	R/W	**Ingress Limit Mode** These bits determine what kinds of frames are limited and counted against ingress rate limiting. = 00, limit and count all frames = 01, limit and count Broadcast, Multicast, and flooded unicast frames = 10, limit and count Broadcast and Multicast frames only = 11, limit and count Broadcast frames only	00
1	Count IFG	R/W	**Count IFG bytes** = 1, each frame's minimum inter frame gap (IFG) bytes (12 per frame) are included in Ingress and Egress rate limiting calculations. = 0, IFG bytes are not counted.	0
0	Count Pre	R/W	**Count Preamble bytes** = 1, each frame's preamble bytes (8 per frame) are included in Ingress and Egress rate limiting calculations. = 0, preamble bytes are not counted.	0

Register 22 (0x16): Port 1 Control 6

Register 38 (0x26): Port 2 Control 6

Register 54 (0x36): Port 3 Control 6

Bit	Name	R/W	Description	Default
7-4	Ingress Pri1 Rate	R/W	**Ingress data rate limit for priority 1 frames** Ingress traffic from this priority queue is shaped according to the ingress rate selected below: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10BT, rate settings above 10Mbps are set to the default value 0000 (Not limited).	0x0
3-0	Ingress Pri0 Rate	R/W	**Ingress data rate limit for priority 0 frames** Ingress traffic from this priority queue is shaped according to the ingress rate selected below: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10BT, rate settings above 10Mbps are set to the default value 0000 (Not limited).	0x0

Register 23 (0x17): Port 1 Control 7

Register 39 (0x27): Port 2 Control 7

Register 55 (0x37): Port 3 Control 7

Bit	Name	R/W	Description	Default
7-4	Ingress Pri3 Rate	R/W	**Ingress data rate limit for priority 3 frames** Ingress traffic from this priority queue is shaped according to the ingress rate selected below: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10BT, rate settings above 10Mbps are set to the default value 0000 (Not limited).	0x0
3-0	Ingress Pri2 Rate	R/W	**Ingress data rate limit for priority 2 frames** Ingress traffic from this priority queue is shaped according to the ingress rate selected below: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10BT, rate settings above 10Mbps are set to the default value 0000 (Not limited).	0x0

Register 24 (0x18): Port 1 Control 8

Register 40 (0x28): Port 2 Control 8

Register 56 (0x38): Port 3 Control 8

Bit	Name	R/W	Description	Default
7-4	Egress Pri1 Rate	R/W	**Egress data rate limit for priority 1 frames** Egress traffic from this priority queue is shaped according to the egress rate selected below: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10BT, rate settings above 10Mbps are set to the default value 0000 (Not limited). When TX multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.	0x0
3-0	Egress Pri0 Rate	R/W	**Egress data rate limit for priority 0 frames.** Egress traffic from this priority queue is shaped according to the egress rate selected below: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10BT, rate settings above 10Mbps are set to the default value 0000 (Not limited). When TX multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.	0x0

Register 25 (0x19): Port 1 Control 9

Register 41 (0x29): Port 2 Control 9

Register 57 (0x39): Port 3 Control 9

Bit	Name	R/W	Description	Default
7-4	Egress Pri3 Rate	R/W	**Egress data rate limit for priority 3 frames** Egress traffic from this priority queue is shaped according to the egress rate selected below: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10BT, rate settings above 10Mbps are set to the default value 0000 (Not limited). When TX multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.	0x0
3-0	Egress Pri2 Rate	R/W	**Egress data rate limit for priority 2 frames** Egress traffic from this priority queue is shaped according to the egress rate selected below: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10BT, rate settings above 10Mbps are set to the default value 0000 (Not limited). When TX multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.	0x0

Note: Most of the contents in registers 26-31 and registers 42-47 for ports 1 and 2, respectively, can also be accessed with the MIIM PHY registers.

Register 26 (0x1A): Port 1 PHY Special Control/Status

Register 42 (0x2A): Port 2 PHY Special Control/Status

Register 58 (0x3A): Reserved, not applied to port 3

Bit	Name	R/W	Description	Default
7	Vct 10M Short	RO	1 = Less than 10 meter short	0
6-5	Vct_result	RO	00 = normal condition 01 = open condition detected in cable 10 = short condition detected in cable 11 = cable diagnostic test has failed	00
4	Vct_en	R/W (SC)	= 1, enable cable diagnostic test. After VCT test has completed, this bit will be self-cleared. = 0, indicate cable diagnostic test (if enabled) has completed and the status information is valid for read.	0
3	Force_lnk	R/W	1 = Force link pass 0 = Normal Operation	0
2	Pwrsave	R/W	0 = Enable power saving 1 = Disable power saving	1
1	Remote Loopback	R/W	1 = Perform Remote loopback, as follows: **Port 1 (reg. 26, bit 1 = '1')** Start: RXP1/RXM1 (port 1) Loopback: PMD/PMA of port 1's PHY End: TXP1/TXM1 (port 1) **Port 2 (reg. 42, bit 1 = '1')** Start: RXP2/RXM2 (port 2) Loopback: PMD/PMA of port 2's PHY End: TXP2/TXM2 (port 2) 0 = Normal Operation	0
0	Vct_fault_count[8]	RO	**Bit[8] of VCT fault count** Distance to the fault. It's approximately 0.4m*vct_fault_count[8:0]	0

Register 27 (0x1B): Port 1 LinkMD Result

Register 43 (0x2B): Port 2 LinkMD Result

Register 59 (0x3B): Reserved, not applied to port 3

Bit	Name	R/W	Description	Default
7-0	Vct_fault_count[7:0]	RO	**Bits[7:0] of VCT fault count** Distance to the fault. It's approximately 0.4m*Vct_fault_count[8:0]	0x00

Register 28 (0x1C): Port 1 Control 12

Register 44 (0x2C): Port 2 Control 12

Register 60 (0x3C): Reserved, not applied to port 3

Bit	Name	R/W	Description	Default
7	Auto Negotiation Enable	R/W	= 0, disable auto negotiation; speed and duplex are determined by bits 6 and 5 of this register. = 1, auto negotiation is on	For port 1, P1ANEN pin value during reset. For port 2, P2ANEN pin value during reset
6	Force Speed	R/W	= 1, forced 100BT if AN is disabled (bit 7) = 0, forced 10BT if AN is disabled (bit 7)	For port 1, P1SPD pin value during reset. For port 2, P2SPD pin value during reset.
5	Force Duplex	R/W	= 1, forced full duplex if (1) AN is disabled or (2) AN is enabled but failed. = 0, forced half duplex if (1) AN is disabled or (2) AN is enabled but failed.	For port 1, P1DPX pin value during reset. For port 2, P2DPX pin value during reset.
4	Advertise Flow Control capability	R/W	= 1, advertise flow control (pause) capability = 0, suppress flow control (pause) capability from transmission to link partner	ADVFC pin value during reset.
3	Advertise 100BT Full Duplex Capability	R/W	= 1, advertise 100BT full duplex capability = 0, suppress 100BT full duplex capability from transmission to link partner	1
2	Advertise 100BT Half Duplex Capability	R/W	= 1, advertise 100BT half duplex capability = 0, suppress 100BT half duplex capability from transmission to link partner	1
1	Advertise 10BT Full Duplex Capability	R/W	= 1, advertise 10BT full duplex capability = 0, suppress 10BT full duplex capability from transmission to link partner	1
0	Advertise 10BT Half Duplex Capability	R/W	= 1, advertise 10BT half duplex capability = 0, suppress 10BT half duplex capability from transmission to link partner	1

Register 29 (0x1D): Port 1 Control 13

Register 45 (0x2D): Port 2 Control 13

Register 61 (0x3D): Reserved, not applied to port 3

Bit	Name	R/W	Description	Default
7	LED Off	R/W	= 1, turn off all port's LEDs (LEDx_3, LEDx_2, LEDx_1, LEDx_0, where "x" is the port number). These pins will be driven high if this bit is set to one. = 0, normal operation	0
6	Txdis	R/W	= 1, disable the port's transmitter = 0, normal operation	0
5	Restart AN	R/W	= 1, restart auto-negotiation = 0, normal operation	0
4	Disable Far-end Fault	R/W	= 1, disable far-end fault detection and pattern transmission. = 0, enable far-end fault detection and pattern transmission	0 Note: Only port 1 supports fiber. This bit is applicable to port 1 only.
3	Power Down	R/W	= 1, power down = 0, normal operation	0
2	Disable Auto MDI/MDI-X	R/W	= 1, disable auto MDI/MDI-X function = 0, enable auto MDI/MDI-X function	0 For port 2, P2MDIXDIS pin value during reset.
1	Force MDI	R/W	If auto MDI/MDI-X is disabled, = 1, force PHY into MDI mode (transmit on RXP/RXM pins) = 0, force PHY into MDI-X mode (transmit on TXP/TXM pins)	0 For port 2, P2MDIX pin value during reset.
0	Loopback	R/W	= 1, perform loopback, as indicated: **Port 1 Loopback (reg. 29, bit 0 = '1')** Start: RXP2/RXM2 (port 2) Loopback: PMD/PMA of port 1's PHY End: TXP2/TXM2 (port 2) **Port 2 Loopback (reg. 45, bit 0 = '1')** Start: RXP1/RXM1 (port 1) Loopback: PMD/PMA of port 2's PHY End: TXP1/TXM1 (port 1) = 0, normal operation	0

Register 30 (0x1E): Port 1 Status 0

Register 46 (0x2E): Port 2 Status 0

Register 62 (0x3E): Reserved, not applied to port 3

Bit	Name	R/W	Description	Default
7	MDI-X Status	RO	= 1, MDI-X = 0, MDI	0
6	AN Done	RO	= 1, auto-negotiation completed = 0, auto-negotiation not completed	0
5	Link Good	RO	= 1, link good = 0, link not good	0
4	Partner Flow Control Capability	RO	= 1, link partner flow control (pause) capable = 0, link partner not flow control (pause) capable	0
3	Partner 100BT Full Duplex Capability	RO	= 1, link partner 100BT full duplex capable = 0, link partner not 100BT full duplex capable	0
2	Partner 100BT Half Duplex Capability	RO	= 1, link partner 100BT half duplex capable = 0, link partner not 100BT half duplex capable	0
1	Partner 10BT Full Duplex Capability	RO	= 1, link partner 10BT full duplex capable = 0, link partner not 10BT full duplex capable	0
0	Partner 10BT Half Duplex Capability	RO	= 1, link partner 10BT half duplex capable = 0, link partner not 10BT half duplex capable	0

Register 31 (0x1F): Port 1 Status 1

Register 47 (0x2F): Port 2 Status 1

Register 63 (0x3F): Port 3 Status 1

Bit	Name	R/W	Description	Default
7	Hp_mdix	R/W	1 = HP Auto MDI/MDI-X mode 0 = Micrel Auto MDI/MDI-X mode	1 Note: Only ports 1 and 2 are PHY ports. This bit is not applicable to port 3 (MII).
6	Reserved	RO	Reserved Do not change the default value.	0
5	Polrvs	RO	1 = polarity is reversed 0 = polarity is not reversed	0 Note: Only ports 1 and 2 are PHY ports. This bit is not applicable to port 3 (MII).
4	Transmit Flow Control Enable	RO	1 = transmit flow control feature is active 0 = transmit flow control feature is inactive	0
3	Receive Flow Control Enable	RO	1 = receive flow control feature is active 0 = receive flow control feature is inactive	0

Register 31 (0x1F): Port 1 Status 1 (continued)

Register 47 (0x2F): Port 2 Status 1 (continued)

Register 63 (0x3F): Port 3 Status 1 (continued)

Bit	Name	R/W	Description	Default
2	Operation Speed	RO	1 = link speed is 100Mbps 0 = link speed is 10Mbps	0
1	Operation Duplex	RO	1 = link duplex is full 0 = link duplex is half	0
0	Far-end Fault	RO	= 1, Far-end fault status detected = 0, no Far-end fault status detected	0 Note: Only port 1 supports fiber. This bit is applicable to port 1 only.

Advanced Control Registers

The IPv4/IPv6 TOS Priority Control Registers implement a fully decoded, 128-bit DSCP (Differentiated Services Code Point) register set that is used to determine priority from the ToS (Type of Service) field in the IP header. The most significant 6 bits of the ToS field are fully decoded into 64 possibilities, and the singular code that results is compared against the corresponding bits in the DSCP register to determine the priority.

Register 96 (0x60): TOS Priority Control Register 0

Bit	Name	R/W	Description	Default
7-6	DSCP[7:6]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x0C.	00
5-4	DSCP[5:4]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x08.	00
3-2	DSCP[3:2]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x04.	00
1-0	DSCP[1:0]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x00.	00

Register 97 (0x61): TOS Priority Control Register 1

Bit	Name	R/W	Description	Default
7-6	DSCP[15:14]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x1C.	00
5-4	DSCP[13:12]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x18.	00
3-2	DSCP[11:10]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x14.	00
1-0	DSCP[9:8]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x10.	00

Register 98 (0x62): TOS Priority Control Register 2

Bit	Name	R/W	Description	Default
7-6	DSCP[23:22]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x2C.	00
5-4	DSCP[21:20]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x28.	00
3-2	DSCP[19:18]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x24.	00
1-0	DSCP[17:16]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x20.	00

Register 99 (0x63): TOS Priority Control Register 3

Bit	Name	R/W	Description	Default
7-6	DSCP[31:30]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x3C.	00
5-4	DSCP[29:28]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x38.	00
3-2	DSCP[27:26]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x34.	00
1-0	DSCP[25:24]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x30.	00

Register 100 (0x64): TOS Priority Control Register 4

Bit	Name	R/W	Description	Default
7-6	DSCP[39:38]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x4C.	00
5-4	DSCP[37:36]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x48.	00
3-2	DSCP[35:34]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x44.	00
1-0	DSCP[33:32]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x40.	00

Register 101 (0x65): TOS Priority Control Register 5

Bit	Name	R/W	Description	Default
7-6	DSCP[47:46]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x5C.	00
5-4	DSCP[45:44]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x58.	00
3-2	DSCP[43:42]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x54.	00
1-0	DSCP[41:40]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x50.	00

Register 102 (0x66): TOS Priority Control Register 6

Bit	Name	R/W	Description	Default
7-6	DSCP[55:54]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x6C.	00
5-4	DSCP[53:52]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x68.	00
3-2	DSCP[51:50]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x64.	00
1-0	DSCP[49:48]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x60.	00

Register 103 (0x67): TOS Priority Control Register 7

Bit	Name	R/W	Description	Default
7-6	DSCP[63:62]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x7C.	00
5-4	DSCP[61:60]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x78.	00
3-2	DSCP[59:58]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x74.	00
1-0	DSCP[57:56]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x70.	00

Register 104 (0x68): TOS Priority Control Register 8

Bit	Name	R/W	Description	Default
7-6	DSCP[71:70]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x8C.	00
5-4	DSCP[69:68]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x88.	00
3-2	DSCP[67:66]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x84.	00
1-0	DSCP[65:64]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x80.	00

Register 105 (0x69): TOS Priority Control Register 9

Bit	Name	R/W	Description	Default
7-6	DSCP[79:78]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x9C.	00
5-4	DSCP[77:76]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x98.	00
3-2	DSCP[75:74]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x94.	00
1-0	DSCP[73:72]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x90.	00

Register 106 (0x6A): TOS Priority Control Register 10

Bit	Name	R/W	Description	Default
7-6	DSCP[87:86]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xAC.	00
5-4	DSCP[85:84]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xA8.	00
3-2	DSCP[83:82]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xA4.	00
1-0	DSCP[81:80]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xA0.	00

Register 107 (0x6B): TOS Priority Control Register 11

Bit	Name	R/W	Description	Default
7-6	DSCP[95:94]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xBC.	00
5-4	DSCP[93:92]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xB8.	00
3-2	DSCP[91:90]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xB4.	00
1-0	DSCP[89:88]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xB0.	00

Register 108 (0x6C): TOS Priority Control Register 12

Bit	Name	R/W	Description	Default
7-6	DSCP[103:102]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xCC.	00
5-4	DSCP[101:100]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xC8.	00
3-2	DSCP[99:98]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xC4.	00
1-0	DSCP[97:96]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xC0.	00

Register 109 (0x6D): TOS Priority Control Register 13

Bit	Name	R/W	Description	Default
7-6	DSCP[111:110]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xDC.	00
5-4	DSCP[109:108]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xD8.	00
3-2	DSCP[107:106]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xD4.	00
1-0	DSCP[105:104]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xD0.	00

Register 110 (0x6E): TOS Priority Control Register 14

Bit	Name	R/W	Description	Default
7-6	DSCP[119:118]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xEC.	00
5-4	DSCP[117:116]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xE8.	00
3-2	DSCP[115:114]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xE4.	00
1-0	DSCP[113:112]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xE0.	00

Register 111 (0x6F): TOS Priority Control Register 15

Bit	Name	R/W	Description	Default
7-6	DSCP[127:126]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xFC.	00
5-4	DSCP[125:124]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xF8.	00
3-2	DSCP[123:122]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xF4.	00
1-0	DSCP[121:120]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xF0.	00

Registers 112 to 117

Registers 112 to 117 contain the switch engine's MAC address. This 48-bit address is used as the Source Address for the MAC's full duplex flow control (PAUSE) frame.

Register 112 (0x70): MAC Address Register 0

Bit	Name	R/W	Description	Default
7-0	MACA[47:40]	R/W		0x00

Register 113 (0x71): MAC Address Register 1

Bit	Name	R/W	Description	Default
7-0	MACA[39:32]	R/W		0x10

Register 114 (0x72): MAC Address Register 2

Bit	Name	R/W	Description	Default
7-0	MACA[31:24]	R/W		0xA1

Register 115 (0x73): MAC Address Register 3

Bit	Name	R/W	Description	Default
7-0	MACA[23:16]	R/W		0xFF

Register 116 (0x74): MAC Address Register 4

Bit	Name	R/W	Description	Default
7-0	MACA[15:8]	R/W		0xFF

Register 117 (0x75): MAC Address Register 5

Bit	Name	R/W	Description	Default
7-0	MACA[7:0]	R/W		0xFF

Registers 118 to 120

Registers 118 to 120 are User Defined Registers (UDRs). These are general purpose read/write registers that can be used to pass user defined control and status information between the KSZ8893MQL/MBL and the external processor.

Register 118 (0x76): User Defined Register 1

Bit	Name	R/W	Description	Default
7-0	UDR1	R/W		0x00

Register 119 (0x77): User Defined Register 2

Bit	Name	R/W	Description	Default
7-0	UDR2	R/W		0x00

Register 120 (0x78): User Defined Register 3

Bit	Name	R/W	Description	Default
7-0	UDR3	R/W		0x00

Registers 121 to 131

Registers 121 to 131 provide read and write access to the static MAC address table, VLAN table, dynamic MAC address table, and MIB counters.

Register 121 (0x79): Indirect Access Control 0

Bit	Name	R/W	Description	Default
7-5	Reserved	R/W	Reserved Do not change the default values.	000
4	Read High / Write Low	R/W	= 1, read cycle = 0, write cycle	0
3-2	Table Select	R/W	00 = static MAC address table selected 01 = VLAN table selected 10 = dynamic MAC address table selected 11 = MIB counter selected	00
1-0	Indirect Address High	R/W	Bits [9:8] of indirect address	00

Register 122 (0x7A): Indirect Access Control 1

Bit	Name	R/W	Description	Default
7-0	Indirect Address Low	R/W	Bits [7:0] of indirect address	0000_0000

Note: A write to register 122 triggers the read/write command. Read or write access is determined by register 121 bit 4.

Register 123 (0x7B): Indirect Data Register 8

Bit	Name	R/W	Description	Default
7	CPU Read Status	RO	This bit is applicable only for dynamic MAC address table and MIB counter reads. = 1, read is still in progress = 0, read has completed	0
6-3	Reserved	RO	Reserved	0000
2-0	Indirect Data [66:64]	RO	Bits [66:64] of indirect data	000

Register 124 (0x7C): Indirect Data Register 7

Bit	Name	R/W	Description	Default
7-0	Indirect Data [63:56]	R/W	Bits [63:56] of indirect data	0000_0000

Register 125 (0x7D): Indirect Data Register 6

Bit	Name	R/W	Description	Default
7-0	Indirect Data [55:48]	R/W	Bits [55:48] of indirect data	0000_0000

Register 126 (0x7E): Indirect Data Register 5

Bit	Name	R/W	Description	Default
7-0	Indirect Data [47:40]	R/W	Bits [47:40] of indirect data	0000_0000

Register 127 (0x7F): Indirect Data Register 4

Bit	Name	R/W	Description	Default
7-0	Indirect Data [39:32]	R/W	Bits [39:32] of indirect data	0000_0000

Register 128 (0x80): Indirect Data Register 3

Bit	Name	R/W	Description	Default
7-0	Indirect Data [31:24]	R/W	Bits [31:24] of indirect data	0000_0000

Register 129 (0x81): Indirect Data Register 2

Bit	Name	R/W	Description	Default
7-0	Indirect Data [23:16]	R/W	Bits [23:16] of indirect data	0000_0000

Register 130 (0x82): Indirect Data Register 1

Bit	Name	R/W	Description	Default
7-0	Indirect Data [15:8]	R/W	Bits [15:8] of indirect data	0000_0000

Register 131 (0x83): Indirect Data Register 0

Bit	Name	R/W	Description	Default
7-0	Indirect Data [7:0]	R/W	Bits [7:0] of indirect data	0000_0000

Registers 132 to 141

Reserved registers 132 to 141 are used by Micrel for internal testing only. Do not change the values of these registers.

Register 132 (0x84): Digital Testing Status 0

Bit	Name	R/W	Description	Default
7-3	Reserved	RO	Factory testing	00000
2-0	Om_split Status	RO	Factory testing	000

Register 133 (0x85): Digital Testing Control 0

Bit	Name	R/W	Description	Default
7-0	Reserved	R/W	Factory testing Dbg[7:0]	0x3F

Register 134 (0x86): Analog Testing Control 0

Bit	Name	R/W	Description	Default
7-0	Reserved	R/W	Factory testing (dgt_actl0)	0x00

Register 135 (0x87): Analog Testing Control 1

Bit	Name	R/W	Description	Default
7-0	Reserved	R/W	Factory testing (dgt_actl1)	0x00

Register 136 (0x88): Analog Testing Control 2

Bit	Name	R/W	Description	Default
7-0	Reserved	R/W	Factory testing (dgt_actl2)	0x00

Register 137 (0x89): Analog Testing Control 3

Bit	Name	R/W	Description	Default
7-0	Reserved	R/W	Factory testing (dgt_actl3)	0x00

Register 138 (0x8A): Analog Testing Status

Bit	Name	R/W	Description	Default
7-0	Reserved	RO	Factory testing	0x00

Register 139 (0x8B): Analog Testing Control 4

Bit	Name	R/W	Description	Default
7-0	Reserved	R/W	Factory testing (dgt_actl4)	0x40

Register 140 (0x8C): QM Debug 1

Bit	Name	R/W	Description	Default
7-0	Reserved	RO	Factory testing QM_Debug bit[7:0]	0x00

Register 141 (0x8D): QM Debug 2

Bit	Name	R/W	Description	Default
7-1	Reserved	RO	Reserved Do not change the default values.	0000_000
0	Reserved	RO	Factory testing QM_Debug bit[8]	0

Static MAC Address Table

The KSZ8893MQL/MBL supports both a static and a dynamic MAC address table. In response to a Destination Address (DA) look up, the KSZ8893MQL/MBL searches both tables to make a packet forwarding decision. In response to a Source Address (SA) look up, only the dynamic table is searched for aging, migration and learning purposes.

The static DA look up result takes precedence over the dynamic DA look up result. If there is a DA match in both tables, the result from the static table is used. The entries in the static table will not be aged out by the KSZ8893MQL/MBL.

The static table is accessed by a external processor via the SMI, SPI or I^2C interfaces. The external processor performs all addition, modification and deletion of static MAC table entries.

Bit	Name	R/W	Description	Default
57-54	FID	R/W	Filter VLAN ID – identifies one of the 16 active VLANs	0000
53	Use FID	R/W	= 1, use (FID+MAC) for static table look ups = 0, use MAC only for static table look ups	0
52	Override	R/W	= 1, override port setting “transmit enable=0” or “receive enable=0” setting = 0, no override	0
51	Valid	R/W	= 1, this entry is valid, the lookup result will be used = 0, this entry is not valid	0
50-48	Forwarding Ports	R/W	These 3 bits control the forwarding port(s): 001, forward to port 1 010, forward to port 2 100, forward to port 3 011, forward to port 1 and port 2 110, forward to port 2 and port 3 101, forward to port 1 and port 3 111, broadcasting (excluding the ingress port)	000
47-0	MAC Address	R/W	48-bit MAC Address	0x0000_0000_0000

Table 16. Format of Static MAC Table (8 Entries)

Examples:

1. Static Address Table Read (Read the 2nd Entry)

Write to reg. 121 (0x79) with 0x10 // Read static table selected
Write to reg. 122 (0x7A) with 0x01 // Trigger the read operation

Then,

Read reg. 124 (0x7C), static table bits [57:56]
Read reg. 125 (0x7D), static table bits [55:48]
Read reg. 126 (0x7E), static table bits [47:40]
Read reg. 127 (0x7F), static table bits [39:32]
Read reg. 128 (0x80), static table bits [31:24]
Read reg. 129 (0x81), static table bits [23:16]
Read reg. 130 (0x82), static table bits [15:8]
Read reg. 131 (0x83), static table bits [7:0]

2. Static Address Table Write (Write the 8th Entry)

Write to reg. 124 (0x7C), static table bits [57:56]
Write to reg. 125 (0x7D), static table bits [55:48]
Write to reg. 126 (0x7E), static table bits [47:40]
Write to reg. 127 (0x7F), static table bits [39:32]
Write to reg. 128 (0x80), static table bits [31:24]
Write to reg. 129 (0x81), static table bits [23:16]
Write to reg. 130 (0x82), static table bits [15:8]
Write to reg. 131 (0x83), static table bits [7:0]
Write to reg. 121 (0x79) with 0x00 // Write static table selected
Write to reg. 122 (0x7A) with 0x07 // Trigger the write operation

VLAN Table

The KSZ8893MQL/MBL uses the VLAN table to perform look ups. If 802.1Q VLAN mode is enabled (register 5, bit 7 = 1), this table will be used to retrieve the VLAN information that is associated with the ingress packet. This information includes FID (filter ID), VID (VLAN ID), and VLAN membership as described in the following table.

Bit	Name	R/W	Description	Default
19	Valid	R/W	= 1, entry is valid = 0, entry is invalid	1
18-16	Membership	R/W	Specify which ports are members of the VLAN. If a DA lookup fails (no match in both static and dynamic tables), the packet associated with this VLAN will be forwarded to ports specified in this field. For example, 101 means port 3 and 1 are in this VLAN.	111
15-12	FID	R/W	Filter ID. KSZ8893MQL/MBL supports 16 active VLANs represented by these four bit fields. FID is the mapped ID. If 802.1Q VLAN is enabled, the look up will be based on FID+DA and FID+SA.	0x0
11-0	VID	R/W	IEEE 802.1Q 12 bits VLAN ID	0x001

Table 17. Format of Static VLAN Table (16 Entries)

If 802.1Q VLAN mode is enabled, KSZ8893MQL/MBL will assign a VID to every ingress packet. If the packet is untagged or tagged with a null VID, the packet is assigned with the default port VID of the ingress port. If the packet is tagged with non null VID, the VID in the tag will be used. The look up process will start from the VLAN table look up. If the VID is not valid, the packet will be dropped and no address learning will take place. If the VID is valid, the FID is retrieved. The FID+DA and FID+SA lookups are performed. The FID+DA look up determines the forwarding ports. If FID+DA fails, the packet will be broadcast to all the members (excluding the ingress port) of the VLAN. If FID+SA fails, the FID+SA will be learned.

Examples:

1. VLAN Table Read (read the 3rd entry)

Write to reg. 121 (0x79) with 0x14 // Read VLAN table selected
Write to reg. 122 (0x7A) with 0x02 // Trigger the read operation

Then,

Read reg. 129 (0x81), VLAN table bits [19:16]
Read reg. 130 (0x82), VLAN table bits [15:8]
Read reg. 131 (0x83), VLAN table bits [7:0]

2. VLAN Table Write (write the 7th entry)

Write to reg. 129 (0x81), VLAN table bits [19:16]
Write to reg. 130 (0x82), VLAN table bits [15:8]
Write to reg. 131 (0x83), VLAN table bits [7:0]
Write to reg. 121 (0x79) with 0x04 // Write VLAN table selected
Write to reg. 122 (0x7A) with 0x06 // Trigger the write operation

Dynamic MAC Address Table

The KSZ8893MQL/MBL maintains the dynamic MAC address table. Read access is allowed only.

Bit	Name	R/W	Description	Default
71	Data Not Ready	RO	= 1, entry is not ready, continue retrying until this bit is set to 0 = 0, entry is ready	
70-67	Reserved	RO	Reserved	
66	MAC Empty	RO	= 1, there is no valid entry in the table = 0, there are valid entries in the table	1
65-56	No of Valid Entries	RO	Indicates how many valid entries in the table 0x3ff means 1K entries 0x001 means 2 entries 0x000 and bit 66 = 0 means 1 entry 0x000 and bit 66 = 1 means 0 entry	00_0000_0000
55-54	Time Stamp	RO	2 bits counter for internal aging	
53-52	Source Port	RO	The source port where FID+MAC is learned 00 : port 1 01 : port 2 10 : port 3	00
51-48	FID	RO	Filter ID	0x0
47-0	MAC Address	RO	48-bit MAC Address	0x0000_0000_0000

Table 18. Format of Dynamic MAC Address Table (1K Entries)

Example:

Dynamic MAC Address Table Read (read the 1st entry and retrieve the MAC table size)

Write to reg. 121 (0x79) with 0x18 // Read dynamic table selected
Write to reg. 122 (0x7A) with 0x00 // Trigger the read operation

Then,

Read reg. 123 (0x7B), bit [7] // if bit 7 = 1, restart (reread) from this register
dynamic table bits [66:64]
Read reg. 124 (0x7C), dynamic table bits [63:56]
Read reg. 125 (0x7D), dynamic table bits [55:48]
Read reg. 126 (0x7E), dynamic table bits [47:40]
Read reg. 127 (0x7F), dynamic table bits [39:32]
Read reg. 128 (0x80), dynamic table bits [31:24]
Read reg. 129 (0x81), dynamic table bits [23:16]
Read reg. 130 (0x82), dynamic table bits [15:8]
Read reg. 131 (0x83), dynamic table bits [7:0]

MIB (Management Information Base) Counters

The KSZ8893MQL/MBL provides 34 MIB counters per port. These counters are used to monitor the port activity for network management. The MIB counters have two format groups: “Per Port” and “All Port Dropped Packet.”

Bit	Name	R/W	Description	Default
31	Overflow	RO	= 1, counter overflow = 0, no counter overflow	0
30	Count valid	RO	= 1, counter value is valid = 0, counter value is not valid	0
29-0	Counter values	RO	Counter value	0

Table 19. Format of “Per Port” MIB Counters

“Per Port” MIB counters are read using indirect memory access. The base address offsets and address ranges for all three ports are:

Port 1, base is 0x00 and range is (0x00-0x1f)
Port 2, base is 0x20 and range is (0x20-0x3f)
Port 3, base is 0x40 and range is (0x40-0x5f)

Port 1 MIB counters are read using the indirect memory offsets in the following table.

Offset	Counter Name	Description
0x0	RxLoPriorityByte	Rx lo-priority (default) octet count including bad packets
0x1	RxHiPriorityByte	Rx hi-priority octet count including bad packets
0x2	RxUndersizePkt	Rx undersize packets w/ good CRC
0x3	RxFragments	Rx fragment packets w/ bad CRC, symbol errors or alignment errors
0x4	RxOversize	Rx oversize packets w/ good CRC (max: 1536 or 1522 bytes)
0x5	RxJabbers	Rx packets longer than 1522 bytes w/ either CRC errors, alignment errors, or symbol errors (depends on max packet size setting)
0x6	RxSymbolError	Rx packets w/ invalid data symbol and legal packet size.
0x7	RxCRCError	Rx packets within (64,1522) bytes w/ an integral number of bytes and a bad CRC (upper limit depends on max packet size setting)
0x8	RxAlignmentError	Rx packets within (64,1522) bytes w/ a non-integral number of bytes and a bad CRC (upper limit depends on max packet size setting)
0x9	RxControl8808Pkts	Number of MAC control frames received by a port with 88-08h in EtherType field
0xA	RxPausePkts	Number of PAUSE frames received by a port. PAUSE frame is qualified with EtherType (88-08h), DA, control opcode (00-01), data length (64B min), and a valid CRC
0xB	RxBroadcast	Rx good broadcast packets (not including error broadcast packets or valid multicast packets)
0xC	RxMulticast	Rx good multicast packets (not including MAC control frames, error multicast packets or valid broadcast packets)
0xD	RxUnicast	Rx good unicast packets
0xE	Rx64Octets	Total Rx packets (bad packets included) that were 64 octets in length
0xF	Rx65to127Octets	Total Rx packets (bad packets included) that are between 65 and 127 octets in length
0x10	Rx128to255Octets	Total Rx packets (bad packets included) that are between 128 and 255 octets in length
0x11	Rx256to511Octets	Total Rx packets (bad packets included) that are between 256 and 511 octets in length
0x12	Rx512to1023Octets	Total Rx packets (bad packets included) that are between 512 and 1023 octets in length

Offset	Counter Name	Description
0x13	Rx1024to1522Octets	Total Rx packets (bad packets included) that are between 1024 and 1522 octets in length (upper limit depends on max packet size setting)
0x14	TxLoPriorityByte	Tx lo-priority good octet count, including PAUSE packets
0x15	TxHiPriorityByte	Tx hi-priority good octet count, including PAUSE packets
0x16	TxLateCollision	The number of times a collision is detected later than 512 bit-times into the Tx of a packet
0x17	TxPausePkts	Number of PAUSE frames transmitted by a port
0x18	TxBroadcastPkts	Tx good broadcast packets (not including error broadcast or valid multicast packets)
0x19	TxMulticastPkts	Tx good multicast packets (not including error multicast packets or valid broadcast packets)
0x1A	TxUnicastPkts	Tx good unicast packets
0x1B	TxDeferred	Tx packets by a port for which the 1st Tx attempt is delayed due to the busy medium
0x1C	TxTotalCollision	Tx total collision, half duplex only
0x1D	TxExcessiveCollision	A count of frames for which Tx fails due to excessive collisions
0x1E	TxSingleCollision	Successfully Tx frames on a port for which Tx is inhibited by exactly one collision
0x1F	TxMultipleCollision	Successfully Tx frames on a port for which Tx is inhibited by more than one collision

Table 20. Port 1's "Per Port" MIB Counters Indirect Memory Offsets

Bit	Name	R/W	Description	Default
30-16	Reserved	N/A	Reserved	N/A
15-0	Counter Value	RO	Counter Value	0

Table 21. Format of "All Port Dropped Packet" MIB Counters

"All Port Dropped Packet" MIB counters are read using indirect memory access. The address offsets for these counters are shown in the following table:

Offset	Counter Name	Description
0x100	Port1 TX Drop Packets	TX packets dropped due to lack of resources
0x101	Port2 TX Drop Packets	TX packets dropped due to lack of resources
0x102	Port3 TX Drop Packets	TX packets dropped due to lack of resources
0x103	Port1 RX Drop Packets	RX packets dropped due to lack of resources
0x104	Port2 RX Drop Packets	RX packets dropped due to lack of resources
0x105	Port3 RX Drop Packets	RX packets dropped due to lack of resources

Table 22. "All Port Dropped Packet" MIB Counters Indirect Memory Offsets

Examples:

1. MIB Counter Read (Read port 1 "Rx64Octets" Counter)

Write to reg. 121 (0x79) with 0x1c // Read MIB counters selected
Write to reg. 122 (0x7A) with 0x0e // Trigger the read operation

Then

```
Read reg. 128 (0x80), overflow bit [31]      // If bit 31 = 1, there was a counter overflow
                      valid bit [30]         // If bit 30 = 0, restart (reread) from this register
                      counter bits [29:24]
Read reg. 129 (0x81), counter bits [23:16]
Read reg. 130 (0x82), counter bits [15:8]
Read reg. 131 (0x83), counter bits [7:0]
```

2. MIB Counter Read (Read port 2 “Rx64Octets” Counter)

```
Write to reg. 121 (0x79) with 0x1c      // Read MIB counter selected
Write to reg. 122 (0x7A) with 0x2e      // Trigger the read operation
```

Then,

```
Read reg. 128 (0x80), overflow bit [31]      // If bit 31 = 1, there was a counter overflow
                      valid bit [30]         // If bit 30 = 0, restart (reread) from this register
                      counter bits [29:24]
Read reg. 129 (0x81), counter bits [23:16]
Read reg. 130 (0x82), counter bits [15:8]
Read reg. 131 (0x83), counter bits [7:0]
```

3. MIB Counter Read (Read “Port1 TX Drop Packets” Counter)

```
Write to reg. 121 (0x79) with 0x1d      // Read MIB counter selected
Write to reg. 122 (0x7A) with 0x00      // Trigger the read operation
```

Then

```
Read reg. 130 (0x82), counter bits [15:8]
Read reg. 131 (0x83), counter bits [7:0]
```

Additional MIB Counter Information

“Per Port” MIB counters are designed as “read clear.” These counters will be cleared after they are read.

“All Port Dropped Packet” MIB counters are not cleared after they are accessed and do not indicate overflow or validity; therefore, the application must keep track of overflow and valid conditions.

To read out all the counters, the best performance over the SPI bus is (160+3)*8*200 = 260ms, where there are 160 registers, 3 overheads, 8 clocks per access, at 5MHz. In the heaviest condition, the counters will overflow in 2 minutes. It is recommended that the software read all the counters at least every 30 seconds.

A high performance SPI master is also recommended to prevent counters overflow.

Absolute Maximum Ratings[1]

Supply Voltage
(V_{DDATX}, V_{DDARX}, V_{DDIO}) ..... –0.5V to +4.0V
Input Voltage (all inputs). ..... –0.5V to +5.0V
Output Voltage (all outputs) ..... –0.5V to +4.0V
Lead Temperature (soldering, 10sec.) ..... 270°C
Storage Temperature (T_s) ..... –55°C to +150°C

Operating Ratings[2]

Supply Voltage
(V_{DDATX}, V_{DDARX}, V_{DDIO}) ..... +3.1V to +3.5V
Ambient Temp. of MQL(T_A) ..... 0°C to +70°C
Ambient Temp. of MQLI/MBL AM(T_A) -40°C to +85°C
Junction Temp. (T_J) ..... 125°C
Package Thermal Resistance[3]
PQFP (θ_{JA}) No Air Flow ..... 42.91°C/W
PQFP (θ_{JC}) No Air Flow ..... 19.6°C/W
LFBGA (θ_{JA}) No Air Flow ..... 38.50°C/W
LFBGA (θ_{JC}) No Air Flow ..... 12.50°C/W

Electrical Characteristics[1]

Parameter	Symbol	Condition	Min	Typ	Max
Supply Current - Current consumption is for the single 3.3V supply KSZ8893MQL/MBL device only, and includes the 1.2V supply voltages (VDDA, VDDAP, VDDC) that are provided by the KSZ8893MQL/MBL via power output pin 22. - Each PHY port's transformer consumes an additional 45mA @ 3.3V for 100BASE-TX and 70mA @ 3.3V for 10BASE-T.					
	100BASE-TX Operation (All Ports @ 100% Utilization)				
100BASE-TX (transceiver + digital I/O)	I_{ddxio}	VDDATX, VDDARX, VDDIO = 3.3V		120mA	
	10BASE-T Operation (All Ports @ 100% Utilization)				
10BASE-T (transceiver + digital I/O)	I_{ddxio}	VDDATX, VDDARX, VDDIO = 3.3V		90mA	
TTL Inputs					
Input High Voltage	V_{ih}		2.0V		
Input Low Voltage	V_{il}				0.8V
Input Current	I_{in}	V_{in} = GND ~ VDDIO	-10µA		10µA
TTL Outputs					
Output High Voltage	V_{oh}	I_{oh} = -8 mA	2.4V		
Output Low Voltage	V_{ol}	I_{ol} = 8 mA			0.4V
Output Tri-State Leakage	$\|I_{oz}\|$				10µA
100BASE-TX Transmit (measured differentially after 1:1 transformer)					
Peak Differential Output Voltage	V_o	100Ω termination across differential output.	0.95V		1.05V
Output Voltage Imbalance	V_{imb}	100Ω termination across differential output			2%
Rise/Fall Time	T_r/T_f		3ns		5ns
Rise/Fall Time Imbalance			0ns		0.5ns
Duty Cycle Distortion					± 0.25ns
Overshoot					5%
Reference Voltage of ISET	V_{set}			0.5V	
Output Jitter		Peak-to-peak		0.7ns	1.4ns
10BASE-T Receive					
Squelch Threshold	V_{sq}	5 MHz square wave		400mV	
10BASE-T Transmit (measured differentially after 1:1 transformer)					
Peak Differential Output Voltage	V_p	100Ω termination across differential output		2.4V	
Output Jitter		Peak-to-peak		1.8ns	3.5ns

Notes:

1. Exceeding the absolute maximum rating may damage the device. Stresses greater than those listed in the table above may cause permanent
   damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification
   is not implied. Maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage
   level.
2. The device is not guaranteed to function outside its operating rating. Unused inputs must always be tied to an appropriate logic voltage level (Ground to V_{DD})
3. No (HS) heat spreader in this package. The thermal junction to ambient (θ_{JA}) and the thermal junction to case (θ_{JC}) are under air velocity 0m/s.
4. Specification for packaged product only. A single port's transformer consumes an additional 45mA at 3.3V for 100BASE-T and 70mA at 3.3V for 10BASE-T.

Timing Specifications

EEPROM Timing

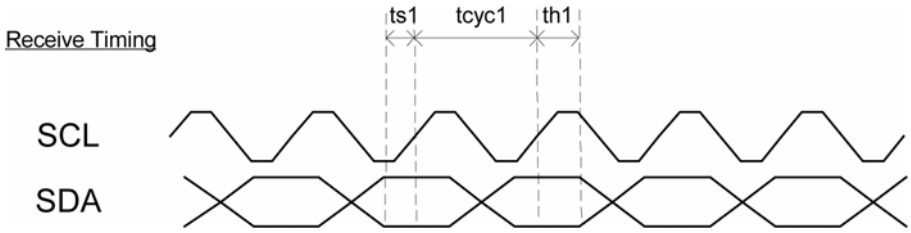


Figure 14. EEPROM Interface Input Timing Diagram

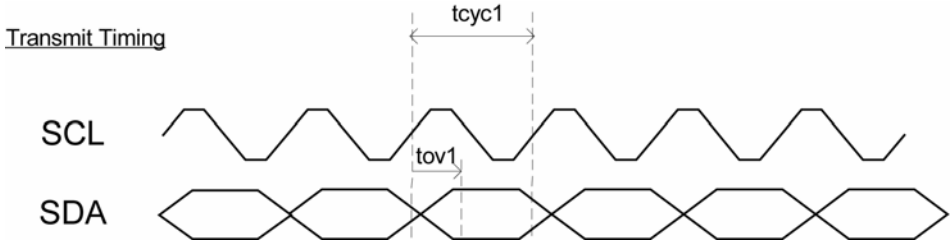


Figure 15. EEPROM Interface Output Timing Diagram

Timing Parameter	Description	Min	Typ	Max	Unit
t_{cyc1}	Clock cycle		16384		ns
t_{s1}	Setup time	20			ns
t_{h1}	Hold time	20			ns
t_{ov1}	Output valid	4096	4112	4128	ns

Table 23. EEPROM Timing Parameters

SNI Timing

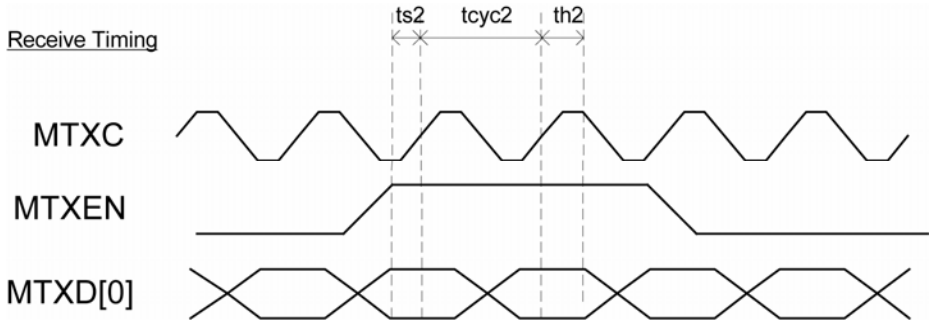


Figure 16. SNI Input Timing Diagram

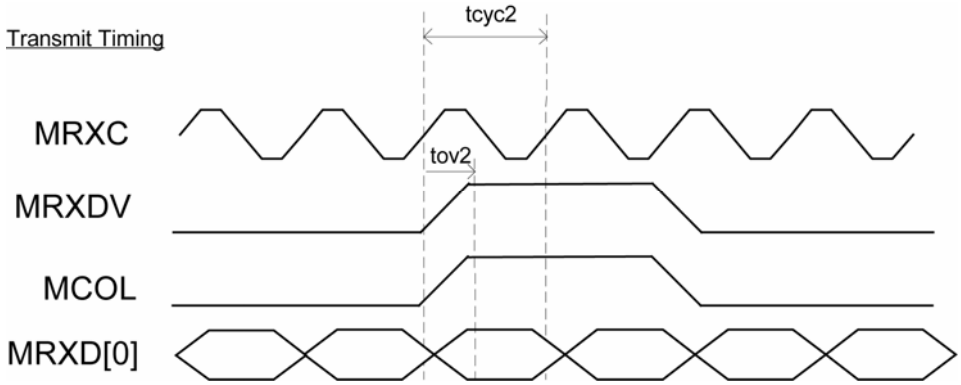


Figure 17. SNI Output Timing Diagram

Timing Parameter	Description	Min	Typ	Max	Unit
t_{cyc2}	Clock cycle		100		ns
t_{s2}	Setup time	10			ns
t_{h2}	Hold time	0			ns
t_{ov2}	Output valid	0	3	6	ns

Table 24. SNI Timing Parameters

MII Timing

MAC Mode MII Timing

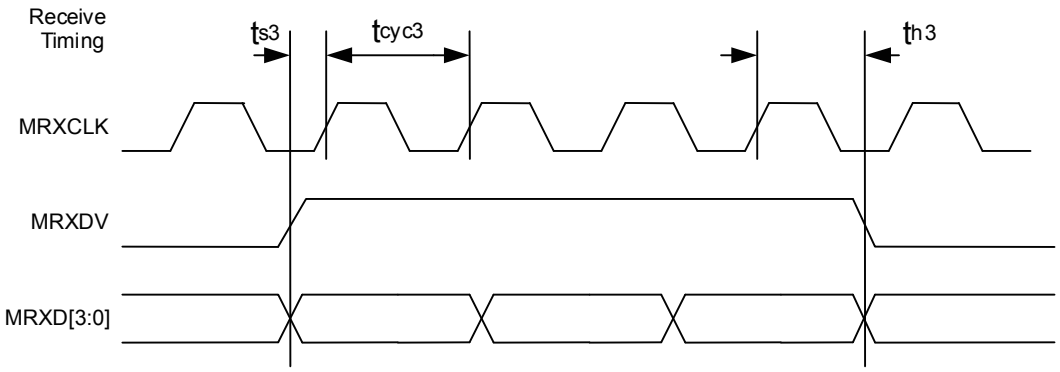


Figure 18. MAC Mode MII Timing – Data Received from MII

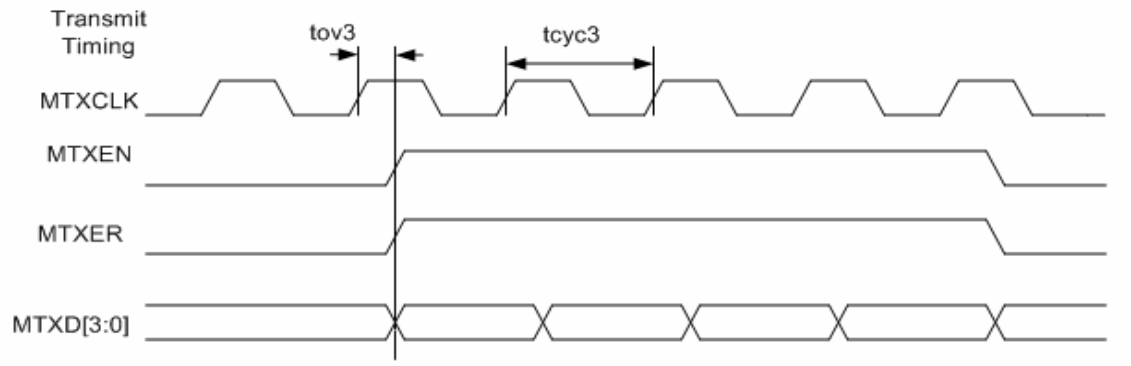


Figure 19. MAC Mode MII Timing – Data Transmitted to MII

Timing Parameter	Description	Min	Typ	Max	Unit
tcyc3 (100BASE-TX)	Clock cycle 100BASE-TX		40		ns
tcyc3 (10BASE-T)	Clock cycle 10BASE-T		400		ns
ts3	Setup time	10			ns
th3	Hold time	3			ns
tov3	Output valid	3		8	ns

Table 25. MAC Mode MII Timing Parameters

PHY Mode MII Timing

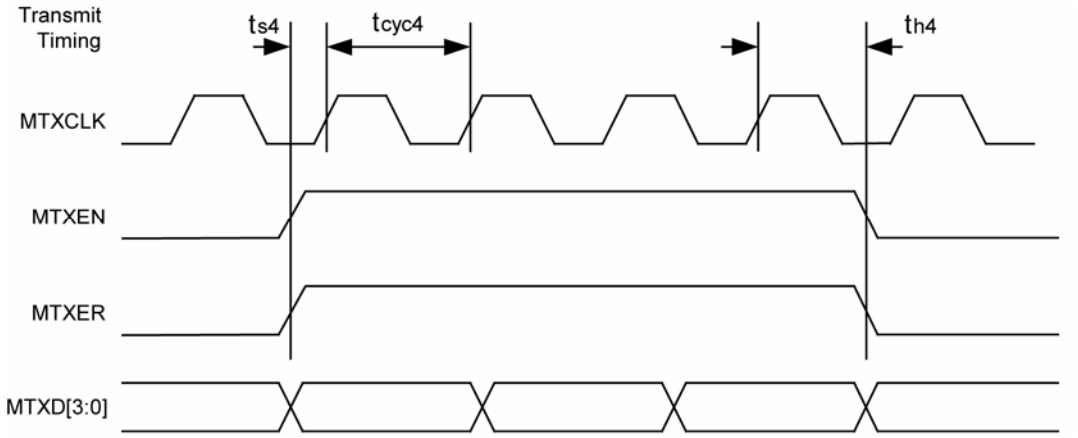


Figure 20. PHY Mode MII Timing – Data Received from MII

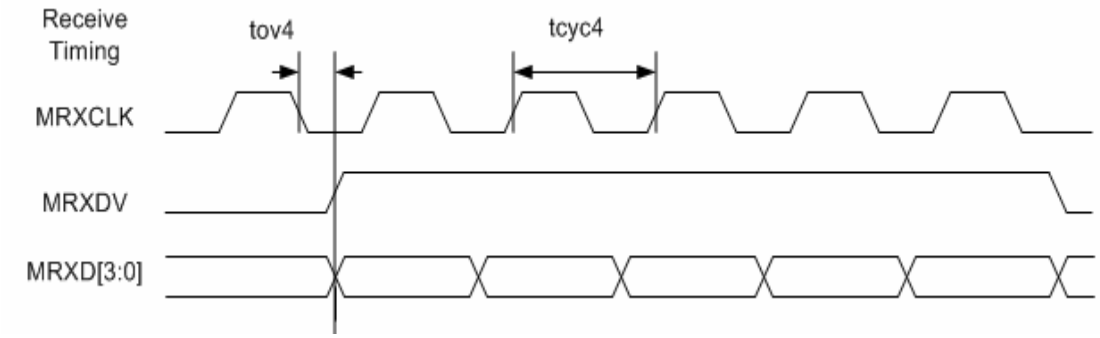


Figure 21. PHY Mode MII Timing – Data Transmitted to MII

Timing Parameter	Description	Min	Typ	Max	Unit
tcyc4 (100BASE-TX)	Clock cycle 100BASE-TX		40		ns
tcyc4 (10BASE-T)	Clock cycle 10BASE-T		400		ns
ts4	Setup time	10			ns
th4	Hold time	1			ns
tov4	Output valid	0		3	ns

Table 26. PHY Mode MII Timing Parameters

RMII Timing

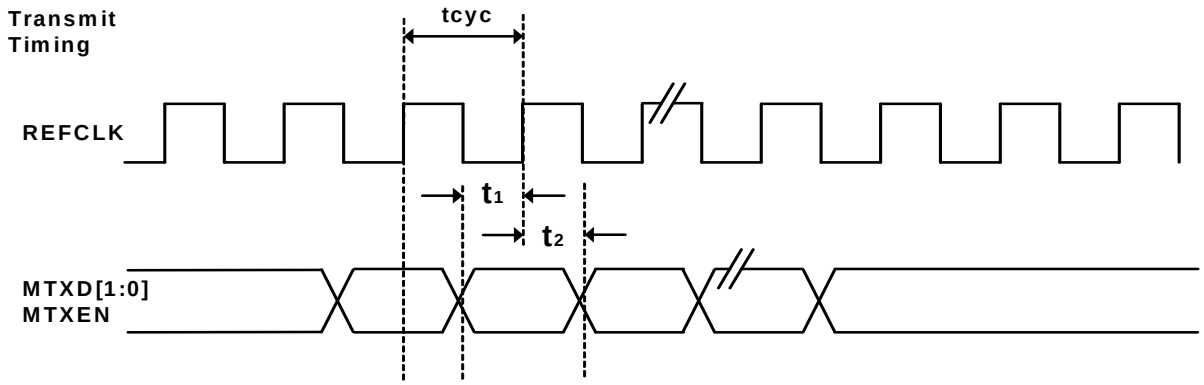


Figure 22: RMII Timing – Data Received from RMII

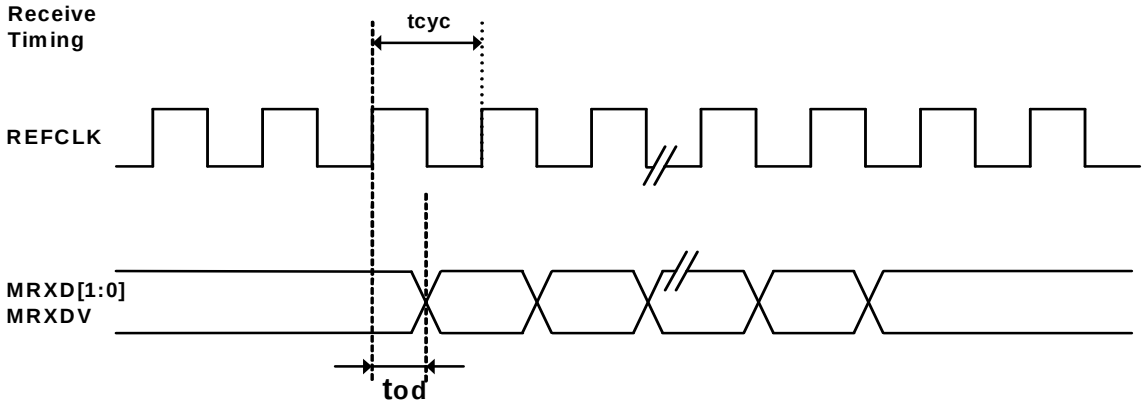


Figure 23: RMII Timing – Data Input to RMII

Timing Parameter	Description	Min	Typ	Max	Unit
tcyc	Clock cycle		20		ns
t1	Setup time	4			ns
t2	Hold time	2			ns
tod	Output delay	2.8		10	ns

Table 27: RMII Timing Parameters

I2C Slave Mode Timing

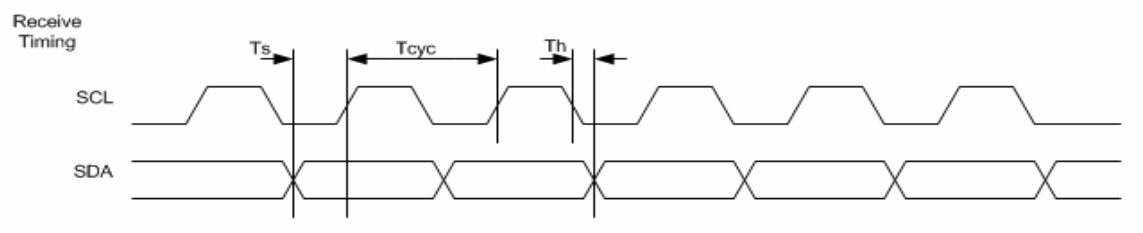


Figure 24. I2C Input Timing

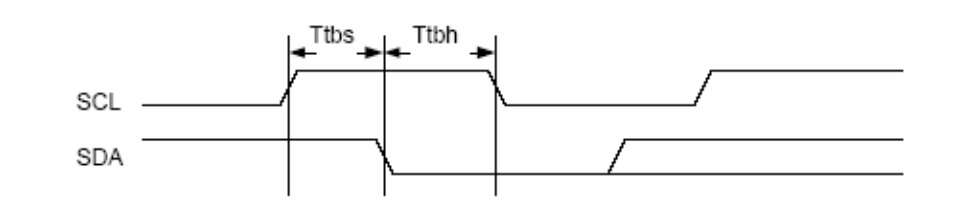


Figure 25. I2C Start Bit Timing

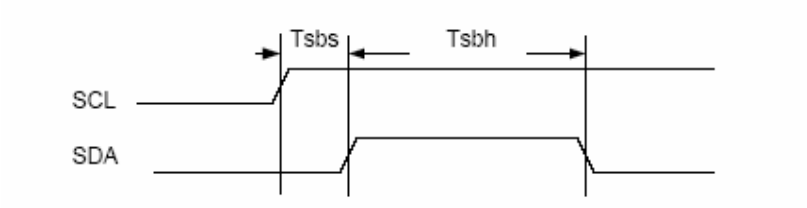


Figure 26. I2C Stop Bit Timing

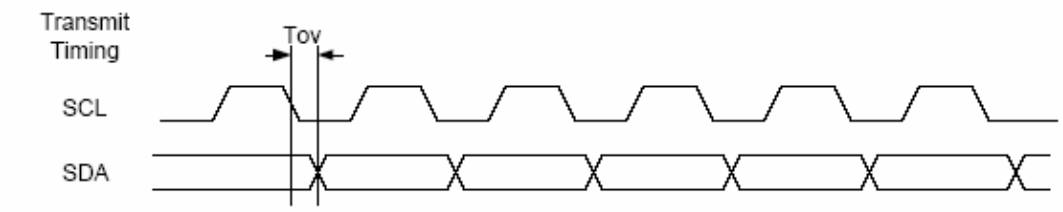


Figure 27. I2C Input Timing

Timing Parameter	Description	Min	Typ	Max	Unit
Tcyc	Clock cycle	400			ns
Ts	Setup time	33		Half-cycle	ns
Th	Hold time	0		Half-cycle	ns
Ttbs	Start bit setup time	33			ns
Ttbh	Start bit hold time	33			ns
Tsbs	Stop bit setup time	2			ns
Tsbh	Stop bit hold time	33			ns
Tov	Output Valid	64		96	ns

Table 28. I2C Timing Parameters

Note: Data is only allowed to change during SCL low time except start and stop bits.

SPI Timing

Input Timing

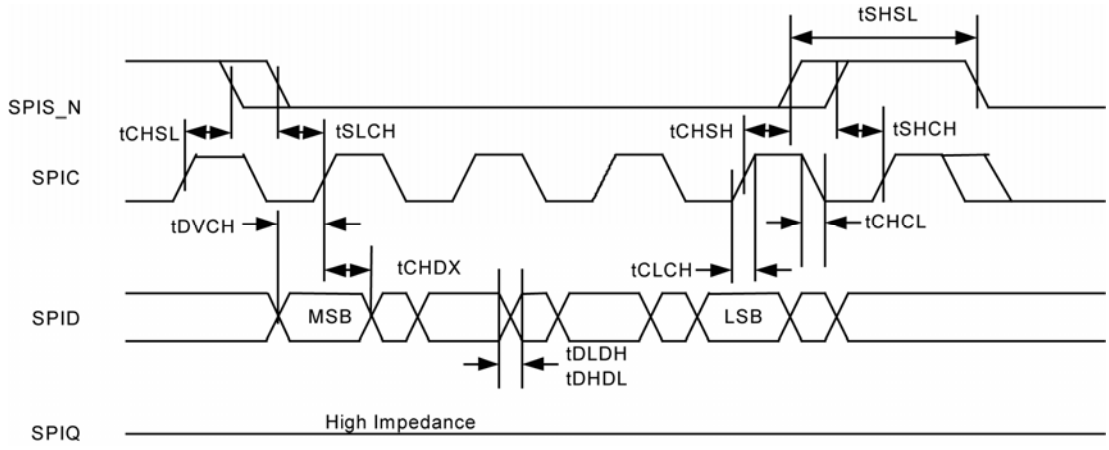


Figure 28. SPI Input Timing

Timing Parameter	Description	Min	Max	Units
fC	Clock frequency		5	MHz
tCHSL	SPIS_N inactive hold time	90		ns
tSLCH	SPIS_N active setup time	90		ns
tCHSH	SPIS_N active old time	90		ns
tSHCH	SPIS_N inactive setup time	90		ns
tSHSL	SPIS_N deselect time	100		ns
tDVCH	Data input setup time	20		ns
tCHDX	Data input hold time	30		ns
tCLCH	Clock rise time		1	us
tCHCL	Clock fall time		1	us
tDLDH	Data input rise time		1	us
tDHDL	Data input fall time		1	us

Table 29. SPI Input Timing Parameters

Output Timing

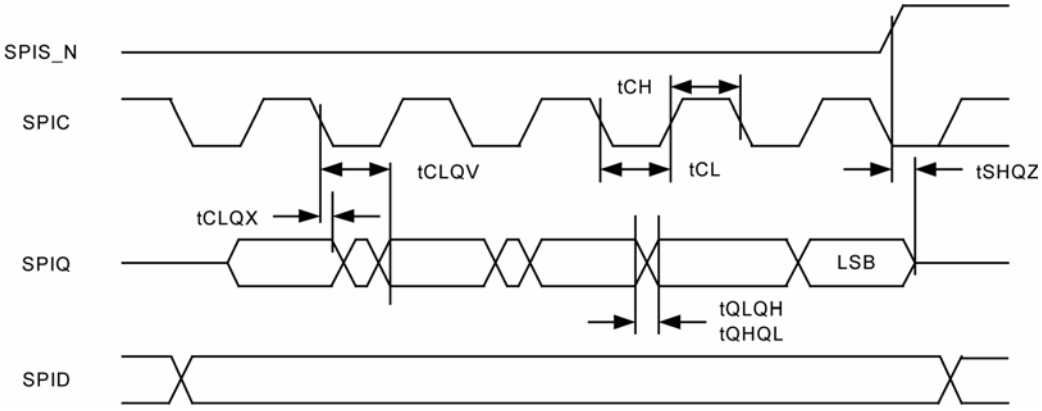


Figure 29. SPI Output Timing

Timing Parameter	Description	Min	Max	Units
fC	Clock frequency		5	MHz
tCLQX	SPIQ hold time	0	0	ns
tCLQV	Clock low to SPIQ valid		60	ns
tCH	Clock high time	90		ns
tCL	Clock low time	90		
tQLQH	SPIQ rise time		50	ns
tQHQL	SPIQ fall time		50	ns
tSHQZ	SPIQ disable time		100	ns

Table 30. SPI Output Timing Parameters

Auto-Negotiation Timing

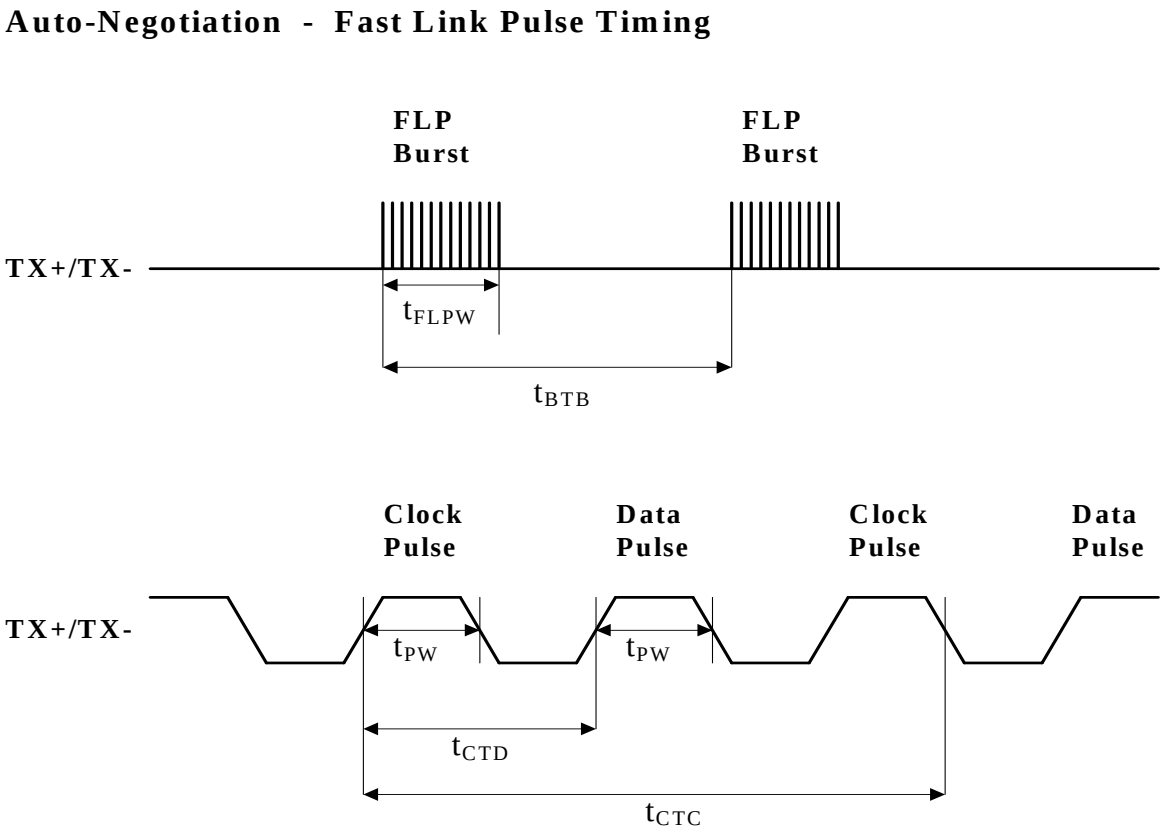


Figure 30: Auto-Negotiation Timing

Timing Parameter	Description	Min	Typ	Max	Units
t_{BTB}	FLP burst to FLP burst	8	16	24	ms
t_{FLPW}	FLP burst width		2		ms
t_{PW}	Clock/Data pulse width		100		ns
t_{CTD}	Clock pulse to Data pulse	55.5	64	69.5	µs
t_{CTC}	Clock pulse to Clock pulse	111	128	139	µs
	Number of Clock/Data pulse per burst	17		33	

Table 31: Auto-Negotiation Timing Parameters

Reset Timing

The KSZ8893MQL/MBL reset timing requirement is summarized in the following figure and table.

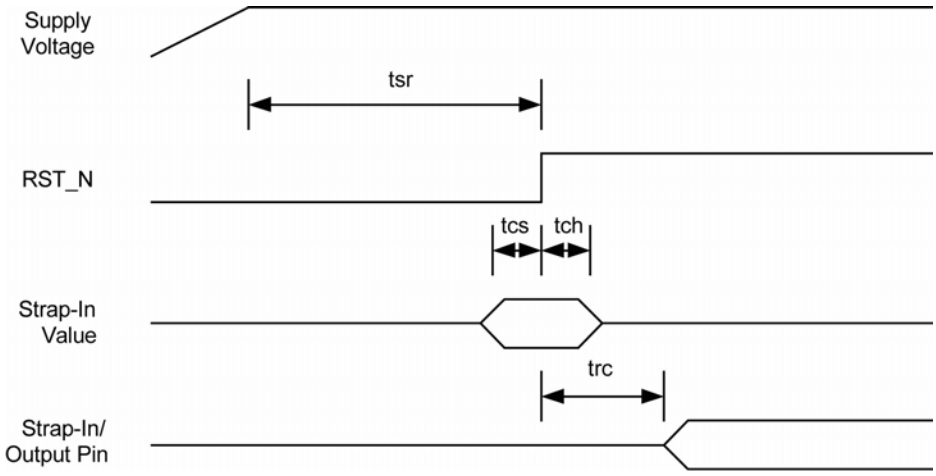


Figure 31. Reset Timing

Parameter	Description	Min	Max	Units
t_{sr}	Stable supply voltages to reset High	10		ms
t_{cs}	Configuration setup time	50		ns
t_{ch}	Configuration hold time	50		ns
t_{rc}	Reset to strap-in pin output	50		us

Table 32. Reset Timing Parameters

After the de-assertion of reset, it is recommended to wait a minimum of 100 us before starting programming on the managed interface (I2C slave, SPI slave, SMI, MIIM).

Reset Circuit

The reset circuit in Figure 32 is recommended for powering up the KSZ8893MQL/MBL if reset is triggered only by the power supply.

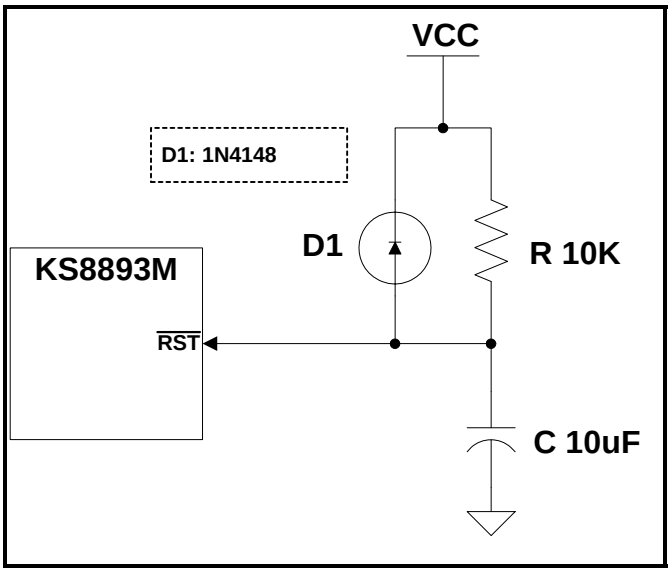


Figure 32. Recommended Reset Circuit

The reset circuit in Figure 33 is recommended for applications where reset is driven by another device (e.g., CPU, FPGA, etc),. At power-on-reset, R, C and D1 provide the necessary ramp rise time to reset the KSZ8893MQL/MBL device. The RST_OUT_n from CPU/FPGA provides the warm reset after power up.

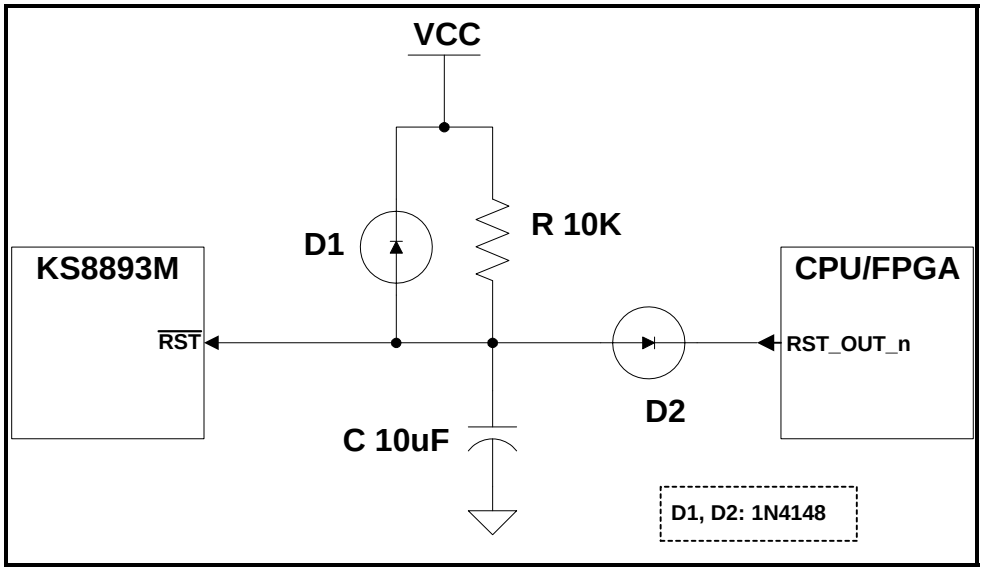


Figure 33. Recommended Reset Circuit for interfacing with CPU/FPGA Reset Output

Selection of Isolation Transformers

An 1:1 isolation transformer is required at the line interface. An isolation transformer with integrated common-mode choke is recommended for exceeding FCC requirements.

The following table gives recommended transformer characteristics.

Parameter	Value	Test Condition
Turns ratio	1 CT : 1 CT	
Open-circuit inductance (min.)	350μH	100mV, 100kHz, 8mA
Leakage inductance (max.)	0.4μH	1MHz (min.)
Inter-winding capacitance (max.)	12pF	
D.C. resistance (max.)	0.9Ω	
Insertion loss (max.)	1.0dB	0MHz – 65MHz
HIPOT (min.)	1500Vrms	

Table 33. Transformer Selection Criteria

Magnetic Manufacturer	Part Number	Auto MDI-X	Number of Port
Bel Fuse	S558-5999-U7	Yes	1
Bel Fuse (MagJack)	SI-46001	Yes	1
Bel Fuse (MagJack)	SI-50170	Yes	1
Delta	LF8505	Yes	1
LanKom	LF-H41S	Yes	1
Pulse	H1102	Yes	1
Pulse (low cost)	H1260	Yes	1
Transpower	HB726	Yes	1
YCL	LF-H41S	Yes	1
TDK (Mag Jack)	TLA-6T718	Yes	1

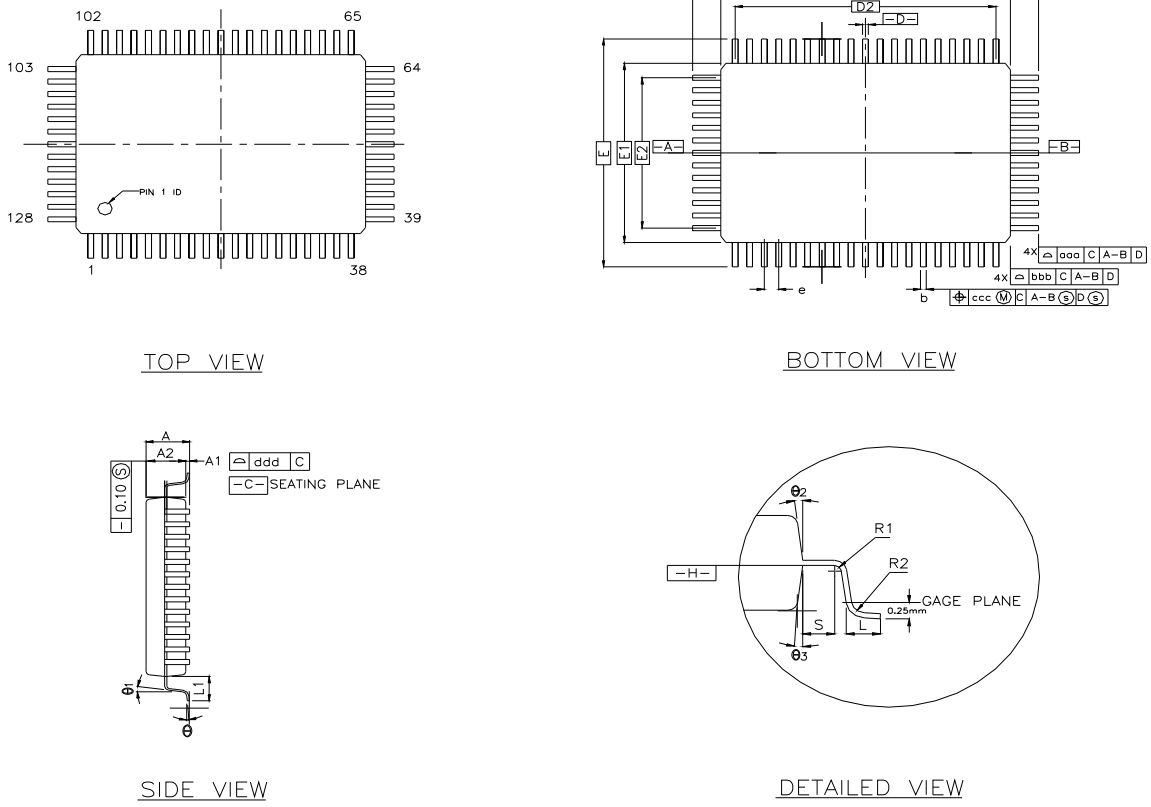
Table 34. Qualified Single Port Magnetics

Selection of Reference Crystal

Chacteristics	Value	Units
Frequency	25.00000	MHz
Frequency tolerance (max)	±50	ppm
Load capacitance (max)	20	pF
Series resistance	25	Ω

Table 35. Typical Reference Crystal Characteristics

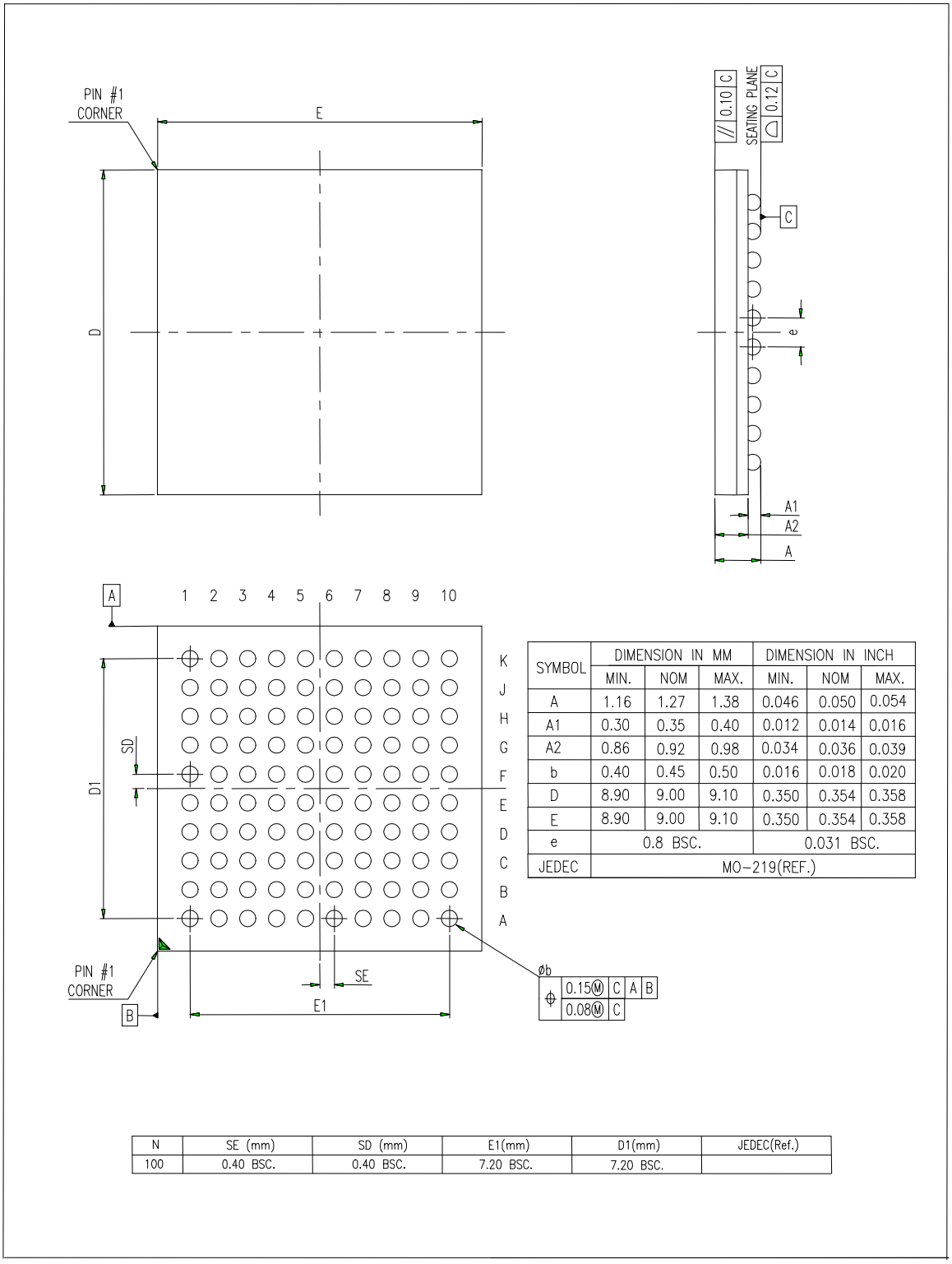
Package Information



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	3.40	—	—	0.134
A1	0.25	—	—	0.010	—	—
A2	2.50	2.72	2.90	0.098	0.107	0.114
D	23.20 BASIC			0.913 BASIC		
D1	20.00 BASIC			0.787 BASIC		
E	17.20 BASIC			0.677 BASIC		
E1	14.00 BASIC			0.551 BASIC		
R2	0.13	—	0.30	0.005	—	0.012
R1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ1	0°	—	—	0°	—	—
θ2 , θ3	15° REF			15° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—
b	0.170	0.200	0.270	0.007	0.008	0.011
e	0.50 BSC.			0.20 BSC		
D2	18.50			0.728		
E2	12.50			0.492		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

COTROL DIMENSIONS ARE IN MILLIMETERS.

Figure 34. 128-Pin PQFP Package



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	1.16	1.27	1.38	0.046	0.050	0.054
A1	0.30	0.35	0.40	0.012	0.014	0.016
A2	0.86	0.92	0.98	0.034	0.036	0.039
b	0.40	0.45	0.50	0.016	0.018	0.020
D	8.90	9.00	9.10	0.350	0.354	0.358
E	8.90	9.00	9.10	0.350	0.354	0.358
e	0.8 BSC.			0.031 BSC.		
JEDEC	MO-219(REF.)					

N	SE (mm)	SD (mm)	E1(mm)	D1(mm)	JEDEC(Ref.)
100	0.40 BSC.	0.40 BSC.	7.20 BSC.	7.20 BSC.	

Figure 35. 100_Ball LFBGA Package

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