

BUK98180-100A

N-channel TrenchMOS logic level FET

16 March 2016

Product data sheet

1. General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

2. Features and benefits

- Low conduction losses due to low on-state resistance
- Q101 compliant
- Suitable for logic level gate drive sources

3. Applications

- 12 V, 24 V and 42 V loads
- Automotive and general purpose power switching
- Motors, lamps and solenoids

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 150 °C	-	-	100	V
I _D	drain current	V _{GS} = 5 V; T _{sp} = 25 °C; <u>Fig. 2</u> ; <u>Fig. 3</u>	-	-	4.6	Α
P _{tot}	total power dissipation	T _{sp} = 25 °C; <u>Fig. 1</u>	-	-	8	W
Static charac	teristics				'	
R _{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A; T_j = 25 °C	-	147	173	mΩ
		V_{GS} = 4.5 V; I_D = 5 A; T_j = 25 °C	-	-	201	mΩ
		$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 ^{\circ}\text{C}; Fig. 12;$ Fig. 13	-	153	180	mΩ
Avalanche ru	ggedness					,
E _{DS(AL)S}	non-repetitive drain- source avalanche energy	I_D = 4 A; V_{sup} ≤ 100 V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped	-	-	16	mJ



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	4	D I
2	D	drain		
3	S	source		G T T
4	D	drain	⊟1 ⊟2 ⊟3 SC-73 (SOT223)	mbb076 S

6. Ordering information

Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
BUK98180-100A	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223			
BUK98180-100A/CU	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223			

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK98180-100A	918010
BUK98180-100A/CU	918010

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 150 °C	-	100	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	100	V
V _{GS}	gate-source voltage		-10	10	V
P _{tot}	total power dissipation	T _{sp} = 25 °C; <u>Fig. 1</u>	-	8	W
I _D	drain current	T _{sp} = 25 °C; V _{GS} = 5 V; <u>Fig. 2</u> ; <u>Fig. 3</u>	-	4.6	Α
		T _{sp} = 100 °C; V _{GS} = 5 V; <u>Fig. 2</u>	-	3	Α
I _{DM}	peak drain current	T_{sp} = 25 °C; pulsed; $t_p \le 10 \mu s$; Fig. 3	-	18	Α

BUK98180-100A

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Symbol	Parameter	Conditions	Min	Max	Unit
T _{stg}	storage temperature		-55	150	°C
T _j	junction temperature		-55	150	°C
V_{GSM}	peak gate-source voltage	pulsed; t _p ≤ 50 μs	-15	15	V
Source-drai	n diode				
I _S	source current	T _{sp} = 25 °C	-	4.6	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{sp} = 25 \ ^{\circ}C$	-	18	Α
Avalanche r	ruggedness				
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 4 A; V_{sup} ≤ 100 V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped	-	16	mJ

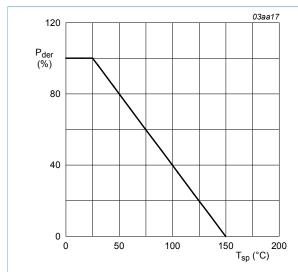


Fig. 1. Normalized total power dissipation as a function of solder point temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

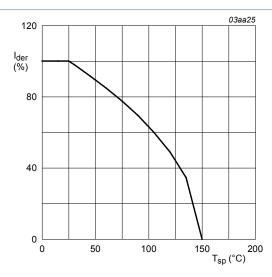


Fig. 2. Normalized continuous drain current as a function of solder point temperature

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100 \%$$

3/12

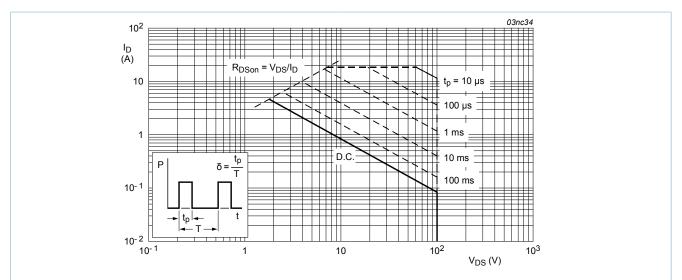


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

 T_{amb} = 25°C; I_{DM} is single pulse

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-sp)}	thermal resistance from junction to solder point	Fig. 4	-	-	15	K/W
R _{th(j-a)}	thermal resistance from junction to ambient		-	120	-	K/W

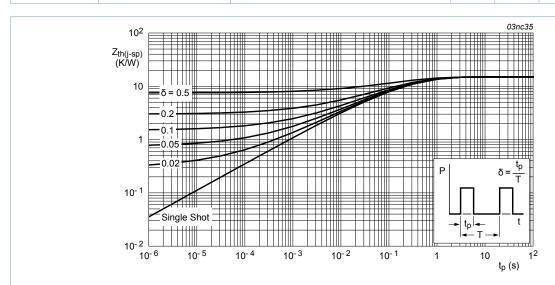


Fig. 4. Transient thermal impedance from junction to solder point as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	racteristics					
V _{(BR)DSS}	drain-source	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	100	-	-	V
br	breakdown voltage	I _D = 0.25 mA; V _{GS} = 0 V; T _j = -55 °C	89	-	-	V
V _{GS(th)}	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS} ; T_j = 25 °C; Fig. 11	1	1.5	2	V
		I_D = 1 mA; V_{DS} = V_{GS} ; T_j = -55 °C; Fig. 11	-	-	2.3	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ °C};$ Fig. 11	0.6	-	-	V
I _{DSS}	drain leakage current	V _{DS} = 100 V; V _{GS} = 0 V; T _j = 150 °C	-	-	500	μA
		V _{DS} = 100 V; V _{GS} = 0 V; T _j = 25 °C	-	0.05	10	μA
I _{GSS}	gate leakage current	V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 5 A; T _j = 25 °C	-	147	173	mΩ
		V _{GS} = 4.5 V; I _D = 5 A; T _j = 25 °C	-	-	201	mΩ
		$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 ^{\circ}\text{C}; Fig. 12;$ Fig. 13	-	153	180	mΩ
		V _{GS} = 5 V; I _D = 5 A; T _j = 150 °C; Fig. 12; Fig. 13	-	-	389	mΩ
Dynamic o	characteristics		'			
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz;	-	464	619	pF
C _{oss}	output capacitance	T _j = 25 °C; <u>Fig. 14</u>	-	60	72	pF
C _{rss}	reverse transfer capacitance		-	36	50	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \Omega; V_{GS} = 5 \text{ V};$	-	7	-	ns
t _r	rise time	$R_{G(ext)} = 10 \Omega; T_j = 25 °C$	-	89	-	ns
t _{d(off)}	turn-off delay time		-	18	-	ns
t _f	fall time		-	25	-	ns
Source-dra	ain diode		1	-		
V_{SD}	source-drain voltage	I _S = 5 A; V _{GS} = 0 V; T _j = 25 °C; <u>Fig. 15</u>	-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/µs;	-	49	-	ns
Q _r	recovered charge	V_{GS} = -10 V; V_{DS} = 30 V; T_j = 25 °C	-	130	-	nC

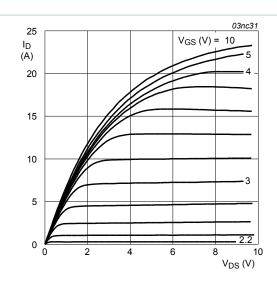


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values



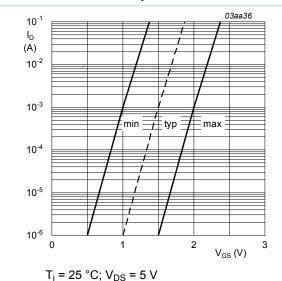


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

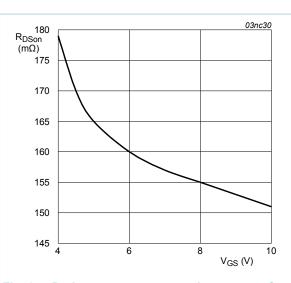


Fig. 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

$$T_i = 25^{\circ}C; I_D = 5A$$

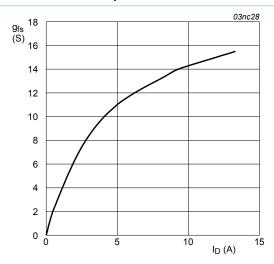


Fig. 8. Forward transconductance as a function of drain current; typical values

$$T_j = 25^{\circ}C; V_{DS} = 25V$$

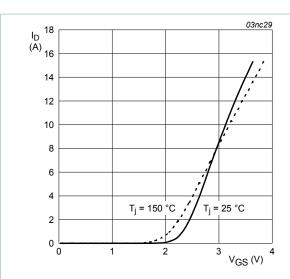


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values



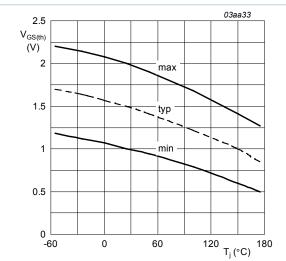


Fig. 11. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1mA; V_{DS} = V_{GS}$$

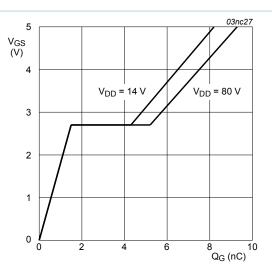


Fig. 10. Gate-source voltage as a function of turn-on gate charge; typical values

$$T_j = 25^{\circ}C; I_D = 5A$$

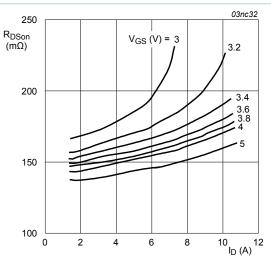


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$$T_{j} = 25^{\circ}C$$

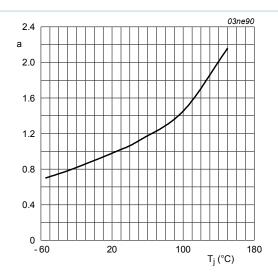


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

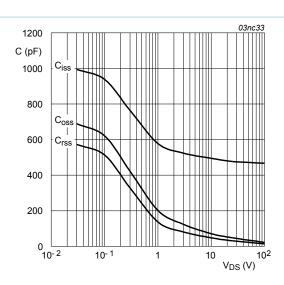


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0V; f = 1MHz$$

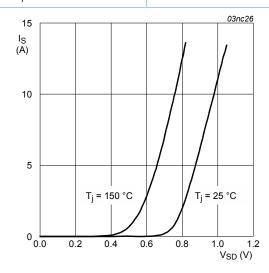
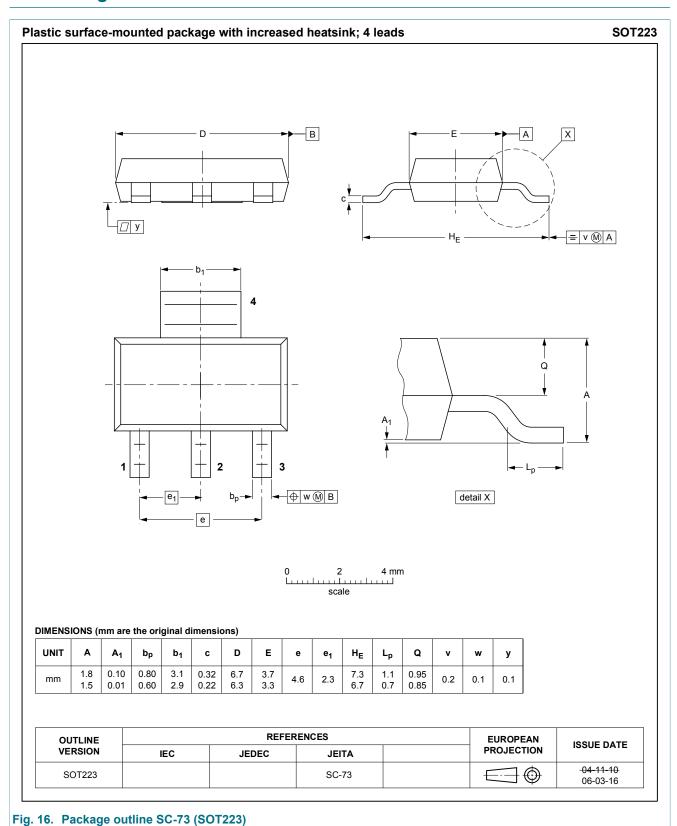


Fig. 15. Reverse diode current as a function of reverse diode voltage; typical value

$$V_{GS} = 0V$$

11. Package outline



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13. Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Quick reference data	1
5	Pinning information	2
6	Ordering information	2
7	Marking	2
8	Limiting values	2
9	Thermal characteristics	4
10	Characteristics	5
11	Package outline	9
12	Legal information	10
12.1	Data sheet status	10
12.2	Definitions	10
12.3	Disclaimers	10
12.4	Trademarks	11

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