

2.5 V or 3.3 V, 200-MHz, 1:12 Clock Distribution Buffer

Features

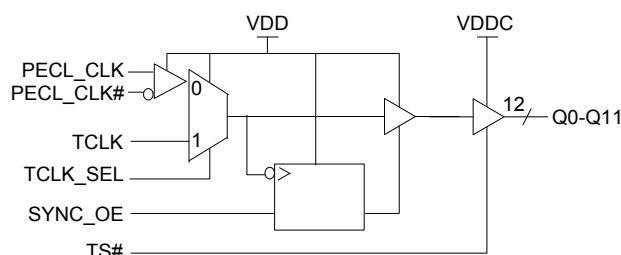
- 2.5 V or 3.3 V operation
- 200-MHz clock support
- LVPECL or LVC MOS/LVTTL clock input
- LVC MOS-/LVTTL-compatible inputs
- 12 clock outputs: drive up to 24 clock lines
- Synchronous Output Enable
- Output three-state control
- 150 ps typical output-to-output skew
- Pin compatible with MPC948, MPC948L, MPC9448
- Available in Commercial and Industrial temp. range
- 32-pin TQFP package

Description

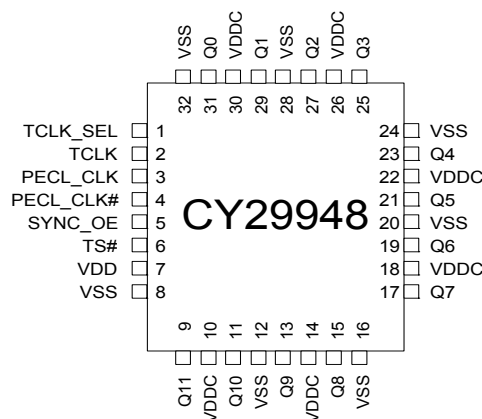
The CY29948 is a low-voltage 200-MHz clock distribution buffer with the capability to select either a differential LVPECL or a LVC MOS/LVTTL compatible input clock. The two clock sources can be used to provide for a test clock as well as the primary system clock. All other control inputs are LVC MOS/LVTTL compatible. The 12 outputs are LVC MOS or LVTTL compatible and can drive 50 Ω series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces giving the device an effective fanout of 1:24. The outputs can also be three-stated via the three-state input TS#. Low output-to-output skews make the CY29948 an ideal clock distribution buffer for nested clock trees in the most demanding of synchronous systems.

The CY29948 also provides a synchronous output enable input for enabling or disabling the output clocks. Since this input is internally synchronized to the input clock, potential output glitching or runt pulse generation is eliminated.

Block Diagram



Pin Configuration



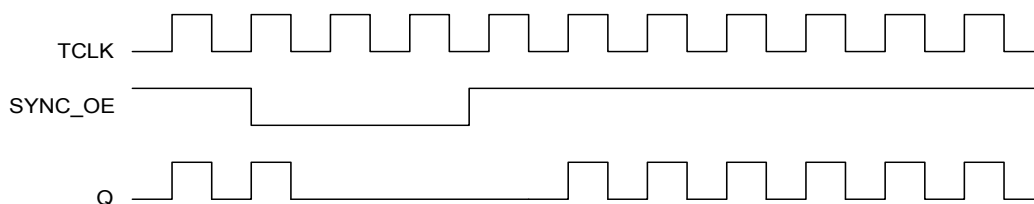
Pin Description^[1]

Pin	Name	PWR	I/O	Description
3	PECL_CLK	–	I, PU	PECL Input Clock
4	PECL_CLK#	–	I, PD	PECL Input Clock
2	TCLK	–	I, PU	External Reference/Test Clock Input
9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31	Q(11:0)	VDDC	O	Clock Outputs
1	TCLK_SEL	–	I, PU	Clock Select Input. When LOW, PECL clock is selected. When HIGH TCLK is selected.
5	SYNC_OE	–	I, PU	Output Enable Input. When asserted HIGH, the outputs are enabled. When set LOW the outputs are disabled in a LOW state.
6	TS#	–	I, PU	Three-state Control Input. When asserted LOW, the output buffers are three-stated. When set HIGH, the output buffers are enabled.
10, 14, 18, 22, 26, 30	VDDC	–	–	2.5 V or 3.3 V Power Supply for Output Clock Buffers
7	VDD	–	–	2.5 V or 3.3 V Power Supply
8, 12, 16, 20, 24, 28, 32	VSS	–	–	Common Ground

Output Enable/Disable

The CY29948 features a control input to enable or disable the outputs. This data is latched on the falling edge of the input clock. When SYNC_OE is asserted LOW, the outputs are disabled in a LOW state. When SYNC_OE is set HIGH, the outputs are enabled as shown in [Figure 1](#).

Figure 1. SYNC_OE Timing Diagram



Note

1. PD = Internal pull-down, PU = Internal pull-up.

Maximum Ratings^[2]

Maximum Input Voltage Relative to V_{SS}	$V_{SS} - 0.3\text{ V}$
Maximum Input Voltage Relative to V_{DD}	$V_{DD} + 0.3\text{ V}$
Storage Temperature.....	$-65\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$
Operating Temperature.....	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$
Maximum ESD protection.....	2 kV
Maximum Power Supply.....	5.5 V
Maximum Input Current.....	$\pm 20\text{ mA}$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters

$V_{DD} = V_{DDC} = 3.3\text{ V} \pm 10\%$ or $2.5\text{ V} \pm 5\%$, over the specified temperature range.

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage	$V_{DD} = 3.3\text{ V}$, PECL_CLK single ended	1.49	–	1.825	V
		$V_{DD} = 2.5\text{ V}$, PECL_CLK single ended	1.10	–	1.45	
		All other inputs	V_{SS}	–	0.8	
V_{IH}	Input High Voltage	$V_{DD} = 3.3\text{ V}$, PECL_CLK single ended	2.135	–	2.42	V
		$V_{DD} = 2.5\text{ V}$, PECL_CLK single ended	1.75	–	2.0	
		All other inputs	2.0	–	V_{DD}	
I_{IL}	Input Low Current ^[3]		–	–	–100	μA
I_{IH}	Input High Current ^[3]		–	–	100	
V_{PP}	Peak-to-Peak Input Voltage PECL_CLK		300	–	1000	mV
V_{CMR}	Common Mode Range ^[4] PECL_CLK	$V_{DD} = 3.3\text{ V}$	$V_{DD} - 2.0$	–	$V_{DD} - 0.6$	V
		$V_{DD} = 2.5\text{ V}$	$V_{DD} - 1.2$	–	$V_{DD} - 0.6$	
V_{OL}	Output Low Voltage ^[5]	$I_{OL} = 20\text{ mA}$	–	–	0.4	V
V_{OH}	Output High Voltage ^[5]	$I_{OH} = -20\text{ mA}$, $V_{DD} = 3.3\text{ V}$	2.5	–	–	V
		$I_{OH} = -20\text{ mA}$, $V_{DD} = 2.5\text{ V}$	1.8	–	–	
I_{DDQ}	Quiescent Supply Current		–	5	7	mA
I_{DD}	Dynamic Supply Current	$V_{DD} = 3.3\text{ V}$, Outputs @ 100 MHz, $C_L = 30\text{ pF}$	–	180	–	mA
		$V_{DD} = 3.3\text{ V}$, Outputs @ 160 MHz, $C_L = 30\text{ pF}$	–	270	–	
		$V_{DD} = 2.5\text{ V}$, Outputs @ 100 MHz, $C_L = 30\text{ pF}$	–	125	–	
		$V_{DD} = 2.5\text{ V}$, Outputs @ 160 MHz, $C_L = 30\text{ pF}$	–	190	–	
Z_{out}	Output Impedance	$V_{DD} = 3.3\text{ V}$	12	15	18	Ω
		$V_{DD} = 2.5\text{ V}$	14	18	22	
C_{in}	Input Capacitance		–	4	–	pF

Notes

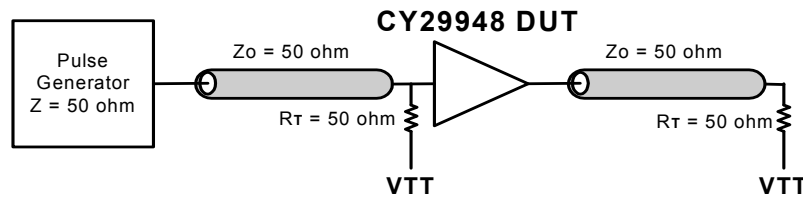
- Multiple Supplies:** The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.
- Inputs have pull-up/pull-down resistors that effect input current.
- The V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the "High" input is within the V_{CMR} range and the input lies within the V_{PP} specification.
- Driving series or parallel terminated 50 Ω (or 50 Ω to $V_{DD}/2$) transmission lines.

AC Parameters^[6]

$V_{DD} = V_{DDC} = 3.3 \text{ V} \pm 10\%$ or $2.5 \text{ V} \pm 5\%$, over the specified operating range.

Parameter	Description	Conditions	Min	Typ	Max	Unit
$F_{\max}$	Input Frequency ^[7]	$V_{DD} = 3.3 \text{ V}$	–	–	200	MHz
		$V_{DD} = 2.5 \text{ V}$	–	–	170	
T_{pd}	PECL_CLK to Q Delay ^[7]	$V_{DD} = 3.3 \text{ V}$	4.0	–	8.0	ns
	TCLK to Q Delay ^[7]		4.4	–	8.9	
	PECL_CLK to Q Delay ^[7]	$V_{DD} = 2.5 \text{ V}$	6.0	–	10.0	
	TCLK to Q Delay ^[7]		6.4	–	10.9	
F_{outDC}	Output Duty Cycle ^[7, 8, 9]	Measured at $V_{DD}/2$	45	–	55	%
t_{pZL}, t_{pZH}	Output Enable Time (all outputs)		2	–	10	ns
t_{pLZ}, t_{pHZ}	Output Disable Time (all outputs)		2	–	10	ns
T_{skew}	Output-to-Output Skew ^[7, 9]		–	150	250	ps
$T_{\text{skew(pp)}}$	Part-to-Part Skew ^[10]	PECL_CLK to Q	–	–	1.5	ns
		TCLK to Q	–	–	2.0	
T_s	Set-up Time ^[7, 11]	SYNC_OE to PECL_CLK	1.0	–	–	ns
		SYNC_OE to TCLK	0.0	–	–	
T_h	Hold Time ^[7, 11]	PECL_CLK to SYNC_OE	0.0	–	–	ns
		TCLK to SYNC_OE	1.0	–	–	
T_r/T_f	Output Clocks Rise/Fall Time ^[9]	0.8 V to 2.0 V, $V_{DD} = 3.3 \text{ V}$	0.20	–	1.0	ns
		0.6 V to 1.8 V, $V_{DD} = 2.5 \text{ V}$	0.20	–	1.3	

Figure 2. LVCMOS_CLK CY29948 Test Reference for $V_{CC} = 3.3 \text{ V}$ and $V_{CC} = 2.5 \text{ V}$



Notes

6. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
7. Outputs driving 50Ω transmission lines.
8. 50% input duty cycle.
9. See [Figure 2](#) and [Figure 3 on page 5](#).
10. Part-to-Part skew at a given temperature and voltage.
11. Setup and hold times are relative to the falling edge of the input clock.

Figure 3. PECL_CLK CY29948 Test Reference for $V_{CC} = 3.3\text{ V}$ and $V_{CC} = 2.5\text{ V}$

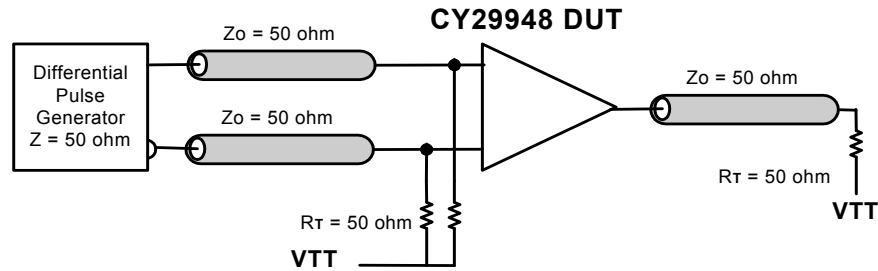


Figure 4. Propagation Delay (t_{PD}) Test Reference

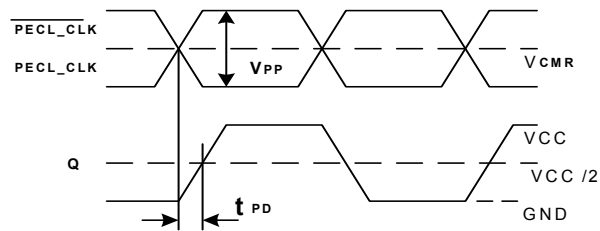


Figure 5. LVCMOS Propagation Delay (t_{PD}) Test Reference

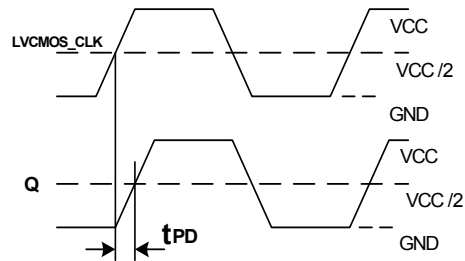


Figure 6. Output Duty Cycle (F_{outDC})

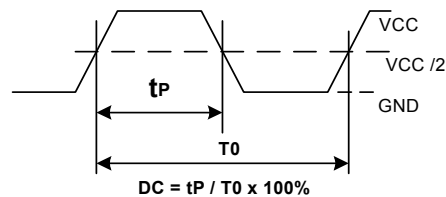
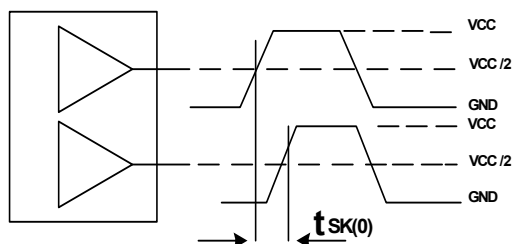
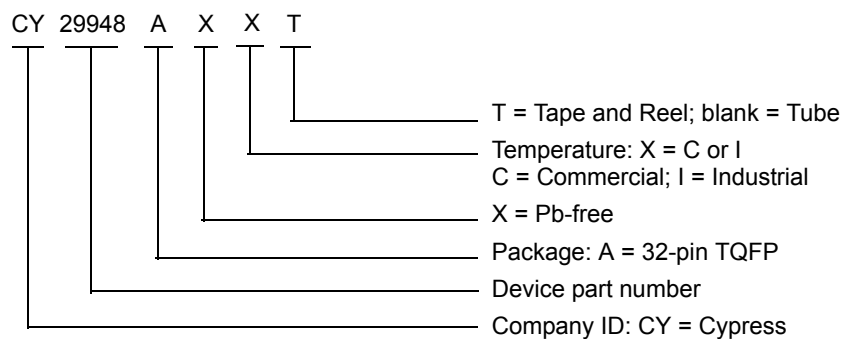


Figure 7. Output-to-Output Skew $t_{SK(0)}$


Ordering Information

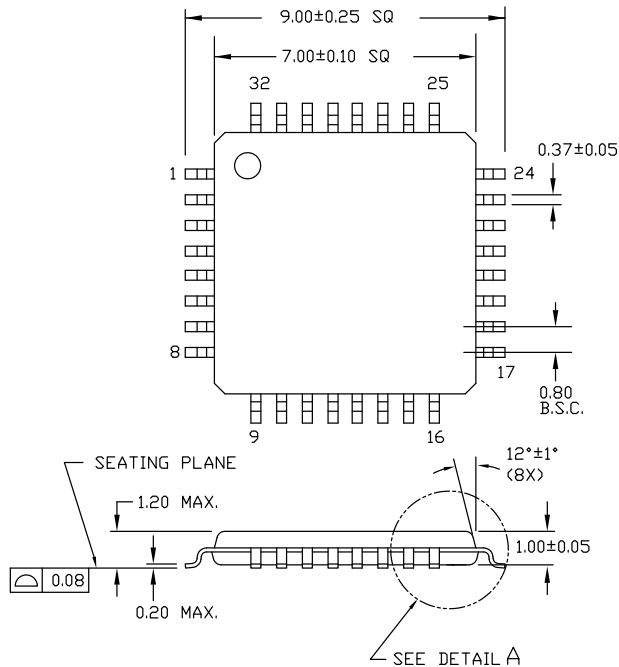
Part Number	Package Type	Production Flow
CY29948AC	32-pin TQFP	Commercial, 0 °C to +70 °C
CY29948ACT	32-pin TQFP - Tape and Reel	Commercial, 0 °C to +70 °C
Pb-free		
CY29948AXC	32-pin TQFP	Commercial, 0 °C to +70 °C
CY29948AXCT	32-pin TQFP - Tape and Reel	Commercial, 0 °C to +70 °C
CY29948AXI	32-pin TQFP	Industrial, -40 °C to +85 °C
CY29948AXIT	32-pin TQFP - Tape and Reel	Industrial, -40 °C to +85 °C

Ordering Code Definitions

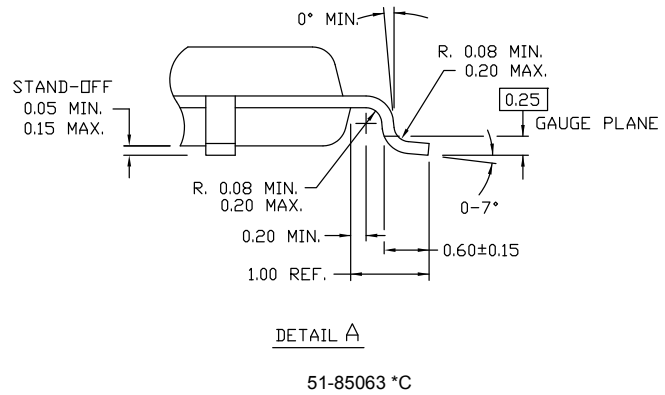


Package Drawing and Dimensions

32 Lead Thin Plastic Quad Flatpack 7 X 7 X 1.0mm – A32



DIMENSIONS ARE IN MILLIMETERS



Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
ESD	electrostatic Discharge
I/O	input/output
LVC MOS	low voltage complementary metal oxide semiconductor
LVPECL	low voltage positive emitter coupled logic
LV TTL	low voltage transistor-transistor logic
PLL	phase locked loop
TQFP	thin quad flat pack

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kV	kilo Volts
MHz	Mega Hertz
μA	micro Amperes
mA	milli Amperes
mm	milli meter
mV	milli Volts
ns	nano seconds
Ω	ohms
%	percent
pF	pico Farad
ps	pico seconds
V	Volts

Document Revision History

Document Title: CY29948, 2.5 V or 3.3 V, 200-MHz, 1:12 Clock Distribution Buffer Document Number: 38-07288				
Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change
**	111099	02/13/02	BRK	New datasheet
*A	116782	08/14/02	HWT	Added Commercial Temperature Range
*B	122880	12/22/02	RBI	Added power up requirements to Maximum Ratings
*C	428221	See ECN	RGL	Added Lead-free devices
*D	2904731	04/05/10	CXQ	Removed inactive part numbers - CY29948AI and CY29948AIT. Updated package diagram.
*E	3246222	05/02/2011	CXQ	Added Ordering Code Definitions . Added Acronyms and Units of Measure . Updated in new template.

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