# CMOS Low Voltage 2 Ω SPST Switches

# ADG701/ADG702

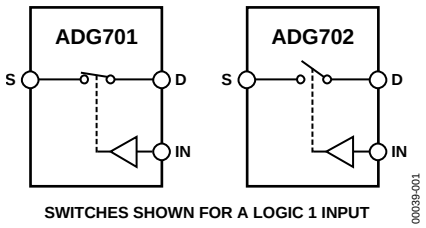
## FEATURES

**1.8 V to 5.5 V single supply**
**2 Ω (typical) on resistance**
**Low on resistance flatness**
**–3 dB bandwidth > 200 MHz**
**Rail-to-rail operation**
**Fast switching times**
**$t_{ON}$ 18 ns**
**$t_{OFF}$ 12 ns**
**Typical power consumption < 0.01 µW**
**TTL/CMOS-compatible**

## APPLICATIONS

**Battery-powered systems**
**Communications systems**
**Sample-and-hold systems**
**Audio signal routing**
**Video switching**
**Mechanical reed relay replacement**

## FUNCTIONAL BLOCK DIAGRAM




SWITCHES SHOWN FOR A LOGIC 1 INPUT

*Figure 1.*

## GENERAL DESCRIPTION

The ADG701/ADG702 are monolithic CMOS SPST switches. These switches are designed on an advanced submicron process that provides low power dissipation yet high switching speed, low on resistance, and low leakage currents. In addition, −3 dB bandwidths of greater than 200 MHz can be achieved.

The ADG701/ADG702 can operate from a single 1.8 V to 5.5 V supply, making it ideal for use in battery-powered instruments and with the new generation of DACs and ADCs from Analog Devices, Inc.

Figure 1 shows that with a logic input of 1, the switch of the ADG701 is closed and that of the ADG702 is open. Each switch conducts equally well in both directions when on.

The ADG701/ADG702 are available in 5-lead SOT-23, 6-lead SOT-23, and 8-lead MSOP packages.

## PRODUCT HIGHLIGHTS

1. 1.8 V to 5.5 V Single-Supply Operation.
   The ADG701/ADG702 offer high performance, including low on resistance and fast switching times, and are fully specified and guaranteed with 3 V and 5 V supply rails.
2. Very Low $R_{ON}$ (3 Ω Maximum at 5 V, 5 Ω Maximum at 3 V). At 1.8 V operation, $R_{ON}$ is typically 40 Ω over the temperature range.
3. On Resistance Flatness $R_{FLAT(ON)}$ (1 Ω Maximum).
4. −3 dB Bandwidth > 200 MHz.
5. Low Power Dissipation.
   CMOS construction ensures low power dissipation.
6. Fast $t_{ON}/t_{OFF}$.

**Table 1. Related Devices**

| Part No. | Description |
|---|---|
| ADG701L/ADG702L | Low voltage 2 Ω SPST switches with guaranteed leakage specifications |

**Rev. C**
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## REVISION HISTORY

**7/06—Rev. B to Rev. C**

Changes to Product Highlights ..... 1
Added Table 1 ..... 1
Changes to Table 2 ..... 3
Changes to Table 3 ..... 4
Added Pb-Free Reflow Soldering to Absolute Maximum Ratings ..... 5
Changes to Ordering Guide ..... 13

**6/04—Rev. A to Rev. B**

Updated Format ..... Universal
Added 5-Lead SOT-23 Package ..... Universal
Updated Outline Dimensions ..... 10
Changes to Ordering Guide ..... 11

**8/98—Rev. 0 to Rev. A**

# SPECIFICATIONS

$V_{DD}$ = 5 V ± 10%, GND = 0 V. Temperature range for B version is −40°C to +85°C, unless otherwise noted.

**Table 2.**

| Parameter | B Version +25°C | B Version −40°C to +85°C | Unit | Test Conditions/Comments |
|---|---|---|---|---|
| ANALOG SWITCH | | | | |
| Analog Signal Range | | 0 V to $V_{DD}$ | V | |
| On Resistance ($R_{ON}$) | 2 | | Ω typ | $V_S$ = 0 V to $V_{DD}$, $I_S$ = –10 mA; Figure 11 |
| | 3 | 4 | Ω max | |
| On Resistance Flatness ($R_{FLAT(ON)}$) | 0.5 | | Ω typ | $V_S$ = 0 V to $V_{DD}$, $I_S$ = –10 mA |
| | | 1.0 | Ω max | |
| LEAKAGE CURRENTS | | | | $V_{DD}$ = 5.5 V |
| Source OFF Leakage, $I_S$ (OFF) | ±0.01 | | nA typ | $V_S$ = 4.5 V/1 V, $V_D$ = 1 V/4.5 V; Figure 12 |
| Drain OFF Leakage, $I_D$ (OFF) | ±0.01 | | nA typ | $V_S$ = 4.5 V/1 V, $V_D$ = 1 V/4.5 V; Figure 12 |
| Channel ON Leakage, $I_D$, $I_S$ (ON) | ±0.01 | | nA typ | $V_S$ = $V_D$ = 1 V, or 4.5 V; Figure 13 |
| DIGITAL INPUTS | | | | |
| Input High Voltage, $V_{INH}$ | | 2.4 | V min | |
| Input Low Voltage, $V_{INL}$ | | 0.8 | V max | |
| Input Current | | | | |
| $I_{INL}$ or $I_{INH}$ | 0.005 | | μA typ | $V_{IN}$ = $V_{INL}$ or $V_{INH}$ |
| | | ±0.1 | μA max | |
| DYNAMIC CHARACTERISTICS[1] | | | | |
| $t_{ON}$ | 12 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF |
| | | 18 | ns max | $V_S$ = 3 V; Figure 14 |
| $t_{OFF}$ | 8 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF |
| | | 12 | ns max | $V_S$ = 3 V; Figure 14 |
| Charge Injection | 5 | | pC typ | $V_S$ = 2 V, $R_S$ = 0 Ω, $C_L$ = 1 nF; Figure 15 |
| Off Isolation | –55 | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 10 MHz |
| | –75 | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz; Figure 16 |
| Bandwidth –3 dB | 200 | | MHz typ | $R_L$ = 50 Ω, $C_L$ = 5 pF; Figure 17 |
| $C_S$ (OFF) | 17 | | pF typ | |
| $C_D$ (OFF) | 17 | | pF typ | |
| $C_D$, $C_S$ (ON) | 38 | | pF typ | |
| POWER REQUIREMENTS | | | | $V_{DD}$ = 5.5 V |
| | | | | Digital inputs = 0 V or 5 V |
| $I_{DD}$ | 0.001 | | μA typ | |
| | | 1.0 | μA max | |

[1] Guaranteed by design, not subject to production test.

$V_{DD}$ = 3 V ± 10%, GND = 0 V. Temperature range for B version is −40°C to +85°C, unless otherwise noted.

**Table 3.**

| Parameter | B Version +25°C | B Version −40°C to +85°C | Unit | Test Conditions/Comments |
|---|---|---|---|---|
| ANALOG SWITCH | | | | |
| Analog Signal Range | | 0 V to $V_{DD}$ | V | |
| On Resistance ($R_{ON}$) | 3.5 | | Ω typ | $V_S$ = 0 V to $V_{DD}$, $I_S$ = −10 mA; Figure 11 |
| | 5 | 6 | Ω max | |
| On Resistance Flatness ($R_{FLAT(ON)}$) | 1.5 | | Ω typ | $V_S$ = 0 V to $V_{DD}$, $I_S$ = −10 mA |
| LEAKAGE CURRENTS | | | | $V_{DD}$ = 3.3 V |
| Source OFF Leakage $I_S$ (OFF) | ±0.01 | | nA typ | $V_S$ = 3 V/1 V, $V_D$ = 1 V/3 V; Figure 12 |
| Drain OFF Leakage $I_D$ (OFF) | ±0.01 | | nA typ | $V_S$ = 3 V/1 V, $V_D$ = 1 V/3 V; Figure 12 |
| Channel ON Leakage $I_D$, $I_S$ (ON) | ±0.01 | | nA typ | V = $V_D$ = 1 V, or 3 V; Figure 13 |
| DIGITAL INPUTS | | | | |
| Input High Voltage, $V_{INH}$ | | 2.0 | V min | |
| Input Low Voltage, $V_{INL}$ | | 0.4 | V max | |
| Input Current | | | | |
| $I_{INL}$ or $I_{INH}$ | 0.005 | | μA typ | $V_{IN}$ = $V_{INL}$ or $V_{INH}$ |
| | | ±0.1 | μA max | |
| DYNAMIC CHARACTERISTICS[1] | | | | |
| $t_{ON}$ | 14 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF |
| | | 20 | ns max | $V_S$ = 2 V, Figure 14 |
| $t_{OFF}$ | 8 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF |
| | | 13 | ns max | $V_S$ = 2 V, Figure 14 |
| Charge Injection | 4 | | pC typ | $V_S$ = 1.5 V, $R_S$ = 0 Ω, $C_L$ = 1 nF; Figure 15 |
| Off Isolation | −55 | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 10 MHz |
| | −75 | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz; Figure 16 |
| Bandwidth −3 dB | 200 | | MHz typ | $R_L$ = 50 Ω, $C_L$ = 5 pF; Figure 17 |
| $C_S$ (OFF) | 17 | | pF typ | |
| $C_D$ (OFF) | 17 | | pF typ | |
| $C_D$, $C_S$ (ON) | 38 | | pF typ | |
| POWER REQUIREMENTS | | | | $V_{DD}$ = 3.3 V<br>Digital inputs = 0 V or 3 V |
| $I_{DD}$ | 0.001 | | μA typ | |
| | | 1.0 | μA max | |

[1] Guaranteed by design, not subject to production test.

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = +25°C, unless otherwise noted.

**Table 4.**

| Parameter | Rating |
|---|---|
| $V_{DD}$ to GND | −0.3 V to +7 V |
| Analog and Digital Inputs[1] | −0.3 V to $V_{DD}$ + 0.3 V or 30 mA, whichever occurs first |
| Continuous Current, S or D | 30 mA |
| Peak Current, S or D | 100 mA, pulsed at 1 ms, 10% duty cycle maximum |
| Operating Temperature Range | |
| Industrial (B Version) | −40°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | 150°C |
| MSOP Package, Power Dissipation | 315 mW |
| $\theta_{JA}$ Thermal Impedance | 206°C/W |
| $\theta_{JC}$ Thermal Impedance | 44°C/W |
| SOT-23 Package, Power Dissipation | 282 mW |
| $\theta_{JA}$ Thermal Impedance | 229.6°C/W |
| $\theta_{JC}$ Thermal Impedance | 91.99°C/W |
| Lead Temperature, Soldering | |
| Vapor Phase (60 sec) | 215°C |
| Infrared (15 sec) | 220°C |
| Pb-free Reflow Soldering | |
| Peak Temperature | 260(+0/−5)°C |
| Time at Peak Temperature | 10 sec to 40 sec |
| ESD | 2 kV |

[1] Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

**Table 5. Truth Table**

| ADG701 In | ADG702 In | Switch Condition |
|---|---|---|
| 0 | 1 | Off |
| 1 | 0 | On |

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

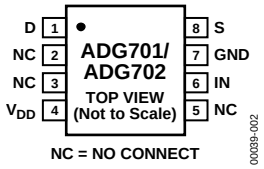


*Figure 2. 8-Lead MSOP*

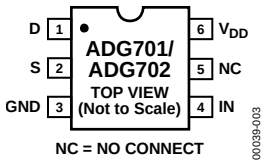


*Figure 3. 6-Lead SOT-23*

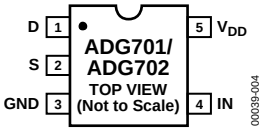


*Figure 4. 5-Lead SOT-23*

**Table 6. Pin Descriptions**

| Pin No. | | | | |
|---|---|---|---|---|
| **8-Lead MSOP** | **6-Lead SOT-23** | **5-Lead SOT-23** | **Mnemonic** | **Description** |
| 1 | 1 | 1 | D | Drain Terminal. Can be an input or output. |
| 2, 3, 5 | 5 | | NC | No Connect |
| 4 | 6 | 5 | $V_{DD}$ | Most Positive Power Supply Potential. |
| 6 | 4 | 4 | IN | Logic Control Input. |
| 7 | 3 | 3 | GND | Ground (0 V) Reference. |
| 8 | 2 | 2 | S | Source Terminal. Can be an input or output. |

# TYPICAL PERFORMANCE CHARACTERISTICS

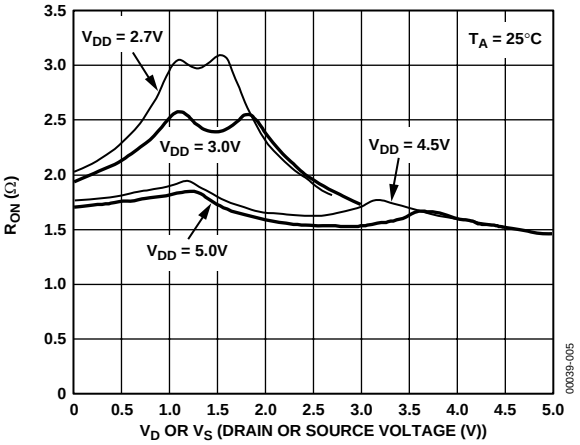


*Figure 5. On Resistance as a Function of $V_D$ ($V_S$) Single Supplies*

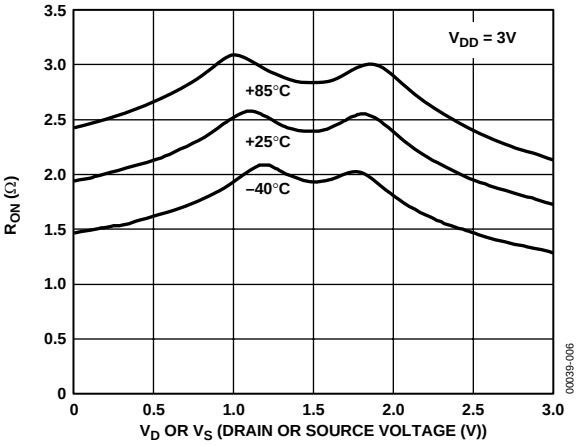


*Figure 6. On Resistance as a Function of $V_D$ ($V_S$) for Different Temperatures*
*$V_{DD}$ = 3 V*

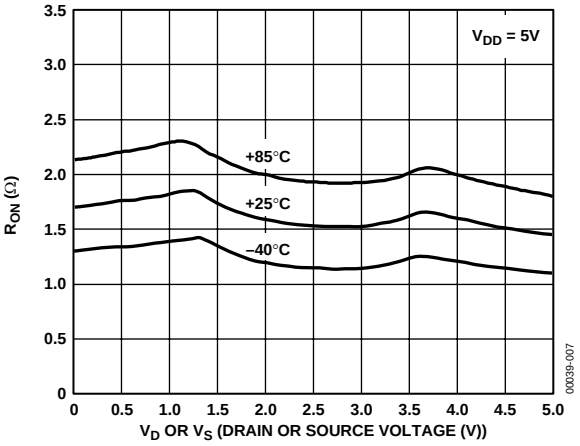


*Figure 7. On Resistance as a Function of $V_D$ ($V_S$) for Different Temperatures*
*$V_{DD}$ = 5 V*

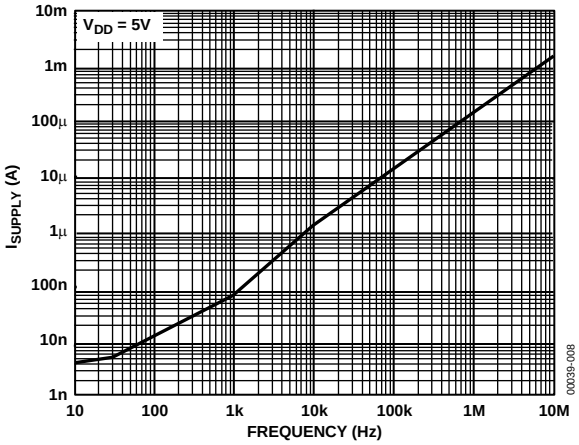


*Figure 8. Supply Current vs. Input Switching Frequency*

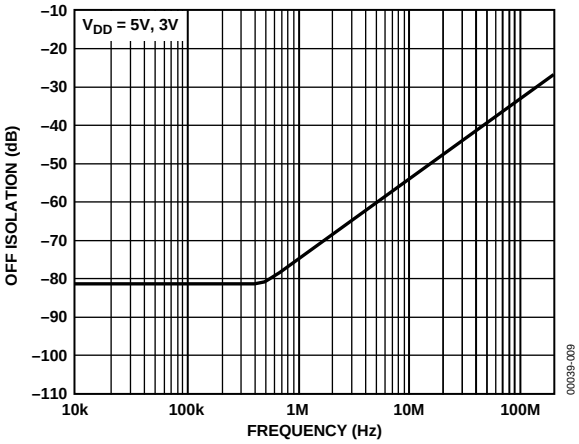


*Figure 9. Off Isolation vs. Frequency*

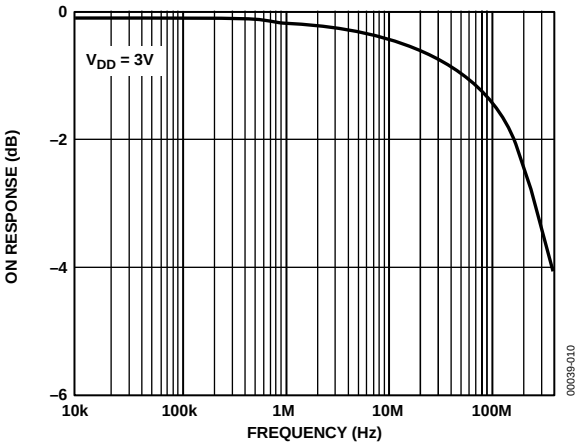


*Figure 10. Bandwidth*

# TERMINOLOGY

**Table 7.**

| Term | Description |
|---|---|
| $R_{ON}$ | Ohmic resistance between D and S. |
| $R_{FLAT(ON)}$ | Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range. |
| $I_S$ (OFF) | Source leakage current with the switch off. |
| $I_D$ (OFF) | Drain leakage current with the switch off. |
| $I_D$, $I_S$ (ON) | Channel leakage current with the switch on. |
| $V_D$ (VS) | Analog voltage on terminals D and S. |
| $C_S$ (OFF) | Off switch source capacitance. |
| $C_D$ (OFF) | Off switch drain capacitance. |
| $C_D$, $C_S$ (ON) | On switch capacitance. |
| $t_{ON}$ | Delay between applying the digital control input and the output switching on. See Figure 14. |
| $t_{OFF}$ | Delay between applying the digital control input and the output switching off. |
| Off Isolation | A measure of unwanted signal coupling through an off switch. |
| Charge Injection | A measure of the glitch impulse transferred from the digital input to the analog output during switching. |
| Bandwidth | The frequency at which the output is attenuated by −3 dB. |
| On Response | The frequency response of the on switch. |
| On Loss | The voltage drop across the on switch seen in Figure 10 as the number of decibels that the signal is from 0 dB at very low frequencies. |

# TEST CIRCUITS

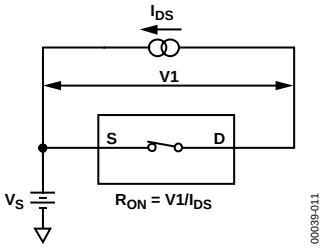


Figure 11. On Resistance

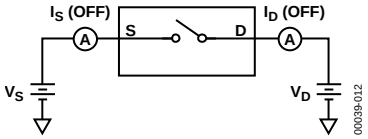


Figure 12. Off Leakage

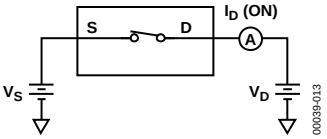


Figure 13. On Leakage

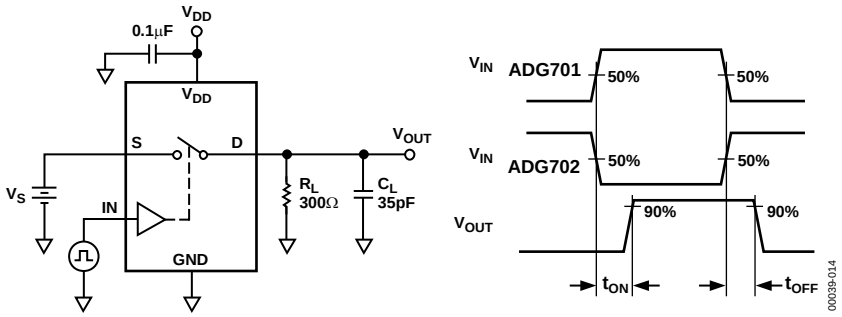


Figure 14. Switching Times

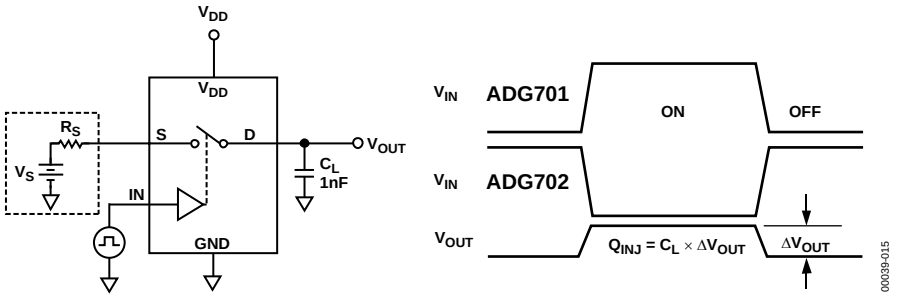


Figure 15. Charge Injection

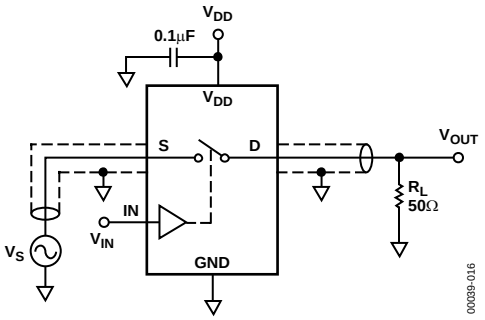


Figure 16. Off Isolation

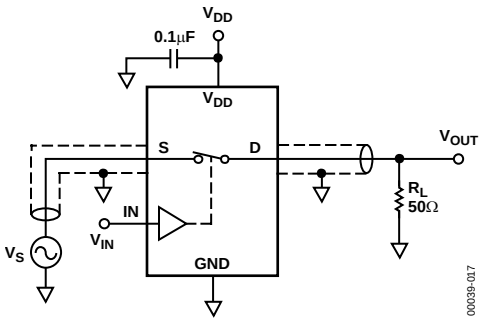


Figure 17. Bandwidth

# APPLICATIONS INFORMATION

The ADG701/ADG702 belong to the Analog Devices family of CMOS switches. This series of general-purpose switches has improved switching times, lower on resistance, higher bandwidth, low power consumption, and low leakage currents.

## ADG701/ADG702 SUPPLY VOLTAGES

Functionality of the ADG701/ADG702 extends from 1.8 V to 5.5 V single supply, making the parts ideal for battery-powered instruments, where power efficiency and performance are important design parameters.

It is important to note that the supply voltage affects the input signal range, on resistance, and switching times of the part. The effects of the power supplies can be clearly seen in the Typical Performance Characteristics and the Specifications sections.

For $V_{DD}$ = 1.8 V operation, $R_{ON}$ is typically 40 Ω over the temperature range.

## BANDWIDTH

Figure 18 illustrates the parasitic components that affect the ac performance of CMOS switches (a box surrounds the switch). Additional external capacitances further degrade performance by affecting feedthrough, crosstalk, and system bandwidth.

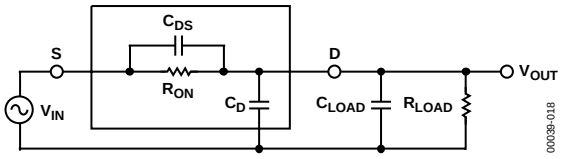


*Figure 18. Switch Represented by Equivalent Parasitic Components*

The transfer function that describes the equivalent diagram of the switch (see Figure 18) is of the form (A)s, shown in the following equation:

$$A(s) = R_T\left[\frac{s(R_{ON}C_{DS})+1}{s(R_{ON}C_TR_T)+1}\right]$$

where $C_T = C_{LOAD} + C_D + C_{DS}$.

The signal transfer characteristic is dependent on the switch channel capacitance, $C_{DS}$. This capacitance creates a frequency zero in the numerator of the transfer function A(s). Because the switch on resistance is small, this zero usually occurs at high frequencies. The bandwidth is a function of the switch output capacitance combined with $C_{DS}$ and the load capacitance. The frequency pole corresponding to these capacitances appears in the denominator of A(s).

The dominant effect of the output capacitance, $C_D$, causes the pole breakpoint frequency to occur first. To maximize bandwidth, a switch must have a low input and output capacitance and low on resistance. The on response vs. frequency for the ADG701/ADG702 can be seen in Figure 10.

## OFF ISOLATION

Off isolation is a measure of the input signal coupled through an off switch to the switch output. The capacitance, $C_{DS}$, couples the input signal to the output load when the switch is off, as shown in Figure 19.

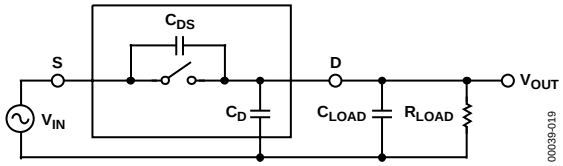


*Figure 19. Off Isolation Is Affected by External Load Resistance and Capacitance*

The larger the value of $C_{DS}$, the larger the values of feedthrough produced. Figure 9 illustrates the drop in off isolation as a function of frequency. From dc to roughly 1 MHz, the switch shows better than −75 dB isolation. Up to frequencies of 10 MHz, the off isolation remains better than −55 dB. As the frequency increases, more of the input signal is coupled through to the output. Off isolation can be maximized by choosing a switch with the smallest $C_{DS}$ possible. The values of load resistance and capacitance also affect off isolation, because they contribute to the coefficients of the poles and zeros in the transfer function of the switch when open.

$$A(s) = R_T\left[\frac{s(R_{LOAD}C_{DS})+1}{s(R_{LOAD})(C_T)+1}\right]$$

# OUTLINE DIMENSIONS

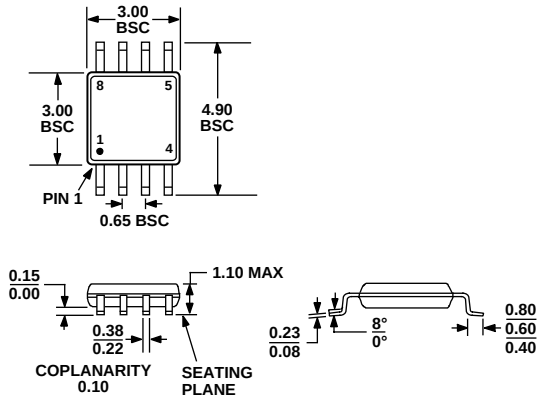


*Figure 20. 8-Lead Mini Small Outline Package [MSOP]*
*(RM-8)*
*Dimensions shown in millimeters*

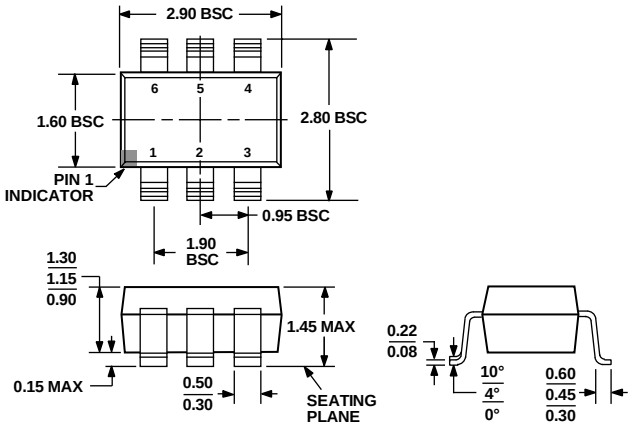


*Figure 21. 6-Lead Small Outline Transistor Package [SOT-23]*
*(RT-6)*
*Dimensions shown in millimeters*

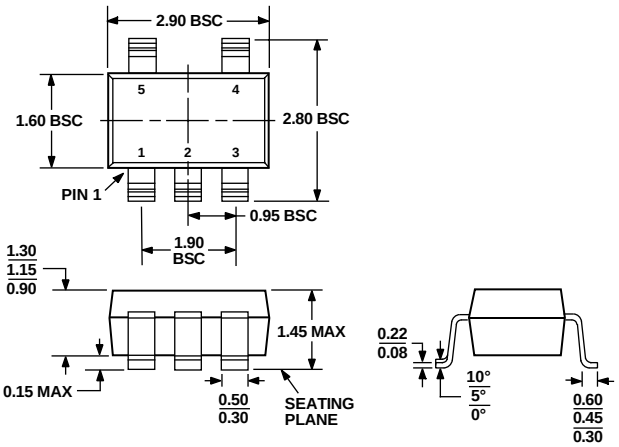


*Figure 22. 5-Lead Small Outline Transistor Package [SOT-23]*
*(RJ-5)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Package Description | Package Option | Branding |
|---|---|---|---|
| ADG701BRJ-500RL7 | 5-Lead Small Outline Transistor Package [SOT-23] | RJ-5 | S3B |
| ADG701BRJ-REEL | 5-Lead Small Outline Transistor Package [SOT-23] | RJ-5 | S3B |
| ADG701BRJ-REEL7 | 5-Lead Small Outline Transistor Package [SOT-23] | RJ-5 | S3B |
| ADG701BRM | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | S3B |
| ADG701BRM-REEL | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | S3B |
| ADG701BRM-REEL7 | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | S3B |
| ADG701BRT-REEL | 6-Lead Small Outline Transistor Package [SOT-23] | RT-6 | S3B |
| ADG701BRT-REEL7 | 6-Lead Small Outline Transistor Package [SOT-23] | RT-6 | S3B |
| ADG701BRJZ-500RL7[1] | 5-Lead Small Outline Transistor Package [SOT-23] | RJ-5 | S3B# |
| ADG701BRJZ-REEL[1] | 5-Lead Small Outline Transistor Package [SOT-23] | RJ-5 | S3B# |
| ADG701BRJZ-REEL7[1] | 5-Lead Small Outline Transistor Package [SOT-23] | RJ-5 | S3B# |
| ADG701BRMZ[1] | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | S0S |
| ADG701BRMZ-REEL7[1] | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | S0S |
| ADG701BRTZ-REEL[1] | 6-Lead Small Outline Transistor Package [SOT-23] | RT-6 | S3B# |
| ADG701BRTZ-REEL7[1] | 6-Lead Small Outline Transistor Package [SOT-23] | RT-6 | S3B# |
| ADG702BRJ-500RL7 | 5-Lead Small Outline Transistor Package [SOT-23] | RJ-5 | S4B |
| ADG702BRJ-REEL | 5-Lead Small Outline Transistor Package [SOT-23] | RJ-5 | S4B |
| ADG702BRJ-REEL7 | 5-Lead Small Outline Transistor Package [SOT-23] | RJ-5 | S4B |
| ADG702BRM | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | S4B |
| ADG702BRM-REEL | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | S4B |
| ADG702BRM-REEL7 | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | S4B |
| ADG702BRT-REEL | 6-Lead Small Outline Transistor Package [SOT-23] | RT-6 | S4B |
| ADG702BRT-REEL7 | 6-Lead Small Outline Transistor Package [SOT-23] | RT-6 | S4B |
| ADG702BRJZ-500RL7[1] | 5-Lead Small Outline Transistor Package [SOT-23] | RJ-5 | S14 |
| ADG702BRJZ-REEL[1] | 5-Lead Small Outline Transistor Package [SOT-23] | RJ-5 | S14 |
| ADG702BRJZ-REEL7[1] | 5-Lead Small Outline Transistor Package [SOT-23] | RJ-5 | S14 |
| ADG702BRMZ[1] | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | S14 |
| ADG702BRMZ-REEL7[1] | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | S14 |
| ADG702BRTZ-REEL[1] | 6-Lead Small Outline Transistor Package [SOT-23] | RT-6 | S4B# |
| ADG702BRTZ-REEL7[1] | 6-Lead Small Outline Transistor Package [SOT-23] | RT-6 | S4B# |

[1] Z = Pb-free part, # denotes lead-free product, may be top or bottom marked.

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