

# 130-dB, 32-Bit High-Performance DAC with Integrated Headphone Driver and Impedance Detection

System Features	Direct Stream Digital (DSD <sup>®</sup> ) path
• Enhanced $\Delta\Sigma$ oversampling DAC architecture	<ul> <li>Patented DSD processor</li> </ul>
— 32-bit resolution	<ul> <li>On-chip 50-kHz filter to meet Scarlet Book Super</li> </ul>
<ul> <li>Up to 384-kHz sampling rate</li> </ul>	Audio Compact Disk (SACD) recommendations
<ul> <li>Low clock jitter sensitivity</li> </ul>	<ul> <li>Matched PCM and DSD analog output levels</li> </ul>
— Auto mute detection	<ul> <li>Nondecimating volume control with 0.5-dB step size and soft ramp</li> </ul>
<ul> <li>Integrated high performance, ground-centered stereo headphone outputs</li> </ul>	<ul> <li>DSD and Pulse-code modulation (PCM) mixing for alerts</li> </ul>
<ul> <li>— 130-dB dynamic range (A-weighted)</li> </ul>	<ul> <li>Dedicated DSD and DoP pin interface</li> </ul>
<ul> <li>— –108-dB total harmonic distortion + noise (THD+N)</li> </ul>	Serial audio input path
<ul> <li>— 110-dB interchannel isolation</li> </ul>	— Five selectable digital filter responses
<ul> <li>Headphone power output</li> </ul>	<ul> <li>Low-latency mode minimizes pre-echo</li> </ul>
– 30 mW per channel into 32 $\Omega$	<ul> <li>– 110 dB of stopband attenuation</li> </ul>
– 5 mW per channel into 600 $\Omega$	<ul> <li>Supports sample rates from 32 to 384 kHz</li> </ul>
Headphone detection	— I <sup>2</sup> S, right-justified, left-justified, TDM, and
<ul> <li>Headphone DC and AC impedance measurement</li> </ul>	DSD-over-PCM (DoP) interface
<ul> <li>Headphone plug-in detection</li> </ul>	<ul> <li>Master or slave operation</li> </ul>
<ul> <li>Popguard<sup>®</sup> technology eliminates pop noise</li> </ul>	<ul> <li>Volume control with 0.5-dB step size and soft ramp</li> </ul>
Integrated PLL	<ul> <li>— 44.1 kHz deemphasis and inverting feature</li> </ul>
- Support for 11.2896-/22.5792-, 12.288-/24.576-, 9.6-/	<ul> <li>Alternate headphone input</li> </ul>
19.2-, 12-/24-, and 13-/26-MHz system MCLK rates	<ul> <li>40-pin QFN or 42-ball CSP package option</li> </ul>
Reference clock sourced from X11/MCLK pin	Applications
— System clock output	Smart phones, tablets, portable media players, lantons
Mono mode support	digital headphones, powered speakers, AVR, home

I<sup>2</sup>C control—up to 1 MHz

theater systems, Blu-ray/DVD/SACD players and pro audio







## **General Description**

The CS43130 is a high-performance, 32-bit resolution, stereo audio DAC that supports up to 384-kHz sampling frequency with integrated low-noise ground-centered headphone amplifiers. The advanced 32-bit oversampled multibit modulator with mismatch shaping technology eliminates distortion due to on-chip component mismatch. Proprietary digital-interpolation filters support five selectable filter responses with pseudo-linear phase and ultralow latency to minimize pre-echos and ringing artifacts. Other features include volume control with 0.5-dB steps and digital deemphasis for 44.1-kHz sample rate.

The integrated ground-centered stereo headphone amplifiers are capable of delivering more than 30 mW into  $32-\Omega$  load or 5 mW into  $600-\Omega$  load per channel. Proprietary headphone impedance detection enables wide-band impedance detection for further digital post-processing. An internal stereo audio switch with true bypass supports an alternate analog input path for interfacing with external audio sources to minimize the overall bill-of-materials cost and PCB area.

The patented on-chip DSD processor preserves audio integrity by allowing signal processing such as volume control and 50-kHz Scarlet Book recommended filtering to be applied directly to the DSD stream without an intermediate decimation stage. Additional features like volume matching and channel mixing enable seamless transition between DSD and PCM playback paths.

The CS43130 accepts I<sup>2</sup>S, right-justified, left-justified, and TDM-format PCM data at sample rates from 32 to 384 kHz. The industry-standard high-speed I<sup>2</sup>C interface capable of up to 1-MHz operation provides easy configuration control. An integrated PLL allows for maximum clocking flexibility in any system. Popguard<sup>®</sup> technology eliminates output transients upon power-up or power-down events.

The CS43130 is available in a commercial-grade 42-ball WLCSP or 40-pin QFN package for operation from –10°C to +70°C.



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# 1 Pin Assignments and Descriptions

# 1.1 40-Pin QFN (Top-Down, Through-Package View)



Figure 1-1. Top-Down (Through-Package) View-QFN 40-Pin Diagram



## 1.2 42-Ball WLCSP (Top-down, Through-Package View)



Figure 1-2. Top-Down (Through-Package) View—42-Ball WLCSP Package



# 1.3 Pin Descriptions

### Table 1-1. Pin Descriptions

Pin Name	QFN Pin #	WLCSP Ball	Power Supply	I/O	Pin Description	Internal Connection	Digital I/O Driver	Digital I/O Receiver
					Digital I/O			
ADR	30	C2	VL	Ι	Address Bit (I <sup>2</sup> C). In I <sup>2</sup> C Mode, ADR is a chip address pin.	—		
CLKOUT	33	B2	VL	0	<b>CLK Output.</b> Single-ended clock output sourced from PLL or buffered crystal.	Weak pull-down	CMOS output	_
SCLK1	34	A2	VL	I/O	Serial Audio Input Bit Clock 1. Serial bit clock for audio data on	Weak	CMOS	Hysteresis
					the SDIN pins.	pull-down	output	on CMOS input
LRCK1	38	В3	VL	1/0	Serial Audio Input Left/Right Clock. Word-rate clock for the audio data on the SDIN pins.	Weak pull-down	CMOS output	Hysteresis on CMOS input
SDIN1	2	A6	VL	Ι	Serial Audio Input Data Port. Audio data serial input pin 1.	Weak pull-down	_	Hysteresis on CMOS input
DSDA/ SDIN2	40	A5	VL	I	<b>DSD Data Input A/Serial Data In 2.</b> DSD audio or PCM audio data serial input pin 2.	Weak pull-down	_	Hysteresis on CMOS input
DSDB/ LRCK2	29	C1	VL	I/O	<b>DSD Data Input B/Serial Audio Input Left/Right Clock 2.</b> DSD audio data serial input pin or word rate clock for the audio data on the SDIN2 pin.	Weak pull-down	CMOS output	Hysteresis on CMOS input
DSDCLK/ SCLK2	32	B1	VL	I/O	<b>DSD Clock Input/Serial Audio Input Bit Clock 2.</b> DSD clock input. Serial bit clock for audio data on the SDIN2 pin.	Weak pull-down	CMOS output	Hysteresis on CMOS input
INT	27	C5	VP	0	<b>Interrupt.</b> When pulled up, works as system interrupt pin. Open drain, active low programmable.	_	CMOS open-drain output	
RESET	28	C4	VP	I	System Reset. The device enters system reset when enabled.	_		Hysteresis on CMOS input
SDA	39	B4	VL	I/O	Serial Control Data I/O (I <sup>2</sup> C). In I <sup>2</sup> C Mode, SDA is the control I/O data line.	_	CMOS open-drain output	Hysteresis on CMOS input
SCL	1	B5	VL	I	<b>Software Clock (I<sup>2</sup>C).</b> Serial control interface clock used to clock control data bits into and out of the CS43130.	_		Hysteresis on CMOS input
XTI/MCLK	37	A4	VL	I	Crystal/Oscillator Input/MCLK In. Crystal or digital clock input for the master clock.	Weak pull-down	—	Hysteresis on CMOS input
ХТО	36	A3	VL	0	Crystal/Oscillator Output. Crystal output.	Weak pull-down	CMOS output	_
					Analog I/O 🔵			
FILT+ FILT–	5 6	D4 D5	VA	0	<b>Positive/Negative Voltage Reference.</b> Positive/negative reference voltage for DAC.		—	—
HP_ DETECT	22	F4	VP	I	<b>Headphone Detect.</b> Can be configured to be debounced on unplugged and plugged events before it is presented as a noninterrupt status bit (HPDETECT).	_	Hi-Z	_
HPINB	15	F3	VCP_	Ι	Headphone Audio Input. For interfacing low power audio source,	Weak	_	—
HPINA	12	G5	FILT±		an alternate analog input path for the headphone output. Refer to analog specification table for full-scale input level.	pull-down		
HPOUTB HPOUTA	16 14	G3 G4	VCP_ FILT±	0	Headphone Audio Output. Refer to analog specification table for full-scale output level.	—	_	_
HPREFB HPREFA	17 13	E3 E4	VCP_ FILT±	I	Headphone Output Reference. Reference for headphone amplifier and detect.	—	_	_
					Power Supplies 🥢			
VL	31	A1	N/A	Ι	Logic Power. Input/Output power supply, typically +1.8 V.	_	_	_
					· · · · · · ·			



Pin Name	QFN Pin #	WLCSP Ball	Power Supply	I/O	Pin Description	Internal Connection	Digital I/O Driver	Digital I/O Receiver	
VD	4	C6	N/A	I	<b>Internal Digital Power.</b> Internal digital power supply, typically +1.8 V.		_	—	
VA	7	D6	N/A	I	Analog Power. Power supply for the internal analog section.	_	—	_	
VCP	25	D2	N/A	I	<b>Charge Pump Supply</b> . Provides charge pump voltage to the headphone Class H analog output circuit.	—	_	—	
VP	26	D1	N/A	I	<b>Battery supply</b> . Provides voltage to the headphone Class H circuit.	—	_	_	
	Ground 🔴								
GNDD	35	C3	N/A	Ι	<b>Digital and I/O Ground.</b> Ground for the I/O and core logic. GNDA, GNDCP, and GNDD must be connected to a common ground area under the chip.	_	_		
GNDA	8	E5	N/A	I	<b>Analog Ground.</b> Ground reference for the internal analog section. GNDA, GNDCP, and GNDD must be connected to a common ground area under the chip.	_	_	_	
GNDCP	19	F2	N/A	I	<b>Charge Pump Ground.</b> Ground reference for the charge pump section. GNDA, GNDCP, and GNDD must be connected to a common ground area under the chip.	_	_	_	
					Charge Pump 🚫				
VCP_FILT+	21	E2	VCP/	I/O	Inverting Charge Pump Filter Connection. Power supply from	_		_	
VCP_FILT-	18	G2	VP 1		the inverting charge pump that provides the positive/negative rail for the analog output. When operating in external VCP_FILT mode, these pins can directly take in supply voltage.				
–VA	9	E6	VA	0	VA Negative Charge Pump Output. Negative charge pump output for DAC rail. It is derived from VA.	_	_	_	
FLYP_VA	10	F6	VA	0	-VA Charge Pump Cap Positive/Negative Node. Positive/	—			
FLYN_VA	11	G6			negative nodes for the DAC negative charge pump's flying capacitor.				
FLYP_VCP	24	E1	VCP/ VP 1	0	<b>-VCP Charge Pump Cap Positive Node</b> . Positive node for the analog output negative charge pump's flying capacitor.	_	_	_	
FLYC_VCP	23	F1	VCP/ VP 1	0	-VCP Charge Pump Cap Center Node. Center node for the analog output negative charge pump's flying capacitor.	—	—	—	
FLYN_VCP	20	G1	VCP_ FILT±	0	<b>-VCP Charge Pump Cap Negative Node.</b> Negative node for the analog output negative charge pump's flying capacitor.	—	—	—	
					Test				
TSO	3	B6	N/A	I/O	Test Output.	—		_	
TSI	_	D3, F5			Test Input.	_	_		

#### Table 1-1. Pin Descriptions (Cont.)

1. The power supply is determined by ADPT\_PWR setting (see Section 4.3.1). VP is used if ADPT\_PWR = 001 (VP\_LDO Mode) or when necessary for ADPTPWR = 111 (Adapt-to-Signal Mode).



## 1.4 Electrostatic Discharge (ESD) Protection Circuitry



ESD-sensitive device. The CS43130 is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to current JEDEC ESD standards.

Fig. 1-3 provides a composite view of the ESD domains showing the ESD protection paths between each pad and the substrate (GND), as well as the interrelations between some domains. Note that this figure represents the structure for the internal protection devices and that additional protections can be implemented as part of the integration into the board.



Figure 1-3. Composite ESD Topology

Table 1-2 shows the individual ESD domains and lists the pins associated with each domain.

Table 1-2. ESD Domains

ESD Domain	Signal Name (See * in Topology Figures for Pad)	Тороlоду
VL/GNDD	ADR DSDCLK/SCLK2 SCL SDA DSDB/LRCK2 DSDA/SDIN2 SDIN1 LRCK1 SCLK1 CLKOUT XTI/MCLK XTO	GNDD GNDD Substrate



## Table 1-2. ESD Domains (Cont.)

ESD Domain	Signal Name (See * in Topology Figures for Pad)	Тороlоду
VA/–VA	FLYN_VA FLYP_VA FILT+ FILT-	GNDA Substrate Substrate
VP/GNDCP VP/VCP_FILT- VCP_FILT+/ VCP_FILT-	RESET INT FLYP_VCP FLYC_VCP HP_DETECT FLYN_VCP HPINA HPOUTA HPOUTA HPREFA HPREFB	VP/GNDCP Domain VCP_FILT-Domain VCP_FILT-Domain VCP_FILT- Substrate



## 2 Typical Connection Diagram



#### Figure 2-1. Typical Connection Diagram

#### **Note:** 1. The value for $R_{P,I}$ can be determined by the interrupt pin specification in Table 3-11.



# **3** Characteristics and Specifications

Table 3-1 defines parameters as they are characterized in this section.

#### Table 3-1. Parameter Definitions

Parameter	Definition
Dynamic range	The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. A signal-to-noise ratio measurement over the specified bandwidth made with a –60-dB signal; 60 dB is added to resulting measurement to refer the measurement to full scale. This technique ensures that distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17–1991, and the Electronic Industries Association of Japan, EIAJ CP–307. Dynamic range is expressed in decibel units.
Gain drift	The change in gain value with temperature, expressed in ppm/°C units.
Idle channel noise	The rms value of the signal with no input applied (properly back-terminated analog input, digital zero, or zero modulation input). Measured over the specified bandwidth.
Interchannel gain mismatch	The gain difference between left and right channel pairs. Interchannel gain mismatch is expressed in decibel units.
Interchannel phase mismatch	The phase difference between left and right channel pairs at 997-Hz sine wave input. Interchannel phase mismatch is expressed in degree units (with respect to 997-Hz sine wave input).
Interchannel isolation	A measure of cross talk between the left and right channel pairs. Interchannel isolation is measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Interchannel isolation is expressed in decibel units.
Load resistance and capacitance	The recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. The load capacitance effectively moves the band-limiting pole of the amp in the output stage. Increasing load capacitance beyond the recommended value can cause the internal op-amp to become unstable.
Output offset voltage	The DC offset voltage present at the amplifier's output when its input signal is in a mute state. The offset exists due to CMOS process limitations and is proportional to analog volume settings. When measuring the offset out of the headphone amplifier, the headphone amplifier is ON.
Total harmonic distortion + noise (THD+N)	The ratio of the rms sum of distortion and noise spectral components across the specified bandwidth (typically 20 Hz–20 kHz) relative to the rms value of the signal. THD+N is measured at –1 and –20 dBFS for the analog input and at 0 and –20 dB for the analog output, as suggested in AES17–1991 Annex A. THD+N is expressed in decibel units.
Turn-on time	Turn-on time is measured from when the PDN_HP = 0 ACK signal is received to when the signal appears on the HP output.

### Table 3-2. Recommended Operating Conditions

GNDD = GNDA= GNDCP = 0 V, all voltages with respect to ground.

	Parameters	1	Symbol	Minimum	Maximum	Units
DC power supply	Analog		VA	1.66	1.94	V
	Charge pump		VCP	1.66	1.94	V
	Filtered charge pump	EXT_VCPFLT = 1	VCP_FILT+	2.85	3.15	V
			VCP_FILT-	-3.15	-2.85	V
	Battery supply	HV_EN = 0, EXT_VCPFILT = 0 HV_EN = 1, EXT_VCPFILT = 0 EXT_VCPFILT = 1	VP	3.0 3.3 3.3	5.25 5.25 5.25	V V V
	Digital Interface		VL	1.66	1.94	V
	Digital Internal		VD	1.66	1.94	V
External voltage applied to pin <sup>2,3</sup>		HP_DETECT pin VCP_FILT± domain pins <sup>4</sup> VL domain pins VA domain pins VP domain pins	V <sub>INHI</sub> Vvcpf V <sub>VL</sub> Vva Vvp	-0.3 - VCP_FILT- -0.3 - VCP_FILT- -0.3 -0.3 -0.3	VP + 0.3 0.3 + VCP_FILT+ VL + 0.3 VA + 0.3 VP + 0.3	V V V V
Ambient temperatur	e		T <sub>A</sub>	-10	+70	°C

1. Device functional operation is guaranteed within these limits. Functionality is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.

2. The maximum over/undervoltage is limited by the input current.

3. Table 1-1 lists the power supply domain in which each CS43130 pin resides.

4.VCP\_FILT± is specified in Table 3-16.



#### Table 3-3. Absolute Maximum Ratings

GNDD = GNDA= GNDCP = 0 V; all voltages with respect to ground.

Parameters	Symbol	Minimum	Maximum	Units	
DC power supply	Analog	VA	-0.3	2.33	V
	Battery	VP	-0.3	6.3	V
	Charge pump	VCP	-0.3	2.33	V
	Filtered charge pump (positive)	VCP_FILT+	-0.3	3.3	V
	Filtered charge pump (negative)	VCP_FILT-	0.3	-3.3	V
	Digital interface	VL	-0.3	2.33	V
	Digital internal	VD	-0.3	2.33	V
Input current <sup>1</sup>		l <sub>in</sub>	_	±10	mA
Ambient operating temperature (power applied)		T <sub>A</sub>	-50	+115	°C
Storage temperature		T <sub>stg</sub>	-65	+150	°C

**Caution:** Stresses beyond "Absolute Maximum Ratings" levels may cause permanent damage to the device. These levels are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Table 3-2, "Recommended Operating Conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. Any pin except supplies and HPINx. Transient currents of up to ±100 mA on the analog input pins do not cause SCR latch-up.

#### Table 3-4. Analog Output Characteristics (HV\_EN = 1) 1

Test conditions (unless otherwise specified): Fig. 2-1 shows CS43130 connections; input test signal is a 32-bit, full-scale 997-Hz sine wave (unless specified otherwise); GNDA = GNDCP = GNDD = 0 V; voltages are with respect to ground; HV\_EN = 1; ASP\_M/Sb = 1; typical, min/max performance data taken with VA = VCP = 1.8 V; VL = VD = 1.8 V; VP = 3.6 V; TA = +25°C; measurement bandwidth is 20 Hz–20 kHz; ASP\_SPRATE = 0001 (LRCK = 44.1-kHz mode); PDN\_XTAL = 0, MCLK\_INT = 1, and MCLK\_SRC\_SEL = 00 (crystal frequency f<sub>XTAL</sub> = 22.5792 MHz); Volume = 0 dB; when testing in DSD processor mode, DSD\_ZERODB = 1; when testing noise related specifications (dynamic range, THD+N, idle channel noise), no external impedance on HPREFx.

	PCM and DSD Proces	sor Mode Parameter <sup>2,3,4</sup>		Minimum	Typical	Maximum	Units
HPOUTx R <sub>L</sub> = 10 kΩ	Dynamic range (defined in Table 3-1)	24-bit, 32-bit, DSD	A-weighted Unweighted	124 121	130 127	_	dB dB
$C_{L} = 200 \text{ pF}$ OUT_FS = 11	, , , , , , , , , , , , , , , , , , ,	16-bit	A-weighted Unweighted	91 88	97 94	_	dB dB
Volume = 0 dB <sup>5</sup> , unless otherwise specified	THD+N (defined in Table 3-1)	24-bit, 32-bit, DSD	0 dB 20 dB	_	-108 -97	-101	dB dB
		16-bit	–60 dB 0 dB –20 dB –60 dB	 	67 94 74 34	61 88  28	dB dB dB dB
	Idle channel noise (A-weighted) (defined in Table 3-1)	24-bit, 32-bit, DSD		_	0.55	_	μV
	Full-scale output voltage	e		4.66	4.90	5.14	Vpp
	Interchannel isolation 6	(defined in Table 3-1)	217 Hz 1 kHz 20 kHz		110 95 68		dB dB dB
HPOUTx $R_L = 600 \Omega$ $C_L = 200 pF$ $OUT_FS = 11$	Dynamic range (defined in Table 3-1)	24-bit, 32-bit, DSD 16-bit	A-weighted Unweighted A-weighted Unweighted	124 121 91 88	130 127 97 94	 	dB dB dB dB
Volume = 0 dB <sup>5</sup> , unless otherwise specified	THD+N (defined in Table 3-1)	24-bit, 32-bit, DSD 16-bit	0 dB -20 dB -60 dB 0 dB -20 dB -60 dB		-108 -97 -67 -94 -74 -34	-101 61 88  -28	dB dB dB dB dB dB
	Idle channel noise (A-weighted) (defined in Table 3-1)	24-bit, 32-bit, DSD		_	0.55	_	μV
	Full-scale output voltage	e		4.66	4.90	5.14	Vpp
	Output power			—	5	—	mW
	Interchannel isolation 6	(defined in Table 3-1)	217 Hz 1 kHz 20 kHz		110 95 68		dB dB dB



#### Table 3-4. Analog Output Characteristics (HV\_EN = 1) 1 (Cont.)

Test conditions (unless otherwise specified): Fig. 2-1 shows CS43130 connections; input test signal is a 32-bit, full-scale 997-Hz sine wave (unless specified otherwise); GNDA = GNDCP = GNDD = 0 V; voltages are with respect to ground; HV\_EN = 1; ASP\_M/Sb = 1; typical, min/max performance data taken with VA = VCP = 1.8 V; VL = VD = 1.8 V; VP = 3.6 V; TA = +25°C; measurement bandwidth is 20 Hz–20 kHz; ASP\_SPRATE = 0001 (LRCK = 44.1-kHz mode); PDN\_XTAL = 0, MCLK\_INT = 1, and MCLK\_SRC\_SEL = 00 (crystal frequency  $f_{XTAL}$  = 22.5792 MHz); Volume = 0 dB; when testing in DSD processor mode, DSD\_ZERODB = 1; when testing noise related specifications (dynamic range, THD+N, idle channel noise), no external impedance on HPREFx.

	PCM and DSD Processor Mode Parameter <sup>2,3,4</sup>		Minimum	Typical	Maximum	Units
Other characteristics for HPOUTx	Interchannel gain mismatch (defined in Table 3-1)		_	±0.1	—	dB
	Interchannel phase mismatch (defined in Table 3-1)		_	±0.05	—	0
	Output offset voltage: Mute (defined in Table 3-1)		_	±0.5	±1	mV
	Gain drift (defined in Table 3-1)		_	±100	—	ppm/°C
	Load resistance (RL)		600	_	—	Ω
	Load capacitance (CL)		_	_	1	nF
	Turn-on time (defined in Table 3-1)		_	_	10	ms
	Click/pop during PDN_HP enable or disable	A-weighted	_	_	-60	dBV

1. This table also applies to external VCP\_FILT supply mode: CS43130 power up procedure is per description in Section 5.10.1; EXT\_VCPFILT = 1;

VCP\_FILT+ and VCP\_FILT- comply to Table 3-2 when EXT\_VCPFILT = 1; in this mode, HV\_EN setting becomes don't care.

2.One LSB of triangular PDF dither is added to PCM data.

3. Referred to the typical full-scale voltage. Applies to all THD+N and dynamic range values in the table.

4.DSD performance may be limited by the source recording. 0 dB-SACD = 50% modulation index.

5. The volume must be configured as indicated to achieve specified output characteristics.

6. Output test configuration. Symbolized component values are specified in the test conditions.



#### Table 3-5. Analog Output Characteristics (HV\_EN = 0) <sup>1</sup>

Test conditions (unless otherwise specified): Fig. 2-1 shows CS43130 connections; input test signal is a 32-bit, full-scale 997-Hz sine wave (unless specified otherwise); GNDA = GNDCP = GNDD = 0 V; voltages are with respect to ground; HV\_EN = 0; ASP\_M/Sb = 1; typical, min/max performance data taken with VA = VCP = 1.8 V; VL = VD = 1.8 V; VP = 3.6 V; TA =  $+25^{\circ}$ C; measurement bandwidth is 20 Hz–20 kHz; ASP\_SPRATE = 0001 (LRCK = 44.1-kHz mode); PDN\_XTAL = 0, MCLK\_INT = 1, and MCLK\_SRC\_SEL = 00 (crystal frequency f<sub>XTAL</sub> = 22.5792 MHz); Volume = 0 dB; when testing in DSD processor mode, DSD\_ZERODB = 1; when testing noise related specifications (dynamic range, THD+N, idle channel noise), no external impedance on HPREFx.

	PCM and DSD Process	or Mode Parameter <sup>2,3,4</sup>		Minimum	Typical	Maximum	Units
$\begin{array}{l} HPOUTx;\\ R_L = 10 \ k\Omega\\ C_L = 200 \ pF\\ OUT_FS = 10\\ Volume = 0 \ dB, 5\\ unless \ otherwise\\ specified \end{array}$	Dynamic range (defined in Table 3-1)	24-bit, 32-bit, DSD	A-weighted	122 119	128 125		dB dB
		16-bit	A-weighted Unweighted	91 88	97 94	_	dB dB
	THD+N (defined in Table 3-1)	24-bit, 32-bit, DSD	0 dB –20 dB –60 dB		-109 -95 -65	-103 	dB dB dB
		16-bit	0 dB -20 dB -60 dB		-94 -74 -34	-88 	dB dB dB
	Idle channel noise (A-weighted) (defined in Table 3-1)	24-bit, 32-bit, DSD		_	0.55	_	μV
	Full-scale output voltage	)		3.76	3.96	4.16	Vpp
	Interchannel isolation <sup>6</sup> (	defined in Table 3-1)	217 Hz 1 kHz 20 kHz		110 94 68	— — —	dB dB dB



#### Table 3-5. Analog Output Characteristics (HV\_EN = 0) <sup>1</sup> (Cont.)

Test conditions (unless otherwise specified): Fig. 2-1 shows CS43130 connections; input test signal is a 32-bit, full-scale 997-Hz sine wave (unless specified otherwise); GNDA = GNDCP = GNDD = 0 V; voltages are with respect to ground; HV\_EN = 0; ASP\_M/Sb = 1; typical, min/max performance data taken with VA = VCP = 1.8 V; VL = VD = 1.8 V; VP = 3.6 V; TA = +25°C; measurement bandwidth is 20 Hz–20 kHz; ASP\_SPRATE = 0001 (LRCK = 44.1-kHz mode); PDN\_XTAL = 0, MCLK\_INT = 1, and MCLK\_SRC\_SEL = 00 (crystal frequency f<sub>XTAL</sub> = 22.5792 MHz); Volume = 0 dB; when testing in DSD processor mode, DSD\_ZERODB = 1; when testing noise related specifications (dynamic range, THD+N, idle channel noise), no external impedance on HPREFx.

	PCM and DSD Process	or Mode Parameter 2,3,4		Minimum	Typical	Maximum	Units
HPOUTx; R <sub>L</sub> = 600 Ω C <sub>1</sub> = 200 pF	Dynamic range (defined in Table 3-1)	24-bit, 32-bit, DSD	A-weighted Unweighted	122 119	128 125		dB dB
OUT_FS = 10		10-DI	A-weighted Unweighted	91 88	97 94	_	dB dB
Volume = 0 dB, unless otherwise specified	THD+N (defined in Table 3-1)	24-bit, 32-bit, DSD	0 dB –20 dB		-109 -95	-103 	dB dB
		16-hit	–60 dB 0 dB	_	-65 -94	-59 -88	dB dB
		10 51	–20 dB	_	-74		dB
			–60 dB	—	-34	-28	dB
	(A-weighted) (defined in Table 3-1)	24-dit, 32-dit, DSD		_	0.55	_	μv
	Full-scale output voltage	e		3.76	3.96	4.16	Vpp
	Output power			—	3.3	—	mW
	Interchannel isolation <sup>6</sup>	(defined in Table 3-1)	217 Hz	—	110	-	dB dB
			20 kHz	_	68	_	dB
HPOUTx;	Dynamic range	24-bit, 32-bit, DSD	A-weighted	119	125	—	dB
$R_L = 32 \Omega$ $C_L = 200 pF$	(defined in Table 3-1)	16-bit	Unweighted A-weighted	116 91	122 97		dB dB
$OUT_FS = 01$		TO SIC	Unweighted	88	94	_	dB
unless otherwise	THD+N	24-bit, 32-bit, DSD	0 dB	_	-106	-96	dB
specified	(defined in Table 3-1)		–20 dB –60 dB	_	-92 -62	-56	dB dB
		16-bit	0 dB	_	-94	-88	dB
			–20 dB –60 dB	_	-74 -34		dB dB
	Idle channel noise	24-bit. 32-bit. DSD	00 00		0.55		uV
	(A-weighted) (defined in Table 3-1)						•
	Full-scale output voltage	9		2.68	2.81	2.96	Vpp
	Output power			—	30.8	—	mW
	Interchannel isolation 6(	defined in Table 3-1)	217 Hz	—	110	-	dB
			20 kHz	_	66	_	dB
HPOUTx;	Dynamic range	24-bit, 32-bit	A-weighted	113	119	_	dB
$R_{L} = 16 \Omega$ $C_{L} = 200 \text{ pF}$	(defined in Table 3-1)	16 bit	Unweighted	110 80	116	—	dB dB
OUT_FS = 00		10-61	Unweighted	86	92	_	dB
volume = 0 dB, unless otherwise	THD+N	24-bit, 32-bit, DSD	0 dB	_	-100	-94	dB
specified	(defined in Table 3-1)		–20 dB –60 dB	_	-86 -56	-50	dB dB
		16-bit	0 dB	_	-94	-88	dB
			–20 dB –60 dB	_	-74 -34		dB dB
	Idle channel noise	24-bit, 32-bit, DSD	-00 GD		0.55		υV
	(A-weighted) (defined in Table 3-1)	,,					F
	Full-scale output voltage	9		1.34	1.41	1.48	Vpp
	Output power				15.6	_	mW
	Interchannel isolation 6	(defined in Table 3-1)	217 Hz		110	_ ]	dB
			20 kHz		58		dB



#### Table 3-5. Analog Output Characteristics (HV\_EN = 0) 1 (Cont.)

Test conditions (unless otherwise specified): Fig. 2-1 shows CS43130 connections; input test signal is a 32-bit, full-scale 997-Hz sine wave (unless specified otherwise); GNDA = GNDCP = GNDD = 0 V; voltages are with respect to ground; HV\_EN = 0; ASP\_M/Sb = 1; typical, min/max performance data taken with VA = VCP = 1.8 V; VL = VD = 1.8 V; VP = 3.6 V; TA = +25°C; measurement bandwidth is 20 Hz–20 kHz; ASP\_SPRATE = 0001 (LRCK = 44.1-kHz mode); PDN\_XTAL = 0, MCLK\_INT = 1, and MCLK\_SRC\_SEL = 00 (crystal frequency  $f_{XTAL} = 22.5792$  MHz); Volume = 0 dB; when testing in DSD processor mode, DSD\_ZERODB = 1; when testing noise related specifications (dynamic range, THD+N, idle channel noise), no external impedance on HPREFx.

	PCM and DSD Processor Mode Parameter <sup>2,3,4</sup>		Minimum	Typical	Maximum	Units
Other characteristics	Interchannel gain mismatch (defined in Table 3-1)		_	±0.1	_	dB
TOF HPOUTX	Interchannel phase mismatch (defined in Table 3-1)		_	±0.05	_	degree
	Output offset voltage: Mute (defined in Table 3-1)		_	±0.5	±1	mV
	Gain drift (defined in Table 3-1)		_	±100	_	ppm/°C
	Load resistance (R <sub>L</sub> )		16	_	_	Ω
	Load capacitance (CL)		_	_	1	nF
	Turn-on time (defined in Table 3-1)		_	_	8	ms
	Audio latency after RESET released 7		_	_	20	ms
	Click/pop during PDN_HP enable or disable	A-weighted	_	_	-60	dBV

1. This table also applies to external VCP\_FILT supply mode: CS43130 power up procedure as described in Section 4.3.5; EXT\_VCPFILT=1; VCP\_ FILT+ and VCP\_FILT- comply to Table 3-2 when EXT\_VCPFILT = 1; in this mode, HV\_EN setting becomes don't care.

2. One LSB of triangular PDF dither is added to PCM data.

3. Referred to the typical full-scale voltage. Applies to all THD+N and dynamic range values in the table.

4.DSD performance may be limited by the source recording. 0 dB-SACD = 50% modulation index.

5. The volume must be configured as indicated to achieve specified output characteristics.

6. HP output test configuration. Symbolized component values are specified in the test conditions.



7.With I<sup>2</sup>C normal speed mode and 22.5792-MHz XTAL used as MCLK source, this specification is measured from reset released to when the audio signal appears on the output per power-up sequence listed in Section 5.10.1. PCM\_SZC should be set to Immediate (PCM\_SZC = 00) to hear audio at 20 ms after startup.

#### Table 3-6. Headphone Load Measurement

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43130 connections; GNDD = GNDCP = GNDA = 0 V; voltages are with respect to ground; typical performance data taken with VP = 3.6 V, VCP = VA = 1.8 V, VL = VD = 1.8 V; min/max performance data taken with VP = 3.6 V, VCP = VA = 1.8 V, VL = VD = 1.8 V; TA = +25°C. MCLK\_INT = 1, PDN\_XTAL = 0, and MCLK\_SRC\_SEL = 00 (crystal frequency  $f_{XTAL} = 22.5792$  MHz)

Parameters		Symbol	Minimum	Typical	Maximum	Units
Frequency range		_	20		20k	Hz
Frequency resolution		—	—	5.94	—	Hz
Low frequency impedance range		_	8		1200	Ω
Relative impedance measurement capability <sup>1</sup>		_	-12 <sup>2</sup>	_	+12	dB
Impedance measurement accuracy <sup>3</sup> G	ain error	_	-5		+5	%
	Offset	—	-1	—	1	Ω

1. Impedance measurement range is relative to low-frequency HP load impedance measured.

2. Or 4  $\Omega$ , whichever is greater.

3. Accuracy is referred to reported impedance.



#### Table 3-7. Alternate Headphone Path

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43130 connections; GNDD = GNDCP = GNDA = 0 V; voltages are with respect to ground; typical performance data taken with VP = 3.6 V, VCP = VA = 1.8 V, VL = VD = 1.8 V; min/max performance data taken with VP = 3.6 V, VCP = 1.8 V, VA = 0 V, VL = VD = 1.8 V; R<sub>L</sub> = 32  $\Omega$ ; TA = +25°C; measurement bandwidth is 20 Hz–20 kHz; MCLK\_SRC\_SEL = 10, PDN\_XTAL = 1.

	Parameters		Symbol	Minimum	Typical	Maximum	Units
Switch on characteristics	Signal range when switch on <sup>1</sup>		V <sub>INAI</sub>	—	_	3.00	Vpp
$ (PDN_HP = 1) $	THD+N with 32 Ω @ 2.82 Vpp		_	—	-99	—	dB
$HP_{IN}EN = 1)$	Interchannel isolation	217 Hz	_	104	110	—	dB
		1 kHz		—	110	—	dB
		20 kHz		—	90	_	dB
	HPINx turn-on time <sup>2</sup>		t <sub>HPIN_ON</sub>	—	_	80	μS
Switch off characteristics	Analog signal range when switched off 3,4		V <sub>INOFF</sub>	—	_	0.3	Vp
$(PDN_HP = 1, UD_HN_FN = 0)$	Turn-off time <sup>5</sup>		t <sub>HPIN_OFF</sub>	—	-	20	μS
$HP_IN_EN = 0)$	Off isolation <sup>6</sup>	217 Hz		_	120	—	dB
		1 kHz		—	120	— —	dB
		20 kHz		—	100	-	dB

1. When switch is on, maximally allowable voltage applied to HPINx pins.

2.HPINx turn-on time is measured when setting HP\_IN\_EN = 1 I<sup>2</sup>C ACK signal is received to when the signal appears on the HP out. MCLK\_SRC\_ SEL = 00, PDN\_XTAL = 0, MCLK\_INT = 1, and VCP\_FILT± has been properly charged to expected nominal values.

3. When switch is off, maximally allowable voltage applied to HPINx pins.

4. Before switch off event, it is required HPINx signal is within this range before the switch is turned off. When the switch is in off state, HPINx signal cannot exceed this specified range.

5. HPINx turn-off time is measured when HP\_IN\_EN = 0 ACK signal is received to when the signal disappears from the HP out. This spec also applies when register settings are: MCLK\_SRC\_SEL = 00, PDN\_XTAL = 0, MCLK\_INT = 1.

6. Off isolation specification is measured with  $V_{INOFF} = 0.1$  Vp input.

#### Table 3-8. Combined DAC Digital, On-Chip Analog and HPOUTx Filter Characteristics

Test conditions (unless specified otherwise): The filter characteristics have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs. Single-Speed Mode refers to 32-, 44.1-, and 48-kHz sample rates. Double-Speed Mode refers to 88.2- and 96-kHz sample rates. Quad-Speed Mode refers to 176.4- and 192-kHz sample rates. Octuple-Speed Mode refers to 352.8- and 384-kHz sample rates. MCLK\_INT is an integer multiple of Fs; HPF disabled; no DC offset applied; group delay does not include serial port delay.

	Parameter		Minimum	Typical	Maximum	Units
Fast Roll-Off	Passband <sup>2</sup>	to –0.01-dB corner	0		0.4535 4	Fs
(FILTER_SLOW_FASTB = 0)		to –3-dB corner	0	_	0.49	Fs
Single-Speed Mode		attenuation @ Fs/2	8.44 <sup>3</sup>	—		dB
	Passband ripple 10 Hz to -0.01-dB corner 5	5	-0.01	_	+0.01	dB
	Stopband		0.547	_	_	Fs
	Stopband attenuation <sup>6</sup>	PHCOMP_LOWLATB = 0	110 <sup>7</sup>			dB
		PHCOMB_LOWLATB = 1	105	_	—	dB
	Group delay (linear phase)	PHCOMB_LOWLATB = 1	—	39.5/Fs <sup>8</sup>	_	S
	Group delay (minimum phase)	PHCOMB_LOWLATB = 0	—	6.3/Fs <sup>9</sup>	—	S
	Deemphasis error <sup>10</sup> (Relative to 1 kHz)	Fs = 44.1 kHz	—		±0.14	dB
Fast Roll-Off	Passband <sup>2</sup>	to –0.01-dB corner	0	_	0.227	Fs
(FILTER SLOW FASTB = 0)		to –3-dB corner	0	—	0.48	Fs
Double-opeed Mode		attenuation @ Fs/2	7.77	_	—	dB
	Passband ripple 10 Hz to –0.01-dB corner		-0.01	—	0.01	dB
	Stopband		0.583	_	—	Fs
	Stopband attenuation <sup>6</sup>		80	_	_	dB
	Group delay (linear phase)	PHCOMB_LOWLATB = 1	—	22.3/Fs	_	S
	Group delay (minimum phase)	PHCOMB_LOWLATB = 0	—	7.5/Fs	—	S
Fast Roll-Off	Passband <sup>2</sup>	to –0.01-dB corner	0		0.114	Fs
(FILTER_SLOW_FASTB = 0)		to –3-dB corner	0	—	0.46	Fs
Quad-Speed Mode		attenuation @ Fs/2	9.44	_	_	dB
	Passband ripple 10 Hz to –0.01-dB corner		-0.01		0.01	dB
	Stopband		0.583		_	Fs
	Stopband attenuation 6		80	_	_	dB
	Group delay (linear phase)	PHCOMB_LOWLATB = 1	—	20.7/Fs	—	S
	Group delay (minimum phase)	PHCOMB_LOWLATB = 0		11.3/Fs	_	S



#### Table 3-8. Combined DAC Digital, On-Chip Analog and HPOUTx Filter Characteristics (Cont.)

Test conditions (unless specified otherwise): The filter characteristics have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs. Single-Speed Mode refers to 32-, 44.1-, and 48-kHz sample rates. Double-Speed Mode refers to 88.2- and 96-kHz sample rates. Quad-Speed Mode refers to 176.4- and 192-kHz sample rates. Octuple-Speed Mode refers to 352.8- and 384-kHz sample rates. MCLK\_INT is an integer multiple of Fs; HPF disabled; no DC offset applied; group delay does not include serial port delay.

Parameter			Minimum	Typical	Maximum	Units
Slow Roll-Off	Passband <sup>2</sup>	to –0.01-dB corner	0	_	0.417	Fs
(FILTER_SLOW_FASTB = 1)		to –3-dB corner	0	—	0.49	Fs
Single-Speed Mode +		attenuation @ Fs/2	6.45 <sup>11</sup>	_		dB
	Passband ripple 10 Hz to –0.01-dB corner 5	5	-0.01		+0.01	dB
	Stopband		0.583	-	_	Fs
	Stopband attenuation <sup>6</sup>		64	_	_	dB
	Group delay (linear phase)	PHCOMB_LOWLATB = 1	—	34.5/Fs 12	—	S
	Group delay (minimum phase)	PHCOMB_LOWLATB = 0	_	5.6/Fs <sup>13</sup>	_	s
	Deemphasis error <sup>10</sup> (Relative to 1 kHz)	Fs = 44.1 kHz	—		±0.14	dB
Slow Roll-Off	Passband <sup>2</sup>	to –0.01-dB corner	0	-	0.208	Fs
Double-Speed Mode 1		to –3-dB corner	0	—	0.458	Fs
		attenuation @ Fs/2	1			aB
	Passband ripple 10 Hz to –0.01-dB corner		-0.01	_	0.01	dB
	Stopband		0.792		_	Fs
	Stopband attenuation 6		70			dB
	Group delay (linear phase)	PHCOMB_LOWLATB = 1	—	22.3/Fs		S
	Group delay (minimum phase)	PHCOMB_LOWLATB = 0	—	6.7/Fs		S
Slow Roll-Off	Passband <sup>2</sup>	to –0.01-dB corner	0	—	0.104	Fs
Quad-Speed Mode 1		to –3-dB corner	0	—	0.43	Fs
	Decement ripple 10 Linte 0.01 dD correct	attenuation @ FS/2	7.00		- 0.01	dR 0
			-0.01		0.01	ub Ee
	Stopband		0.792	_	_	FS
			75			ав
	Group delay (linear phase)	PHCOMB_LOWLATE = 1	_	20.7/FS		S
	Group delay (minimum phase)	PHCOMB_LOWLATB = 0	_	10.6/⊢s		S
Nonoversampling (NOS)	Passband 2	to -0.01-dB corner	0	_	0.026	⊢s Fs
Single-Spéed Mode 1	Passband droop 10 Hz to 20 kHz				3 2 14	dB
	Group delay			2 7/Fs	0.2	GD S
Nonoversampling (NOS)	Passband 2	to -0.01-dB corper	0	2.171 0	0.0246	Fs
(NOS = 1)		to –3-dB corner	0	_	0.446	Fs
Double-Speed Mode 1	Passband droop 10 Hz to 20 kHz		_	_	0.73	dB
	Group delay		_	4.5/Fs	_	S
Nonoversampling (NOS)	Passband <sup>2</sup>	to -0.01-dB corner	0	_	0.026	Fs
(NOS = 1) Quad-Speed Mode 1		to –3-dB corner	0	—	0.405	Fs
Quad-Opeed Mode	Passband droop 10 Hz to 20 kHz		_	_	0.167	dB
	Group delay		—	8.4/Fs	_	S
Octuple-Speed Mode 1	Passband <sup>2</sup>	to -0.01-dB corner	0	—	0.0299	Fs
		to -3-dB corner	0		0.302	Fs
	Passband droop 10 Hz to 20 kHz				0.037	dB
	Group delay		—	17/Fs		S

1. Filter response is by design.

2. Response is clock-dependent and scales with Fs.

3. 8.5 dB for 32-kHz sample rate.

4. 0.454 Fs for 32-kHz sample rate.

5. Filter ripple specification is invalid with deemphasis enabled.

6. For Single-Speed Mode, the measurement bandwidth is from stopband to 3 Fs. For Double-Speed Mode, the measurement bandwidth is from stopband to 3 Fs.

For Quad-Speed Mode, the measurement bandwidth is from stopband to 1.34 Fs.

7.105 dB for 32-kHz sample rate. 8. 39/Fs for 32-kHz sample rate.

8. 39/FS for 32-KHZ sample rate.

9. 5.9/Fs for 32-kHz sample rate.

10. Deemphasis is available only in 44.1 kHz.

11. 6.5 dB for 32-kHz sample rate.

12. 34/Fs for 32-kHz sample rate.



13. 5.2/Fs for 32-kHz sample rate.

14. 3.9 dB for 32-kHz sample rate (passband droop 10 Hz to 15 kHz).

#### Table 3-9. DAC High-Pass Filter (HPF) Characteristics

Test conditions (unless specified otherwise): Gains are all set to 0 dB;  $T_A = +25^{\circ}C$ .

Parameter <sup>1</sup>		Typical	Maximum	Units
Passband <sup>2</sup> –0.05-dB corner	—	0.18 x 10 <sup>-3</sup> /N	_	Fs
–3.0-dB corner	—	19.5 x 10 <sup>-6</sup> /N	—	Fs
Passband ripple (0.417x10 <sup>-3</sup> /N Fs to 0.417/N Fs; normalized to 0.417/N Fs) <sup>2</sup>	—	—	0.01	dB
Phase deviation @ 0.453x10 <sup>-3</sup> /N Fs <sup>2</sup>	—	2.45	_	0
Filter settling time <sup>3</sup>	—	0.56 4	_	S

1. Response scales with Fs in PCM Mode. Specifications are normalized to Fs and are denormalized by multiplying by Fs. For DSD Mode, Fs is 44.1 kHz. 2. For PCM Single-Speed Mode, N = 1.

For PCM Double-Speed Mode, N = 2.

For PCM Quad-Speed Mode, N = 4.

For PCM Octuple-Speed Mode, N = 8.

For DSD 64 x Fs Mode, N = 1.

For DSD 128 x Fs Mode, N = 1.

3. Required time for the magnitude of the DC component present at the output of the HPF to reach 5% of the applied DC signal.

4. Filter settling time is 0.775 seconds at Fs = 32 kHz.

#### Table 3-10. DSD Combined Digital and On-Chip Analog Filter Response <sup>1</sup>

Test conditions (unless specified otherwise): Digital gains are all set to 0 dB;  $T_A = +25^{\circ}C$ ; PDN\_XTAL = 0, MCLK\_INT = 1, and MCLK\_SRC\_SEL = 00 (crystal frequency  $f_{XTAL} = 22.5792$  MHz).

	Parameter		Minimum	Typical	Maximum	Units
DSD Mode	Passband	to –3-dB corner	—	50	—	kHz
	Frequency response 20 Hz to 20 kHz		-0.05	_	0.05	dB
	Roll-off		27	_	_	dB/Oct

1. Filter response is by design.



#### Table 3-11. Digital Interface Specifications and Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43130 connections; GNDD = GNDCP = GNDA = 0 V; voltages are with respect to ground; parameters can vary with VL and VP; typical performance data taken with VP = 3.6 V, VCP = VA = 1.8 V, VD = 1.8 V and VL = 1.8 V; min/max performance data taken with VP = 3.6 V, VCP = VA = 1.8 V, VD = 1.8V and VL = 1.8 V;  $T_A$  = +25°C;  $C_L$  = 60 pF.

	Parameters <sup>1</sup>	Symbol	Minimum	Maximum	Units
Input leakage current <sup>2,3</sup>	LRCK1, DSDB/LRCK2	l <sub>in</sub>	_	±4	μA
	SDIN1, SCLK1, DSDA/SDIN2, DSDCLK/SCLK2		—	±3	μA
	HP_DETECT			±100	nA
	<u>SDA, SCL</u>		—	±100	nA
	INT, RESET		—	±100	nA
Internal weak pull-down			550	2450	kΩ
Input capacitance		_	—	10	pF
INT current sink (V <sub>OL</sub> = 0.3 V maximum)		-	825	—	μA
VL Logic (non-I <sup>2</sup> C)	High-level output voltage ( $I_{OH} = -100 \ \mu A$ )	V <sub>OH</sub>	0.9•VL		V
	Low-level output voltage	V <sub>OL</sub>	—	0.1•VL	V
	High-level input voltage	VIH	0.7•VL		V
	Low-level input voltage	VIL	—	0.3•VL	V
VL Logic (I <sup>2</sup> C only)	Hysteresis voltage (Fast Mode and Fast Mode Plus)	V <sub>HYS</sub>	0.05•VL	—	V
	Low-level output voltage	V <sub>OL</sub>		0.2•VL	V
	High-level input voltage	VIH	0.7•VL		V
	Low-level input voltage	VIL	—	0.3•VL	V
HP_DETECT <sup>4</sup>	High-level input voltage	VIH	0.93•VP	—	V
	Low-level input voltage	V <sub>IL</sub>	—	2.0	V
HP_DETECT current to VCP_FILT- 4		I <sub>HP_DETECT</sub>	1.00	2.91	μA

1.See Table 1-1 for serial and control-port power rails.

2. Specification is per pin.

3. Includes current through internal pull-up or pull-down resistors on pin. 4. The HP\_DETECT input circuit allows the HP\_DETECT signal to be as low of a voltage as VCP\_FILT– and as high as VP. Section 4.5.1 provides configuration details.

#### Table 3-12. CLKOUT Characteristics

Test conditions (unless specified otherwise): GNDD = GNDCP = GNDA = 0 V; voltages are with respect to ground; VP = 3.6 V, VCP = VA = 1.8 V, VL = VD = 1.8 V; CL = 60 pF; PLL reference input must meet the phase-noise mask specified in Fig. 4-15; TA = +25°C; Output jitter is measured from 100 Hz to half of the output frequency.

Parameters		Symbol	Minimum	Typical	Maximum	Units
CLKOUT output frequency		<b>f</b> CLKOUT	2.8224	3	3.072	MHz
			5.6448	6	6.144	MHz
			7.5264	8	8.192	MHz
			11.2896	12	12.288	MHz
CLKOUT output duty cycle			40	50	60	%
CLKOUT output TIE jitter (RMS)	CLKOUT_SRC_SEL = 01	t <sub>JIT</sub>	—	500	_	ps

#### Table 3-13. PLL Characteristics

Test conditions (unless specified otherwise): GNDD = GNDCP = GNDA = 0 V; voltages are with respect to ground; VP = 3.6 V, VCP = VA = 1.8 V, VL = VD = 1.8 V; PLL reference input must meet the phase-noise mask specified in Fig. 4-15; TA = +25°C.

Parameters	Symbol	Minimum	Typical	Maximum	Units
PLL output frequency	f <sub>out</sub>	22.5792	24	24.576	MHz
PLL lock time	t <sub>Lock</sub>	—	620	1000	μs
PLL reference clock input	—	—	11.2896		MHz
		—	22.5792		MHz
		—	12.2880		MHz
		_	24.5760		MHz
		_	9.6000		MHz
		_	19.2000		MHz
		_	12.0000		MHz
		—	24.0000		MHz
		_	13.0000		MHz
		—	26.000		MHz
PLL reference clock input jitter		-	_	50	ps



#### Table 3-14. Crystal Characteristics

Test conditions (unless specified otherwise): GNDD = GNDCP = GNDA = 0 V; voltages are with respect to ground; VP = 3.6 V, VCP = VA = 1.8 V, VL = VD = 1.8 V; TA =  $+25^{\circ}$ C

Parameters <sup>1</sup>	Symbol	Minimum	Typical	Maximum	Units
Crystal oscillator frequency	f <sub>XTAL</sub>	22.57	22.5792/ 24.576	24.58	MHz
Crystal load capacitance	C <sub>L_XTAL</sub>	5	—	8	pF
Equivalent series resistance	esr <sub>XTAL</sub>	—	—	100	Ω
Startup time	t <sub>XTAL_pup</sub>	—	_	8	ms
Shunt capacitance	Co	—	_	0.8	pF
Maximum drive level	_	200	_	_	μŴ

1. Refer to Section 5.3 for supported crystal options.

#### Table 3-15. Power-Supply Rejection Ratio (PSRR) Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43130 connections; input test signal held low (all zero data); GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground; VL = VA = VD = 1.8 V, VP = 3.6 V; When testing PSRR, PCM input test signal held low (all zero data);  $T_A = +25^{\circ}C$ ; PCM\_AMUTE = 0.

Parameter <sup>1</sup>		Minimum	Typical	Maximum	Units
HPOUTx       21         PSRR with 100-mVpp signal AC coupled to VA supply       1         PDN       HP       0         PDN       HP       0	17 Hz 1 kHz	_	75 75 70	_	dB dB
PDN_III         O, III         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O         O <t< td=""><td>17 Hz 1 kHz 0 kHz</td><td> </td><td>80 80 60</td><td> </td><td>dB dB dB dB</td></t<>	17 Hz 1 kHz 0 kHz	 	80 80 60	 	dB dB dB dB
HPOUTx       21         PSRR with 100-mVpp signal AC coupled to VP supply       1         PDN_HP = 0, HP_IN_EN = 0       20	17 Hz 1 kHz ) kHz		100 100 80		dB dB dB
$\begin{array}{ll} \mbox{HPOUTx (0-dB analog gain)} & 21 \\ \mbox{PSRR with 100-mVpp signal AC coupled to VCP supply} & 1 \\ \mbox{PDN_HP} = 1, \mbox{HP_IN_EN} = 1, \mbox{R}_L = 32 \ \Omega & 20 \end{array}$	17 Hz 1 kHz ) kHz		80 80 60		dB dB dB
$ \begin{array}{ll} \mbox{HPOUTx (0-dB analog gain)} & 21 \\ \mbox{PSRR with 100-mVpp signal AC coupled to VP supply} & 1 \\ \mbox{PDN_HP = 1, HP_IN_EN = 1, R_L = 32 } \Omega & 20 \\ \end{array} $	17 Hz 1 kHz ) kHz		100 100 80		dB dB dB

1.PSRR test configuration: Typical PSRR can vary by approximately 6 dB below the indicated values.



#### Table 3-16. DC Characteristics

Test conditions (unless otherwise specified): Fig. 2-1 shows CS43130 connections; GNDD = GNDA = GNDCP = 0 V; all voltages with respect to ground.

Parameters			Minimum	Typical	Maximum	Units
VCP_FILT (No load connected to HPOUTx)	VP_LDO Mode	VCP_FILT+ pin (HV_EN = 1)	_	3.0	_	V
EXT_VCPFILT = 0		VCP_FILT+ pin (HV_EN = 0)	—	2.6	—	V
		VCP_FILT- pin (HV_EN = 1)	—	-3.0	—	V
		VCP_FILT- pin (HV_EN = 0)	—	-2.6	—	V
	VCP Mode	VCP_FILT+ pin	_	VCP	—	V
		VCP_FILT- pin	—	-VCP	—	V
-VA		–VA pin	—	– VA	—	V
Alternate headphone path	On-resistance		—	1	—	Ω
switch-on characteristics PDN_HP = 1, HP_IN_EN = 1	r <sub>ON</sub> matching between channels		_	0.05	_	Ω



#### Table 3-16. DC Characteristics (Cont.)

Test conditions (unless otherwise specified): Fig. 2-1 shows CS43130 connections; GNDD = GNDA = GNDCP = 0 V; all voltages with respect to ground.

Parameters			Minimum	Typical	Maximum	Units
Other DC filter characteristics	FILT+ voltage		_	-0.35	—	V
	FILT– voltage		_	0.35	_	V
	HP output current limiter on threshold.		_	120	160	mA
	VD power-on reset threshold (V <sub>POR</sub> )	Up Down		1.15 0.950	_	V V

#### Table 3-17. Power Consumption

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43130 connections; GNDA = GNDCP = GNDD = 0 V; voltages are with respect to ground; performance data taken with VA = VCP = VD = VL = 1.8 V; VP = 3.6 V;  $T_A = +25^{\circ}C$ ; ASP\_SPRATE = 0001(44.1-kHz mode); MCLK\_INT = 1 (22.5792 MHz); MCLK\_SRC\_SEL = 00; all other fields are set to defaults; no signal on any input; control port inactive; all serial ports are set to Slave or Master Mode as indicated, input clock/data are held low unless active; test load is  $R_L = 32 \Omega$  and  $C_L = 1$  nF for HPOUTx; measured values include currents consumed by the DAC and do not include current delivered to external loads unless specified otherwise (e.g., from HPOUTx outputs); see Fig. 2-1.

		Typical Current (μA)						Total
	Use Cases	P <sub>OUT</sub>	İ <sub>VCP</sub>	iva	i <sub>VD</sub>	ivL	i <sub>VP</sub>	Power (µW)
1	Off 1	—	0	0	0	0	6	22
2	Standby <sup>2</sup> HPDETECT enabled	—	0	0	256	0	32	576
3	A Playback External MCLK = 22.5792 MHz, I <sup>2</sup> S/DoP	Quiescent 3	4021	7302	1444	40	32	23167
	3 Stereo HPOUT	0.1mW	12363	7862	2004	40	32	40199
4	Alternate HP path stereo HPIN enabled <sup>4</sup>	Quiescent	209	110	393	3	66	1524

1.Off configuration: Clock/data lines held low; RESET = LOW; VA = VD = VL = 0 V, VCP = 0 V, VP = 3.6 V.

2.Standby configuration: Clock/data lines held low; RESET = HIGH; VA = VD = VL = 1.8 V, VCP = 1.8 V, VP = 3.6 V; HP\_DETECT\_CTRL = 11 (enabled); HPDETECT\_PLUG\_INT\_MASK=0 (unmasked); PDN\_XTAL = 1, MCLK\_SRC\_SEL = 10 (RCO selected as MCLK source).

3.Quiescent configuration: data lines held low; RESET = HIGH; VA = 1.8 V, VD = VL = VCP = 1.8 V, VP = 3.6 V. Serial port, I<sup>2</sup>S/DoP Mode (ASP and SDIN, ASP\_M/Sb = 0); PDN\_XTAL = 1.

4.Quiescent configuration: PDN\_XTAL = 1; MCLK\_SRC\_SEL = 10 (RCO selected as MCLK source); alternate headphone path (PDN\_HP = 1, HPOUT\_ CLAMP = 1, HP\_IN\_EN = 1); data lines held low; RESET = HIGH; VA = 1.8 V, VD = VL = VCP = 1.8 V, VP = 3.6 V.

#### **Table 3-18. Serial-Port Interface Characteristics**

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43130 connections; GNDA = GNDCP = GNDD = 0 V; voltages are with respect to ground; parameters can vary with VL; typical performance data taken with VL = VD = VA = VCP = 1.8 V, VP = 3.6 V; min/max performance data taken with VL = 1.8 V; VD = VA = VCP = 1.8 V, VP = 3.6 V; T<sub>A</sub> = +25°C; C<sub>L</sub> = 60 pF; Logic 0 = ground, Logic 1 = VL; output timings are measured at V<sub>OL</sub> and V<sub>OH</sub> thresholds (see Table 3-11).

	Parameters 1,2,3,4,5		Minimum	Typical	Maximum	Units
FSYNC frame rate		Fs	(See Section 4.9.5)			kHz
FSYNC hig	h period <sup>6</sup>	t <sub>HI:FSYNC</sub>	1/f <sub>SCLK</sub>	—	(n–1)/f <sub>SCLK</sub>	S
Master	FSYNC duty cycle xSP_5050 = 1	—	45	—	55	%
Mode	FSYNC delay time after SCLK launching edge 7	t <sub>D:CLK-FSYNC</sub>	_	—	20	ns
	SCLK frequency	f <sub>SCLK</sub>	—	—	f <sub>MCLK_INT</sub>	MHz
	SCLK high period <sup>8</sup>	thi:SCLK	1/(2•f <sub>SCLK</sub> ) – 1/f <sub>MCLK_</sub> INT	—	1/(2•f <sub>SCLK</sub> ) + 1/f <sub>MCLK_INT</sub>	ns
	SDIN setup time before SCLK latching edge 7	t <sub>SU:SDI</sub>	10	—	_	ns
	SDIN hold time after SCLK latching edge <sup>7</sup>	t <sub>H:SDI</sub>	5	—	_	ns
Slave	FSYNC setup time before SCLK latching edge 7	t <sub>SU:FSYNC</sub>	10	—	—	ns
Mode	FSYNC hold time after SCLK latching edge 7	t <sub>H:FSYNC</sub>	5	—	_	ns
	SCLK frequency	f <sub>SCLK</sub>	—	—	24.58	MHz
	SCLK high period	t <sub>HI:SCLK</sub>	16	—	—	ns
	SCLK low period	t <sub>LO:SCLK</sub>	16	—	_	ns
	SDIN setup time before SCLK latching edge 9	t <sub>SU:SDI</sub>	10	—	—	ns
	SDIN hold time after SCLK latching edge 7	t <sub>H:SDI</sub>	5	—	—	ns

1.MCLK in this table refers to the external clock supplied to the MCLK pin (MCLK<sub>EXT</sub>).

 Output clock frequencies follow the master clock (MCLK<sub>EXT</sub>) frequency proportionally. Any deviation of the clock source from the nominal supported rates are directly imparted to the output clock rate by the same factor (e.g., +100-ppm offset in the frequency of MCLK<sub>EXT</sub> becomes a +100-ppm offset in LRCK/FSYNC and SCLK).



#### 3.12S interface timing



5. Applies to Master and Slave Modes, unless specified otherwise.

- 6. Maximum LRCK duty cycle is equal to frame length, in SCLK periods, minus 1. Maximum duty cycle occurs when LRCK high (xSP\_LCHI) is set to 768 SCLK periods and LRCK period (xSP\_LCPR) is set to 769 SCLK periods.
- 7. Data may be latched/launched on either the rising or falling edge of SCLK.
- 8.SCLK duty cycle in Master Mode depends on Master Mode clock configuration, and can vary by up to 1 MCLKEXT period.
- 9. Data is latched/launched on the rising or falling edge of SCLK as determined by xSP\_SCPOL\_OUT, xSP\_SCPOL\_IN, and xSP\_FSD bits. See the SCLK launching specs in Table 3-18.

#### Table 3-19. DSD Switching Characteristic

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43130 connections; GNDA = GNDCP = GNDD = 0 V; voltages are with respect to ground; parameters can vary with VL; typical performance data taken with VL = VD = VA = VCP = 1.8 V, VP = 3.6 V; min/max performance data taken with VL = 1.8 V; VD = VA = VCP = 1.8 V, VP = 3.6 V; T<sub>A</sub> = +25°C; C<sub>L</sub> = 60 pF; Logic 0 = ground, Logic 1 = VL; output timings are measured at V<sub>OL</sub> and V<sub>OH</sub> thresholds (see Table 3-11).

Parameter <sup>1,2</sup>		Symbol	Minimum	Typical	Maximum	Units
DSDCLK duty cycle		—	40	_	60	%
DSDCLK pulse width low		t <sub>SCLKL</sub>	80	_	—	ns
DSDCLK pulse width high		t <sub>SCLKH</sub>	80	_	—	ns
DSDCLK frequency	(64× oversampled)	—	1.024	2.8224	f <sub>MCLK INT</sub> /8	MHz
	(128× oversampled)		2.048	5.6448	f <sub>MCLK_INT</sub> /4	MHz
DSDA/DSDB valid to DSDCLK rising setup time		t <sub>SDLRS</sub>	20	_	—	ns
DSDCLK rising to DSDA or DSDB hold time		t <sub>SDH</sub>	20	—	—	ns
DSD clock to data transition (Phase Modulation Mod	le)	t <sub>DPM</sub>	-20	_	20	ns

1. Serial audio input interface timing



2. Phase modulation mode serial audio input interface timing



#### Table 3-20. I<sup>2</sup>C Slave Port Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows typical connections; Inputs: GNDA = GNDL = GNDCP = 0 V; all voltages with respect to ground; VL = 1.8 V; inputs: Logic 0 = GNDA = 0 V, Logic 1 = VL;  $T_A = +25^{\circ}C$ ; SDA load capacitance equal to maximum value of  $C_B = 400 \text{ pF}$ ; minimum SDA pull-up resistance,  $R_{P(min)}$ .<sup>1</sup> Table 3-1 describes some parameters in detail. All specifications are valid for the signals at the pins of the CS43130 with the specified load capacitance.

Parameter	Symbol <sup>3</sup>	Minimum	Maximum	Units	
SCL clock frequency		f <sub>SCL</sub>	—	1000	kHz
Clock low time		t <sub>LOW</sub>	500	—	ns
Clock high time		t <sub>HIGH</sub>	260	—	ns
Start condition hold time (before first clock pulse	)	t <sub>HDST</sub>	260	—	ns
Setup time for repeated start		tsust	260	—	ns
Rise time of SCL and SDA	Standard Mode Fast Mode Fast Mode Plus	t <sub>RC</sub>		1000 300 120	ns ns ns
Fall time of SCL and SDA	Standard Mode Fast Mode Fast Mode Plus	t <sub>FC</sub>		300 300 120	ns ns ns
Setup time for stop condition		t <sub>SUSP</sub>	260	—	ns
SDA setup time to SCL rising		t <sub>SUD</sub>	50	—	ns
SDA input hold time from SCL falling 4		t <sub>HDDI</sub>	0	—	ns
Output data valid (Data/Ack) <sup>5</sup>	Standard Mode Fast Mode Fast Mode Plus	t <sub>VDDO</sub>		3450 900 450	ns ns ns
Bus free time between transmissions		t <sub>BUF</sub>	500	—	ns
SDA bus capacitance	SCL frequency = 1 MHz, V <sub>L</sub> = 1.8 V SCL frequency ≤ 400 kHz	CB	_	400 400	pF pF
SCL/SDA pull-up resistance <sup>1</sup>	V <sub>L</sub> = 1.8 V	R <sub>P</sub>	350	—	Ω
Pulse width of spikes to be suppressed		t <sub>PS</sub>	—	50	ns
Switching time between RCO and MCLK_INT 6		—	150	—	μs
Power-up delay (delay before I2C can communic	cate after RESET released)	t <sub>PUD</sub>	1500	—	μs

1. The minimum R<sub>P</sub> value (resistor shown in Fig. 2-1) is determined by using the maximum level of VL, the minimum sink current strength of its respective output, and the maximum low-level output voltage V<sub>OL</sub>. The maximum R<sub>P</sub> value may be determined by how fast its associated signal must transition (e.g., the lower the value of R<sub>P</sub>, the faster the I<sup>2</sup>C bus is able to operate for a given bus load capacitance). See I<sup>2</sup>C bus specification referenced in Section 13.

2. All timing is relative to thresholds specified in Table 3-11, V<sub>IL</sub> and V<sub>IH</sub> for input signals, and V<sub>OL</sub> and V<sub>OH</sub> for output signals.

3.I<sup>2</sup>C control-port timing



4.Data must be held long enough to bridge the transition time, t<sub>F</sub>, of SCL.

5. Time from falling edge of SCL until data output is valid.

6.Upon setting MCLK\_SRC\_SEL and sending the I<sup>2</sup>C stop condition, the switching of RCO and other MCLK\_INT sources occurs. A least wait time as specified is required after changing MCLK\_SRC\_SEL and sending the I<sup>2</sup>C stop condition before the next I<sup>2</sup>C transaction is initiated.



# 4 Functional Description

This section describes the general theory of operation of the CS43130, tracing the signal and control flow through the various blocks within the device. It comprises the following sections:

- Section 4.1, "Overview"
- Section 4.2, "Analog Outputs"
- Section 4.3, "Class H Amplifier Output"
- Section 4.4, "Alternate Headphone Inputs"
- Section 4.5, "Headphone Presence Detect and Output Load Detection"
- Section 4.6, "Clocking Architecture"
- Section 4.7, "Clock Output and Fractional-N PLL"
- Section 4.8, "Filtering Options"
- Section 4.9, "Audio Serial Port (ASP)"
- Section 4.10, "DSD Interface"
- Section 4.11, "DSD and PCM Mixing"
- Section 4.12, "Standard Interrupts"
- Section 4.13, "Control Port Operation"

## 4.1 Overview

## 4.1.1 Analog Outputs

The analog output block includes separate pseudodifferential headphone Class H amplifiers output. An on-chip inverting charge pump creates a positive and negative voltage equal to the input, allowing an adaptable, full-scale output swing centered around ground. The resulting internal amplifier supply can be  $\pm$ VCP, or  $\pm$ VP\_LDO (either  $\pm$ 3.0 V with HV\_EN = 1 or  $\pm$ 2.6 V with HV\_EN = 0).

The inverting architecture eliminates the need for large DC-blocking capacitors and allows the amplifier to deliver more power to HP loads at lower supply voltages. This adaptive power supply scheme converts traditional Class AB amplifiers into more power-efficient Class H amplifiers.

## 4.1.2 Alternate Headphone Inputs

The alternate headphone inputs provide an integrated selectable path to interface between the system codec output and the headphone connector, which allows for lower-power operation in applications such as voice or compressed music playback. These inputs eliminate the need for an external audio switch and prevent the high-fidelity headphone outputs of CS43130 from degradation by the external audio switch.

## 4.1.3 Headphone Detection

The CS43130 detects the presence of a headphone and notifies the application processor to wake up through an interrupt event.

## 4.1.4 Headphone Impedance Measurement

The CS43130 detects headphone impedance information at low frequencies, which can be used to adjust the system properly to accommodate different load conditions. One example is to adjust signal chain gain to avoid distortion.

The CS43130 also provides impedance measurement functions to evaluate the headphone load within 20 Hz to 20 kHz. A specific frequency is selected and the impedance measurement process is initiated by setting the register. Through a series of interrupt events, the CS43130 notifies application processor to retrieve the impedance information after completion.



### 4.1.5 Audio Interfaces and Supported Formats

There are two serial input ports on the CS43130, the audio serial port (ASP) and the auxiliary serial port (XSP). The ASP on the CS43130 supports I<sup>2</sup>S, TDM, and DoP (DSD over PCM) formats up to a 384-kHz sample rate. The XSP on the CS43130 supports the DoP format up to a 352.8-kHz sample rate.

The CS43130 also has a dedicated DSD interface to support up to 128•Fs. The DSD interface shares pins with the XSP.

## 4.1.6 System Clocking

The CS43130 internal MCLK can be sourced from three options:

- Direct MCLK/crystal mode. The internal MCLK is provided through XTI/MCLK pin directly or generated by crystal oscillator.
- PLL mode. A PLL reference CLK is provided externally through XTI/MCLK. The PLL is configured, and output is used as the internal MCLK.
- RCO mode. An internal RCO is used as the internal MCLK. Note that HPIN input path is the only supported audio playback feature in this mode for optimized power consumption. This mode can also support HP detection and I<sup>2</sup>C communication. DAC playback and headphone impedance measurement function s are not supported.

The clock output is provided for audio applications that require high quality audio rate system clock. This clock output can be sourced from the following two options:

- The clock generated by the CS43130 crystal oscillator.
- Output of the internal Fractional-N PLL that refers to MCLK input. See Section 4.7.1 for supported frequencies.

The internal MCLK is used to generate serial port clocks. See Table 4-6 for supported LRCK combinations.

### 4.1.7 System Interrupts

The CS43130 includes an open-drain interrupt output ( $\overline{INT}$  pin). Interrupt mask registers control whether an event associated with an interrupt status/mask bit pair triggers the assertion of  $\overline{INT}$ . All types of interrupts are described in Section 4.11.

## 4.1.8 System Reset

The CS43130 offers two types of reset options:

- Asserting RESET. If RESET is asserted, all registers and all state machines are immediately set to their default values/states. No operation can begin until RESET is deasserted. Before normal operation can begin, RESET must be asserted at least once after the VP supply is first brought up.
- Power-on reset (POR). If the VD supply is lower than the POR threshold specified in Table 3-16, the VD register fields and the state machines are held in reset, setting them to their default values/states. The POR releases the reset when the VD supply goes above the POR threshold. When the VD supply is turned on, the VL and VA supplies must also be turned on at the same time.

### 4.1.9 Power Down

The CS43130 has a register byte to power down individual components on the chip. Before any change can be applied to an individual component (except PLL), the block must be powered down first. For the PLL, changes can be applied after PLL\_START is cleared.

The PDN\_HP bit is responsible for enabling or disabling the playback signal chain operation. All the necessary components for playback operation need to be powered up and configured properly before PDN\_HP is cleared. To disable the playback signal chain, PDN\_HP is set. PDN\_HP needs to be set before making any changes to the playback signal chain setup, except the following functions:

- · Volume and mute related functions
- PCM filter settings (see Section 7.5.2)



Before ASP, XSP, or DSDIF can safely power down, PDN\_HP must be asserted, and PDN\_DONE\_INT must be present. For XTAL or PLL used as the source of internal MCLK, PDN\_HP needs to be set first and MCLK source needs to be properly switched away before PDN\_XTAL or PDN\_PLL is set. If PLL output is only used as the source of CLKOUT, PDN\_ PLL can be set without PDN\_HP being asserted. If the steps described above are not followed, the CS43130 enters an unresponsive state.

PDN\_CLKOUT does not require PDN\_HP to be set before it is asserted.

PDN\_HP should be set before using headphone input path and load detection function. Refer to the functional description of these two components for further details.

Recommended power-up and power-down sequences can be found in the Section 5.2.



## 4.2 Analog Outputs

The CS43130 provides an analog output that is derived from the digital audio input ports. This section describes the general flow of the analog outputs.

## 4.2.1 Analog Output Signal Flow

The CS43130 signal flow is shown in Fig. 4-1.



Figure 4-1. Analog Output Signal Flow

The CS43130 has 4 settings of full scale voltage, which are determined by OUT\_FS[1:0]. The proper full scale voltage must be set first, and the digital volume settings is used to control signal levels.

The CS43130 digital volume control allows independent control of the signal level in 1/2 dB increments from 0 dB (0b0000 0000) to -127 dB (0b1111 1110) by using x\_VOLUME\_y (where "x" is either PCM or DSD; "y" is either A or B) register. When the x\_VOL\_BEQA bit is set, both volumes can be changed simultaneously using x\_VOLUME\_A). The volume changes are implemented as dictated by PCM\_SZC[1:0] and DSD\_SZC in the signal control register (see Section 7.4.3 and Section 7.5.5). If soft ramping is enabled, gain and attenuation changes are carried out by incrementally changing the volume level in 1/8-dB steps, from the previous level to the new level. For PCM, when PCM\_SZC[1:0] = 2, the volume level changes at an approximate rate of 1 dB/ms. For DSD, when DSD\_SZC = 1, the volume level also changes at an approximate rate of 1 dB/ms during power up or when coming out of a mute state (DSD\_MUTE\_x = 1). Note that when recovering from an error state caused by static DSD data (DSD\_STUCK\_INT = 1), the volume output will resume at the level specified in DSD\_VOLUME\_x registers. Both channels can be inverted by setting the INV\_A and INV\_B bits.

The CS43130 provides individual ramp-up control option (from the global soft ramp settings) for a specific scenario. The PCM\_RAMP\_DOWN bit is for the scenario when the interpolation filter switches during PCM playback. Refer to the register description for setting details.

The CS43130 can mute both channels simultaneously or independently. Also, it can auto-mute on both PCM stream and DSD stream when mute pattern is identified (defined in PCM\_AMUTE and DSD\_AMUTE). Additional signal and mute control options can be found in Section 7.4.3 and Section 7.5.5.

The CS43130 has an independent set of controls for the DSD processor path as shown in Fig. 4-1. The DSD processor also offers the control bit SIGCTL\_DSDEQPCM, which maps the PCM\_x setting to DSD\_x setting, once enabled. As a result, some of the DSD\_x register settings are ignored. The registers affected are DSD\_VOL\_BEQA, DSD\_SZC, DSD\_



AMUTE, DSD\_AMUTE\_BEQA, DSD\_MUTE\_A, DSD\_MUTE\_B, DSD\_INV\_A, DSD\_INV\_B, DSD\_SWAP\_CHAN, and DSD\_COPY\_CHAN. Refer to Section 7.4.1–Section 7.4.7 for control register details.

## 4.3 Class H Amplifier Output

Fig. 4-2 shows the Class H operation.



Figure 4-2. Class H Operation

The CS43130 headphone output amplifiers use Cirrus Logic two-mode Class H technology. This technology maximizes operating efficiency of the typical Class AB amplifier while maintaining high performance. In a Class H amplifier design, the rail voltages supplied to the amplifier vary with the needs of the music passage that is being amplified. This prevents unnecessarily wasting energy during low power passages of program material or when the program material is played back at a low volume level.

The internal charge pump, which creates the rail voltages for the headphone amplifiers, is the central component of the two-mode Class H technology implemented in the CS43130. The charge pump receives its input voltage from the voltage present on the VCP or VP pin. From this input voltage, the charge pump creates the differential rail voltages supplied to the amplifier output stages. The charge pump can supply two sets of differential rail voltages: ±VCP and ±VP\_LDO.

HV\_EN setting, as shown in Fig. 4-3, determines the VP\_LDO voltage as shown in Table 4-1. HV\_EN = 1 setting is required to support the 1.7-V full-scale voltage for a 600- $\Omega$  load and above. In this setting, minimum VP is required to be higher than 3.3 V, and any load below 600  $\Omega$  is not supported. When HV\_EN = 0, the max output voltage is 1.4-V RMS full-scale voltage. In this setting, minimum VP is required to be higher than 3 V, and the full headphone load range is supported.



Figure 4-3. Internal LDO Configuration

Table 4-1. VP\_LDO Voltage Per HV\_EN Setting

HV_EN	VP_LDO Voltage
0	2.6 V
1	3.0 V



Table 4-2 shows the nominal signal and volume level ranges when the output is set to the adapt modes explained in Section 4.3.1. If the signal level is greater than the maximum value of this range, then clipping can occur.

#### Table 4-2. Class H Supply Modes

Mode	Class H Supply Level	Signal <sup>1</sup> or Volume Level Range <sup>2,3,4</sup>
0	±VP_LDO V, internally regulated from VP	≥ –11 dB
1	±VCP	< –11 dB

1. In adapt-to-signal, the volume level ranges are approximations but are within –0.5 dB from the values shown. 2. Relative to digital full scale with output gain set to 0 dB.

3. In fixed modes, clipping can occur if the signal level exceeds the maximum of this range due to setting the amplifier's supply too low.

4. Thresholds shown are nominal for a  $16-\Omega$  stereo load.

## 4.3.1 Power Supply Control Options

This section describes the two types of operation: standard Class AB and adapt-to-output signal. The set of rail voltages supplied to the amplifier output stages depends on the ADPT\_PWR (see p. 112) setting.

### 4.3.1.1 Standard Class AB Operation (ADPT\_PWR = 001 or 010)

If ADPT\_PWR is set to 001 or 010, the rail voltages supplied to the amplifiers are held to ±VP\_LDO or ±VCP, respectively. The rail voltages supplied to the output stages are held constant, regardless of the output signal level. The CS43130 amplifiers simply operate in a traditional Class AB configuration.

## 4.3.1.2 Adapt-to-Output Signal (ADPT\_PWR = 111)

If ADPT\_PWR is set to 111, the rail voltage sent to the amplifiers is based solely on whether the signal sent to the amplifiers would cause the amplifiers to clip when operating on the lower set of rail voltages at certain threshold values.

- If it would cause clipping, the control logic instructs the charge pump to provide the next higher set of rail voltages to the amplifiers.
- If it would not cause clipping, the control logic instructs the charge pump to provide the lower set of rail voltages to the amplifiers, eliminating the need to advise the CS43130 of volume settings external to the device.

## 4.3.2 Power-Supply Transitions

Charge-pump transitions from the lower to the higher set of rail voltages occur on the next FLYN/FLYP clock cycle. Despite the system's fast response time, the VCP\_FILT pin's capacitive elements prevent rail voltages from changing instantly. Instead, the rail voltages ramp up from the lower to the higher supply, based on the time constant created by the output impedance of the charge pump and the capacitor on the VCP\_FILT pin (the transition time is approximately 20 µs).

Fig. 4-4 shows Class H supply switching. During this charging transition, a high dv/dt transient on the inputs may briefly clip the outputs before the rail voltages charge to the full higher supply level. This transitory clipping has been found to be inaudible in listening tests.





When the charge pump transitions from the lower to higher set of rail voltage, there is no delay associated with the transition.

When the charge pump transitions from the higher to the lower set of rail voltages, there is an approximate 5.5-s delay before the charge pump supplies the lower rail voltages to the amplifiers. This hysteresis ensures that the charge pump does not toggle between the two rail voltages as signals approach the clip threshold. It also prevents clipping in the instance of repetitive high-level transients in the input signal. Fig. 4-5 shows examples of this transitional behavior.





### 4.3.3 HP Current Limiter

The CS43130 features built-in current-limit protection for the headphone output. Table 3-16 lists the threshold for the current limit during the short-circuit conditions shown in Fig. 4-6. For the HP amplifiers, current is from the internal charge pump output, and, as such, applies the current from VCP or VP.



Figure 4-6. HP Short Circuit Setup

## 4.3.4 External VCP\_FILT Supply Mode

To bypass the CS43130 Class-H charge-pump circuit, provide external VCP\_FILT± supply with the following conditions:

- When CS43130 is operating, apply +3.0 V with ±5% accuracy to VCP\_FILT+ and apply -3.0 V with ±5% accuracy to VCP\_FILT-.
- When CS43130 is powered down, external circuits present Hi-Z state to the VCP\_FILT+ pin (>1k impedance) and VCP\_FILT- pin (>10k impedance).
- To avoid possible damage, VCP\_FILT± pins must remain within the absolute maximum rating specified.



Figure 4-7. External VCP\_FILT Power-Up Sequence

For powering up CS43130 in this mode, the recommended sequence must be followed. This assumes that the CS43130 starts from the status where VCP\_FILT± pin are presented with Hi-Z.

- 1. Set EXT\_VCPFILT.
- 2. Wait 8 ms after I<sup>2</sup>C ACK.
- 3. Release and start to ramp external voltage on VCP\_FILT± pin.
- 4. Wait until VCP\_FILT+ pin voltage to be greater than +2.6V and VCP\_FILT- to be less than -2.6 V.



5. Clear the PDN\_HP bit.



Figure 4-8. External VCP\_FILT Power-Down Sequence

For powering down in this mode, use the following recommended sequence. This assumes that the CS43130 starts from the status where VCP\_FILT± pin are presented with ±3.0 V, respectively.

- 1. Execute the power down sequence per Section 5.7.
- 2. Wait 8 ms after I<sup>2</sup>C ACK.
- 3. Start to shut-off external supply to VCP\_FILT± pins.
- 4. Wait until Hi-Z mode is presented on VCP\_FILT± pins.
- 5. Clear EXT\_VCPFILT.

## 4.4 Alternate Headphone Inputs

The top-level schematic of the alternate headphone inputs is shown in Fig. 4-9. Bits PDN\_HP and HP\_IN\_EN configure the audio source for the HPOUT pins. The switches connected to HPINx are controlled by HP\_IN\_EN. The switches connected to the internal headphone driver are controlled by PDN\_HP. When the alternate headphone inputs are selected (HP\_IN\_EN = 1), the CS43130 internal headphone driver output needs to be disconnected (PDN\_HP = 1). Likewise, when the CS43130 internal headphone drivers are enabled, the HPINx switch needs to be open and not in the signal path. User should refer to the Applications section for details on the required sequence of enable and disable HPINx path.



Figure 4-9. Alternative Headphone Input Setup



Before opening the HPINx switches, ramp down any active signal on HPINx pins to a voltage less than the V<sub>INOFF</sub> value specified in Table 3-7. Similarly, the voltage cannot exceed the same voltage requirement before the switches are closed. To prevent any pop on the headphone, the input should be muted during these transition. The CS43130 has ultralow offset when muted. For pop-free transition on the headphone, it is expected that the source on HPINx pins have low offset to ground when muted.

The recommended sequence to switch from CS43130 to HPINx is as follows:

- 1. Soft ramp content on CS43130 down to mute.
- 2. Set PDN\_HP and wait for PDN\_DONE\_INT event.
- 3. If saving power is desired, switch MCLK\_INT source to RCO.
- 4. Enable HPINx path.

The recommended sequence to switch from HPINx to CS43130 is as follows:

- 1. Setup CS43130 intended MCLK source for DAC operation (if needed)
- 2. Soft ramp content on HPINx down to mute.
- 3. Disable HPINx path.
- 4. Switch MCLK\_INT to the intended MCLK source when ready.
- 5. Clear PDN\_HP.

## 4.5 Headphone Presence Detect and Output Load Detection

The CS43130 provides headphone presence-detect and load-detection functionalities functionality.

## 4.5.1 Headphone Presence Detect

The CS43130 supports headphone presence-detect capability via the HP\_DETECT sense pin. HP\_DETECT is debounced to filter out brief events before being reported to the corresponding presence-detect status bit and generating an interrupt if appropriate.

## 4.5.1.1 Headphone Plug Types

The presence detect scheme is designed to support the following plug types:

- Tip-Ring-Sleeve (TRS). Consists of a segmented metal barrel with the tip connector used for HPOUTA, a ring connector used for HPOUTB, and a sleeve connector used for HPGND.
- Tip-Ring-Ring-Sleeve (TRRS). Similar to TRS, with an additional ring connector for the HSIN connection. There are two common pinouts for TRRS plugs:
  - The tip is used for HPOUTA, the first ring for HPOUTB, the second ring for HSGND, and the sleeve for HSIN.
  - An alternate pinout, OMTP (open mobile terminal platform), also called "China headset," swaps the third and fourth connections so that the second ring carries HSIN and the sleeve carries HSGND.

Note that if both TRRS plug types need to be supported at the same time, the CS43130 requires an additional IC to perform the OMTP detect functions and to present the identified HSGND to the CS43130 HPREFx. However, the switch inside the detect IC may degrade the CS43130 performance.

## 4.5.1.2 Headphone Detect Methods

CS43130 can detect the presence or absence of a plug. For a headphone-presence detect, a sense pin is connected to a terminal on the receptacle such that, if no plug is inserted, the pin is floating. If a plug is inserted, the pin is shorted to the tip (T) terminal. The presence detect function is accomplished by having a small current source inside the CS43130 to pull up the pin if it is left floating (no plug). If a plug is inserted and the sense pin is shorted to HPOUTA, when HP amp is powered down, it is assumed that the sense pin is pulled low via clamps at the HP amp output. If the HP amp is running,



the sense pin is shorted to the output signal and, therefore, is pulled below a certain threshold via the output stage of the HP amp. Thus, a low level at the sense pin indicates plug inserted, and a high level at the sense pin indicates plug removed.

## 4.5.1.3 Headphone Detect Registers

This section describes the behavior and interaction of the headphone-detect debounce register fields. See Fig. 4-10 for reference.



### Figure 4-10. Headphone Detect Block Diagram

- HPDETECT\_CTRL configures the operation of the HP detect circuit.
- HPDETECT\_INV inverts the signal from the HP detect circuit.
- HPDETECT\_FALL\_DBC\_TIME configures the HP\_DETECT falling debounce time.
- HPDETECT\_RISE\_DBC\_TIME configures the HP\_DETECT rising debounce time.
- HPDETECT\_PLUG\_DBC shows the falling-edge-debounced version of HP\_DETECT signal.
- HPDETECT\_UNPLUG\_DBC shows the rising-edge-debounced version of HP\_DETECT signal.
- HPDETECT\_PLUG\_INT shows the headphone plug-in event status.
- HPDETECT\_UNPLUG\_INT shows the headphone unplug event status.
- HPDETECT\_PLUG\_INT\_MASK is the interrupt mask of headphone plug-in event status.
- HPDETECT\_UNPLUG\_INT\_MASK is the interrupt mask of headphone unplug event status.

## 4.5.1.4 Headphone Detect and Interrupts Setup Instructions

The following steps are required for activation of headphone-detect debounce interrupt status:

- 1. Ensure the I<sup>2</sup>C is ready to respond to control port command.
- 2. Clear the interrupt masks.
- 3. Write to HPDETECT\_RISE\_DBC\_TIME and HPDETECT\_FALL\_DBC\_TIME (see p. 112) to enable debounce for presence detect plug/unplug.
- 4. Set HPDETECT\_CTRL to 11 to enable the HPDETECT functions.

The interrupt status bits can be found in Section 7.6.1. The status does not contain an event-capture latch (a read always yields the current condition).



### 4.5.2 HP Load Detection

The CS43130 can measure the impedance of headphone DC load. Before taking measurements, the following criteria must be met:

- The CS43130 is out of reset.
- XTAL is powered on, an external MCLK is provided or PLL mode is used to generate internal MCLK. MCLK\_INT is
  properly configured.
- The headphone output is powered down (PDN\_HP = 1).
- The alternate headphone input is powered down (HP\_IN\_EN = 0).
- HPDETECT is high to indicate a headphone is plugged in.
- The HPLOAD\_EN bit is set to turn on the impedance measurement subsystem. HPLOAD\_ON\_INT is unmasked and there has been a long enough wait to confirm the subsystem is properly started.
- The HPLOAD\_DC\_DONE interrupt is unmasked.

Either Channel A or Channel B to be measured by setting HPLOAD\_CHN\_SEL. The measurement process by clearing and setting the HPLOAD\_DC\_START bit. Once started, HPLOAD\_DC\_BUSY bit is set and a slowly ramping voltage is asserted on the headphone load for a maximum of 200 ms, then holds constant for 100 ms. Fig. 4-11 shows the a waveform of the impedance detection voltage.



rigure 4-11. Impedance Detection VC

Upon measurement completion, the following occurs:

- 1. The voltage asserted ramps down for 200 ms and is then removed.
- 2. The result of the measured resistance is reported in RL\_DC\_STAT.
- 3. HPLOAD\_DC\_DONE bit is set and the interrupt is triggered.
- 4. If HPLOAD\_DC\_ONCE bit has not been set, it is set. This bit is sticky until an HP unplug event has happened.

Once interrupted, the application processor services the interrupt by reading HPLOAD\_DC\_DONE\_INT. At this point, another measurement process can be initiated by clearing and setting the HPLOAD\_DC\_START bit. The impedance measurement subsystem can also be turned off by clearing the HPLOAD\_EN bit. HPLOAD\_EN must be cleared (and confirmed by unmasked HPLOAD\_OFF\_INT) before enabling the headphone output or the alternate headphone input.

During the impedance measurement process, the following conditions trigger the error interrupt bits:

- The headphone load is not present or is unplugged before the impedance measurement is complete (HPLOAD\_ UNPLUG\_INT).
- The headphone load is out of range, as specified in Table 3-6 (HPLOAD\_OOR\_INT).
- The AC headphone load measurement process is initiated before the HPLOAD\_DC\_ONCE bit is set (HPLOAD\_ NO\_DC\_INT).

The HPLOAD error interrupt bits are sticky. If any HPLOAD error interrupt bits are flagged, the RL\_DC\_STAT value should be treated as invalid.



### 4.5.2.1 AC Load Detection

The CS43130 can also measure the headphone load impedance in the frequency range of 20 Hz to 20 kHz. The required conditions before the measurement is similar to the low frequency load measurement, with one exception—HPLOAD\_MEAS\_FREQ is set at the frequency of interest. Refer to Section 7.5.11 and Section 7.5.12 for details.

After HPLOAD\_AC\_START bit is cleared and set:

- 1. HPLOAD\_AC\_BUSY bit is set
- 2. The result of the measured resistance is reported in RL\_AC\_STAT.
- 3. HPLOAD\_AC\_DONE\_INT is set and the interrupt is triggered.

For each headphone, the low-frequency load measurement must be performed (as indicated by the HPLOAD\_DC\_ONCE bit) before any impedance is measured at other frequencies. If the low-frequency load measurement is not performed and the process is initiated by pulsing the HPLOAD\_AC\_START bit low and high, the CS43130 can not generate a test signal and sets the HPLOAD\_NO\_DC\_INT error interrupt bit. Any RL\_AC\_STAT value should be treated as invalid.

Once the HPLOAD\_MEAS\_FREQ is set to a non-zero value and HPLOAD\_EN = 1, a tone at the specified frequency is applied on the headphone load. Because the test tone is in the audio frequency range, it can be audible by the headphone user. It is recommended that the user system notify the headphone user of the expected events before initiating this measurement.

For each frequency, the measurement completion time is affected by the frequency of interest. The lower the frequency, the longer the measurement time. For the relationship between the frequency under test and the measurement time, the following applies:

- For frequencies under test less than 6 kHz or when the CS43130 comes out of reset, measurement time is up to 11 periods of the test tone.
- For frequencies under test between 6 and 13 kHz, measurement time is up to 22 periods of the test tone.
- For frequencies under test between 13 and 20 kHz, measurement time is up to 33 periods of the test tone.

See Section 5.11.3 for example code of AC impedance measurement.

## 4.6 Clocking Architecture

## 4.6.1 Master Clock (MCLK) Sources

The MCLK is required by the CS43130 to operate any functionality associated with control, serial-port operation, or data conversion. Depending on the setting of MCLK\_SRC\_SEL (see p. 96), the MCLK can be provided by one of following methods:

- Sourced from a crystal oscillator between XTI/MCLK and XTO pins (see Fig. 4-12), then used directly as MCLK\_INT
- Externally sourced through the XTI/MCLK input pin (see Fig. 4-13)
- PLL reference clock is provided through the XTI/MCLK input pin (see Fig. 4-13), then use internal PLL to convert into MCLK\_INT
- Use internal RCO as MCLK. Note that for optimized power consumption, the HPIN input path is the only supported audio playback feature in this mode. Also, this mode can support HP detection and I<sup>2</sup>C communication. DAC playback and headphone impedance measurement functions are not supported.



Figure 4-12. System Clocking—Crystal Mode




Figure 4-13. System Clocking—External MCLK Mode

If XTAL is used, the supported crystal characteristics and frequencies are listed in Table 3-14. Based on the crystal selection, XTAL\_IBIAS must be set properly before powering up. The XTAL\_IBIAS information can be found in Section 5.3. PDN\_XTAL is cleared to start the crystal oscillator. PDN\_XTAL is set to power down the crystal oscillator. The XTAL\_READY\_INT and XTAL\_ERROR\_INT status bits indicate the status of crystal operation after power-up. At t<sub>XTAL\_pup</sub> after the crystal oscillator is powered up, if the crystal is started successfully and ready to be used, XTAL\_READY\_INT is set; if the crystal is started unsuccessfully, XTAL\_ERROR\_INT is set. The two bits are mutually exclusive when set. Both status bits have corresponding interrupt status bits and interrupt mask bits. To be informed on the crystal status at t<sub>XTAL\_pup</sub> after power-up, unmask both interrupts before powering up the crystal.

When the MCLK is supplied to the device through the XTI/MCLK pin, it must comply with the phase-noise mask shown in Fig. 4-14. Its frequency must be one of the nominal MCLK\_INT frequencies (22.5792 or 24.576 MHz), and its duty cycle must be between 45% to 55%.



Figure 4-14. MCLK Phase Noise Mask Without PLL



When the PLL reference clock is supplied to the device through the XTI/MCLK pin, it must comply with the phase-noise mask shown in Fig. 4-15.



Figure 4-15. MCLK Phase Noise Mask With PLL

Further restrictions are listed in Table 4-3.

Table 4-3.	MCLK	Source	Restrictions
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Internal MCLK Source	MCLK_SRC_SEL	MCLK_INT	Restrictions
Direct MCLK	00	0	Nominal MCLK_INT frequency = 24.576 MHz
or XTAL			<ul> <li>All specified CLKOUT frequencies (generated by PLL or XTAL) are supported</li> </ul>
			<ul> <li>CLKOUT outputs (/2, /3, /4, /8 divide) optionally</li> </ul>
		1	Nominal MCLK_INT frequency = 22.5792 MHz
			<ul> <li>All specified CLKOUT frequencies (generated by PLL or XTAL) are supported</li> </ul>
			<ul> <li>CLKOUT outputs (/2, /3, /4, /8 divide) optionally</li> </ul>
PLL	01	0	Nominal MCLK_INT frequency = 24.576 MHz
			<ul> <li>PDN_PLL = 0 and PLL properly configured to generate 24.576 MHz given reference input frequency on XTI/MCLK pin</li> </ul>
			<ul> <li>Only MCLK_INT on CLKOUT is supported on CLKOUT pin</li> </ul>
			<ul> <li>CLKOUT outputs (/2, /3, /4, /8 divide) optionally</li> </ul>
		1	Nominal MCLK_INT frequency = 22.5792MHz
			<ul> <li>PDN_PLL = 0 and PLL properly configured to generate 22.5792 MHz given reference input frequency on XTI/MCLK pin</li> </ul>
			<ul> <li>Only MCLK_INT on CLKOUT is supported on CLKOUT pin</li> </ul>
			CLKOUT outputs (/2, /3, /4, /8 divide) optionally
RCO	10	X	<ul> <li>No MCLK_INT selection necessary. DAC playback is not supported. I2C port and HPIN_x pins are supported.</li> </ul>





Figure 4-16. MCLK Source Switching

A source to MCLK\_INT, either the XTAL (or external MCLK), the PLL, or the RCO, must be provided as long as the CS43130 is operating; otherwise, the CS43130 enters a nonresponsive state, and I<sup>2</sup>C SDA signal can be held low. The only way to recover from this nonresponsive state is either through a reset or a POR event. Switching MCLK sources during DAC operation causes audible artifacts, but does not put the device in an unrecoverable state. In an MCLK source-switching event, the intended clock source must be present and ready before switching occurs.

After POR or reset event, RCO is selected as default source of MCLK\_INT.

### 4.6.1.1 Internal RC Oscillator

As described in Section 4.6.1, the CS43130 includes an internal RC oscillator that can be used as a clock source for peripheral circuit such as control port or charge pump.

# 4.7 Clock Output and Fractional-N PLL

The CS43130 clock output can be used as a master clock for other data-conversion or signal-processing components, which requires synchronous timing to the CS43130.

The CLKOUT output is enabled by clearing PDN\_CLKOUT.



Figure 4-17. CLKOUT Source Selection

Once enabled, CLKOUT is generated either from the internal crystal oscillator output (when used) or from the integrated fractional-N PLL; it can be selected by CLKOUT\_SEL. CLKOUT\_DIV can be used to set /2, /3, /4, or /8 to divide the selected clock source to targeted frequency.

## 4.7.1 Fractional-N PLL

The CS43130 has an integrated fractional-N PLL to support the clocking requirements of various applications. This PLL can be enabled or disabled by clearing or setting PDN\_PLL bit. The input reference clock for the PLL is signal on XTI/ MCLK pin (crystal-generated or external-feed).



### 4.7.2 Fractional-N PLL Internal Interface

Fig. 4-18 shows how PLL operation can be configured.



Figure 4-18. Fractional-N PLL

Use Eq. 4-1 to calculate the PLL output frequency.

$$PLL_OUT = \frac{PLL_REF}{PLL_REF_PREDIV} \times \frac{PLL_DIV_INT + PLL_DIV_FRAC}{\frac{500}{512}} \text{ or } 1, \text{ selected by PLL_Mode} \times \frac{1}{PLL_OUT_DIV}$$

**Equation 4-1. PLL Output Frequency Equation** 

PLL\_REF source must be in range below:

PLL_REF Source	PLL_REF_PREDIV Input				
	Minimum	Maximum			
MCLK/XIN pin	9.6 MHz	26 MHz			

Table 4-4 lists common settings with XTAL input as PLL reference.

Table 4-4. PLL Configuration for	r Typical Use Case (XTAL	as the PLL Reference)
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XTAL (MHz)	PLL_REF_PREDIV (Divide-by Value)	PLL_REF_PREDIV (Setting)	PLL_ DIV_INT	PLL_DIV_FRAC	PLL_OUT_DIV	PLL_ MODE	PLL OUT (MHz)	PLL_CAL_ RATIO
22.5792	8	0x3	0x44	0x06 F700	0x08	0	24.576	139
24.576	8	0x3	0x49	0x80 0000	0x0A	1	22.5792	118

Table 4-5 lists common settings with MCLK input as PLL reference.

Table 4-5. FLL Configuration for Typical Use Case (Ally/MCLK as the FLL Reference	Table 4-5.	PLL Configuration for	r Typical Use Case	(XIN/MCLK as the	PLL Reference)
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XIN/MCLK (MHz)	PLL_REF_PREDIV (Divide-by Value)	PLL_REF_PREDIV (Setting)	PLL_DIV_INT	PLL_DIV_FRAC	PLL_OUT_DIV	PLL_ MODE	PLL_OUT (MHz)	PLL_CAL_ RATIO
11.2896	4	0x2	0x40	0x00 0000	0x08	1	22.5792	128
	4	0x2	0x44	0x06 F700	0x08	0	24.576	139
22.5792	8	0x3	0x44	0x06 F700	0x08	0	24.576	139
12.000	4	0x2	0x49	0x80 0000	0x0A	0	22.5792	120
	4	0x2	0x40	0x00 0000	0x08	0	24.576	131
24.000	8	0x3	0x49	0x80 0000	0x0A	0	22.5792	120
	8	0x3	0x40	0x00 0000	0x08	0	24.576	131
12.288	4	0x2	0x49	0x80 0000	0x0A	1	22.5792	118
	4	0x2	0x40	0x00 0000	0x08	1	24.576	128
24.576	8	0x3	0x49	0x80 0000	0x0A	1	22.5792	118
9.600	4	0x2	0x49	0x80 0000	0x08	0	22.5792	151
	4	0x2	0x50	0x00 0000	0x08	0	24.576	164



XIN/MCLK (MHz)	PLL_REF_PREDIV (Divide-by Value)	PLL_REF_PREDIV (Setting)	PLL_DIV_INT	PLL_DIV_FRAC	PLL_OUT_DIV	PLL_ MODE	PLL_OUT (MHz)	PLL_CAL_ RATIO
19.200	8	0x3	0x49	0x80 0000	0x08	0	22.5792	151
	8	0x3	0x50	0x00 0000	0x08	0	24.576	164
13.000	4	0x2	0x45	0x79 7680	0x0A	1	22.5792	111
	4	0x2	0x3C	0x7E A940	0x08	1	24.576	121
26.000	8	0x3	0x45	0x79 7680	0x0A	1	22.5792	111
	8	0x3	0x3C	0x7E A940	0x08	1	24.576	121

Note that in Table 4-4 and Table 4-5:

- The PLL\_OUT\_DIV value must be even.
- PLL\_OUT frequencies are at 22.5792 or 24.576 MHz. CLKOUT frequencies can be obtained by configuring the CLKOUT\_DIV value:

PLL_OUT	CLKOUT_DIV (2)	CLKOUT_DIV (3)	CLKOUT_DIV (4)	CLKOUT_DIV (8)
22.5792 MHz	11.2896 MHz	7.5264 MHz	5.6448 MHz	2.8224 MHz
24.576 MHz	12.288 MHz	8.192 MHz	6.144 MHz	4.096 MHz

• PLL\_ERROR\_INT constantly monitors the PLL error status after PLL\_START is set, assuming the PLL reference input is stable and accurate.

### 4.7.2.1 Powering Up the PLLs

To power up the PLL, follow the following default sequence:

- 1. Enable the PLL by clearing PDN\_PLL.
- 2. Configure PLL\_REF\_PREDIV.
- 3. Configure PLL\_OUT\_DIV.
- 4. Configure the three fractional factor registers, PLL\_DIV\_FRAC.
- 5. Set the integer factor, PLL\_DIV\_INT, to the desired value.
- 6. Configure PLL\_MODE and PLL\_CAL\_RATIO.
- After properly unmasked (clearing PLL\_READY\_INT\_MASK and PLL\_ERROR\_INT\_MASK), PLL\_READY\_INT, and PLL\_ERROR\_INT are used to monitor if PLL has been successfully started.
- 8. Turn on the PLL by setting PLL\_START.

#### 4.7.2.2 Powering Down the PLL

- 1. Clear PLL\_START to stop the PLL operation.
- 2. For further power saving, set PDN\_PLL to disable the PLL block.

## 4.8 Filtering Options

To accommodate the increasingly complex requirements of digital audio systems, the CS43130 incorporates selectable filters in different playback modes. Note that when switching between filter options, the CS43130 headphone needs to be powered down in accordance with the sequence specified in Section 5.7.1 first before applying any filter changes. After the filter is changed, for audio playback, the CS43130 headphone must be powered up.

For PCM/TDM mode, the following interpolation filtering options can be selected:

- Fast roll-off and slow roll-off interpolation filter options.
- In each option above, both low-latency and normal phase-compensation filtering options can be used.
- Nonoversampling (NOS) mode is provided, which minimizes the internal digital processing. Once NOS mode is set, the settings on the above two options are ignored.



The combination of the options results in five different filter combinations. The specifications for each filter can be found in Table 3-8, and response plots can be found in Section 9. These filters have been designed to accommodate a variety of musical tastes and styles. The PCM filter option register (see Section 7.5.2) is used to select filter options.

When in octuple-speed mode, the filter options above are not available and the internal digital processing is minimized. See the specification in Table 3-8 for filter characteristics.

The DSD processor mode uses a decimation-free DSD processing technique that allows for features such as matched PCM level output, DSD volume control, and 50-kHz on-chip filter.

# 4.9 Audio Serial Port (ASP)

The independent, highly configurable ASPs and auxiliary serial ports (XSPs) communicate audio data from other system devices, such as applications processors. Both ports can be configured to support common audio interfaces, TDM/I<sup>2</sup>S and left-justified (LJ).

ASP supports both PCM and DoP stream playback. XSP can only support DoP stream playback. For DAC playback, only one port needs to be enabled. Both ports are enabled only in specific application, such as PCM notification mixing with DSD/DoP content. Details regarding this application setup can be found in Section 4.12.

In this section, the reference to both ports is generalized as "xSP" to explain the common settings between the two ports.

# 4.9.1 Master and Slave Timing

Each serial port can operate as either the master of timing or as a slave to another device's timing. If  $xSP_M/\overline{S}$  is set, the serial port acts as a clock master. If  $xSP_M/\overline{S}$  is cleared, the serial port acts as a clock slave.

- In Master Mode, xSP\_SCLK and xSP\_LRCK are outputs derived from the internal MCLK.
- In Slave Mode, xSP\_SCLK and xSP\_LRCK are inputs. Although the CS43130 does not generate the interface timings in Slave Mode, the expected LRCK and SCLK format must be programmed in the same way as in Master Mode (see Table 3-18).
- In both modes, the serial port sample rate register (xSP\_SPRATE) must be set per audio content before enabling the serial port.
- When using ASP for PCM playback, the audio serial port sample bit size register (ASP\_SPSIZE) must be set per audio content before enabling the ASP.
- When using XSP or ASP for DoP playback, the serial port sample bit size register (XSP\_SPSIZE or ASP\_SPSIZE) must be set per audio content before enabling the XSP or ASP. Note that the XSP\_SPSIZE or ASP\_SPSIZE must reflect the length of both DSD marker bits together with audio bits.

## 4.9.2 Power-Up, Power-Down, and Tristate

The xSP has separate power-down and tristate controls (PDN\_xSP and xSP\_3ST) for input data paths, which minimizes power consumption if the input port is not used. xSP master/slave operation is controlled only by the xSP\_M/S setting, irrespective of the PDN\_xSP and xSP\_3ST settings.

- PDN\_xSP. If a serial port's SDIN functionality is not required, xSP can be powered down by setting PDN\_xSP, which powers down the input data path and clocks of the serial port.
- xSP\_3ST. In Master Mode, setting xSP\_3ST tri-states the SCLK and LRCK clocks. Before setting an xSP\_3ST bit, the associated serial port must be powered down and must not be powered up until the xSP\_3ST bit is cleared. In Slave Mode, xSP\_3ST does not affect the functionality of SCLK and LRCK clocks, given both pins are input pins.

## 4.9.3 I/O

The ASP port is associated with SDIN1, SCLK1, and LRCK1. The XSP port is associated with SDIN2, SCLK2, and LRCK2, which are shared with DSD interface:

• SCLKx—Serial data shift clock



- LRCKx—Toggles at external sample rate (Fs<sub>ext</sub>). LRCK (left/right, I<sup>2</sup>S) identifies each channel's (left or right) location in the data word when I<sup>2</sup>S format is used. LRCK identifies the start of each serialized data word. FSYNC (frame sync clock, TDM) identifies the start of each TDM frame.
- SDINx—Serial data input

# 4.9.4 High-Impedance Mode

Serial ports can be placed on a clock bus that allows multiple masters without the need for external buffers. xSP\_3ST bits place the internal buffers for the respective serial-port interface signals in a high-impedance state, allowing another device to transmit clocks without bus contention. When the CS43130 serial port is a timing slave, its SCLK and LRCK I/Os are always inputs and are thus unaffected by the xSP\_3ST control. Fig. 4-19 shows the busing for CS43130 master timing serial-port use case.



Note: x = XSP or ASP

Figure 4-19. Serial Port Busing when Master Timed

## 4.9.5 Clock Generation and Control

The CS43130 has a flexible serial port clock generation subsystem that allows independent clocking of the two serial ports. When operating as a master port, the serial port provides a bit clock (xSP\_SCLK) and a left-right/frame sync signal (xSP\_LRCK/FSYNC).

Fig. 4-20 and Fig. 4-21 show the serial port clocking architecture.



Figure 4-20. xSP SCLK and MCLK Architecture



As shown in Fig. 4-20, the master-mode SCLK output for each serial port is derived from the internal MCLK. The SCLK output can be configured to various frequencies to accommodate many sample rates, sample sizes, and channel counts. The SCLK is output of a fractional divide from the internal MCLK input, where N is the numerator and M is the denominator.

**Note:** Depending on the chosen fractional divide configuration, the SCLK duty cycle can vary by one MCLK period.

Input and output SCLK polarity controls (xSP\_SCPOL\_IN and xSP\_SCPOL\_OUT) are also available. As shown in Fig. 4-20, if Master Mode is used, both polarity controls affect the SCLK used by the serial port module. For example, both polarity controls must be set to invert (xSP\_SCPOL\_IN = xSP\_SCPOL\_OUT = 1) to invert the SCLK output and output data on the falling edge. In typical use cases, the values of xSP\_SCPOL\_IN equals xSP\_SCPOL\_OUT in each serial port. See Fig. 4-23 for example waveforms showing the various settings of the SCLK polarity controls.

Likewise, input and output LRCK polarity controls (xSP\_LCPOL\_IN and xSP\_LCPOL\_OUT) are available. In Master Mode, both LRCK polarity controls affect the LRCK used by the serial-port module as shown in Fig. 4-21. In typical-use cases, the value of xSP\_LCPOL\_IN equals xSP\_LCPOL\_OUT in each serial port.



Figure 4-21. xSP LRCK Architecture

As shown in Fig. 4-22, xSP\_LCPR determines the LRCK/FSYNC period, in units of SCLK periods. The LRCK period effectively sets the length of the frame and the number of SCLK periods per Fs. Frame length may be programmed in single SCLK period multiples from a minimum of 16 SCLK:Fs up to 1536 SCLK:Fs.

The LRCK-high width (xSP\_LCHI) controls the number of SCLK periods for which the LRCK signal is held high during each frame. Like the LRCK period, the LRCK-high width is programmable in single SCLK periods, from a minimum of one period to a maximum of the LRCK period minus one (and an absolute maximum of 768 SCLK periods). That is, LRCK-high width must be less than the LRCK period.



Figure 4-22. xSP LRCK Period, High Width



As shown in Fig. 4-23, if Serial Port 50/50 Mode is enabled ( $xSP_5050 = 1$ ), the LRCK high duration must be programmed to the LRCK period divided by two (rounded down to the nearest integer when the LRCK period is odd). When the serial port is in 50/50 Mode, setting the LRCK high duration to a value other than half of the period results in erroneous operation.



Figure 4-23. xSP\_LRCK Period, High Width, 50/50 Mode



Fig. 4-24 shows how LRCK frame start delay (xSP\_FSD) controls the number of SCLK periods delay from the LRCK synchronization edge to the start of frame data.



#### Figure 4-24. LRCK FSD and SCLK Polarity Example Diagram

Table 4-6.	Serial Port Clock	Generation-	-Supported C	Configurations	for 32 bits	and 2 Channels

Eroquoney (MHz)	LRCK/FSYNC	SCLKs per	LRCK Frame	VCD N[15-0]	VSD M[15.0]
i requency (winz)	Rate (kHz)	xSP_LCPR + 1	xSP_LCPR[10:0]	X3F_N[13.0]	X3F_W[13.0]
22.5792	32.000	64	63	40	441
	44.100	64	63	1	8
	48.000	64	63	20	147
	88.200	64	63	1	4
	96.000	64	63	40	147
	176.400	64	63	1	2
	192.000	64	63	80	147
	352.800	64	63	1	1
24.576	32.000	64	63	1	12
	44.100	64	63	147	1280
	48.000	64	63	1	8
	88.200	64	63	147	640
	96.000	64	63	1	4
	176.400	64	63	147	320
	192.000	64	63	1	2
	352.800	64	63	147	160
	384.000	64	63	1	1



Frequency (MHz)	LRCK/FSYNC	SCLKs per	LRCK Frame	VSP N[15:0]	VSD M[15:0]	
i requericy (wiriz)	Rate (kHz)	xSP_LCPR + 1	xSP_LCPR[10:0]	xoi _it[10:0]	ve:[.o.o]	
22.5792	32.000	128	127	80	441	
	44.100	128	127	1	4	
	48.000	128	127	40	147	
	88.200	128	127	1	2	
	96.000	128	127	80	147	
	176.400	128	127	1	1	
24.576	32.000	128	127	1	6	
	44.100	128	127	147	640	
	48.000	128	127	1	4	
	88.200	128	127	147	320	
	96.000	128	127	1	2	
	176.400	128	127	147	160	
	192.000	128	127	1	1	

Table 4-7. Serial Port Clock Generation—Supported Configurations for 32-bits and 4 Channels

# 4.9.6 Channel Location and Size

Each serial-port channel has a programmable location offset (xSP\_RX\_CHn). Channel location is programmable in single SCLK period resolution. When set to the minimum location offset, the channel transmits or receives on the first SCLK period of a new frame.

Channel size is programmable in byte resolution from 8 to 32 bits using xSP\_RX\_CHn\_RES. Channel size and location must not be programmed such that channel data extends beyond the frame boundary. Size and location must not be programmed such that data from a given SCLK period is assigned to more than one channel. The example in Fig. 4-25 shows channel location and size.



Figure 4-25. Example Channel Location and Size

# 4.9.7 Frame Start Phase

The serial port can start a frame when xSP\_LRCK/FSYNC is high or low, depending on xSP\_STP. In typical TDM use cases, a frame starts when FSYNC is high (xSP\_STP = 1).



• If xSP\_STP = 0, the frame begins when LRCK/FSYNC transitions from high to low. See Fig. 4-26 for an example in 50/50 mode. The TDM Mode behaves similarly.



Note: This diagram assumes xSP \_FSD = 0.

#### Figure 4-26. Example 50/50 Mode (ASP\_STP = 0)

 If xSP\_STP = 1, the frame begins when LRCK/FSYNC transitions from low to high. See Fig. 4-27 for an example in 50/50 mode. TDM mode is similar.



Figure 4-27. Example 50/50 Mode (ASP\_STP = 1)

### 4.9.8 50/50 Mode

In typical two-channel I<sup>2</sup>S operation (50/50 Mode, xSP\_5050 = 1), the LRCK duty cycle is 50%, and each channel is transferred during one of the two LRCK phases. In this mode, each serial port channel can be independently programmed to output when LRCK/FSYNC is high or low; this is called the *channel-active phase*.

If the active-phase control bit (xSP\_RX\_CHn\_AP) is set, the respective channel is output when LRCK/FSYNC is high. If xSP\_RX\_CHn\_AP is cleared, the respective channel is output if LRCK/FSYNC is low. Examples of each setting of xSP\_RX\_CHn\_AP are shown in Fig. 4-26 and Fig. 4-27.

In 50/50 Mode, the channel location (see Section 4.9.6) is calculated within the channel-active phase. If there are N bits in a frame, the location of the last bit of each active phase is equal to (N/2) - 1.

**Note:** If xSP\_5050 is set, xSP\_LCHI must be programmed to half of xSP\_LCPR for a 50% duty cycle. Also, only two channels can be enabled for the corresponding serial port.



### 4.9.9 Serial Port Status

Each serial port has five status bits. Each bit is sticky and must be read to be cleared. The status bits have associated mask bits to mask setting the INT pin when the status bit sets. A brief description of each status bit is shown in Table 4-8.

Table 4-8.	Serial	Port	Status
------------	--------	------	--------

Name	Description	Register Reference
Request Overload	Set when too many input buffers request processing at the same time. If all channel size and location registers are properly configured to non-overlapping values, this error status must never set.	ASP_OVFL_INT p. 115 XSP_OVFL_INT p. 116
LRCK Early	Set when the number of SCLK periods per LRCK phase (high or low) is less than the expected count as determined by xSP_LCPR and xSP_LCHI.	ASP_EARLY_INT p. 116 XSP_EARLY_INT p. 116
	<b>Note:</b> The Rx LRCK early interrupt status is set during the first receive LRCK early event. Subsequent receive LRCK early events are not indicated until after valid LRCK transitions are detected.	
LRCK Late	Set when the number of SCLK periods per LRCK phase (high or low) is greater than the expected count as determined by xSP_LCPR and xSP_LCHI.	ASP_LATE_INT p. 116 XSP_LATE_INT p. 116
LRCK Error	Logical OR of LRCK early and LRCK late.	ASP_ERROR_INT p. 116 XSP_ERROR_INT p. 116
No LRCK	Set when the number of SCLK periods counted exceeds twice the value of LRCK period (xSP_LCPR) without an LRCK edge.	ASP_NOLRCK_INT p. 116 XSP_NOLRCK_INT p. 116
	The Tx No LRCK interrupt status is set during the first instance of a no transmit LRCK condition. Subsequent no transmit LRCK conditions are not indicated until after valid LRCK transitions are detected.	

# 4.9.10 Serial Port Clock Pin Status

There are various control bits available that affect the output state of the serial port clock and data pins. Table 4-9 summarizes the possible states depending on these bit settings.

xSP_3ST	xSP_M/S	PDN_xSP	xSP_SCLK Pin State	xSP_LRCK/FSYNC Pin State
1	Х	Х	Hi-Z with weak pull-down	Hi-Z with weak pull-down
0	0	Х	Hi-Z with weak pull-down	Hi-Z with weak pull-down
0	1	0	Active	Active
0	1	1	Inactive	Inactive <sup>1</sup>

Table 4-9. xSP\_SCLK and xSP\_LRCK/FSYNC Pin States

1.If xSP\_LCPOL\_OUT is set, xSP\_LRCK/FSYNC inactive output is high. If xSP\_LCPOL\_OUT is cleared, xSP\_LRCK/FSYNC inactive output is low.

## 4.9.11 DoP (DSD over PCM) Mode

DoP is a protocol for packetizing DSD data into a PCM frame for transmission over an existing I<sup>2</sup>S interface. The ASP or XSP can accept DSD data in DoP format.

To use the DoP interface in Slave Mode, if MCLK\_INT = 22.5792 MHz, the DoP interface clocks are required to be synchronous to MCLK\_INT.



Each sample is 24 bits, as shown in Fig. 4-28, where the 8 most significant bits are used for the DSD marker and alternate with each sample between 0x05/0xFA. Each channel within a sample contains the same marker. The remaining 16 least significant bits are then used for the DSD data, with the first or oldest bit in Slot t0. It is required that markers are provided continuously when the DoP interface is enabled, or a random sustained DC voltage asserts on loads from CS43130 outputs.



Data Stream Example of Stereo DoP

#### Figure 4-28. DoP Data Sample and Stereo Stream Example

Each PCM frame is assigned to a specific channel (left or right), and when used for DSD streaming, each PCM frame contains only DSD data corresponding to its assigned channel. The CS43130 unpacks the received DoP data and reforms it into a DSD stream to feed the internal DSD data paths.

It includes the following features:

- 24 bits per PCM data sample
- I<sup>2</sup>S format is supported
- DoP data is unpacked internally for DSD playback
- Clock Master and Slave Mode
- Up to 128 Fs DSD stream
  - Accepts a 64•Fs DSD stream with LRCK@176.4 kHz
  - Accepts a 128•Fs DSD stream with LRCK@352.8 kHz

To enable DoP interface on the ASP to take in DSD source:

- 1. Configure the ASP per clocking/format required by DoP content.
- 2. Configure DSD\_SPEED per DoP content.
- 3. Set DSD\_PRC\_SRC = 01 and DSD\_EN = 1.

# 4.10 DSD Interface

The DSD interface is enabled or disabled by PDN\_DSDIF bit. When cleared, the DSD data interface is enabled. When using this interface, the DSD interface clock can be mastered by the CS43130 (DSD\_M/SB=1). If set to Master Mode, DSDCLK toggles if both PDN\_DSDIF and XSP\_3ST bits are cleared, and DSD\_EN is set.

If the DSD interface clock is slaved (DSD\_M/SB=0), when MCLK\_INT is set as 22.5792 MHz, DSDCLK is required to be synchronous to MCLK\_INT. The DSDCLK can be derived by either:

• Exporting 1/4 or 1/8 the frequency of the CS43130 crystal to CLKOUT, or



• Sourcing MCLK\_INT and DSDCLK from the same external clock source

The DSD\_EN bit, when set, is used to configure the device for processing DSD sources. DSD\_PRC\_SRC configures the DSD interface used for feeding into the DSD processor. DSD\_SPEED specifies if a 64•Fs or 128•Fs DSD stream is provided. If PDN\_DSDIF = 0 and DSD\_M/SB = 1, DSD\_SPEED determines the DSDCLK clock frequency generated. When configuring the DSD interface, follow these steps:

- 1. Configure the DSD\_M/SB, DSD\_SPEED, DSD\_PRC\_SRC, and XSP\_3ST.
- 2. Release PDN\_DSDIF.
- 3. Enable DSD\_EN.

The DSD\_PM\_EN bit selects phase modulation (data plus data inverted) as the style of data input. In this mode, the DSD\_ PM\_SEL bit selects whether a 128•Fs or 64•Fs clock is used for phase-modulated 64•Fs data (see Fig. 4-29). Use of phase modulation mode may not directly affect the performance of the CS43130, but may lower the sensitivity of other board-level components to the DSD data signals. Note that phase modulation mode is supported only for DSD 64•Fs data rate.

The CS43130 can detect overmodulation errors in the DSD data that do not comply to the SACD specification. Setting INV\_DSD\_DET enables detection of overmodulation errors. This condition is reported through the DSD\_INVAL\_A\_INT and DSD\_INVAL\_B\_INT status bits. Overmodulated DSD data is converted as received without intervention, but performance at these levels cannot be guaranteed. Setting STA\_DSD\_DET allows the CS43130 to mute a DSD stream that is stuck at 1 or 0. This condition is reported through the DSD\_STUCK\_INT status bit. See Section 7.6.5 for descriptions of the DSD error reporting bits.

More information for these register bits can be found in Section 7.

The DSD input structure and analog outputs are designed to handle a nominal 0 dB-SACD (50% modulation index) at full-rated performance. When 0 dB-SACD and 0 dBFS PCM need to be level matched, DSD\_ZERODB must be set. In this mode, signals of +3-dB SACD may be applied for brief periods of time; however, performance at these levels is not guaranteed. If sustained levels approaching +3-dB SACD levels are required, DSD\_ZERODB must be cleared, which matches a +3-dB SACD output level.



Figure 4-29. DSD Phase Modulation Mode Diagram



# 4.11 DSD and PCM Mixing

For mobile application, the CS43130 provides a feature for mixing in PCM notification during DSD playback, with the setup in Table 4-10.

PC	M Input Confi	guration		DSD Input Configurati	ion
I <sup>2</sup> S or TDM on	44.1 kHz	Master	DSD on DSD IF	2.8224 or 5.6448 MHz	Master
ASP		Slave <sup>1</sup>		on DSDCLK	Slave <sup>1</sup>
		Master	DoP on XSP	176.4 or 352.8 kHz	Master
		Slave <sup>1</sup>			Slave <sup>1</sup>

 Table 4-10. Mixing Configurations Supported by the CS43130

1. The ASP/XSP subclocks and DSDCLK are required to be synchronous.

It is assumed that the DSD path has been properly configured for DSD playback, and DSD\_AMUTE function is disabled.

During normal DSD playback, the ASP can be shut down. At the PCM notification event, the ASP must be properly configured to receive PCM samples at 44.1 kHz. After the ASP subclocks are running, set MIX\_PCM\_PREP to indicate to the CS43130 that the PCM mixing event is imminent. After 1.6 ms, MIX\_PCM\_DSD can be safely set to initiate the mixing process. After the PCM notification mixing is complete, clear both MIX\_PCM\_DSD and MIX\_PCM\_PREP at the same time. If desired, the ASP can be shut down to save power.

When mixing, use both PCM and DSD volume controls to attenuate the signal content on both paths (e.g., at least –6-dB attenuation on each) to avoid clipping on the mixing product. Use PCM\_VOLUMEx to adjust the PCM path and DSD\_VOLUMEx to adjust the DSD path. All the signal path settings apply to both path's individual settings.



Figure 4-30. PCM and DSD Mixing Signal Flow

# 4.12 Standard Interrupts

The interrupt output pin, INT, is used to signal the occurrence of events within the device's interrupt status registers. Events can be masked individually by setting corresponding bits in the interrupt mask registers. Table 4-11 lists interrupt status and mask registers. The configuration of mask bits determines which events cause the immediate assertion of INT:

- When an unmasked interrupt status event is detected, the status bit is set, and INT is asserted.
- When a masked interrupt status event is detected, the interrupt status bit is set, but INT is not affected.

Once INT is asserted, it remains asserted until all status bits that are unmasked and set have been read. Interrupt status bits are sticky and read-to-clear. Once set, they remain set until the register is read and the associated interrupt condition is not present. If a condition is still present and the status bit is read, although INT is deasserted, the status bit remains set.

To clear status bits set due to the initiation of a block, all interrupt status bits must be read after the corresponding module is enabled and before normal operation begins. Otherwise, unmasking these previously set status bits causes assertion of INT.

Interrupt source bits are set when edge-detect interrupts is detected, and they remain set until the register is read and the condition that caused the bit to assert is no longer present.



#### Fig. 4-31 shows sticky-bit behavior.



Figure 4-31. Example of Rising-Edge-Sensitive, Sticky, Interrupt-Status-Bit Behavior

#### Table 4-11. Interrupts Events and Register Bit Fields

Interrupt	Register Bit Field	Interrupt Mask Field
DAC overflow	DAC_OVFL_INT	DAC_OVFL_INT_MASK
HP unplug detect	HPDETECT_UNPLUG_INT	HPDETECT_UNPLUG_INT_MASK
HP plug detect	HPDETECT_PLUG_INT	HPDETECT_PLUG_INT_MASK
XTAL is ready	XTAL_READY_INT	XTAL_READY_INT_MASK
XTAL error detected	XTAL_ERROR_INT	XTAL_ERROR_INT_MASK
ASP overload	ASP_OVLD_INT	ASP_OVLD_INT_MASK
ASP error	ASP_ERR_INT	ASP_ERR_INT_MASK
ASP late	ASP_LATE_INT	ASP_LATE_INT_MASK
ASP early	ASP_EARLY_INT	ASP_EARLY_INT_MASK
ASP no LRCK	ASP_NOLRCK_INT	ASP_NOLRCK_INT_MASK
XSP overload	XSP_OVLD_INT	XSP_OVLD_INT_MASK
XSP error	XSP_ERR_INT	XSP_ERR_INT_MASK
XSP late	XSP_LATE_INT	XSP_LATE_INT_MASK
XSP early	XSP_EARLY_INT	XSP_EARLY_INT_MASK
XSP no LRCK	XSP_NOLRCK_INT	XSP_NOLRCK_INT_MASK
PLL is ready	PLL_READY_INT	PLL_READY_INT_MASK
PLL error detected	PLL_ERROR_INT	PLL_ERROR_INT_MASK
Power down done	PDN_DONE_INT	PDN_DONE_INT_MASK
HP load error: DC measurement is not performed before AC measurement	HPLOAD_NO_DC_INT	HPLOAD_NO_DC_INT_MASK
HP load error: HP is unplugged during the measurement process		HPLOAD_UNPLUG_INI_MASK
HP load error: out of range result is measured	HPLOAD_OOR_INT	HPLOAD_OOR_IN1_MASK
HP load AC detection done	HPLOAD_AC_DONE_INT	HPLOAD_AC_DONE_INT_MASK
HP load DC detection done	HPLOAD_DC_DONE_INT	HPLOAD_DC_DONE_INT_MASK
HP load state machine turned off properly	HPLOAD_OFF_INT	HPLOAD_OFF_INT_MASK
HP load state machine turned on properly	HPLOAD_ON_INT	HPLOAD_ON_INT_MASK
DSD stuck Error	DSD_STUCK_INT	DSD_STUCK_INT_MASK
DSD channel A invalid error	DSD_INVAL_A_INT	DSD_INVAL_A_INT_MASK
DSD channel B invalid error	DSD_INVAL_B_INT	DSD_INVAL_B_INT_MASK
DSD channel A silence pattern detected	DSD_SILENCE_A_INT	DSD_SILENCE_A_INT_MASK
DSD channel B silence pattern detected	DSD_SILENCE_B_INT	DSD_SILENCE_B_INT_MASK
DSD rate error detected	DSD_RATE_INT	DSD_RATE_INT_MASK
DoP marker detected	DOP_MRK_DET_INT	DOP_MRK_DET_INT_MASK
DoP engine on	DOP_ON_INT	DOP_ON_INT_MASK

# 4.13 Control Port Operation

The control port is used to access control registers and on-chip memory locations, allowing the device to be configured for desired operational modes and formats. Control port operation may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, control port pins must remain static if no operation is required.



The control port operates using a I<sup>2</sup>C interface with the CS43130 acting as a <u>slave device</u>. Device communication must not begin until t<sub>PUD</sub> (refer to <u>Table 3-20</u>) after power conditions are ready and <u>RESET</u> is released.

# 4.13.1 I<sup>2</sup>C Control Port Operation

The I<sup>2</sup>C control port operates completely asynchronously with the audio sample rates. However, to avoid interference problems, the I<sup>2</sup>C control-port pins must remain static if no operation is required.

The control-port uses the I<sup>2</sup>C interface, with the chip acting as a slave device. The I<sup>2</sup>C control port can operate in the following modes:

- Standard Mode (SM), with a bit rate of up to 100 kbit/s
- · Fast Mode (FM), with a bit rate of up to 400 kbit/s
- Fast Mode Plus (FM+), with a bit rate of up to 1 Mbit/s

SDA is a bidirectional data line. Data is clocked into and out of the CS43130 by the SCL clock. Fig. 4-32, Fig. 4-33, and Fig. 4-34 show signal timings for read and write cycles. A Start condition is defined as a falling transition of SDA while SCL is high. A stop condition is defined as a rising transition of SDA while SCL is high. All other transitions of SDA must occur while SCL is low.

To configure the last two bits of I<sup>2</sup>C address, CS43130 detects the ADR resistor connection type and measures the resistance upon a device power up (POR event) or after a hardware reset event (RESET deasserted). Based on the detected resistance, the I<sup>2</sup>C address is latched and cannot be changed until the next hardware reset event. The I<sup>2</sup>C address configuration is not ready until t<sub>PUD</sub> after the hardware reset event. During this period, the CS43130 does not respond to any user-issued I<sup>2</sup>C command. After configuration, the IC tristates the ADR pin and becomes high impedance internally to avoid a constant bias current.

When the ADR pin is directly connected to ground, the last two bits of the I<sup>2</sup>C address are configured as 00 (default). For the other options, use a resistor (with 5% accuracy) as suggested in the Table 4-12.

Connection Type	Resistor Value (Ω)	Last Two Bits of I <sup>2</sup> C Address
Pull-up to VL	0	11
Pull-up to VL	4990	10
Pull-down to GND	4990	01
Pull-down to GND	0	00 (Default)

#### Table 4-12. I<sup>2</sup>C Address Configurations

If the operation is a write, the 3 bytes after the chip address are the memory address pointer (MAP) that select the address of the register to be read or written to next. The byte following the MAP is the control byte. Bit[0] of the control byte, INCR, selects whether autoincrementing is to be used (INCR = 1), allowing successive reads or writes of consecutive registers. Bits[2:1] of the control byte indicate the size of the data for the autoincrement to be acted on. Table 4-13 explains the format for the I<sup>2</sup>C control byte.

Table 4-13. I <sup>2</sup> C Control-Byte Forma	Table 4-13.	I <sup>2</sup> C Cont	rol-Byte	Format
-------------------------------------------------	-------------	-----------------------	----------	--------

Bit	Name	Description
7:3	_	Reserved
		Default: 0
2:1	SIZE	Register access width. Specifies the width of the register access.
		00 8-bit (1 byte) 01–11 Reserved
0	INCR	Setting this bit allows the MAP address to autoincrement. The MAP address automatically increments every SIZE + 1 bytes accessed consecutively.
		0 Disabled 1 Enabled

Each byte transferred on the I<sup>2</sup>C bus is separated by an acknowledge (ACK) bit. The CS43130 acknowledges each input byte read from the host, and the host must acknowledge each byte transmitted from the CS43130.



For write operations, the data bytes following the MAP byte are written to the CS43130 register addresses pointed to by the last received MAP address, plus however many autoincrements have occurred. Fig. 4-32 shows a write pattern with autoincrementing.



Figure 4-32. Control Port Timing, I<sup>2</sup>C Writes with Autoincrement (8-bit Data Access)

For read operations, the contents of the register pointed to by the last received MAP address (plus however many autoincrements have occurred if INCR was previously set) are output in the next byte. Fig. 4-33 shows a read pattern following the write pattern in Fig. 4-32. Notice how read addresses are based on the MAP bytes from Fig. 4-32.



Figure 4-33. Control Port Timing, I<sup>2</sup>C Reads with Autoincrement (8-Bit Data Access)

To generate a read address not based on the last received MAP address, an aborted write operation can be used as a preamble (see Fig. 4-34). Here, a write operation is aborted (after the ACK for the control byte) by sending a Stop condition.



Figure 4-34. Control Port Timing, I<sup>2</sup>C Reads with Preamble and Autoincrement (8-Bit Data Access)



# **5** Applications

This section provides recommended application procedures and instruction sequences for standard CS43130 operations.

# 5.1 PLL Clocking

Data-path logic is in the MCLK\_INT domain, where MCLK\_INT is expected to be 22.5792 or 24.576 MHz. For clocking scenarios in which the external system MCLK provided to CS43130 is neither 22.5792 nor 24.576 MHz, the PLL must be turned on to provide the desired internal MCLK. At start up, the system uses RCO as the internal MCLK for PLL programming over I<sup>2</sup>C and switches to the PLL output after it settles. PLL start-up time is a maximum of 1 ms.

# 5.2 Power Sequencing

Note the following for power-up sequencing on the CS43130:

- VP must be powered up first.
- All other supplies can come up in any order before RESET is released.

Note the following for power-down sequencing on the CS43130:

- After RESET is asserted, VA/VCP/VL/VD can be removed in any order.
- VP must be powered down last.

# 5.3 Crystal Tuning

The CS43130 uses an external crystal as the source for internal MCLK. Refer to Table 3-14 for the load capacitance that is supported by CS43130. Table 5-1 lists supported crystals that meet the requirements for CS43130 and also shows also shows the XTAL\_IBIAS settings for different crystals.

Manufacturer <sup>1</sup>	Part Number <sup>1</sup>	Frequency (MHz)	Bias Current Strength (μA)	Crystal Setting Register (0x20052)
River Electronics	FCX-06-22.5792J51933	22.5792	12.5	0x04
	FCX-06-24.5760J51930	24.576	7.5	0x06
NDK	NX2016SA 22.5792M EXS00A-CS09116	22.5792	15	0x02
	NX2016SA 24.576M EXS00A-CS09117	24.576		
TXC	8Y22570001	22.5792	12.5	0x04
	8Y24570001	24.576		

#### Table 5-1. Example List of Supported Crystals

1. Contact your local Cirrus Logic representative for a list of supported manufacturers and part numbers.

The crystal setting register (0x20052) must be set appropriately based on the crystal used.

The frequency at which the crystal eventually oscillates can be calculated using the formula below:

 $F_{osc} = 1/(2^{*}\pi^{*}sqrt[Lm^{*}(C_{m}(C_{0}+C_{L}))/(C_{m}+C_{0}+C_{L})])$ ,

#### where

L<sub>m</sub> = motional inductance of crystal

C<sub>m</sub> = motional capacitance of crystal

C<sub>0</sub> = shunt capacitance

C<sub>L</sub> = load capacitance

Trace capacitance and pad capacitance (approximately 0.5 pF) must also be taken into account while calculating the value of the load capacitors. Below are the steps to tune the crystal to the correct frequency:

1. Select load capacitor values that match the load capacitance spec in crystal manufacturer's data sheet.



- 2. Power up and verify communication with CS43130. If there is no communication, it is possible that the crystal did not start. Check power rails and load capacitance and try again.
- 3. Clear PDN\_CLKOUT in the Power Down Control (0x20000) register. This sets the clock output at MCLK\_INT/2 frequency from CLKOUT pin.
- 4. Measure the frequency and verify that it is within acceptable range of the desired frequency. If yes, continue normal operation. If not, power down the chip, change the load capacitor values and go back to step 2.

Note: These steps need to be performed only once per PCB.

# 5.4 Alert Mixing Shutdown

To prevent a DSD mute pattern from turning off the DAC while mixing DSD data with PCM data, turn off the auto mute by clearing the DSD\_AMUTE bit.

# 5.5 Enable/Disable Nonoversampling Filter

If the user decides to use the nonoversampling filter, the following sequences must be followed to enable/disable the nonoversampling filter.

## 5.5.1 Nonoversampling Filter Enable Sequence

Task	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
Configure PCM filter	0x10010	0x99	
	0xC0001	0x0C	
	PCM Filter Option 0x90000	0x22	
	FILTER_SLOW_FASTB PHCOMP_LOWLATB	0 0 1	Nonoversempling filter is selected
	Reserved	0 00	Nonoversampling linter is selected
	HIGH_PASS DEEMP_ON	1 0	High-pass filter is selected
	0x10010	0x0	

## 5.5.2 Nonoversampling Filter Disable Sequence

Task	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
Configure PCM filter	0x10010	0x99	
	0xC0001	0x0D	
	PCM Filter Option 0x90000	0x02	
	FILTER_SLOW_FASTB PHCOMP_LOWLATB NOS	0 0 0	
	Reserved HIGH_PASS DEEMP_ON	0 00 1 0	High-pass filter is selected
	0x10010	0x0	



# 5.6 Enable/Disable Alternate Headphone Path (HPINx)

If the user decides to use the HPINx path, the following sequences must be followed to enable/disable the alternate headphone path (HPINx).

### 5.6.1 HPINx Alternate Headphone Path Enable Sequence

To enable HPINx path when EXT\_VCPFILT = 0, the following sequences should be followed:

#### Example 5-1. HPINx Enable Sequence when EXT\_VCPFILT = 0

TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
Enable headphone input	0x10010	0x99	
	0x20019	0x01	
	0xB0006	0xDC	
	0xB0005	0xE4	
	HP Output Control 1. 0x80000	0x38	
	HP_CLAMPA HP_CLAMPB OUT_FS HP_IN_EN Reserved	0 0 11 1 000	Function Disabled Function Disabled Headphone output voltage setting is irrelevant Enable HPIN switch
	0x10010	0x00	

To enable HPINx path when EXT\_VCPFILT = 1, the following sequences should be followed:

#### Example 5-2. HPINx Enable Sequence when EXT\_VCPFILT = 1

TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
Enable headphone input	0x10010	0x99	
	0x20019	0x01	
	HP Output Control 1. 0x80000	0x38	
	HP_CLAMPA HP_CLAMPB OUT_FS HP_IN_EN Reserved	0 0 11 1 000	Function Disabled Function Disabled Headphone output voltage setting is irrelevant Enable HPIN switch
	0x10010	0x00	

### 5.6.2 HPINx Disable Sequence

To disable HPINx path when EXT\_VCPFILT = 0, the following sequences should be followed:

#### Example 5-3. HPINx Disable when EXT\_VCPFILT = 0

Task	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
Disable headphone input	0x10010	0x99	
	HP Output Control 1. 0x80000	0x30	
	HP_CLAMPA	0	
	HP_CLAMPB	0	
	OUT FS	11	
	HP_IN_EN	0	Disable HPIN
	Reserved	000	
	0xB0005	0x64	
	0xB0006	0x00	
	0x20019	0x00	
	0x10010	0x00	



To disable HPINx path when EXT\_VCPFILT = 1, the following sequences should be followed:

#### Example 5-4. HPINx Disable when EXT\_VCPFILT = 1

Task	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
Disable headphone input	0x10010	0x99	
	HP Output Control 1. 0x80000	0x30	
	HP_CLAMPA HP_CLAMPB OUT_FS HP_IN_EN Reserved	0 0 11 0 000	Disable HPIN
	0x20019	0x00	
	0x10010	0x00	

## 5.7 Headphone Power Down Sequences

Examples of power down sequences for PCM and DSD are shown in Ex. 5-5 and Ex. 5-6, respectively. Follow the stated sequence every time to shut down the headphone output. The sequence assumes that the PDN\_DONE\_INT interrupt bit is unmasked.

# 5.7.1 PCM Power Down Sequence

#### Example 5-5. PCM Power Down Sequence

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Enable PDN_DONE	Interrupt Mask 1. 0xF0010	data(0xF0010)	
	Interrupt		AND (UXFE)	
		DAC_OVFL_INT_MASK	x	
		HPDETECT_PLUG_INT_MASK	х	
		HPDETECT_UNPLUG_INT_MASK	x	
		XTAL_READY_INT_MASK	x	
		XTAL_ERROR_INT_MASK	х	
		PLL_READY_INT_MASK	x	
		PLL_ERROR_INT_MASK	x	
		PDN_DONE_INT_MASK	0	Enable PDN_DONE Interrupt
2	Pop-free power down	0x10010	0x99	
		0xC0002	0x12	
		0xC000E	0x02	
		0xC0009	0x12	
3	Mute	PCM Path Signal Control 1. 0x90003	data(0x90003)	
		C C	OR (0x03)	
		PCM_RAMP_DOWN	х	
		PCM_VOL_BEQA	x	
		PCM_SZC	x	
		Reserved	x	
		PCM_AMUTE	x	
		PCM_AMUTEBEQA	x	
		PCM_MUTE_A	1	Mute channel A
		PCM_MUTE_B	1	Mute channel B
4	Wait time delay. If PCM_S	ZC = 2, then delay = (255 - max(PCM_VOLU	UME_A, PCM_VOLUME	_B)) / 2 ms. Else, delay = 130 ms.
5	Power down amplifier	Power Down Control. 0x20000	data(0x20000)	
			OR (0x10)	
		PDN_XSP	х	
		PDN_ASP	x	
		PDN_DSDIF	x	
		PDN_HP	1	Turn off HP
		PDN_XTAL	x	
		PDN_PLL	х	
		PDN_CLKOUT	х	
		Reserved	X	
6	Wait for interrupt. Check for	or PDN_DONE_INT = 1 in Interrupt Status 1	register (0xF0000).	
7	Reset data buffer	0x90097	0x01	



#### Example 5-5. PCM Power Down Sequence (Cont.)

				-
STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
8	Power down ASP	Power Down Control. 0x20000	data(0x20000)	
			OR (0x40)	
		PDN XSP	х	
		PDNTASP	1	Turn off ASP
		PDN_DSDIF	х	
		PDN_HP	х	
		PDN_XTAL	х	
		PDN_PLL	х	
		PDN_CLKOUT	х	
		Reserved	х	
9	Unmute	PCM Path Signal Control 1. 0x90003	data(0x90003)	
		-	AND (0xFC)	
		PCM RAMP DOWN	х	
		PCM <sup>-</sup> VOL BEQA	х	
		PCM_SZC_	х	
		Reserved	х	
		PCM_AMUTE	х	
		PCM_AMUTEBEQA	х	
		PCM_MUTE_A	0	Unmute channel A
		PCM_MUTE_B	0	Unmute channel B
10	Restore defaults	0xC0002	0x10	
		0xC000E	0x00	
		0xC0009	0x16	
		0x10010	0x00	

# 5.7.2 DSD Power Down Sequence

#### Example 5-6. DSD Power Down Sequence

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Enable PDN_DONE interrupt	Interrupt Mask 1. 0xF0010	data(0xF0010) AND (0xFE)	
		DAC_OVFL_INT_MASK	х	
		HPDĒTECT_PLŪG_INT_MASK	х	
		HPDETECT_UNPLŪG_INT_MASK	х	
		XTAL_READY_INT_MASK	х	
		XTAL_ERROR_INT_MASK	х	
			X	
		PLL_ERROR_INT_WASK	X	Enable RDN DONE interrupt
	Den fra e never dever		0	
2	Pop-free power down	0x10010	0x99	
		0xC0002	0x12	
		0xC000E	0x02	
		0xC0009	0x12	
3	Mute	DSD Processor Path Signal Control 1. 0x70002	data(0x70002)	
		-	OR (0x03)	
		Reserved	х	
		DSD_VOL_BEQA	х	
		DSD_SZC	Х	
		Reserved	Х	
			X	
			X 1	Mute channel A
			1	Mute channel B
	Wait time delay If DSD	SZC = 1 then dology = (255 max/DSD )/OLUME		$ME(\mathbf{P}) / 2$ ma Elas delay = 120 ma
4	Wait time delay. II DSD_		_A, D3D_VOLU	ME_D)) / 2 IIIS. EISE, UEIDY - 130 IIIS.
5	Power down amplifier	Power Down Control. 0x20000	data(0x20000)	
		PDN_XSP	х	
			X	
			X 1	
			I Y	Turn on the
		PDN PLL	x	
		PDN CLKOUT	x	
		Reserved	х	
6	Wait for interrupt. Check	for PDN_DONE_INT = 1 in Interrupt Status 1 regi	ster (0xF0000).	
7	Reset data buffer	0x90097	0x01	



#### Example 5-6. DSD Power Down Sequence (Cont.)

STEP	Task	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
8	Power down DSD/XSP/ ASP interfaces	Power Down Control. 0x20000	data(0x20000) OR (0xE0)	
		PDN XSP	1	
		PDNASP	1	
		PDN_DSDIF	1	
		PDN_HP	Х	
		PDN_XTAL	х	
		PDN_PLL	Х	
		PDN_CLKOUT	Х	
		Reserved	х	
9	Unmute	DSD Processor Path Signal Control 1. 0x70002	data(0x70002)	
		-	AND (0xFC)	
		Reserved	1	
		DSD VOL BEQA	х	
		DSD_SZC	Х	
		Reserved	0	
		DSD_AMUTE	Х	
		DSD_AMUTEBEQA	Х	
		DSD_MUTE_A	0	Unmute channel A
		DSD_MUTE_B	0	Unmute channel B
10	Restore defaults	0xC0002	0x10	
		0xC000E	0x00	
		0xC0009	0x16	
		0x10010	0x00	

# 5.8 Headphone Power-Up Initialization

An example of the power-up initialization for PCM and DSD are shown in Ex. 5-7 and Ex. 5-8, respectively. Follow the stated sequence every time to initialize the headphone output.

### 5.8.1 PCM Power-Up Initialization

#### Example 5-7. PCM Power-Up Initialization

STEP	Task	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1 1	PCM Power-Up Initialization	0x10010	0x99	
		0x10025	0x01	
		0x1002E	0x00	
		0xC0006	0x01	
		0xC0002	0x12	
		0xC0009	0x00	
		0xC0003	0x28	
		0xC0005	0x28	

### 5.8.2 DSD Power-Up Initialization

#### Example 5-8. DSD Power-Up Initialization

STEP	P Task		REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	DSD Power-Up Initialization	0x10010		0x99	
		0x10025		0x01	
		0x1002E		0x00	
		0xC0006		0x01	
		0xC0002		0x12	
		0xC0009		0x00	
		0xC0003		0x1E	
		0xC0005		0x20	



# 5.9 Headphone Power-Up Sequence

An example of the power-up sequence for PCM and DSD are shown in Ex. 5-9 and Ex. 5-10, respectively. Follow the stated sequence every time to power up the headphone output.

# 5.9.1 PCM Power-Up Sequence

### Example 5-9. PCM Power-Up Sequence

STEP	Task	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Run PCM power-up initialization	on sequence in Ex. 5-7.		
2	Power up ASP	Power Down Control. 0x20000	data (0x20000) AND (0xBF)	
		PDN_XSP PDN_ASP PDN_DSDIF PDN_HP PDN_XTAL PDN_PLL PDN_CLKOUT Reserved	X O X X X X X X X	Power up ASP
3	Pop-free startup	0x1002C	0x0A	
4	Power on amplifier	Power Down Control. 0x20000	data (0x20000) AND (0xEF)	
		PDN_XSP PDN_ASP PDN_DSDIF PDN_HP PDN_XTAL PDN_PLL PDN_CLKOUT Reserved	X X O X X X X X	Power up HP
5	Wait for 10 ms			
6	Restore defaults	0xC0006	0x0C	
		0xC0002	0x10	
		0xC0009	0x20	
7	Audio output will be active. Wa	ait for 1000 ms.		
8	Restore defaults	0x1002C	0x00	
		0x10010	0x00	



# 5.9.2 DSD Power-Up Sequence

### Example 5-10. DSD Power-Up Sequence

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Run DSD power-up initia	alization sequence in Ex. 5-8.		
2	Power on appropriate interface. Power Down Control. 0x20000		data (0x20000) AND (0xHH)	For DoP on XSP, HH = 7F. For DoP on ASP, HH = BF. For DSD interface, HH = DF.
		PDN_XSP PDN_ASP PDN_DSDIF PDN_HP PDN_XTAL PDN_PLL PDN_CLKOUT Reserved	B B X X X X X X	XSP interface enable ASP interface enable DSD interface enable
3	Pop-free startup	0x1002C	0x0A	
4	Power on amplifier	Power Down Control. 0x20000	data (0x20000) AND (0xEF)	
		PDN_XSP PDN_ASP PDN_DSDIF PDN_HP PDN_XTAL PDN_PLL PDN_CLKOUT Reserved	x x 0 x x x 0	Power up HP
5	Wait for 10 ms			
6	Restore defaults	0xC0006	0x0C	
		0xC0002	0x10	
		0xC0009	0x20	
7	Audio output will be activ	ve. Wait for 1000 ms.		
8	Restore defaults	0x1002C	0x00	
		0x10010	0x00	



# 5.10 Example Sequences

This section provides recommended instruction sequences for standard CS43130 operations.

### 5.10.1 Power-up Sequence to I<sup>2</sup>S Playback

In Ex. 5-11, a 22.5792-MHz crystal is used, ASP is set to I<sup>2</sup>S master at 44.1 kHz, and full-scale output is 1.732 Vrms.

#### Example 5-11. Startup to I<sup>2</sup>S Playback

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Apply all relevant power su	upplies, then assert RESET.		
2	Wait for 1.5 ms			
3	Configure XTAL driver			
4	Configure XTAL bias	Crystal Setting. 0x20052	0x04	
	current strength (assuming	Reserved	0000 0	
	22.5792 MHz)	XTAL_IBIAS	100	Bias current set to 12.5 µA
5	Read Interrupt Status 1 re	gister (0xF0000) to clear any pending interrupts.		
6	Enable XTAL interrupts	Interrupt Mask 1. 0xF0010	0xE7	
		DAC_OVFL_INT_MASK	1	
		HPDETECT_PLUG_INT_MASK HPDETECT_UNPLUG_INT_MASK	1	Enable XTAL_READY Interrupt
		XTAL READY INT MASK	Ö	
			0	
		PLL_READY_INT_MASK	1	
		PDN_DONE_INT_MASK	1	
7	Start XTAL	Power Down Control. 0x20000	0xF6	
		PDN_XSP	1	
			1	
		PDN HP	1	
		PDN_XTAL	0	Power up XTAL driver
			1	
		Reserved	ò	
8	Apply PCM power-up initia	alization in Ex. 5-7		
9	Configure ASP interface.	Sample rate set to 44.1 kHz. ASP is clock master.		
10	Set ASP sample rate	Serial Port Sample Rate. 0x1000B	0x01	
		Reserved	0000	Sat comple rate to 11 1 kHz
11	Set ASP sample hit size	Serial Port Sample Bit Size 0v10000	0001	
	XSP is don't care	Reserved	0000	
		XSP SPSIZE	01	XSP sample bit size set to 24 bits
		ASP_SPSIZE	00	ASP sample bit size set to 32 bits
12	Set ASP numerator	ASP Numerator 1. 0x40010	0x01	
		ASP_N_LSB	0x01	LSB of ASP sample rate fractional divide numerator
		ASP Numerator 2. 0x40011	0x00	
		ASP_N_MSB	0x00	MSB of ASP sample rate fractional divide numerator
13	Set ASP denominator	ASP Denominator 1. 0x40012	0x08	
		ASP_M_LSB	0x08	LSB of ASP sample rate fractional divide denominator
		ASP Denominator 2. 0x40013	0x00	
		ASP_M_MSB	0x00	MSB of ASP sample rate fractional divide denominator
14	Set ASP LRCK high time	ASP LRCK High Time 1. 0x40014	0x1F	
			0x1F	LSB of ASP LRCK high time duration
		ASP LRCK High Time 2. 0x40015	0x00	
		ASP_LCHI_MSB	0x00	MSB of ASP LRCK high time duration
15	Set ASP LRCK period	ASP LRCK Period 1. 0x40016	0x3F	
		ASP_LCPR_LSB	0x3F	LSB of ASP LRCK period
		ASP LRCK Period 2. 0x40017	0x00	
		ASP_LCPR_MSB	0x00	MSB of ASP LRCK period



#### STEP TASK **REGISTER/BIT FIELDS** VALUE DESCRIPTION 16 Configure ASP clock ASP Clock Configuration. 0x40018 0x1C 000 Reserved ASP\_M/SB ASP\_SCPOL\_OUT ASP\_SCPOL\_IN ASP\_LCPOL\_OUT ASP\_LCPOL\_IN 1 Set ASP port to be master Configure clock polarity for I2S input 1 1 0 Õ Configure ASP frame ASP Frame Configuration. 0x40019 0x0A 17 Reserved 000 Configure ASP port to accept I<sup>2</sup>S input ASP\_STP ASP\_5050 0 1 ASP\_FSD 010 18 Set ASP channel location ASP Channel 1 Location. 0x50000 0x00 ASP RX CH1 0x00 ASP Channel 1 starts on SCLK0 ASP Channel 2 Location. 0x50001 0x00 ASP RX CH2 0x00 ASP Channel 2 starts on SCLK0 Set ASP channel size and ASP Channel 1 Size and Enable. 0x5000A 0x07 19 enable Reserved 0000 ASP\_RX\_CH1\_AP ASP\_RX\_CH1\_EN ASP\_RX\_CH1\_EN ASP\_RX\_CH1\_RES 0 ASP Channel 1 Active Phase ASP Channel 1 Enable 1 ASP Channel 1 Size is 32 bits 11 ASP Channel 2 Size and Enable. 0x5000B 0x0F 0000 Reserved ASP\_RX\_CH2\_AP ASP\_RX\_CH2\_EN ASP Channel 2 Active Phase ASP Channel 2 Enable 1 1 ASP\_RX\_CH2\_RES 11 ASP Channel 2 Size is 32 bits 20 Configure PCM interface. HPF filter is used. Deemphasis off. PCM Filter Option. 0x90000 21 Configure PCM filter 0x02 FILTER\_SLOW\_FASTB PHCOMP\_LOWLATB 0 0 NOS 0 0 00 Reserved HIGH\_PASS DEEMP\_ON High pass filter is selected 1 0 22 Set volume for channel B PCM Volume B. 0x90001 0x00 PCM VOLUME B 0x00 Set volume to 0 dB Set volume for channel A PCM Volume A. 0x90002 0x00 23 PCM VOLUME A 0x00 Set volume to 0 dB 0xEC Configure PCM path signal PCM Path Signal Control 1. 0x90003 24 contro PCM\_RAMP\_DOWN PCM\_VOL\_BEQA Soft ramp down of volume on filter change 1 1 Volume setting on both channels controlled by PCM\_ VOLUME A PCM\_SZC 10 Enable soft ramp PCM\_AMUTE Mute after reception of 8192 samples of 0 or -1. 1 PCM\_AMUTEBEQA 1 Mute only when AMUTE condition is detected on both channels Function is disabled PCM\_MUTE\_A 0 PCM\_MUTE\_B 0 Function is disabled PCM Path Signal Control 2, 0x90004 0x00 Reserved 0000 PCM\_INV\_A PCM\_INV\_B PCM\_SWAP\_CHAN PCM\_COPY\_CHAN 0 0 Disable all functions in this register ŏ 0 Configure HP 25 Configure Class H 26 Class H Control. 0xB0000 0x1E amplifier Reserved 000 ADPT PWR 1 11 Output signal determines voltage level HV\_EN EXT\_VCPFILT High voltage mode enabled 1 Using internal VCPFILT source. 0 27 Set HP output to full scale HP Output Control 1. 0x80000 0x30 HP CLAMPA 0 HP\_CLAMPB OUT FS 0 11 Set headphone output to full scale (1.732 V rms) HP\_IN\_EN 0 000 Reserved

#### Example 5-11. Startup to I<sup>2</sup>S Playback (Cont.)



STED	TASK		VALUE	
28	Configure Headphone	HP Detect 0xD0000	0x04	DESCRIPTION
20	detect		00	HD detect disabled
			00	HP detect input is not inverted
		HPDETECT RISE DBC TIME	00	Tin sense rising debounce time set to 0 ms
			10	Tip sense falling debounce time set to 500 ms
		Reserved	0	
29	Headphone detect	HP Detect. 0xD0000	0xC4	
		HPDETECT_CTRL	11	HP detect enabled
		HPDETECT_INV	0	HP detect input is not inverted
		HPDETECT_RISE_DBC_TIME	0 0	Tip sense rising debounce time set to 0 ms
		HPDETECT_FALL_DBC_TIME	10	Tip sense falling debounce time set to 500 ms
		Reserved	0	
30	Enable interrupts			
31	Read Interrupt Status 1 reg	gister (0xF0000) and Interrupt Status 2 reg	gister (0xF0001) to	clear sticky bits.
32	Enable headphone detect	Interrupt Mask 1. 0xF0010	0x87	
	interrupts	DAC_OVFL_INT_MASK	1	
		HPDETECT_PLUG_INT_MASK	0	Enable HPDETECT_PLUG interrupt
		HPDETECT_UNPLUG_INT_MASK	0	Enable HPDETECT_UNPLUG interrupt
		XTAL_READY_INT_MASK	0	
			0	
			1	
		PLL_ERROR_INT_MASK	1	
22	Enable ACD interrupte		0,07	
33	Enable ASP Interrupts		0.07	
		ASP_OVEL_INT_MASK	0	Enable ASP_OVFL Interrupt
		ASP_ERROR_INT_MASK	0	Enable ASP_ERROR Interrupt
		ASP_LATE_INT_WASK	0	Enable ASP_LATE Interrupt
		ASP NOI RCK INT MASK	0	Enable ASP_LARET Interrupt
		Reserved	111	
34	Wait for interrupt. Check if	XTAL READY INT = 1 in Interrupt Status	s 1 register (0xF000	00).
35	Switch MCLK source to	System Clocking Control 1. 0x10006	0x04	•
	XTAL	Reserved	0 0000	MCLK Source set to XTAL. MCLK_INT frequency set to
		MCLK_INT	1	22.5792 MHz
		MCLK_SRC_SEL	00	
36	Wait at least 150 µs.			
37	Enable ASP clocks	Pad Interface Configuration. 0x1000D	0x02	
		Reserved	0000 00	
		XSP_3ST	1	XSP Interface status is don't care (set to default)
		ASP_3ST	0	Enable serial clocks in Master Mode
38	Power up HP	Refer to Ex. 5-9 for PCM power-up sequ	ence. Skip Step 1 o	f Ex. 5-9 (completed in Step 8 above).

#### Example 5-11. Startup to I<sup>2</sup>S Playback (Cont.)

# 5.10.2 Power-Up Sequence to DSD Playback

In Ex. 5-12, a 22.5792-MHz crystal is used, the PLL is used to create a 24.576-MHz MCLK, XSP is set as DSD slave at 2.8224 MHz, and full-scale output is 1.732 Vrms.

Example	5-12.	Startup	to DSD	Play	vback
---------	-------	---------	--------	------	-------

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Apply all relevant power supplie	s, then assert RESET.		
2	Wait for 1.5 ms			
3	Configure XTAL driver			
4	Configure XTAL bias current	Crystal Setting. 0x20052	0x04	
	strength (assuming River Crysta	al Reserved	0 0000	
	at 22.5792 MHZ)	XTAL_IBIAS	100	Bias current set to 12.5 µA
5	Read Interrupt Status 1 register	(0xF0000) to clear any pending interrupts.		
6	Enable XTAL interrupts	Interrupt Mask 1. 0xF0010	0xE7	
		DAC_OVFL_INT_MASK HPDETECT_PLUG_INT_MASK HPDETECT_UNPLUG_INT_MASK XTAL_READY_INT_MASK XTAL_ERROR_INT_MASK PLL_READY_INT_MASK PLL_ERROR_INT_MASK PDN_DONE_INT_MASK	1 1 0 0 1 1	Enable XTAL_READY interrupt Enable XTAL_ERROR interrupt



	· · · · · · · · · · · · ·	_ · · · · <b>,</b>		
STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
7	Start XTAL	Power Down Control. 0x20000	Ux⊢6	
		PDN_XSP	1	
			1	
		PDN HP	1	
		PDN_XTAL	Ó	Power up XTAL driver
		PDN_PLL	1	
		PDN_CLKOUT	1	
		Reserved	0	
8	Apply DSD power-up initializati	on in Ex. 5-8		
9	Configure PLL. Input is 22.5792	2 MHz. Output is 24.576 MHz.		
10	Power up PLL	Power Down Control. 0x20000	0xF2	
		PDN_XSP	1	
			1	
			1	
		PDN_XTAL	ò	
		PDN_PLL	0	Power up PLL
		PDN_CLKOUT	1	
<u> </u>		Reserved	0	
11	Set PLL Pre-Divide	PLL Setting 9. 0x40002	0x03	
		PLL_REF_PREDIV	11	Divide PLL Reference by 8
			00 0000	
12	Set PLL Output Divide	PLL Setting 6. 0x30008	0x08	
		PLL_OUT_DIV	0x08	Divide PLL output by 8
13	Set Fractional portion of PLL	PLL Setting 2. 0x30002	0x00	
	divide ratio	PLL_DIV_FRAC_0	0x00	
		PLL Setting 3. 0x30003	0xF7	
		PLL DIV FRAC 1	0xF7	
		PLL Setting 4. 0x30004	0x06	
			0x06	
- 14	Cot integer partice of DLL divid	FLL_DIV_INAC_2	0x00	
14	set integer portion of PLL divid		0x44	
		PLL_DIV_IN1	0x44	
15	Set PLL Mode	PLL Setting 8. 0x3001B	0x01	
		Reserved	0000 00	
		PLL_MODE Reserved	0	Use 500/512 factor
16	Set DLL Calibration Datio	DLL Sotting 7, 0x20004		
10	Set FLL Calibration Ratio	PLL Setting 7. 0x3000A	0,00	
	<b>B</b>	PLL_CAL_RATIO	0X8B	Set PLL Cal Ratio to 139
17	Read Interrupt Status 1 register	r (0xF0000) to clear any pending interrupts.		
18	Enable PLL Interrupts	Interrupt Mask 1. 0xF0010	0xE1	
		DAC_OVFL_INT_MASK	1	
			1	Enable DLL Deady and Error Interrupte
		XTAL READY INT MASK	1 0	LINADIE FLE REAUY AND ENDI INTERTUPIS
		XTAL ERROR INT MASK	ŏ	
		PLL_READY_INT_MASK	0	
		PLL_ERROR_INT_MASK	0	
- 40	Chart DLL		I 0+04	
19	Start PLL	PLL Setting 1. UX30001	UXU1	
		Reserved	000 0001	Start DLL
		FLL_STAKT	U	Jidii MLL
20	Configure DSDIF to playback 6	A++S USU stream. USUIF is configured as a	a slave.	
21	Configure DSD Volume	DSD Volume A. 0x70001	0x00	
		DSD_VOLUME_A	0x00	Channel A volume set to 0dB
22	Configure DSD path Signal Control1	DSD Processor Path Signal Control 1. 0x70002	0xEC	
		Reserved	1	
		DSD_VOL_BEQA	1	DSD Volume B equals DSD volume A
		DSD_SZC Reserved	1 0	Soft ramp control enabled
		DSD AMUTE	1	Mute occurs after 256 repeated 8-bit DSD mute
			·	patterns
		DSD_AMUTE_BEQA	1	Mute happens only when mute pattern is detected in both channels
		DSD_MUTE_A	0	Function is disabled
		DOD WUTE D	0	

### Example 5-12. Startup to DSD Playback (Cont.)



	<u> </u>			
STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
23	Configure DSD Interface	DSD Interface Configuration. 0x70003	0x00	
		Reserved	00000	DSD is clock slave
		DSD_M/SB DSD_PM_EN	0	Function is disabled
		DSD_PM_SEL	Ō	Function is disabled
24	Configure DSD path Signal	DSD Processor Path Signal Control 2.	0x13	
	Control 2	0x70004		
		Reserved	0	
			00	Set source of DSD processor to DSDIF
		Reserved	ò	
		DSD_SPEED	0	Set DSD clock speed to 64•FS
			1	Static DSD detection enabled
25			I	Invalid DOD detection enabled
20	Configure Class H Amplifier	Class H Control 0xB0000	0v1E	
20	Configure Class IT Amplifier	Reserved	000	
		ADPT PWR	111	Output Signal determines voltage level
		HV_EN	1	High Voltage Mode Enabled
		EXT_VCPFILT	0	Using Internal VCPFILT source.
27	Set HP output to full scale	HP Output Control 1. 0x80000	0x30	
			0	
		OUT ES	11	Set headphone output to Full Scale (1 732 V rms)
		HP_IN_EN	0	
		Reserved	000	
28	Configure Headphone Detect	HP Detect. 0xD0000	0x04	
			00	HP Detect disabled
		HPDETECT_INV HPDETECT_RISE_DBC_TIME	00	Tip Sense rising debounce time set to 0ms
		HPDETECT_FALL_DBC_TIME	10	Tip sense falling debounce time set to 500ms
		Reserved	0	
29	Headphone Detect	HP Detect. 0xD0000	0xC4	
			11	HP Detect enabled
		HPDETECT RISE DBC TIME	00	Tip Sense rising debounce time set to 0ms
		HPDETECT_FALL_DBC_TIME	10	Tip sense falling debounce time set to 500ms
		Reserved	0	
30	Enable Interrupts			
31	Read Interrupt Status 1 registe	r (0xF0000) and Interrupt Status 5 register	(0xF0004) to cl	ear sticky bits
32	Enable Headphone Detect	Interrupt Mask 1. 0xF0010	0x81	
	Interrupts	DAC_OVFL_INT_MASK	1	Linmonk HDDETECT, DLUC interrupt and
			0	HPDETECT_PLOG Interrupt and HPDETECT_UNPLUG interrupt
		XTAL_READY_INT_MASK	Ō	
		ATAL ERROR INT MASK	0	
		PLL_READT_INT_MASK	0	
		PDN_DONE_INT_MASK	1	
33	Enable DSD Interrupts	Interrupt Mask 5. 0xF0014	0x03	
		DSD_STUCK_INT_MASK	0	Enable DSD_STUCK interrupt
		DSD_INVAL_A_INT_MASK	0	Enable DSD_INVAL_A interrupt
		DSD_INVAL_D_INT_IMASK	0	
		DSD_SILENCE_B_INT_MASK	Õ	Enable DSD_SILENCE_B interrupt
		DSD_RATE_ERROR_INT_MASK	0	Enable DSD_RATE_ERROR interrupt
		DOP_WIRK_DET_INT_WASK DOP ON INT MASK	1	Disable DOP_MIKK_DET Interrupt Disable DOP_ON interrupt
34	Wait for interrupt. Check if PLL	READY INT = 1 in Interrupt Status 1 regis	ster(0xF0000)	
35	Switch MCLK source to PLL	System Clocking Control 1. 0x10006	0x01	
		Reserved	0000 0	MCLK Source set to PLL. MCLK INT frequency set
		MCLK_INT	0	to 24.576 MHz
		MCLK_SRC_SEL	01	
36	Wait at least 150 µs			
37	Power up HP	Reter to Ex. 5-10 for DSD power-up sequ	uence. Skip Ste	p 1 of Ex. 5-10 (completed in Step 8 above).

#### Example 5-12. Startup to DSD Playback (Cont.)



# 5.10.3 Power-Up Sequence to DoP Playback with PLL

In Ex. 5-13, an external 19.2-MHz MCLK is used with a PLL to generate an internal MCLK or 22.5792 MHz, and the ASP is in clock master receiving DoP data with LRCLK at 176.4 kHz and SCLK at 8.4672 MHz.

#### Example 5-13. DoP Playback with PLL

STEE	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Apply all relevant power supplies then assert	RESET	VALUE	
2	Wait for 1.5 ms			
3	Apply DSD power-up initialization in Ex. 5-8			
4	Configure PLL. XTI/MCLK input coming from a settings for other frequency combinations	an external 19.2 MHz source with PLL	output set	t to 22.5792 MHz. Refer to Section 4.7.2 for register
5	Power up PLL	Power Down Control. 0x20000	0xFA	
		PDN_XSP	х	
		PDN_ASP PDN_DSDIF	x	
		PDN_HP	x	
			X O	Power un PLL block
		PDN_CLKOUT	x	
		Reserved	0	
6	Set PLL Predivide value	PLL Setting 9. 0x40002	0x03	
		Reserved PLL_REF_PREDIV	11	Set PLL predivide value to 8
7	Set PLL output divide	PLL Setting 6. 0x30008	0x08	
	Oct Freeding of DLL Divide Datio	PLL_OUT_DIV	0x08	Set PLL output divide value to 8
8	Set Fractional portion of PLL Divide Ratio	PLL Setting 2. 0x30002	0000	Oct I OD of DI I for ation of all initian values to 0
		PLL_DIV_FRAC_0	000	Set LSB of PLL fractional divider value to U
			000	Cat Middle Dute of DLL fractional divider value to 0
		PLL_DIV_FRAC_1	00x00	Set Middle Byte of PLL fractional divider value to 0
			000	Set MSR of PLL fractional divider value to 0x80
Q	Set Integer portion of PLL Divide Ratio	PLL_DIV_INAC_2	0x00	
5	bet meger portion of r EE Divide Ratio	PLL DIV INT	0x49	Set PLL integer Divide value to 0x49
10	Set PLL mode	PLL Setting 8. 0x3001B	0x01	
		Reserved PLL MODE	0000 00	) 500/512 factor is used in PLL frequency calculation
		Reserved	1	
11	Read Interrupt Status 1 register (0xF0000) to	clear sticky bits.		
12	Set PLL calibration ratio	PLL Setting 7. 0x3000A	0x97	
		PLL_CAL_RATIO	0x97	PLL Calibration Ratio is set to 0x97 (151)
13	Enable PLL interrupts	Interrupt Mask 1. 0xF0010	0xF9	
		DAC_OVEL_INT_MASK HPDETECT_PLUG_INT_MASK	1	DAC_OVFL_INT is don't care
		HPDETECT_UNPLUG_INT_MAS	кi	Unmask HPDETECT_UNPLUG interrupt
		XTAL_READY_INT_MASK	1	XTAL_READY_INT is Don't Care
		PLL READY INT MASK	0	PLL READY Interrupt is already unmasked
		PLL_ERROR_INT_MASK	0	PLL_ERROR Interrupt is already unmasked
14	Start PLI	PUL Setting 1 0x30001	0x01	PDN_DONE_INT is Don't Care
17	Otarriel	Reserved	0000 00	0
		PLL_START	1	Enable PLL Output
15	Playback DoP audio. Assuming 64•Fs DSD s	tream		
16	Configure ASP interface for DoP input			
17	Set ASP sample rate	Serial Port Sample Rate. 0x1000B	0x05	
		RESERVED	0000	Set sample rate to 176.4 kHz
18	Set ASP sample bit size XSP is don't care	Serial Port Sample Bit Size 0x1000	C 0x05	
		Reserved	0000	
		XSP_SPSIZE	01	XSP sample bit size set to 24 bits
		ASP_SPSIZE	01	ASP sample bit size set to 24 bits



#### STEP TASK **REGISTER/BIT FIELDS** VALUE DESCRIPTION 19 Set ASP numerator ASP Numerator 1. 0x40010 0x03 ASP\_N\_LSB 0x03 LSB of ASP sample rate fractional divide numerator ASP Numerator 2. 0x40011 0x00 0x00 ASP\_N\_MSB MSB of ASP sample rate fractional divide numerator 20 Set ASP denominator ASP Denominator 1. 0x40012 0x08 ASP\_M\_LSB 0x08 LSB of ASP sample rate fractional divide denominator ASP Denominator 2. 0x40013 0x00 ASP M MSB MSB of ASP sample rate fractional divide 0x00 denominator 21 Set ASP LRCK high time ASP LRCK High Time 1. 0x40014 0x17 ASP\_LCHI\_LSB LSB of ASP LRCK high time duration 0x17 ASP LRCK High Time 2. 0x40015 0x00 ASP LCHI MSB 0x00 MSB of ASP LRCK high time duration 22 Set ASP LRCK period ASP LRCK Period 1. 0x40016 0x2F ASP LCPR LSB 0x2F LSB of ASP LRCK period ASP LRCK Period 2. 0x40017 0x00 0x00 ASP\_LCPR\_MSB MSB of ASP LRCK period 23 Configure ASP clock ASP Clock Configuration. 0x40018 0x1C Reserved ASP\_M/SB ASP\_SCPOL\_OUT ASP\_SCPOL\_IN ASP\_LCPOL\_OUT 000 Set ASP port to be Master 1 Set output SCLK polarity 1 1 Input SCLK polarity is don't care 0 Set Output LRCK polarity ASP<sup>L</sup>CPOL<sup>IN</sup> 0 Input LRCK polarity is don't care 24 Configure ASP frame ASP Frame Configuration. 0x40019 0x0A 000 Reserved ASP\_STP ASP\_5050 0 1 Configure ASP port to accept I2S input ASP\_FSD 010 25 Set ASP channel location ASP Channel 1 Location. 0x50000 0x00 ASP RX CH1 0x00 ASP Channel 1 starts on SCLK0 ASP Channel 2 Location. 0x50001 0x00 ASP\_RX\_CH2 0x00 ASP Channel 2 starts on SCLK0 ASP Channel 1 Size and Enable. 26 Set ASP channel size and enable 0x06 0x5000A Reserved ASP\_RX\_CH1\_AP ASP\_RX\_CH1\_EN ASP\_RX\_CH1\_RES 0000 ASP Channel 1 active phase 0 ASP Channel 1 enable 1 ASP Channel 1 size is 24 bits 10 ASP Channel 2 Size and Enable. 0x0E 0x5000B Reserved 0000 ASP\_RX\_CH2\_AP ASP\_RX\_CH2\_EN ASP\_RX\_CH2\_RES ASP Channel 2 active phase 1 1 ASP Channel 2 enable ASP Channel 2 size is 24 bits 10 27 Wait for interrupt. Check if PLL READY INT = 1 in Interrupt Status 1 register(0xF0000). 28 Configure DSD processor 29 Configure DSD volume DSD Volume A. 0x70001 0x00 DSD\_VOLUME\_A 0x00 Channel A volume set to 0 dB 30 Configure DSD Path Signal Control 1 DSD Processor Path Signal Control 1. 0xEC 0x70002 Reserved 1 DSD\_VOL\_BEQA DSD\_SZC DSD Volume B equals DSD volume A 1 Soft ramp control enabled 1 Ò Reserved Mute occurs after 256 repeated 8-bit DSD mute DSD AMUTE 1 patterns Mute happens only when mute pattern is detected DSD AMUTE BEQA 1 in both channels DSD MUTE A Function is disabled 0

DSD\_MUTE\_B

Õ

Function is disabled

#### Example 5-13. DoP Playback with PLL (Cont.)



### Example 5-13. DoP Playback with PLL (Cont.)

STEP TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
31 Configure DSD interface	DSD Interface Configuration.	0x04	
C C	0x70003		
	Posonyod	0000 0	
		10000	DSD is clock master
		ů.	Function is disabled
		0	Function is disabled
	DSD_PM_SEL	U	Function is disabled
32 Configure DSD Path Signal Control 2	DSD Processor Path Signal Control 2.	0x50	
	0x70004		
	Reserved	0	
	DSD PRC SRC	10	Set source of DSD processor to ASP
		1	Enable DSD playback
	Beserved	Ó	
		ñ	Set DSD clock speed to 64.Es
		ñ	Static DSD detection disabled
		ň	Invalid DSD detection disabled
00. Or a firmer DOD a atta Oirar al Or a tarl 0		000	
33 Configure DSD path Signal Control 3	DSD Processor Path Signal Control 3.	UXCO	
	0x70006		
	DSD ZERODB	1	The SACD 0–dB reference level (50%modulation
			index) matches PCM 0-dB full scale.
	DSD HPF EN	1	Enable HPF in DSD processor
	Reserved	0	
	SIGCTL DSDEOPCM	õ	Function is disabled
	DSD INV A	õ	Function is disabled
	DSD_INV_B	Õ	Function is disabled
	DSD SWAP CHAN	õ	Function is disabled
	DSD_COPY_CHAN	õ	Function is disabled
24 Configure boodshane outsut for 4 700 1/		•	
34 Configure neadphone output for 1.732 V rms			
35 Configure Class H amplifier	Class H Control. 0xB0000	0x1E	
	Reserved	000	
	ADPT PWR	1 11	Output signal determines voltage level
	HV FN	1	High voltage mode enabled
		ó	Using internal VCPFILT source
			Cong internal Vol 1 IE1 Source.
36 Set HP output to full scale	HP Output Control 1. 0x80000	0x30	
	HP CLAMPA	0	
	HP <sup>-</sup> CLAMPB	0	
	OUT FS	11	Set headphone output to full scale (1.732 V rms)
	HP IN EN	0	
	Reserved	000	
37 Headphone detect	HP Detect 0xD0000	0×C4	
57 Treadphone delect		0104	
	HPDETECT_CTRL	11	HP detect enabled
	HPDETECT_INV	0	HP detect input is not inverted
	HPDETECT_RISE_DBC_TIME	00	Tip Sense rising debounce time set to 0 ms
	HPDETECT_FALL_DBC_TIME	10	Tip sense falling debounce time set to 500 ms
	Reserved	0	
38 Enable interrupts			
39 Read Interrupt Status 1 register (0xE0000) In	terrupt Status 2 register (0xE0001) and	Interrunt	Status 5 register (0xE0004) to clear sticky bits
40. Enable beedshane detect interrunte	Interrupt Maak 1, 0xE0010	0,000	
40 Enable headphone delect interrupts	Interrupt Mask 1. 0xF0010	0,039	
	DAC_OVFL_INT_MASK	1	DAC_OVFL_INT is don't care
	HPDETECT_PLUG_INT_MASK	0	Enable HPDETECT_PLUG interrupt
	HPDETECT_UNPLUG_INT_MASK	0	Enable HPDETECT_UNPLUG interrupt
	XTAL_READY_INT_MASK	1	XTAL_READY_INT is don't care
	XTAL_ERROR_INT_MASK	1	XTAL_ERROR_INT is don't care
	PLL_READY_INT_MASK	0	PLL_READY interrupt already enabled
	PLL_ERROR_INT_MASK	0	PLL_ERROR interrupt already enabled
	PDN_DONE_INT_MASK	1	PDN_DONE_INT is don't care
41 Enable ASP interrupts	Interrupt Mask 2 0xF0011	0x07	
		0	Frankla ACD OVEL interrest
	ASP_UVFL_INI_MASK	Ŭ	
	ASP_EKKUK_INI_MASK	Ŭ	
	ASP_LATE_INT_MASK	Ŭ	
	ASP_EAKLY_INT_MASK	Ŭ	
	ASP_NULKUK_INT_MASK	0	Enable ASP_NULKUK Interrupt
	Reserved	111	
42 Enable DSD and DoP interrupts	Interrupt Mask 5. 0xF0014	0x01	
	DSD STUCK INT MASK	0	Enable DSD STUCK interrupt
	DSD INVAL A INT MASK	õ	Enable DSD INVAL A interrupt
	DSD INVAL B INT MASK	Õ	Enable DSD_INVAL_B interrupt
	DSD SILENCE A INT MASK	õ	Enable DSD_SILENCF A interrupt
	DSD_SILENCE_B_INT_MASK	õ	Enable DSD_SILENCE_R interrupt
	DSD RATE ERROR INT MASK	ñ	Enable DSD_BATE_ERROR interrupt
	DOP MRK DET INT MACK	ň	Enable DOP_MRK_DET interrupt
	DOP ON INT MASK	1	Disable DOP ON interrupt
		1	Disable DOF_ON Interrupt
43 Wait for interrupt. Check if PLL READY INT:	= 1 in Interrupt Status 1 register(0xF000	)0).	



#### Example 5-13. DoP Playback with PLL (Cont.)

STEF	D TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
44	Set MCLK source and frequency	System Clocking Control. 0x10006	0x05	
		Reserved MCLK_INT MCLK_SRC_SEL	0000 0 1 01	MCLK Frequency is set to 22.5792 MHz MCLK Source is set to PLL
45	Wait for at least 150 µs.			
46	Enable ASP clocks	Pad Interface Configuration. 0x1000E	) 0x02	
		Reserved XSP_3ST ASP_3ST	0000 00 1 0	XSP Interface status is don't care (set to default) Enable serial clocks in Master Mode
47	Power up HP	Refer to Ex. 5-10 for DSD power-up s ASP interface. Skip Step 1 of Ex. 5-1	equence. 0 (comple	Note that in Step 2 of Ex. 5-10, HH = BF for DoP on eted in Step 3 above).

## 5.10.4 Analog-In Startup

Ex. 5-14 shows an example sequence of starting up the CS43130 in analog passthrough mode.

#### Example 5-14. Start Up to Analog-In

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION	
1	Apply all relevant power supplies, then assert RESET.				
2	Wait for 1.5 ms. MCLK Source is set to RCO by default.				
3	Enable Headphone detect. See Section 5.10.8 "Headphone Detection"				
4	Enable HPINx path. See See Section 5.6.1 "HPINx Alternate Headphone Path Enable Sequence"				

# 5.10.5 Switching from Analog-In to PCM Playback

Ex. 5-15 assumes that:

- The CS43130 is powered up, out of reset, and is currently operating in analog passthrough mode as in Ex. 5-14.
- The ASP and PCM interfaces are not yet configured.
- CS43130 XTI/XTO is connected to a 22.5792-MHz crystal.
- ASP interface is slave.

#### Example 5-15. Switching from Analog-In to PCM Playback

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Configure XTAL driver.			
2	Configure XTAL bias current	Crystal Setting, 0x20052	0x04	
	strength (assuming River Crystal	Reserved	0000 0	
	at 22.5792 MHz)	XTAL_IBIAS	100	Bias current set to 12.5 µA
3	Read Interrupt Status 1 register	(0xF0000) to clear sticky bits.		
4	Enable XTAL interrupts	Interrupt Mask 1. 0xF0010	data(0xF0010) AND 0xE7	
		DAC_OVFL_INT_MASK HPDETECT_PLUG_INT_MASK HPDETECT_UNPLUG_INT_MASK XTAL_READY_INT_MASK XTAL_ERROR_INT_MASK PLL_READY_INT_MASK PLL_ERROR_INT_MASK PDN_DONE_INT_MASK	x x 0 0 x x x x	Enable XTAL_READY interrupt Enable XTAL_ERROR interrupt
5	Start XTAL	Power Down Control. 0x20000	data (0x20000) AND 0xF6	
		PDN_XSP PDN_ASP PDN_DSDIF PDN_HP PDN_XTAL PDN_PLL PDN_CLKOUT Reserved	x x x 0 x x x 0	Power up XTAL driver
6	Apply PCM power-up initializatio	n. Refer to Ex. 5-7		
7	Configure ASP interface. Sample	e rate set to 44.1 kHz. ASP is slave to in	coming clock.	
8	Set ASP sample rate	Serial Port Sample Rate. 0x1000B	0x01	
		Reserved ASP_SPRATE	0000 0001	Set sample rate to 44.1 kHz


## Example 5-15. Switching from Analog-In to PCM Playback (Cont.)

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
9	don't care		0000	
		XSP SPSIZE	0000	XSP sample bit size is don't care
		ASP_SPSIZE	00	ASP sample bit size set to 32 bits
10	Set ASP numerator	ASP Numerator 1. 0x40010	0x01	
		ASP_N_LSB	0x01	LSB of ASP sample rate fractional divide numerator
		ASP Numerator 2. 0x40011	0x00	
		ASP_N_MSB	0x00	MSB of ASP sample rate fractional divide numerator
11	Set ASP denominator	ASP Denominator 1. 0x40012	0x08	
		ASP_M_LSB	0x08	LSB of ASP sample rate fractional divide denominator
		ASP Denominator 2. 0x40013	0x00	
		ASP_M_MSB	0x00	MSB of ASP sample rate fractional divide denominator
12	Set ASP LRCK high time	ASP LRCK High Time 1. 0x40014	0x1F	
		ASP_LCHI_LSB	0x1F	LSB of ASP LRCK high time duration
		ASP LRCK High Time 2. 0x40015	0x00	
		ASP_LCHI_MSB	0x00	MSB of ASP LRCK high time duration
13	Set ASP LRCK period	ASP LRCK Period 1. 0x40016	0x3F	-
		ASP LCPR LSB	0x3F	LSB of ASP LRCK period
		ASP LRCK Period 2. 0x40017	0x00	
		ASP LCPR MSB	0x00	MSB of ASP LRCK period
14	Configure ASP clock	ASP Clock Configuration. 0x40018	0x0C	•
	J.	Reserved	000	
		ASP_M/SB	0	Set ASP port to be Slave
		ASP_SCPOL_OUT	1	Configure clock polarity for I2S input
		ASP LCPOL OUT	ò	
		ASP_LCPOL_IN	0	
15	Configure ASP frame	ASP Frame Configuration. 0x40019	0x0A	
		Reserved	000	Configure ASP port to accept I <sup>2</sup> S input
		ASP_STP ASP_5050	0	
		ASP_FSD	010	
16	Set ASP channel location	ASP Channel 1 Location. 0x50000	0x00	
		ASP_RX_CH1	0x00	ASP Channel 1 starts on SCLK0
		ASP Channel 2 Location. 0x50001	0x00	
		ASP_RX_CH2	0x00	ASP Channel 2 starts on SCLK0
17	Set ASP channel size and ena	bleASP Channel 1 Size and Enable.	0x07	
		0x5000A		
			0000	ASD Channel 1 active phase
		ASP_RX_CH1_AP ASP_RX_CH1_EN	1	ASP Channel 1 enable
		ASP_RX_CH1_RES	11	ASP Channel 1 size is 32 bits
		ASP Channel 2 Size and Enable.	0x0F	
		Beeenved	0000	
		ASP RX CH2 AP	1	ASP Channel 2 active phase
		ASP_RX_CH2_EN	1	ASP Channel 2 enable
		ASP_RX_CH2_RES	11	ASP Channel 2 size is 32 bits
18	Configure PCM interface. HP	filter is used. Deemphasis off.		
19	Configure PCM Filter	PCM Filter Option. 0x90000	0x02	
		FILTER SLOW FASTB	0	High Pass Filter is selected
		NOS	0	
		Reserved	0 00	
		HIGH_PASS DEEMP_ON	1 0	
20	Set Volume for Channel B		0v00	
20			0x00	Set volume to 0 dB
21	Set Volume for Channel A	PCM Volume A 0x90002	0x00	
21			0v00	Set volume to 0 dB
			0,00	



## Example 5-15. Switching from Analog-In to PCM Playback (Cont.)

OTED	TAOK		N / =	D=
22	IASK Configure PCM Path Signal	REGISTER/BIT FIELDS PCM Path Signal Control 1 0x90003		DESCRIPTION
22	Control	PCM_RAMP_DOWN PCM_VOL_BEQA	1	Soft ramp down of volume on filter change
				VOLUME_A
		PCM_SZC PCM_AMUTE	10 1	Enable soft ramp
		PCM_AMUTEBEQA	1	Mute only when AMUTE condition is detected on both channels
		PCM_MUTE_A PCM_MUTE_B	0 0	Function is disabled Function is disabled
		PCM Path Signal Control 2. 0x90004	0x00	
		Reserved	0000	Disable all functions in this register
		PCM_INV_A PCM_INV_B	0	
		PCM_SWAP_CHAN	0	
		PCM_COPY_CHAN	0	
23	Configure HP Interface	Close II Control Ov B0000	0.45	
24	Configure Class H Amplifier	Class H Control. 0xB0000	000	
		ADPT PWR	1 11	Output signal determines voltage level
			1	High voltage mode enabled
- 05	Headahana Data d		0	Using Internal VCPFILT source.
25	Headphone Detect		0xC4	
		HPDETECT_CTRL HPDETECT_INV	0	HP detect input is not inverted
		HPDETECT_RISE_DBC_TIME	0 0	Tip Sense rising debounce time set to 0 ms
		HPDETECT_FALL_DBC_TIME	10	Tip sense falling debounce time set to 500 ms
26	Enable interrupts	Reserved	0	
27	Read Interrupt Status 1 register	(0xE0000) and Interrupt Status 2 register	er (0xF0001) to	clear sticky bits
28	Enable headphone detect	Interrupt Mask 1. 0xF0010	data(0xF0010	)
	interrupts		AND 0x9F	,
		DAC_OVFL_INT_MASK	x	
		HPDETECT_PLUG_INT_MASK HPDETECT_UNPLUG_INT_MASK	0	Enable HPDETECT_UNPLUG Interrupt
		XTAL_READY_INT_MASK	x	
		NTAL ERROR INT MASK	x	
		PLL ERROR INT MASK	x	
		PDN_DONE_INT_MASK	х	
29	Enable ASP interrupts	Interrupt Mask 2. 0xF0011	0x07	
		ASP_OVFL_INT_MASK	0	Enable ASP_OVFL interrupt
		ASP LATE INT MASK	0	Enable ASP_LATE interrupt
		ASP_EARLY_INT_MASK	0	Enable ASP_EARLY interrupt
		ASP_NOLRCK_INT_MASK Reserved	0 111	Enable ASP_NOLRCK Interrupt
30	Initiate a soft ramp down of HP	INx input to mute.		
31	Disable HPINx	Refer to Section 5.6.2		
32	Wait for interrupt. Check if XTA	L_READY_INT = 1 in Interrupt Status 1 r	egister(0xF000	0).
33	Switch MCLK source to XTAL	System Clocking Control 1. 0x10006	0x04	
	OWIGH MOLK SOURCE TO KIAL	, , , , , , , , , , , , , , , , , , , ,		
	Owner molek source to XTAL	Reserved	0 0000	
		Reserved MCLK_INT MCLK_SRC_SEL	0000 0 1 00	MCLK Source set to XTAL. MCLK_INT frequency set
34	Wait at least 150 us	Reserved MCLK_INT MCLK_SRC_SEL	0000 0 1 00	MCLK Source set to XTAL. MCLK_INT frequency set to 22.5792MHz
34	Wait at least 150 µs.	Reserved MCLK_INT MCLK_SRC_SEL Refer to Ex. 5-9 for PCM power-up sec	0000 0 1 00	MCLK Source set to XTAL. MCLK_INT frequency set to 22.5792MHz



## 5.10.6 Switching from PCM to Analog-In Playback

Ex. 5-16 makes the following assumptions:

- The CS43130 is powered up, out of reset, and currently operating in PCM playback mode.
- A headphone is connected to the headphone jack.
- Headphone detect is enabled and HPDETECT\_PLUG\_INT = 1.
- XTAL is used as MCLK source.

#### Example 5-16. Switching from PCM to Analog-In Playback

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Enable soft ramp	PCM Path Signal Control 1. 0x90003	data(0x90003) OR (0xA0)	
		PCM_RAMP_DOWN PCM_VOL_BEQA PCM_SZC PCM_AMUTE PCM_AMUTEBEQA PCM_MUTE_A PCM_MUTE_B	1 x 10 x x 0 0	Enable soft ramp
2	PCM Power Down Sequence	Refer to Section 5.7.1		
3	Set MCLK Source to RCO	System Clocking Control 1. 0x10006	0x06	
		Reserved MCLK_INT MCLK_SRC_SEL	0000 0 1 10	Frequency of MCLK_INT is don't care MCLK source set to RCO
4	Wait for 150 µs.			
5	Power down crystal	Power Down Control. 0x20000	data (0x20000) OR (0x08)	
		PDN_XSP PDN_ASP PDN_DSDIF PDN_HP PDN_XTAL PDN_PLL PDN_CLKOUT Reserved	x 1 x 1 x x x 0	ASP already powered down HP already powered down Power down XTAL.
6	Enable HPINx	Refer to Section 5.6.1		



## 5.10.7 Switching MCLK Frequency

Ex. 5-17 shows steps necessary to switch the MCLK frequency in order to play audio at a different sample rate that is no longer an integer divide of current MCLK. It makes the following assumptions:

- The CS43130 is already powered up and out of reset.
- MCLK is sourced directly from external clock input (Direct MCLK). MCLK\_INT is 22.5792 MHz, and the sample rate is an integer divide of MCLK.
- ASP is used for audio delivery and PDN\_HP = 0.

#### Example 5-17. Sequence for Switching MCLK Frequency

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Power down PCM Refer to Ex. 5-5 for PCM power-down sequence			
2	Switch MCLK Source to RCO			
3	Set MCLK Source to RCO	System Clocking Control 1. 0x10006	0x06	
		Reserved MCLK_INT MCLK_SRC_SEL	0000 0 1 10	Frequency of MCLK_INT is don't care MCLK source set to RCO
4	Wait for 150 µs			
5	Switch to a different MCLK Frequency. A	ssuming new MCLK frequency is 24.576M	/Hz.	
6	Change MCLK_INT frequency to	System Clocking Control 1. 0x10006	0x02	
	24.576 MHz	Reserved MCLK_INT MCLK_SRC_SEL	0000 0 0 10	MCLK_INT frequency set to 24.576 MHz
7	Apply PCM power-up initialization in Ex.	5-7		
8	8 Configure ASP for appropriate sample rate, bit size and clock mode. Unmute PCM CHA and CHB outputs. Enable appropriate interrupts			
9	Switch MCLK source to direct MCLK mod	de System Clocking Control 1. 0x10006	0x0	
		Reserved MCLK_INT MCLK_SRC_SEL	0000 0 0 00	MCLK_INT frequency set to 24.576 MHz MCLK source set to direct MCLK mode
10	Wait at least 150 µs.			
11	Power up HP	Refer to Ex. 5-9 for PCM power-up seq	uence. Skip	Step 1 of Ex. 5-9 (completed in Step 7 above).

### 5.10.8 Headphone Detection

Ex. 5-18 shows steps necessary to detect the presence of a headphone. It makes the following assumptions:

- The CS43130 is already powered up and out of reset.
- The HP Detect register is not configured.

#### Example 5-18. Sequence for Headphone Detection

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Read Interrupt Status 1 register (0xF000	0) to clear any sticky bits.		
2	Read HP Status register (0xD0001) to c	lear any sticky bits.		
3	Enable HPDETECT interrupts	Interrupt Mask 1. 0xF0010	data (0xF0010) AND 0x9F	
		DAC_OVFL_INT_MASK HPDETECT_PLUG_INT_MASK HPDETECT_UNPLUG_INT_MASK XTAL_READY_INT_MASK XTAL_ERROR_INT_MASK PLL_READY_INT_MASK PLL_READY_INT_MASK	x 0 0 x x x	Enable HPDETECT interrupts
		PDN_DONE_INT_MASK	x x	
4	Configure HP Detect parameters	HP Detect. 0xD0000	0x04	
		HPDETECT_CTRL HPDETECT_INV HPDETECT_RISE_DBC_TIME HPDETECT_FALL_DBC_TIME Reserved	00 0 0 0 10 0	Rising edge debounce time set to 0 ms Falling edge debounce time set to 500 ms
5	Enable HP Detect	HP Detect. 0xD0000	data (0xD0000) OR (0xC0)	
		HPDETECT_CTRL HPDETECT_INV HPDETECT_RISE_DBC_TIME HPDETECT_FALL_DBC_TIME Reserved	11 x x x xx 0	Enable headphone detection



#### Example 5-18. Sequence for Headphone Detection (Cont.)

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
6	Wait for interrupt. Check if HPDETECT_F	PLUG_INT or HPDETECT_UNPLUG_	INT is set in the Inter	rupt Status 1 register (0xF0000).

## 5.10.9 DoP and PCM Mixing

Ex. 5-19 shows steps necessary to mix DoP and PCM. The XSP is in clock master receiving DoP data with LRCLK at 176.4 kHz and SCLK at 8.4672 MHz. The ASP is clock master receiving PCM data with LRCLK at 44.1 kHz and SCLK at 2.8224 MHz.

#### Example 5-19. DoP and PCM Mixing

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION	
1	Apply all relevant power supp	blies, then assert RESET.			
2	Wait for 1.5 ms				
3	Configure XTAL Driver				
4	Configure XTAL bias current	Crystal Setting. 0x20052	0x04		
	strength (assuming River Crystal at 22.5792 MHz)	Reserved XTAL_IBIAS	0000 0 100	Bias current set to 12.5 µA	
5	Enable XTAL interrupts	Interrupt Mask 1. 0xF0010	0xE7		
		DAC_OVFL_INT_MASK HPDETECT_PLUG_INT_MASK HPDETECT_UNPLUG_INT_MASK XTAL_READY_INT_MASK XTAL_ERROR_INT_MASK PLL_READY_INT_MASK PLL_ERROR_INT_MASK PDN_DONE_INT_MASK	1 1 0 1 1 1	Enable XTAL_READY interrupt Enable XTAL_ERROR interrupt	
6	Start XTAL	Power Down Control. 0x20000	0xF6		
	Angly DCD generation in Westing	PDN_XSP PDN_XSP PDN_DSDIF PDN_HP PDN_XTAL PDN_PLL PDN_CLKOUT Reserved	1 1 1 0 1 0	Power up XTAL driver	
	7 Apply DSD power-up initialization in Ex. 5-6				
8	8 Playback DoP audio. Assuming 64•Fs DSD stream				
9	Configure XSP interface for L	JoP input.			
10	Set sample bit size.	Serial Port Sample Bit Size. 0x1000C	0x05		
		Reserved XSP_SPSIZE ASP_SPSIZE	0000 01 01	XSP sample bit size is set to 24 bits ASP sample bit size is set to 24 bits	
11	Set XSP Numerator	XSP Numerator 1. 0x40020	0x03		
		XSP_N_LSB	0x03	LSB of XSP sample rate fractional divide numerator	
		XSP Numerator 2. 0x40021	0x00		
		XSP_N_MSB	0x00	MSB of XSP sample rate fractional divide numerator	
12	Set XSP Denominator	XSP Denominator 1. 0x40022	0x08		
		XSP_M_LSB	0x08	LSB of XSP sample rate fractional divide denominator	
		XSP Denominator 2. 0x40023	0x00		
		XSP_M_MSB	0x00	MSB of XSP sample rate fractional divide denominator	
13	Set XSP LRCK high Time	XSP LRCK High Time 1. 0x40024	0x17		
		XSP_LCHI_LSB	0x17	LSB of XSP LRCK high time duration	
		XSP LRCK High Time 2. 0x40025	0x00		
		XSP_LCHI_MSB	0x00	MSB of XSP LRCK high time duration	
14	Set XSP LRCK period	XSP LRCK Period 1. 0x40026	0x2F		
		XSP_LCPR_LSB	0x2F	LSB of XSP LRCK period	
		XSP LRCK Period 2. 0x40027	0x00		
		XSP_LCPR_MSB	0x00	MSB of XSP LRCK period	
15	Configure XSP Clock	XSP Clock Configuration. 0x40028	0x1C		
		Reserved XSP_M/SB XSP_SCPOL_OUT XSP_SCPOL_IN XSP_LCPOL_OUT XSP_LCPOL_IN	000 1 1 0 0	Set XSP port to be Master Set output SCLK polarity Input SCLK polarity is don't care Set Output LRCLK polarity Input LRCLK polarity is don't care	



				-
STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
10	Conligure ASP Frame	ASP Frame Comiguration. 0x40029	000	
		XSP STP	000	Configure XSP port to accept I <sup>2</sup> S input
		XSP_5050	Ĩ	
		XSP_FSD	010	
17	Set XSP Channel Location	XSP Channel 1 Location. 0x60000	0x00	
		XSP_RX_CH1	0x00	XSP Channel 1 starts on SCLK0
		XSP Channel 2 Location. 0x60001	0x00	
		XSP_RX_CH2	0x00	XSP Channel 2 starts on SCLK0
18	Set XSP Channel Size and	XSP Channel 1 Size and Enable.	0x06	
	LIADIE	Besonved	0000	
		XSP RX CH1 AP	0000	XSP Channel 1 Active Phase
		XSP_RX_CH1_EN	1	XSP Channel 1 Enable
		XSP_RX_CH1_RES	10	XSP Channel 1 Size is 24 bits
		XSP Channel 2 Size and Enable. 0x6000B	0x0E	
		Reserved	0000	VCD Channel 2 Active Phase
		XSP_RX_CH2_AP XSP_RX_CH2_FN	1	XSP Channel 2 Active Phase XSP Channel 2 Enable
		XSP_RX_CH2_RES	10	XSP Channel 2 Size is 24 bits
19	Configure DSD Processor			
20	Configure DSD Volume	DSD Volume A. 0x70001	0x00	
		DSD_VOLUME_A	0x00	Channel A volume set to 0 dB
21	Configure DSD path Signal Control 1	DSD Processor Path Signal Control 1. 0x70002	0xEC	
		Reserved	1	
		DSD_VOL_BEQA	1	DSD Volume B equals DSD volume A
		DSD_SZC Boson/od	1	Soft ramp control enabled
		DSD AMUTE	1	Mute occurs after 256 repeated 8-bit DSD mute patterns
		DSD_AMUTE_BEQA	1	Mute happens only when mute pattern is detected in both
		DSD_MUTE_A DSD_MUTE_B	0	channels Function is disabled
			0	Function is disabled
22	Configure DSD Interface	DSD Interface Configuration.	0x00	
		0x70003		
		Reserved	00000	DSD M/SB is don't care
		DSD_PM_EN	ŏ	Function is disabled
		DSD_PM_SEL	0	Function is disabled
23	Configure DSD path Signal	DSD Processor Path Signal Control 2.	0x70	
	Control 2	Reserved	0	
		DSD_PRC_SRC	11	Set source of DSD processor to XSP
		DSD_EN	1	Enable DSD playback
		Reserved DSD_SPEED	0	Set DSD clock speed to 64•ES
		STA_DSD_DET	ŏ	Static DSD detection disabled
		INV_DSD_DET	0	Invalid DSD detection disabled
24	Configure DSD path Signal Control 3	DSD Processor Path Signal Control 3. 0x70006	0xC0	
		DSD_ZERODB	1	DSD stream volume setting
		DSD_HPF_EN Reserved	0	Enable DSD HPF
		SIGCTL_DSDEQPCM	õ	Function is disabled
			0	Function is disabled
		DSD_INV_B DSD_SWAP_CHAN	0	Function is disabled
		DSD_COPY_CHAN	Õ	Function is disabled
25	Configure HP Output for 1.73	32 Vrms		
26	Configure Class H	Class H Control. 0xB0000	0x1E	
	Amplitter	Reserved	000	
		ADMI MWK HV FN	111 1	Output Signal determines voltage level High Voltage Mode enabled
		EXT_VCPFILT	Ó	Using Internal VCPFILT source.
27	Set HP output to full	HP Output Control 1. 0x80000	0x30	
	scale	Reserved	00	Set HP output to Full Scale (1.732 Vrms)
		UUI_FS Reserved	11 0000	
		I COCIVEU	0000	



	•			
STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
28	Headphone Detect	HP Detect. 0xD0000	0xC4	
		HPDETECT_CTRL	11	HP Detect enabled
			0	HP detect input is not inverted
		HPDETECT_FALL_DBC_TIME	10	Tip sense falling debounce time set to 500 ms
		Reserved	0	
29	Enable Interrupts			
30	Read Interrupt Status 1 regis	ster (0xF0000). Interrupt Status 2 registe	er (0xF00	01) and Interrupt Status 5 register (0xF0004) to clear sticky bits
31	Enable Headphone Detect	Interrupt Mask 1 0xE0010	0x99	
	Interrupts	DAC OVEL INT MASK	1	DAC_OVEL_INT is don't care
		HPDETECT_PLUG_INT_MASK	Ó	Unmask HPDETECT_PLUG interrupt
		HPDETECT_UNPLUG_INT_MASK	0	Unmask HPDETECT_UNPLUG interrupt
		XTAL_READY_INT_MASK	1	XTAL_READY_INT is don't care
		PLL READY INT MASK	ò	PLL READY Interrupt is already unmasked
		PLL_ERROR_INT_MASK	0	PLL_ERROR Interrupt is already unmasked
		PDN_DONE_INT_MASK	1	PDN_DONE_INT is don't care
32	Enable XSP Interrupts	Interrupt Mask 2. 0xF0011	0x07	
		XSP_OVFL_INT_MASK	0	Enable XSP_OVFL interrupt
		XSP_ERROR_INT_MASK	0	Enable XSP_ERROR Interrupt
		XSP EARLY INT MASK	Ő	Enable XSP EARLY interrupt
		XSP_NOLRCK_INT_MASK	0	Enable XSP_NOLRCK interrupt
		Reserved	111	
33	Enable DSD and DoP	Interrupt Mask 5. 0xF0014	0x01	
	interrupts	DSD_STUCK_INT_MASK	0	Enable DSD_STUCK interrupt
		DSD_INVAL_A_INT_MASK DSD_INVAL_B_INT_MASK	0	Enable DSD_INVAL_A Interrupt
		DSD_SILENCE A INT MASK	ŏ	Enable DSD_SILENCE A interrupt
		DSD_SILENCE_B_INT_MASK	0	Enable DSD_SILENCE_B interrupt
		DSD_RATE_ERROR_INT_MASK	0	Enable DSD_RATE_ERROR interrupt
		DOP_MIRK_DET_INT_MASK	1	Disable DOP_MRK_DET Interrupt
34	Set MCLK Source and	System Clocking Control 0x10006	0x04	
• •	Frequency	Reserved	0000 0	
		MCLK_INT	1	MCLK Frequency is set to 22.5792 MHz
		MCLK_SRC_SEL	00	MCLK Source is set to XTAL
35	Wait for at least 150 µs			
36	Enable XSP Clocks	Pad Interface Configuration. 0x1000D	0x01	
		Reserved	0000 00	ACD Interface status is den't same (act to default)
		ASP_3ST ASP_3ST	0	Finable XSP serial clocks in master mode
37	Apply DSD Power-up Seque	nce in Ex 5-10 Note that in Step 2 of Ex	5-10 HH	= 7E for DoP on XSP interface. Skip Step 1 of Ex. 5-10 (completed)
•••	in Step 7 above).		• • • • • • • • •	
38	Enable ASP			
39	Set ASP sample rate	Serial Port Sample Rate. 0x1000B	0x01	
		Reserved	0000	
		ASP_SPRATE	0001	Set sample rate to 44.1 kHz
40	Set ASP sample bit size	Serial Port Sample Bit Size. 0x1000C	0x04	
		Reserved	0000	
		ASP_SPSIZE ASP_SPSIZE	01	ASP sample hit size set to 32 hits
11	Sot ASP Numerator		0v01	
+1			0x01	I SP of ASP sample rate fractional divide numerator
		AGF_N_LOB	0x01	
			0000	MOD of AOD communicate for effort of divide momentum
- 40			0000	NIGE OF ASP sample rate fractional divide numerator
42	Set ASP Denominator	ASP Denominator 1. 0x40012	0x08	
		ASP_M_LSB	0x08	LSB of ASP sample rate fractional divide denominator
		ASP Denominator 2. 0x40013	0x00	
		ASP_M_MSB	0x00	MSB of ASP sample rate fractional divide denominator
43	Set ASP LRCK high Time	ASP LRCK High Time 1. 0x40014	0x1F	
		ASP_LCHI_LSB	0x1F	LSB of ASP LRCK high time duration
		ASP LRCK High Time 2. 0x40015	0x00	
		ASP_LCHI_MSB	0x00	MSB of ASP LRCK high time duration
44	Set ASP LRCK period	ASP LRCK Period 1. 0x40016	0x3F	
		ASP_LCPR_LSB	0x3F	LSB of ASP LRCK period
		ASP LRCK Period 2. 0x40017	0x00	
		ASP_LCPR_MSB	0x00	MSB of ASP LRCK period
				•



STEP 45	TASK Configure ASP Clock	REGISTER/BIT FIELDS ASP Clock Configuration 0x40018	VALUE	DESCRIPTION
40	Configure / Ch Clock	Reserved	000	
		ASP_M/SB	1	Set ASP port to be Master
		ASP_SCPOL_OUT ASP_SCPOL_IN	1	Set output SCLK polarity Input SCLK polarity is don't care
		ASP_LCPOL_OUT	Ó	Set Output LRCLK polarity
		ASP_LCPOL_IN	0	Input LRCLK polarity is don't care
46	Configure ASP Frame	ASP Frame Configuration. 0x40019	0x0A	
		ASP STP	000	Configure ASP port to accept I2S input
		ASP_5050	1	
		ASP_FSD	010	
47	Set ASP Channel	ASP Channel 1 Location. 0x50000	0x00	
	Loodion	ASP_RX_CH1	000	ASP Channel 1 starts on SCLKU
		ASP Channel 2 Location. 0x50001	000	ASD Channel 2 starte en SCLK0
10	Sat ASD Channel Size and	ASP_RA_CH2	0x00	ASP Channel 2 starts on SCLRU
40	Enable	0x5000A	0.07	
		ASP RX CH1 AP	0000	ASP Channel 1 Active Phase
		ASP_RX_CH1_EN	1	ASP Channel 1 Enable
		ASP_RX_CH1_RES	11	ASP Channel 1 Size is 32 bits
		ASP Channel 2 Size and Enable. 0x5000B	0x0F	
		Reserved	0000	ASD Channel 2 Active Phase
		ASP_RX_CH2_AP ASP_RX_CH2_EN	1	ASP Channel 2 Enable
		ASP_RX_CH2_RES	11	ASP Channel 2 Size is 32 bits
49	Setup PCM			
50	Configure PCM Filter	PCM Filter Option. 0x90000	0x02	
			0	High Pass Filter is selected
		NOS	Ő	
		Reserved	0 00	
		DEEMP ON	0	
51	Set Volume for Channel B	PCM Volume B. 0x90001	0x0C	
		PCM_VOLUME_B	0x0C	Set volume to –6 dB
52	Set Volume for Channel A	PCM Volume A. 0x90002	0x0C	
		PCM_VOLUME_A	0x0C	Set volume to –6 dB
53	Configure PCM Path Signal	PCM Path Signal Control 1. 0x90003	0xEC	
	Control	PCM_RAMP_DOWN	1	Soft ramp down of volume on filter change
		PCM_VOL_BEQA PCM_SZC	10	Enable soft ramp
		PCM_AMUTE	1	Mute after reception of 8192 samples of 0 or -1.
		PCM_AMUTEBEQA PCM_MUTE_A	1	Mute only when AMU I E condition is detected on both channels Function is disabled
		PCM_MUTE_B	Õ	Function is disabled
		PCM Path Signal Control 2. 0x90004	0x00	
		Reserved	0000	Disable all functions in this register
		PCM_INV_A PCM_INV_B	0	
		PCM_SWAP_CHAN	Õ	
		PCM_COPY_CHAN	0	
54	Read Interrupt status 2 register	Interrupt Status 2. 0xF0001		Clear Sticky Dits
55	Enable ASP Interrupts	Interrupt Mask 2. 0xF0011	0x07	
		ASP_OVFL_INT_MASK	0	Enable ASP_OVFL interrupt
		ASP_LATE_INT_MASK	Ő	Enable ASP_LATE interrupt
		ASP_EARLY_INT_MASK	0	Enable ASP_EARLY interrupt
		Reserved	111	Enable ASP_NULKUN IIIleitupi
56	Enable ASP Clocks	Pad Interface Configuration. 0x1000D	0x00	
		Reserved	0000 00	
		XSP_3ST	0	Enable ASP serial clocks
		ASK-321	U	



STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
57	Enable ASP	Power Down Control. 0x20000	0x24	
		PDN_XSP	0	
		PDN_ASP	0	Enable ASP
		PDN_DSDIF	1	
		PDN_HP	0	
		PDN_XTAL	0	
		PDN_PLL	1	
		PDN_CLKOUT	0	
		Reserved	0	
58	Enable PCM/DoP mix			
59	Configure DSD Volume	DSD Volume A. 0x70001	0x0C	
		DSD_VOLUME_A	0x0C	Channel A volume set to 0 dB
60	Prepare for PCM/DoP Mix operation	DSD and PCM Mixing Control. 0x70005	0x02	
		Reserved	0000 00	Enable PCM playback path for DoP Mixing
		MIX_PCM_PREP	1	
		MIX_PCM_DSD	0	
61	Wait for 6 ms			
62	Enable PCM/DoP mix	DSD and PCM Mixing Control. 0x70005	0x03	
		Reserved	0000 00	Enable PCM/DoP Mixing
		MIX_PCM_PREP	1	-
		MIX_PCM_DSD	1	



## 5.11 Headphone Load Measurement

The CS43130 can be configured to measure the impedance of headphone load. Please refer to Section 4.5.2 for a description of headphone load detection. Fig. 5-1 and the following subsections describe the steps needed to measure DC and AC impedance of the headphone.



Figure 5-1. AC and DC Impedance Measurement Flowchart



## 5.11.1 Enabling the Impedance Measurement Subsystem

Fig. 5-2 shows and Ex. 5-20 describes the steps necessary for enabling the impedance measurement subsystem.



Figure 5-2. Enabling the Impedance Measurement Subsystem Flowchart

Example 5-20.	Sequence for Ena	bling the Impedance	Measurement Subsystem
---------------	------------------	---------------------	-----------------------

STEF	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	If PDN_HP = 1, go to Step 3.			
2	Power down headphone output. See he	adphone power down sequence in Sectio	n 5.7, "Headphone	Power Down Sequences."
3	Measure headphone DC impedance			



#### Example 5-20. Sequence for Enabling the Impedance Measurement Subsystem (Cont.)

STE	P TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
4	Read Interrupt Status 4 register (0xF0	0003) to clear sticky bits.		
5	Enable HP Load Interrupts	Interrupt Mask 4. 0xF0013	0x20	
		HPLOAD_NO_DC_INT_MASK	0	Enable HPLOAD_NO_DC interrupt
		HPLOAD_UNPLUG_INT_MASK	0	Enable HPLOAD_UNPLUG interrupt
		Reserved	1	
		HPLOAD_OOR_INT_MASK	0	Enable HPLOAD_OOR interrupt
		HPLOAD_AC_DONE_INT_MASK	0	Enable HPLOAD_AC_DONE interrupt
		HPLOAD_DC_DONE_INT_MASK	0	Enable HPLOAD_DC_DONE interrupt
		HPLOAD_OFF_INT_MASK	0	Enable HPLOAD_OFF interrupt
		HPLOAD_ON_INT_MASK	0	Enable HPLOAD_ON interrupt
6	Enable calibration	0x10010	0x99	
		0x80024	0xBB	
		0x1002C	0x01	
		0x10026	0xCB	
		0x10027	0x95	
		0x10028	0x0B	
		0x10010	0x00	
7	Turn on impedance measurement	HP Load 1. 0xE0000	0x80	
	subsystem	HPLOAD EN	1	Enable impedance measurement subsystem
		Reserved	00	,
		HPLOAD CHN SEL	0	
		Reserved	00	
		HPLOAD AC START	0	
		HPLOAD_DC_START	0	
8	Wait for interrupt Check if HPLOAD	ON_INT = 1 in Interrupt Status 4 register (0x	F0003)	



## 5.11.2 Measuring DC Impedance

Fig. 5-3 shows and Ex. 5-21 describes the steps necessary for measuring DC impedance with the following assumptions:

- The CS43130 is already powered up and out of reset.
- MCLK\_INT is 22.5792 or 24.576 MHz sourced from MCLK/XTAL or PLL (MCLK\_SRC\_SEL = 00 or 01).
- HP\_IN\_EN = 0 and HPLOAD\_EN = 0.
- A headphone is already plugged in and HPDETECT\_PLUG\_INT = 1.



Figure 5-3. DC Impedance Measurement Flowchart



STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Enable impedance measurement subsyste	em. Refer to Ex. 5-20.		



STE				DESCRIPTION
2	Select Channel A	0x10010	0x99	DESCRIPTION
-		0x10026	0x0A	
		0x10027	0x93	
		0x10028	0x0A	
		0x10010	0x00	
		HP Load 1. 0xE0000	0x80	
		HPLOAD_EN	1	
			00	
		Reserved	ŏŏ	The OUTA selected
		HPLOAD_AC_START	0	
3	Enable DC impedance measurement	HPLOAD_DC_START	0v81	
0			1	
		Reserved	oo	
		HPLOAD_CHN_SEL	0	
		HPLOAD AC START	0	
		HPLOAD_DC_START	1	Start DC impedance measurement
4	Wait for interrupt. Read Interrupt Status HPLOAD_OOR_INT = 1, go to the last	4 register (0xF0003). If HPLOAD step as an error has occurred. Ot	_UNPLUG_INT = 1, go herwise, if HPLOAD_D	to the last step as an error has occurred. If C_DONE_INT = 1, go to the next step.
5	DC impedance values are available in H	IP DC Load Status 0 (0xE000D) a	and HP DC Load Status	s 1 (0xE000E) registers.
6	Disable DC impedance measurement	HP Load 1. 0xE0000	0x80	
		HPLOAD_EN Reserved	1	
		HPLOAD_CHN_SEL	0	
			00	
		HPLOAD_AC_START HPLOAD_DC_START	0	Stop DC impedance measurement
7	Select Channel B	 0x10010	0x99	
		0x10026	0x8A	
		0x10027	0x15	
		0x10028	0x06	
		0x10010	0x00	
		HP Load 1. 0xE0000	0x90	
		HPLOAD_EN	1	
		HPLOAD CHN SEL	1	HPOUTB selected
			00	
		HPLOAD_AC_START HPLOAD_DC_START	0	
8	Enable DC impedance measurement	HP Load 1. 0xE0000	0x91	
	·	HPLOAD_EN	1	
		Reserved	00	
		Reserved	00	HPOOTE selected
		HPLOAD_AC_START	0	Chart DC impedance manual
	Wait for interrupt Dood Interrupt Otaling	HPLUAD_DC_START		Start DC Impedance measurement
9	HPLOAD_OOR_INT = 1, go to the last	step as an error has occurred. Ot	herwise, if HPLOAD_D	C_DONE_INT = 1, go to the next step.
10	DC impedance values are available in F	IP DC Load Status 0 (0xE000D) a	and HP DC Load Status	s 1 (0xE000E) registers.
11	To measure AC impedance, go to Step	3 OT EX. 5-22.		

## Example 5-21. Sequence for DC Impedance Measurement (Cont.)

12 Disable impedance measurement subsystem. Refer to Ex. 5-23.



## 5.11.3 Measuring AC Impedance at 1 kHz

Fig. 5-4 shows and Ex. 5-22 describes the steps necessary to measure AC impedance at 1 kHz with the following assumptions:

 Continuing from Step 11 of Ex. 5-21 since DC impedance measurement is required to be run before AC impedance measurement.





#### Example 5-22. AC Impedance Measurement at 1 kHz

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION					
1	Enable impedance measurement subsy	stem. Refer to Ex. 5-20.							
2	Check if DC impedance was already measured. Read HP Load Status (0xE001A) and verify HPLOAD_DC_ONCE (bit 8) is set.								
3	Measure headphone AC impedance								
4	Select Channel A	0x10010	0x99						
		0x10026	0x0A						
		0x10027	0x93						
		0x10028	0x0A						
		0x10010	0x00						
		HP Load 1. 0xE0000	0x80						
		HPLOAD_EN Reserved HPLOAD_CHN_SEL Reserved HPLOAD_AC_START HPLOAD_DC_START	1 00 0 00 0 0	HPOUTA selected					



## Example 5-22. AC Impedance Measurement at 1 kHz (Cont.)

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
5	Set HP load measurement frequency to	HP Load Measurement 1. 0xE0003	0xA8	
	desired frequency. Assuming 1 kHz.	HPLOAD MEAS FREQ LSB	0xA8	Set measurement frequency = 1 kHz
		HP Load Measurement 2 0xF0004	0x00	
		HPLOAD MEAS FREO MSB	0x00	MSB of load measurement frequency
6	Enable AC impedance measurement	HP   oad 1_0xE0000	0x82	meb of load measurement nequency
0			1	
		Reserved	00	
		HPLOAD_CHN_SEL	0	
		Reserved	00	Start AC impedance measurement
		HPLOAD_AC_START	0	Start AC impedance measurement
7	Wait for interrupt. Read Interrupt Status 4 HPLOAD OOR INT = 1, go to the last s	4 register (0xF0003). If HPLOAD_UNP tep as an error has occurred. Otherwis	LUG_INT = 1, go to the if HPLOAD AC DO	he last step as an error has occurred. If DNE INT = 1, go to the next step.
8	AC impedance values are available in HI	PAC Load Status 0 (0xE0010) and HP	AC Load Status 1 (0)	E0011) registers.
9	Disable AC impedance measurement	HP Load 1. 0xE0000	0x80	
		HPLOAD EN	1	
		Reserved	00	
		HPLOAD_CHN_SEL Reserved	0	
		HPLOAD AC START	0	Stop AC impedance measurement
		HPLOAD_DC_START	0	
10	Select Channel B	0x10010	0x99	
		0x10026	0x0A	
		0x10027	0x93	
		0x10028	0x0A	
		0x10010	0x00	
		HP Load 1. 0xE0000	0x90	
		HPLOAD_EN	1	
		Reserved	00	
		HPLOAD_CHN_SEL Reserved	1	HPOUTB selected
		HPLOAD AC START	0	
		HPLOAD_DC_START	0	
11	Set HP load measurement frequency to	HP Load Measurement 1. 0xE0003	0xA8	
	desired frequency. Assuming 1 kHz.	HPLOAD_MEAS_FREQ_LSB	0xA8	Set measurement frequency = 1 kHz
		HP Load Measurement 2. 0xE0004	0x00	
		HPLOAD_MEAS_FREQ_MSB	0x00	MSB of load measurement frequency
12	Enable AC impedance measurement	HP Load 1. 0xE0000	0x92	
		HPLOAD_EN	1	
		Reserved	00	
		Reserved	00	HPOUTB selected
		HPLOAD_AC_START	1	Start AC impedance measurement
		HPLOAD_DC_START	0	•
13	Wait for interrupt. Read Interrupt Status 4 HPLOAD_OOR_INT = 1, go to the last s	4 register (0xF0003). If HPLOAD_UNP tep as an error has occurred. Otherwis	LUG_INT = 1, go to the e, if HPLOAD_AC_DO	ne last step as an error has occurred. If DNE_INT = 1, go to the next step.
14	AC impedance values are available in HI	P AC Load Status 0 (0xE0010) and HP	PAC Load Status 1 (02	E0011) registers.
15	Disable impedance measurement subsystem	stem. Refer to Ex. 5-23.		



## 5.11.4 Disabling the Impedance Measurement Subsystem

Fig. 5-5 shows and Ex. 5-23 describes the steps necessary for enabling the impedance measurement subsystem.





Example 5-23. Sequence for Disabling the Impedance Measurement Subsystem

STE	D TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Disable DC impedance measurement	HP Load 1. 0xE0000	0x90	
		HPLOAD_EN	1	
		Reserved	00	
		HPLOAD_CHN_SEL	1	HPOUTB selected
		Reserved	00	
		HPLOAD AC START	0	
		HPLOAD_DC_START	0	Stop DC impedance measurement
2	To continue with measuring AC impeda	nce, see Section 5.11.3. To end mea	asurement, go to the	next step.
3	Disable impedance measurement			
4	Restore defaults	0x10010	0x99	
		0x1002C	0x00	
		0x10010	0x00	



#### Example 5-23. Sequence for Disabling the Impedance Measurement Subsystem (Cont.)

STE	P TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
5	Turn off impedance measurement	HP Load 1. 0xE0000		
	subsystem	HPLOAD EN	0	Disable impedance measurement subsystem
		Reserved	00	
		HPLOAD_CHN_SEL	0	
		Reserved	00	
		HPLOAD_AC_START	0	
		HPLOAD_DC_START	0	
6	Wait for interrupt. Check if HPLOAD_OF	F_INT = 1 in Interrupt Status 4 registe	r (0xF0003).	
7	Disable HP Load Interrupts	Interrupt Mask 4. 0xF0013	0xFF	
8	Reset HP load measurement frequency	HP Load Measurement 1. 0xE0003	0x00	
	to 0 Hz	HPLOAD_MEAS_FREQ_LSB	0x00	LSB of load measurement frequency
		HP Load Measurement 2. 0xE0004	0x00	
		HPLOAD_MEAS_FREQ_MSB	0x00	MSB of load measurement frequency



# 6 Register Quick Reference

Notes: Default values are shown below the bit field names. The default values in all reserved bits must be preserved.

Address	Function	7	6	5	4	3	2	1	0
0x01 0000	Device ID A and B		DE	VIDA		-	DF\	/IDB	-
p. 95	(Read Only)	0	1	0	0	0	0	1	1
0x01 0001	Device ID C and D	•			0	Ŭ		י חחו/	•
0,010001	(Read Only)	0	0		1	0	0	1	1
p. 55	Dovice ID E (Pood	U			I	U	U	I	I
0x01 0002	Device ID E (Read	0	DE	VIDE	0		-	-	0
p. 95	5	0	0	0	0	0	0	0	0
0x01 0004	Revision ID (Read		ARI	EVID			MTLF	REVID	
p. 95	Only)	х	х	х	х	х	х	Х	х
0x01 0005	Subrevision ID (Read				SUBF	REVID			
p. 95	Only)	х	х	х	х	х	х	х	х
0x01 0006	System Clocking			_			MCLK_INT	MCLK_S	RC_SEL
p. 96	Control	0	0	0	0	0	1	1	0
0x01 0007-	Reserved				-			•	
0x01 000A		0	0	0	0	0	0	0	0
001.000D	Carial Dart Carrala	0	0	0	0	0			0
0x01 000B	Serial Port Sample	_		-	_	_	ASP_S	PRATE	
p. 96		0	0	0	0	0	0	0	1
0x01 000C	Serial Port Sample Bit		-	_		XSP_S	PSIZE	ASP_S	PSIZE
p. 96	Size	0	0	0	0	0	1	0	1
0x01 000D	Pad Interface			-	_			XSP_3ST	ASP_3ST
p. 96	Configuration	0	0	0	0	0	0	1	1
0x01 000E-	Reserved				_	_		•	
0x01 FFFF		0	0	0	0	0	0	0	0
0,02,0000	Dower Down Control								0
0x02 0000	Power Down Control	PDN_X5P	PDN_ASP	PDN_DSDIF	PDN_HP	PDN_XIAL	PDN_PLL	PDN_CLKOUT	_
p. 97		1	1	1	1	1	1	1	0
0x02 0001-	Reserved				-	_			
0x02 005 1		0	0	0	0	0	0	0	0
0x02 0052	Crystal Setting			_				XTAL IBIAS	
n 97		0	0	0	0	0	1	0	0
0x02.0052	Reserved	•	0	0	Ŭ	ŭ	•	Ū	•
0x02 0000									
0x03 0000		0	0	0	0	0	0	0	0
0x03 0001	PLL Setting 1				—				PLL_START
p. 98		0	0	0	0	0	0	0	0
0x03 0002	PLL Setting 2				PLL_DIV	_FRAC_0			
p. 98		0	0	0	0	0	0	0	0
0x03 0003	PLL Setting 3				PLL DIV	FRAC 1			
p. 98	Ũ	0	0	0	0		0	0	0
0x03 0004	PLL Setting 4				PLL DIV	FRAC 2			
n 98	·	0	0	0	0		0	0	0
0x03.0005	PLL Setting 5	0	0	0			0	Ū	0
0,00 0000	I LL Octuring 5	0	1	0	0	0	0	0	0
p. 90	Decerved	U	I	U	U	U	U	U	U
0x03 0006-	Reserved				-	_			
0.0000		0	0	0	0	0	0	0	0
0x03 0008	PLL Setting 6				PLL_O	UT_DIV			
p. 99		0	0	0	1	0	0	0	0
0x03 0009	Reserved				-	_			
		0	0	0	0	0	0	0	0
0x03 000A	PLL Setting 7	-	-	-	PII CA		-	-	~
n 99	coung /	1	0	0	0	0	0	0	0
p. 33	Reserved	1	0	0	0	5	0	0	5
0x03 000B-	I VESEI VEU				-	_			
0x03 001A		0	0	0	0	0	0	0	0
0x03 001B	PLL Setting 8		-	_		—	_	PLL_MODE	_
p. 99		0	0	0	0	0	0	1	1
0x03 001C-	Reserved				-	_			
0x04 0001		0	0	0	0	0	0	0	0
0x04 0002	PLL Setting 9	-	-	-	_	-	-	PII RFF	PREDIV
n 99		0	0	0	0	0	0	1	
0x04 0003	Reserved	U	v	v	U	_	U		0
0.04 0003	I VESELVEU	0	0	0	-		0	0	0
		U	U	U	U	U	U	U	U

#### Table 6-1. Register Quick Reference



## Table 6-1. Register Quick Reference (Cont.)

Address	Function	7	6	5	4	3	2	1	0
0x04 0004	CLKOUT Control		_			CLKOUT_DIV		CLKOL	JT_SEL
p. 100		0	0	0	0	0	0	0	0
0x04 0005-	Reserved				-	_			
0x04 000F		0	0	0	0	0	0	0	0
0x04 0010	ASP Numerator 1	Ŭ	Ŭ	Ŭ			Ū	Ŭ	•
0,04 0010	ASF Numerator 1	0	0	0	A3F_	N_LOD 0	0	0	1
p. 100	ASD Numerator 2	0	0	0			0	0	I
0004 0011	ASP NUMERALOF 2	0	0	0	ASF_I	N_INISE	0	0	0
p. 100		0	0	0	U	0	0	0	0
0x04 0012	ASP Denominator 1	0	•	0	ASP_	M_LSB	•	0	0
p. 100		0	0	0	0	1	0	0	0
0x04 0013	ASP Denominator 2				ASP_I	M_MSB			
p. 101		0	0	0	0	0	0	0	0
0x04 0014	ASP LRCK High Time				ASP_L0	CHI_LSB			
p. 101	1	0	0	0	1	1	1	1	1
0x04 0015	ASP LRCK High Time				ASP_LC	CHI_MSB			
p. 101	2	0	0	0	0	0	0	0	0
0x04 0016	ASP LRCK Period 1				ASP_LC	PR_LSB			
p. 101		0	0	1	1	1	1	1	1
0x04 0017	ASP LRCK Period 2				ASP LC	PR MSB			
p. 101		0	0	0	0 -	- 0	0	0	0
0x04 0018	ASP Clock		_		ASP M/SB	ASP SCPOL	ASP SCPOL	ASP LCPOL	ASP LCPOL
	Configuration					TUO		TUO	IN
p. 102		0	0	0	0	1	1	0	0
0x04 0019	ASP Frame		_		ASP STP	ASP 5050		ASP FSD	
p. 102	Configuration	0	0	0	0	1	0	1	0
0x04.0014	Reserved	-				_			-
0x04 001/t		0	0	0	0	0	0	0	0
0,04 0011		0	0	0	0	0	0	0	0
0x04 0020	XSP Numerator 1				XSP_	N_LSB			
p. 102		0	0	0	0	0	0	0	1
0x04 0021	XSP Numerator 2				XSP_I	N_MSB			
p. 103		0	0	0	0	0	0	0	0
0x04 0022	XSP Denominator 1				XSP_	M_LSB			
p. 103		0	0	0	0	0	0	1	0
0x04 0023	XSP Denominator 2				XSP_I	M_MSB			
p. 103		0	0	0	0	0	0	0	0
0x04 0024	XSP LRCK High Time				XSP LO	CHI LSB			
p 103	1	0	0	0	1	1	1	1	1
0x04 0025	XSP   RCK High Time		,	Ŭ	XSP LC	HI MSB			•
p 103	2	0	0	0	0	0	0	0	0
p. 100	VSD L BCK Deried 1	0	0	0			0	0	0
0,04 0020	AGE LIKEN FEITUUT	0	0	1	1 × × × ×	/FIX_LOD	1	1	1
p. 104	VOD L DOK Dariad 0	0	0	I			I	I	ļ
0x04 0027	XSP LRCK Period 2				XSP_LC	PR_INSB			•
p. 104		0	0	0	0	0	0	0	0
0x04 0028	XSP Clock Configuration		—		XSP_M/SB	XSP_SCPOL_	XSP_SCPOL_	XSP_LCPOL_	IN XSP_LCPOL_
p 104	Comgaration	0	0	0	0	1	1	0	0
0x04 0020	VSD Eramo	0	0	0		VSD 5050	-		0
0,04 0029	Configuration	0		0	AGF_GTF	AGF_0000	0	X3F_1 3D	0
p. 104	Deserved	U	U	U	U	1	U	I	U
0x04 002A-	Reserved				-	_			
0x04 FFFF		0	0	0	0	0	0	0	0
0x05 0000	ASP Channel 1				ASP_F	X_CH1			
p. 105	Location	0	0	0	0	0	0	0	0
0x05 0001	ASP Channel 2				ASP F	X CH2			
p. 105	Location	0	0	0	0	0	0	0	0
0x05 0002-	Reserved	-	-	-	-	_		-	
0x05 0002			•	0	0	•	•	0	•
0,00,0009		U	U	U	U	0	U	U	0
0x05 000A	ASP Channel 1 Size		-	_		ASP_RX_	ASP_RX_	ASP_RX_	CH1_RES
p 105		0	0	0	0			1	0
p. 100	ACD Chapter 1 0 01-1	U	U	U	U				
0x05 000B	and Enable		-	_		ASP_KX_ CH2 AP	ASP_KX_ CH2_FN	ASP_RX_	UHZ_KES
p 105		0	0	0	0	1	1	1	0
	Reserved	, , , , , , , , , , , , , , , , , , ,	v	v	v			I '	~
	i tesei veu				-	_			
UXUS FFFF		0	0	0	0	0	0	0	0



## Table 6-1. Register Quick Reference (Cont.)

Address	Function	7	6	5	4	3	2	1	0
0x06.0000	YSP Channel 1		Ŭ	Ū			-	•	•
0,0000000	Location	0	0	0		0_0111	0	0	0
p. 100	YOD OLIVINI O	0	0	U	U 		0	0	0
0x06 0001	XSP Channel 2				XSP_R	IX_CH2			
p. 106	Location	0	0	0	0	0	0	0	0
0x06 0002-	Reserved				-	_			
0x06 0009		0	0	0	0	0	0	0	0
0x06.0004	VSP Channel 1 Size		Ū.	•	Ū.				
0,000,0004	and Enable		-	_		CH1 AP	CH1 EN		
n 106		0	0	0	0	0	1	1	0
0x06.000B	VSP Channel 2 Size	•	0	0	0				
0000 0000	and Enable		-	_		CH2 AP	CH2 EN		
n 106		0	0	0	0	1	1	1	0
p. 100	Descried	0	0	0	0	1	1	1	0
0x06 000C-	Reserved				-	_			
0x06 FFFF		0	0	0	0	0	0	0	0
0x07 0000	DSD Volume B				DSD VC	LUME B			
p. 106		0	1	1	1 –	-	0	0	0
0x07.0001		-		-				-	-
0,07 0001	DOD Volume A	0	4	4	1		0	0	0
p. 107	<b>DOD D</b>	0		1	1				
0x07 0002	DSD Processor Path	_	DSD_VOL_	DSD_SZC	-	DSD_AMUTE	DSD_AMUTE_	DSD_MUTE_A	DSD_MUTE_B
	Signal Control 1		BEQA				BEQA	-	
p. 107		1	0	1	0	1	0	0	0
0x07 0003	DSD Interface			—			DSD_M_SB	DSD_PM_EN	DSD_PM_SEL
p. 107	Configuration	0	0	0	0	0	0	0	0
0x07 0004	DSD Processor Path	—	DSD PF	RC_SRC	DSD EN	_	DSD_SPEED	STA_DSD	INV_DSD
	Signal Control 2		-	-	-		-	DET -	Det -
p. 108		0	0	0	0	0	0	1	0
0x07 0005	DSD and PCM Mixing			_	-			MIX PCM	MIX PCM
	Control							PREP	DSD
p. 108		0	0	0	0	0	0	0	0
0x07.0006	DSD Processor Path		DSD HPE EN	_	SIGCTI				
0.07 0000	Signal Control 3	DOD_ZEIKODD			DSDEQPCM			CHAN _	CHAN
n 108		0	1	0	0	0	0	0	0
0:07 0007	Descried	v		0	Ū	0	0	0	v
0x07 0007-	Reserved				-	_			
0,0711111		0	0	0	0	0	0	0	0
0x08 0000	HP Output Control 1	0 HP CLAMPA	0 HP CLAMPB	0	0 FS	0 HP IN EN	0	0	0
0x08 0000	HP Output Control 1	0 HP_CLAMPA 0	0 HP_CLAMPB 0	0 OUT 1	0 _FS 1	0 HP_IN_EN 0	0	0 — I 0	0
0x08 0000 p. 109	HP Output Control 1	0 HP_CLAMPA 0	0 HP_CLAMPB 0	0 OUT 1	0 _FS 1	0 HP_IN_EN 0	0	0  0	0
0x08 0000 p. 109 0x08 0001-	HP Output Control 1 Reserved	0 HP_CLAMPA 0	0 HP_CLAMPB 0	0 OUT 1	0 FS 1 -	0 HP_IN_EN 0	0	0  0	0
0x08 0000 p. 109 0x08 0001– 0x08 FFFF	HP Output Control 1 Reserved	0 HP_CLAMPA 0 0	0 HP_CLAMPB 0	0 OUT 1	0 FS 1 - 0	0 HP_IN_EN 0 -	0	0  0	0 0 0
0x08 0000 p. 109 0x08 0001– 0x08 FFFF 0x09 0000	HP Output Control 1 Reserved PCM Filter Option	0 HP_CLAMPA 0 0 FILTER	0 HP_CLAMPB 0 0 PHCOMP	0 0 1 0 NOS	0 FS 1 	0 HP_IN_EN 0 	0 0 0	0 — 0 HIGH PASS	0 0 0 DEEMP ON
0x08 0000 p. 109 0x08 0001– 0x08 FFFF 0x09 0000	HP Output Control 1 Reserved PCM Filter Option	0 HP_CLAMPA 0 0 FILTER SLOW_FASTB	0 HP_CLAMPB 0 0 PHCOMP_ LOWLATB	0 0 1 0 NOS	0 FS 1 	0 HP_IN_EN 0 	0	0  0 HIGH_PASS	0 0 0 DEEMP_ON
0x08 0000 p. 109 0x08 0001– 0x08 FFFF 0x09 0000 p. 110	HP Output Control 1 Reserved PCM Filter Option	0 HP_CLAMPA 0 0 FILTER SLOW_FASTB 0	0 HP_CLAMPB 0 0 PHCOMP_ LOWLATB 0	0 0UT 1 0 NOS 0	0 FS 1 0	0 HP_IN_EN 0 - 0 0	0 0 0	0 0 0 HIGH_PASS 1	0 0 0 DEEMP_ON 0
0x08 0000 p. 109 0x08 0001– 0x08 FFFF 0x09 0000 p. 110 0x09 0001	HP Output Control 1 Reserved PCM Filter Option PCM Volume B	0 HP_CLAMPA 0 0 FILTER_ SLOW_FASTB 0	0 HP_CLAMPB 0 0 PHCOMP LOWLATB 0	0 0UT 1 0 NOS 0	0 FS 0 0 0 PCM_VC	0 HP_IN_EN 0 	0 0 0	0 — 0 HIGH_PASS 1	0 0 0 DEEMP_ON 0
0x08 0000 p. 109 0x08 0001- 0x08 FFFF 0x09 0000 p. 110 0x09 0001 p. 110	HP Output Control 1 Reserved PCM Filter Option PCM Volume B	0 HP_CLAMPA 0 0 FILTER_ SLOW_FASTB 0	0 HP_CLAMPB 0 0 PHCOMP LOWLATB 0	0 0UT 1 0 NOS 0	0 FS 0 0 PCM_VC 1	0 HP_IN_EN 0 	0 0 0	0 — 0 HIGH_PASS 1	0 0 0 DEEMP_ON 0
0x08 0000 p. 109 0x08 0001– 0x08 FFFF 0x09 0000 p. 110 0x09 0001 p. 110	HP Output Control 1 Reserved PCM Filter Option PCM Volume B	0 HP_CLAMPA 0 0 FILTER_ SLOW_FASTB 0 0	0 HP_CLAMPB 0 PHCOMP LOWLATB 0 1	0 0UT 0 NOS 0 1	0 FS 0 0 PCM_VC 1 PCM_VC	0 HP_IN_EN 0 	0 0 0 0	0 — 0 HIGH_PASS 1 0	0 0 DEEMP_ON 0 0
0x09 1111 0x08 0000 p. 109 0x08 0001– 0x08 FFFF 0x09 0000 p. 110 0x09 0001 p. 110 0x09 0002	HP Output Control 1 Reserved PCM Filter Option PCM Volume B PCM Volume A	0 HP_CLAMPA 0 0 FILTER_ SLOW_FASTB 0 0	0 HP_CLAMPB 0 PHCOMP_ LOWLATB 0 1	0 0UT 1 0 NOS 0 1	0 FS 0 	0 HP_IN_EN 0 	0 0 0 0	0 	0 0 0 0 0 0
0x09 1111 0x08 0000 p. 109 0x08 0001– 0x08 FFFF 0x09 0000 p. 110 0x09 0001 p. 110 0x09 0002 p. 110	HP Output Control 1 Reserved PCM Filter Option PCM Volume B PCM Volume A	0 HP_CLAMPA 0 0 FILTER_ SLOW_FASTB 0 0 0	0 HP_CLAMPB 0 PHCOMP_ LOWLATB 0 1	0 0UT 1 0 NOS 0 1 1	0 FS 0 	0 HP_IN_EN 0 		0 	0 0 0 0 0 0 0
0x09 1111 0x08 0000 p. 109 0x08 0001– 0x08 FFFF 0x09 0000 p. 110 0x09 0001 p. 110 0x09 0002 p. 110 0x09 0002	HP Output Control 1 Reserved PCM Filter Option PCM Volume B PCM Volume A PCM Path Signal	0 HP_CLAMPA 0 0 FILTER SLOW_FASTB 0 0 0 PCM_RAMP_	0 HP_CLAMPB 0 0 PHCOMP_ LOWLATB 0 1 1 PCM_VOL_	0 0UT 1 0 NOS 0 1 1 PCM	0 FS 0 	0 HP_IN_EN 0 	0 0 0 0 0 0 0	0 — 0 HIGH_PASS 1 0 0 PCM_MUTE_A	0 0 DEEMP_ON 0 0 0 PCM_MUTE_B
0x09 1111 0x08 0000 p. 109 0x08 0001– 0x08 FFFF 0x09 0000 p. 110 0x09 0001 p. 110 0x09 0002 p. 110 0x09 0002 p. 110	HP Output Control 1 Reserved PCM Filter Option PCM Volume B PCM Volume A PCM Path Signal Control 1	0 HP_CLAMPA 0 0 FILTER SLOW_FASTB 0 0 0 0 PCM_RAMP_ DOWN	0 HP_CLAMPB 0 0 PHCOMP LOWLATB 0 1 1 PCM_VOL BEQA	0 0UT 1 0 NOS 0 1 1 PCM	0 FS 0 0 PCM_VC 1 	0 HP_IN_EN 0 	0 0 0 0 0 PCM AMUTEBEQA	0  0 HIGH_PASS 1 0 0 PCM_MUTE_A	0 0 DEEMP_ON 0 0 PCM_MUTE_B
0x09 1111 0x08 0000 p. 109 0x08 0001– 0x08 FFFF 0x09 0000 p. 110 0x09 0001 p. 110 0x09 0002 p. 110 0x09 0003 p. 111	HP Output Control 1 Reserved PCM Filter Option PCM Volume B PCM Volume A PCM Path Signal Control 1	0 HP_CLAMPA 0 0 FILTER SLOW_FASTB 0 0 0 PCM_RAMP_ DOWN 1	0 HP_CLAMPB 0 0 PHCOMP_ LOWLATB 0 1 1 PCM_VOL_ BEQA 0	0 0UT 1 0 NOS 0 1 1 PCM 1	0 FS 0 0 PCM_VC 1 SZC 0	0 HP_IN_EN 0 	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0  0 HIGH_PASS 1 0 PCM_MUTE_A 0	0 0 DEEMP_ON 0 0 PCM_MUTE_B 0
0x09 1111 0x08 0000 p. 109 0x08 0001– 0x08 FFFF 0x09 0000 p. 110 0x09 0001 p. 110 0x09 0002 p. 110 0x09 0003 p. 111 0x09 0004	HP Output Control 1 Reserved PCM Filter Option PCM Volume B PCM Volume A PCM Path Signal Control 1 PCM Path Signal	0 HP_CLAMPA 0 0 FILTER SLOW_FASTB 0 0 0 0 PCM_RAMP_ DOWN 1	0 HP_CLAMPB 0 0 PHCOMP LOWLATB 0 1 1 PCM_VOL_ BEQA 0	0 0UT 1 0 NOS 0 1 1 1 2 1	0 FS 0 	0 HP_IN_EN 0 	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 	0 0 DEEMP_ON 0 0 PCM_MUTE_B 0 PCM_COPY_
0x09 1111 0x08 0000 p. 109 0x08 0001– 0x08 FFFF 0x09 0000 p. 110 0x09 0001 p. 110 0x09 0002 p. 110 0x09 0003 p. 111 0x09 0004	HP Output Control 1 Reserved PCM Filter Option PCM Volume B PCM Volume A PCM Path Signal Control 1 PCM Path Signal Control 2	0 HP_CLAMPA 0 0 FILTER_ SLOW_FASTB 0 0 0 PCM_RAMP_ DOWN 1	0 HP_CLAMPB 0 PHCOMP LOWLATB 0 1 1 PCM_VOL_ BEQA 0	0 0UT 1 0 NOS 0 1 1 PCM 1	0 FS 1 0 PCM_VC 1 PCM_VC 1  SZC 0	0 HP_IN_EN 0 	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 	0 0 DEEMP_ON 0 0 PCM_MUTE_B 0 PCM_COPY_ CHAN
0x09 1111 0x08 0000 p. 109 0x08 0001– 0x08 FFFF 0x09 0000 p. 110 0x09 0001 p. 110 0x09 0002 p. 110 0x09 0003 p. 111 0x09 0004 p. 111	HP Output Control 1 Reserved PCM Filter Option PCM Volume B PCM Volume A PCM Path Signal Control 1 PCM Path Signal Control 2	0 HP_CLAMPA 0 0 FILTER SLOW_FASTB 0 0 0 PCM_RAMP_ DOWN 1 0	0 HP_CLAMPB 0 PHCOMP LOWLATB 0 1 1 PCM_VOL_ BEQA 0 0	0 0UT 1 0 NOS 0 1 1 1 PCM 1 - 0	0 FS 0 0 PCM_VC 1 PCM_VC 1 SZC 0	0 HP_IN_EN 0 	0 0 0 0 0 0 0 0 0 0 0 PCM_INV_B 0	0 	0 0 DEEMP_ON 0 0 PCM_MUTE_B 0 PCM_COPY_ CHAN 0
0x09 1111 0x08 0000 p. 109 0x08 0001– 0x08 FFFF 0x09 0000 p. 110 0x09 0001 p. 110 0x09 0002 p. 110 0x09 0003 p. 111 0x09 0004 p. 111 0x09 0005–	HP Output Control 1 Reserved PCM Filter Option PCM Volume B PCM Volume A PCM Path Signal Control 1 PCM Path Signal Control 2 Reserved	0 HP_CLAMPA 0 0 FILTER_ SLOW_FASTB 0 0 0 PCM_RAMP_ DOWN 1 0	0 HP_CLAMPB 0 PHCOMP_ LOWLATB 0 1 1 PCM_VOL_ BEQA 0 - 0	0 0UT 1 0 NOS 0 1 1 1 PCM 1 -	0 FS 1 0 PCM_VC 1 PCM_VC 1 	0 HP_IN_EN 0 	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 	0 0 DEEMP_ON 0 0 PCM_MUTE_B 0 PCM_COPY_ CHAN 0
0x09 1111 0x08 0000 p. 109 0x08 0001– 0x08 FFFF 0x09 0000 p. 110 0x09 0001 p. 110 0x09 0002 p. 110 0x09 0003 p. 111 0x09 0004 p. 111 0x09 0005– 0x0A FFFF	HP Output Control 1 Reserved PCM Filter Option PCM Volume B PCM Volume A PCM Path Signal Control 1 PCM Path Signal Control 2 Reserved	0 HP_CLAMPA 0 0 FILTER SLOW_FASTB 0 0 0 PCM_RAMP_ DOWN 1 0	0 HP_CLAMPB 0 PHCOMP_ LOWLATB 0 1 1 PCM_VOL_ BEQA 0 - 0	0 0UT 1 0 NOS 0 1 1 1 PCM 1 - 0	0 FS 0 	0 HP_IN_EN 0 	0 0 0 0 0 0 0 0 0 0 0 0 PCM_ AMUTEBEQA 0 PCM_INV_B 0 0	0 	0 0 DEEMP_ON 0 0 PCM_MUTE_B 0 PCM_COPY_ CHAN 0
0x09 1111 0x08 0000 p. 109 0x08 0001– 0x08 FFFF 0x09 0000 p. 110 0x09 0001 p. 110 0x09 0002 p. 110 0x09 0002 p. 111 0x09 0004 p. 111 0x09 0005– 0x0A FFFF 0x0B 0005–	HP Output Control 1 Reserved PCM Filter Option PCM Volume B PCM Volume A PCM Path Signal Control 1 PCM Path Signal Control 2 Reserved	0 HP_CLAMPA 0 0 FILTER SLOW_FASTB 0 0 0 PCM_RAMP_ DOWN 1 0 0	0 HP_CLAMPB 0 0 PHCOMP_ LOWLATB 0 1 1 PCM_VOL_ BEQA 0 - 0	0 0UT 1 0 0 0 1 1 1 PCM 1 - 0 0	0 FS 0 0 PCM_VC 1 PCM_VC 1 	0 HP_IN_EN 0 	0 0 0 0 0 0 0 0 0 0 0 0 PCM_ 0 PCM_INV_B 0 0	0 	0 0 DEEMP_ON 0 0 0 PCM_MUTE_B 0 PCM_COPY_ CHAN 0 0
0x08 0000 p. 109 0x08 0001– 0x08 FFFF 0x09 0000 p. 110 0x09 0001 p. 110 0x09 0002 p. 110 0x09 0002 p. 111 0x09 0003– 0x09 0004 p. 111 0x09 0005– 0x0A FFFF 0x0B 0000	HP Output Control 1 Reserved PCM Filter Option PCM Volume B PCM Volume A PCM Path Signal Control 1 PCM Path Signal Control 2 Reserved Class H Control	0 HP_CLAMPA 0 0 FILTER SLOW_FASTB 0 0 0 PCM_RAMP_ DOWN 1 0 0	0 HP_CLAMPB 0 0 PHCOMP LOWLATB 0 1 1 PCM_VOL_ BEQA 0 0 0 0	0 0UT 1 0 NOS 0 1 1 1 PCM 1 - 0 0	0 FS 1 0 PCM_VC 1 PCM_VC 1 	0 HP_IN_EN 0 	0 0 0 0 0 0 0 0 0 0 PCM_ 0 PCM_INV_B 0 0	0 	0 0 DEEMP_ON 0 0 PCM_MUTE_B 0 PCM_COPY_ CHAN 0 0 EXT_VCPFILT
0x08 0000 p. 109 0x08 0001– 0x08 FFFF 0x09 0000 p. 110 0x09 0001 p. 110 0x09 0002 p. 110 0x09 0002 p. 111 0x09 0003 p. 111 0x09 0004 p. 111 0x09 0005– 0x0A FFFF 0x0B 0000 p. 112	HP Output Control 1 Reserved PCM Filter Option PCM Volume B PCM Volume A PCM Path Signal Control 1 PCM Path Signal Control 2 Reserved Class H Control	0 HP_CLAMPA 0 0 FILTER SLOW_FASTB 0 0 0 PCM_RAMP_ DOWN 1 0 0 0 0	0 HP_CLAMPB 0 PHCOMP LOWLATB 0 1 1 PCM_VOL_ BEQA 0 0 0 0 0	0 0UT 1 0 NOS 0 1 1 1 PCM 1 - 0 0 0	0 FS 0 0 PCM_VC 1 	0 HP_IN_EN 0 	0 0 0 0 0 0 0 0 0 PCM_ 0 PCM_INV_B 0 0 0 1	0 	0 0 DEEMP_ON 0 0 PCM_MUTE_B 0 PCM_COPY_ CHAN 0 0 EXT_VCPFILT 0
0x08 0000 p. 109 0x08 0001– 0x08 FFFF 0x09 0000 p. 110 0x09 0001 p. 110 0x09 0002 p. 110 0x09 0002 p. 111 0x09 0004 p. 111 0x09 0004 p. 111 0x09 0005– 0x0A FFFF 0x0B 0000 p. 112 0x0B 0001–	HP Output Control 1 Reserved PCM Filter Option PCM Volume B PCM Volume A PCM Path Signal Control 1 PCM Path Signal Control 2 Reserved Class H Control Reserved	0 HP_CLAMPA 0 0 FILTER_ SLOW_FASTB 0 0 0 PCM_RAMP_ DOWN 1 0 0 0 0	0 HP_CLAMPB 0 PHCOMP LOWLATB 0 1 1 PCM_VOL_ BEQA 0 0 0 0 0	0 0UT 1 0 NOS 0 1 1 1 1 0 0 0	0 FS 1 0 PCM_VC 1 PCM_VC 1 	0 HP_IN_EN 0 	0 0 0 0 0 0 0 0 0 PCM_INV_B 0 PCM_INV_B 0 1	0 	0 0 DEEMP_ON 0 0 PCM_MUTE_B 0 PCM_COPY_ CHAN 0 PCM_COPY_ 0 EXT_VCPFILT 0
0x08 0000 p. 109 0x08 0001– 0x08 FFFF 0x09 0000 p. 110 0x09 0001 p. 110 0x09 0002 p. 110 0x09 0002 p. 111 0x09 0004 p. 111 0x09 0004 p. 111 0x09 0005– 0x0A FFFF 0x0B 0000 p. 112 0x0B 0001– 0x0F FFFF	HP Output Control 1 Reserved PCM Filter Option PCM Volume B PCM Volume A PCM Path Signal Control 1 PCM Path Signal Control 2 Reserved Class H Control Reserved	0 HP_CLAMPA 0 0 FILTER_ SLOW_FASTB 0 0 0 PCM_RAMP_ DOWN 1 0 0 0 0 0	0 HP_CLAMPB 0 PHCOMP LOWLATB 0 1 1 PCM_VOL_ BEQA 0 	0 0UT 1 0 0 0 1 1 1 0 0 0 0 0	0 FS 1 0 PCM_VC 1 PCM_VC 1 SZC 0 0 0 	0 HP_IN_EN 0 	0 0 0 0 0 0 0 0 0 PCM_INV_B 0 PCM_INV_B 0 1	0 	0 0 DEEMP_ON 0 0 PCM_MUTE_B 0 PCM_COPY_ CHAN 0 PCM_COPY_ 0 EXT_VCPFILT 0
0x09 1111 0x08 0000 p. 109 0x08 0001– 0x08 FFFF 0x09 0000 p. 110 0x09 0001 p. 110 0x09 0002 p. 110 0x09 0002 p. 111 0x09 0004 p. 111 0x09 0004 p. 111 0x09 0005– 0x0A FFFF 0x0B 0000– 0x0B 0001– 0x0C FFFF 0x0D 0002	HP Output Control 1 Reserved PCM Filter Option PCM Volume B PCM Volume A PCM Path Signal Control 1 PCM Path Signal Control 2 Reserved Class H Control Reserved	0 HP_CLAMPA 0 0 FILTER_ SLOW_FASTB 0 0 0 PCM_RAMP_ DOWN 1 0 0 0 0 0	0 HP_CLAMPB 0 0 PHCOMP_ LOWLATB 0 1 1 PCM_VOL_ BEQA 0 - 0 0 0	0 0UT 1 0 0 0 1 1 1 0 0 0 0 0	0 FS 1 0 PCM_VC 1 PCM_VC 1 	0 HP_IN_EN 0 	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0	0 	0 0 DEEMP_ON 0 0 PCM_MUTE_B 0 PCM_COPY_ CHAN 0 EXT_VCPFILT 0
0x08 0000 p. 109 0x08 0001– 0x08 FFFF 0x09 0000 p. 110 0x09 0001 p. 110 0x09 0002 p. 110 0x09 0002 p. 111 0x09 0004 p. 111 0x09 0005– 0x0A FFFF 0x0B 0000 p. 112 0x0B 0001– 0x0C FFFF 0x0D 0000	HP Output Control 1 Reserved PCM Filter Option PCM Volume B PCM Volume A PCM Path Signal Control 1 PCM Path Signal Control 2 Reserved Class H Control Reserved HP Detect	0 HP_CLAMPA 0 0 FILTER SLOW_FASTB 0 0 0 PCM_RAMP_ DOWN 1 0 0 0 0 0 0 0 0 0 0	0 HP_CLAMPB 0 0 PHCOMP_ LOWLATB 0 1 1 PCM_VOL_ BEQA 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0UT 1 0 0 0 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0	0 FS 1 0 PCM_VC 1 PCM_VC 1 	0 HP_IN_EN 0 	0 0 0 0 0 0 0 0 AMUTEBEQA 0 PCM_INV_B 0 PCM_INV_B 0 1 0 1 0 1	0 	0 0 DEEMP_ON 0 0 PCM_MUTE_B 0 PCM_COPY_ CHAN 0 PCM_COPY_ 0 0 EXT_VCPFILT 0 0
0x08 0000 p. 109 0x08 0001– 0x08 FFFF 0x09 0000 p. 110 0x09 0001 p. 110 0x09 0002 p. 110 0x09 0002 p. 111 0x09 0003 p. 111 0x09 0005– 0x0A FFFF 0x0B 0000 p. 112 0x0B 0000 p. 112 0x0B 0000 p. 112	HP Output Control 1 Reserved PCM Filter Option PCM Volume B PCM Volume A PCM Path Signal Control 1 PCM Path Signal Control 2 Reserved Class H Control Reserved HP Detect	0 HP_CLAMPA 0 0 FILTER SLOW_FASTB 0 0 0 PCM_RAMP_ DOWN 1 0 0 0 0 0 0 0 0 0 0 0 0 0	0 HP_CLAMPB 0 0 PHCOMP_ LOWLATB 0 1 1 PCM_VOL_ BEQA 0 0 0 0 0 0 CT_CTRL 0	0 0UT 1 0 0 0 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0	0 FS 0 	0 HP_IN_EN 0 	0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 1 0 1	0 	0 0 0 DEEMP_ON 0 0 0 PCM_MUTE_B 0 PCM_COPY_ CHAN 0 PCM_COPY_ 0 0 EXT_VCPFILT 0 0
0x08 0000 p. 109 0x08 0001– 0x08 FFFF 0x09 0000 p. 110 0x09 0001 p. 110 0x09 0002 p. 110 0x09 0002 p. 111 0x09 0003 p. 111 0x09 0004 p. 111 0x09 0005– 0x0A FFFF 0x0B 0000 p. 112 0x0B 0001– 0x0C FFFF 0x0D 0000 p. 112	HP Output Control 1 Reserved PCM Filter Option PCM Volume B PCM Volume A PCM Path Signal Control 1 PCM Path Signal Control 2 Reserved Class H Control Reserved HP Detect	0 HP_CLAMPA 0 0 FILTER SLOW_FASTB 0 0 0 PCM_RAMP_ DOWN 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 HP_CLAMPB 0 PHCOMP LOWLATB 0 1 PCM_VOL_ BEQA 0 0 0 0 0 0 0 CT_CTRL 0	0 OUT 1 0 NOS 0 1 1 PCM 1 - 0 0 0 0 0 0 0 0 0 0 0 0 0	0 FS 1 0 PCM_VC 1 	0 HP_IN_EN 0 0 0 0 0 0 0 0 ADPT_PWR 1 0 SE_DBC_TIME 0	0 0 0 0 0 0 0 0 0 PCM_INV_B 0 PCM_INV_B 0 0 1 0 1 0 1 1 0 1	0 	0 0 0 DEEMP_ON 0 0 0 PCM_MUTE_B 0 PCM_COPY_ CHAN 0 0 EXT_VCPFILT 0 0 0 0 0
0x08 0000           p. 109           0x08 0001-           0x08 FFFF           0x09 0000           p. 110           0x09 0001           p. 110           0x09 0002           p. 110           0x09 0003           p. 111           0x09 0004           p. 111           0x09 0005-           0x0A FFFF           0x0B 0000           p. 112           0x0D 0000           p. 112           0x0D 0001	HP Output Control 1 Reserved PCM Filter Option PCM Volume B PCM Volume A PCM Path Signal Control 1 PCM Path Signal Control 2 Reserved Class H Control Reserved HP Detect HP Status (Read Only)	0 HP_CLAMPA 0 0 FILTER_SLOW_FASTB 0 0 0 PCM_RAMP_ DOWN 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 HP_CLAMPB 0 PHCOMP LOWLATB 0 1 1 PCM_VOL_ BEQA 0 0 0 0 0 CT_CTRL 0 HPDETECT PLUG DBC	0 OUT 1 0 NOS 0 1 1 1 PCM 1 - 0 0 0 0 HPDETECT_ INV 0 HPDETECT_ INV 0	0 FS 1 0 PCM_VC 1 PCM_VC 1 PCM_VC 1 	0 HP_IN_EN 0 	0 0 0 0 0 0 0 0 0 PCM_INV_B 0 PCM_INV_B 0 0 1 0 1 0 1 0 1 0 1 0 0 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0x08 0000           p. 109           0x08 0001-           0x08 FFFF           0x09 0000           p. 110           0x09 0001           p. 110           0x09 0002           p. 110           0x09 0003           p. 111           0x09 0004           p. 111           0x09 0005-           0x0A FFFF           0x0B 0000           p. 112           0x0D 0000           p. 112           0x0D 0001           0x0D 0001	HP Output Control 1 Reserved PCM Filter Option PCM Volume B PCM Volume A PCM Path Signal Control 1 PCM Path Signal Control 2 Reserved Class H Control Reserved HP Detect HP Status (Read Only)	0 HP_CLAMPA 0 0 FILTER SLOW_FASTB 0 0 0 PCM_RAMP_ DOWN 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 HP_CLAMPB 0 0 PHCOMP LOWLATB 0 1 1 PCM_VOL_ BEQA 0 0 0 0 0 0 CT_CTRL 0 0 HPDETECT_ PLUG_DBC 0	0 OUT 1 0 NOS 0 1 1 1 1 1 - 0 0 0 0 0 0 0 0 0 0 0 0 0	0 FS 1 0 PCM_VC 1 PCM_VC 1 PCM_VC 1 SZC 0 0 	0 HP_IN_EN 0 	0 0 0 0 0 0 0 0 0 PCM_INV_B 0 PCM_INV_B 0 1 0 1 0 1 0 1 0 0 1 0 0	0 	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0x07 1111 0x08 0000 p. 109 0x08 0001– 0x08 FFFF 0x09 0000 p. 110 0x09 0001 p. 110 0x09 0002 p. 110 0x09 0002 p. 111 0x09 0004 p. 111 0x09 0004 p. 111 0x09 0005– 0x0A FFFF 0x0B 0000– 0x0B 0000– 0x0B 0001– 0x0D 0000 p. 112 0x0D 00001 p. 112 0x0D 0001– 0x0D 0001	HP Output Control 1 Reserved PCM Filter Option PCM Volume B PCM Volume A PCM Path Signal Control 1 PCM Path Signal Control 2 Reserved Class H Control Reserved HP Detect HP Status (Read Only)	0 HP_CLAMPA 0 0 FILTER SLOW_FASTB 0 0 0 PCM_RAMP_ DOWN 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 HP_CLAMPB 0 0 PHCOMP LOWLATB 0 1 1 PCM VOL_ BEQA 0  0 0 0  0 0 CT_CTRL 0 HPDETECT PLUG_DBC 0	0 OUT 1 0 NOS 0 1 1 1 1 PCM 1  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 FS 1 0 PCM_VC 1 PCM_VC 1 PCM_VC 1 	0 HP_IN_EN 0 	0 0 0 0 0 0 0 0 AMUTEBEQA 0 PCM_INV_B 0 PCM_INV_B 0 1 1 0 HPDETECT_FA 1 0	0 	0 0 0 DEEMP_ON 0 0 0 PCM_MUTE_B 0 PCM_COPY_ CHAN 0 0 EXT_VCPFILT 0 0 0 EXT_VCPFILT 0
0x08 0000 p. 109 0x08 0001– 0x08 FFFF 0x09 0000 p. 110 0x09 0001 p. 110 0x09 0002 p. 111 0x09 0003 p. 111 0x09 0004 p. 111 0x09 0004 p. 111 0x09 0005– 0x0A FFFF 0x0B 0000– 0x0A CFFFF 0x0B 0001– 0x0D 0000 p. 112 0x0D 0001 p. 112 0x0D 0001– 0x0D 0000 p. 112	HP Output Control 1 Reserved PCM Filter Option PCM Volume B PCM Volume A PCM Path Signal Control 1 PCM Path Signal Control 2 Reserved Class H Control Reserved HP Detect HP Status (Read Only) Reserved	0 HP_CLAMPA 0 0 FILTER_ SLOW_FASTB 0 0 0 PCM_RAMP_ DOWN 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 HP_CLAMPB 0 0 PHCOMP_ LOWLATB 0 1 1 PCM VOL_ BEQA 0 - 0 0 0 - 0 0 CT_CTRL 0 HPDETECT_ PLUG_DBC 0	0 OUT 1 0 NOS 0 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 FS 1 0 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC 1 PCM_VC PCM_VC 1 PCM_VC PCM_VC PCM_VC PCM_VC PCM_VC PCM_VC	0 HP_IN_EN 0 	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 	0 0 0 DEEMP_ON 0 0 PCM_MUTE_B 0 PCM_COPY_ CHAN 0 PCM_COPY_ 0 0 EXT_VCPFILT 0 0 0 EXT_VCPFILT 0



## Table 6-1. Register Quick Reference (Cont.)

Address	Function	7	6	5	4	3	2	1	0
0x0E 0000	HP Load 1	HPLOAD_EN	-	- -	HPLOAD_	-	_	HPLOAD_AC_	HPLOAD_DC_
		_			CHN_SEE			START	START
p. 113		0	0	0	0	0	0	0	0
0x0E 0001-	Reserved				-	_			
0x0E 0002		0	0	0	0	0	0	0	0
0x0E 0003	HP Load Measurement				HPLOAD MEA	AS FREQ LSB			
p. 113	1	0	0	0	0 -		0	0	0
0x0E 0004	HP Load Measurement				HPLOAD MEA	S FREQ MSB			
p. 113	2	0	0	0	0		0	0	0
0x0E 0005-	Reserved	-	-	-	_	_		-	-
0x0F 000C		0	0	0	0	0	0	0	0
0.05.0000		0	0	0	0	0	0	0	0
UXUE UUUD	(Read Only)	0	0	0	RL_DC_	_SIAI_U	0	0	0
p. 114		0	0	0			0	0	0
UXUE UUUE	(Read Only)	0	•	0	RL_DC_	_STAT_1	•	0	0
p. 114	(nodu onij)	0	0	0	0	0	0	0	0
0X0E 000F	Reserved	0	0	0	-	-	0	0	0
0.05.0010		0	0	0	0	0	0	0	0
0x0E 0010	HP AC Load Status 0 (Read Only)	•			RL_AC_	_STAT_0		•	•
p. 114		0	0	0	0	0	0	0	0
0x0E 0011	HP AC Load Status 1 (Read Only)				RL_AC_	_STAT_1			
p. 114		0	0	0	0	0	0	0	0
0x0E 0012-	Reserved				-	_			
0x0E 0019		0	0	0	0	0	0	0	0
0x0E 001A	HP Load Status (Read	HPLOAD_DC_	HPLOAD_	-	_	HPLOAD_AC_	HPLOAD_AC_	HPLOAD_DC_	HPLOAD_DC_
	Only)	ONCE	BUSY		•	DONE	BUSY	DONE	BUSY
p. 114		0	0	0	0	0	0	0	0
0x0E 001B-	Reserved				-	_			
0x0E FFFF		0	0	0	0	0	0	0	0
0x0F 0000	Interrupt Status 1	DAC_OVFL_	HP_DETECT_	HP_DETECT_	XTAL_	XTAL_	PLL_READY_	PLL_ERROR_	PDN_DONE_
	(Read Only)	INT	PLUG_INT	UNPLUG_INT	READY_INT	ERROR_INT	INT	INT	INT
p. 115		0	0	0	0	0	0	0	0
0x0F 0001	Interrupt Status 2	ASP_OVFL_	ASP_ERROR_	ASP_LATE_	ASP_EARLY_			_	
D 115	(Read Only)						0	0	0
р. 115 0уог 0002	Interrunt Status 2					VCD	0	0	0
0X0F 0002	(Read Only)	INT	INT	INT	INT	NOLRCK INT		_	
p. 116	(	0	0	0	0	0	0	0	0
0x0F 0003	Interrupt Status 4	HPLOAD NO	HPLOAD		HPLOAD	HPLOAD AC	HPLOAD DC	HPLOAD	HPLOAD ON
	(Read Only)	DC_INT	UNPLUG_INT		OOR_INT	DONE_INT	DONE_INT	OFF_INT	INT -
p. 116		0	0	0	0	0	0	0	0
0x0F 0004	Interrupt Status 5	DSD_STUCK_	DSD_INVAL_	DSD_INVAL_	DSD_	DSD_	DSD_RATE_	DOP_MRK_	DOP_ON_INT
	(Read Only)	INT	A_INT	B_INT	SILENCE_A_	SILENCE_B_	ERROR_INT	DET_INT	
n 117		Ο	0	0	0		0	Ο	0
p. 117	Pasanyad	0	0	0	0	0	0	0	0
0x0F 0005-	Reserved				-	_			
UXUF UUUF		0	0	0	0	0	0	0	0
0x0F 0010	Interrupt Mask 1	DAC_OVFL_	HP_DETECT_	HP_DETECT_		XTAL_	PLL_READY_	PLL_ERROR_	PDN_DONE_
		INT_INIASK	MASK	INT MASK	MASK	MASK	INI_INIASK	INI_INIASK	INI_WASK
p. 117		1	1	-	1	1	1	1	1
0x0F 0011	Interrupt Mask 2	ASP OVFL	ASP ERROR	ASP LATE	ASP EARLY	ASP			
		INT_MASK	INT_MASK	INT_MASK	INT_MASK	NOLRCK_			
						INT_MASK			
p. 118		1	1	1	1	1	1	1	1
0x0F 0012	Interrupt Mask 3	XSP_OVFL_	XSP_ERROR_	XSP_LATE_	XSP_EARLY_			—	
						INT_MASK			
p. 118		1	1	1	1	1	1	1	1
0x0F 0013	Interrupt Mask 4	HPLOAD NO	HPLOAD	_	HPLOAD	HPLOAD AC	HPLOAD DC	HPLOAD	HPLOAD ON
					OOR_INT_	DONE_INT_	DONE_INT_	OFF_INT_	INT_MĀSK
		MASK	IN I_MASK		MASK	MASK	MASK	MASK	, I
p. 119		1	1	1	1	1	1	1	1
0x0F 0014	Interrupt Mask 5	USD_STUCK_	DSD_INVAL	DSD_INVAL B_INT_MASE		DSD_ SILENCE B	DSD_RATE_	DOP_MRK_	DOP_ON_ INT_MASK
					INT_MASK	INT_MASK	MASK	MASK	
p. 120		1	1	1	-	1	1	1	1
0x0F 0015-	Reserved					•			
0x0F FFFF		0	0	0	0	0	0	0	0
		U	U	U	U	U	U	U	U



# 7 Register Descriptions

All registers are read/write, except for the device's ID, revision, and status registers, which are read only. The following tables describe bit assignments. The default state of each bit after a power-up sequence or reset is listed in each bit description. All reserved bits must maintain their default state.

## 7.1 Global Registers

7.1.1	Devic	e ID A and B					Α	ddress 0x10000
R/0	D 7	6	5	4	3	2	1	0
		DEV	IDA			DEV	/IDB	
Defau	lt O	1	0	0	0	0	1	1
Bits	Name				Description			
7:4	DEVIDA	Part number first dig	git: 4					
3:0	DEVIDB	Part number second	d digit: 3					
7.1.2	Devic	e ID C and D					А	ddress 0x10001
R/0	D 7	6	5	4	3	2	1	0
		DEV	IDC			DEV	/IDD	
Defau	lt O	0	0	1	0	0	1	1
Bits	Name				Description			
7:4	DEVIDC	Part number third di	igit: 1					
3:0	DEVIDD	Part number fourth	digit: 3					
7.1.3	Devic	e ID E					А	ddress 0x10002
R/0	7	6	5	4	3	2	1	0
		DEV	IDE			_	_	
Defau	lt O	0	0	0	0	0	0	0
Bits	Name				Description			
7:4	DEVIDE	Part number fifth dig	git: O					
3:0	—	Reserved						
7.1.4	Revis	ion ID					А	ddress 0x10004
R/0	7	6	5	4	3	2	1	0
		ARE	VID			MTLR	REVID	
Defau	lt x	Х	х	Х	Х	Х	х	x
Bits	Name				Description			
7:4	AREVID	Alpha revision. ARE	VID and MTLR	EVID form the co	mplete device rev	ision ID (e.g., A	0, B2).	
3:0	MTLREVID	Metal revision. ARE	VID and MTLR	EVID form the cor	mplete device rev	vision ID (e.g., A0	), B2).	
7.1.5	5 Subre	vision ID					А	ddress 0x10005
R/0	7 (	6	5	4	3	2	1	0
				SUBF	REVID			
Defau	lt x	х	х	х	Х	Х	х	х
Bits	Name				Description			
7:0	SUBREVID	Subrevision level.						



#### 7.1.6 System Clocking Control

		•										
R/	W 7	6	5	4	3	2	1	0				
			_			MCLK_INT	MCLK_S	RC_SEL				
Defa	ult 0	0	0	0	0	1	1	0				
Bits	Name				Description							
7:3	_	Reserved										
2	MCLK_INT	The frequency of in 0 Internal MCLK is 1 (Default) Interna	he frequency of internal MCLK. 0 Internal MCLK is expected to be 24.576 MHz 1 (Default) Internal MCLK is expected to be 22.5792 MHz									
1:0	MCLK_SRC_ SEL	Select the source of 00 Direct MCLK/X 01 PLL Mode 10 (Default) RCO 11 Reserved	elect the source of internal MCLK. 00 Direct MCLK/XTAL Mode 01 PLL Mode 10 (Default) RCO Mode 11 Reserved									

#### 7.1.7 **Serial Port Sample Rate**

R/W	7	6	5	4	3	2	1	0	
		_	_		ASP_SPRATE				
Default	0	0	0	0	0	0	0	1	

Bits	Name	Description
7:4	_	Reserved
3:0	ASP_SPRATE	ASP sample rate. This register must be programmed for both Master Mode and Slave Mode operation. 0000 32 kHz 0001 (Default) 44.1 kHz 0010 48 kHz 0011 88.2 kHz 0100 96 kHz 0100 96 kHz 0101 176.4 kHz 0110 192 kHz 0111 352.8 kHz 1000 384 kHz 1001–1111 Reserved

## 7.1.8 Serial Port Sample Bit Size

R/W	7	6	5	4	3	2	1	0
					XSP_SPSIZE		ASP_SPSIZE	
Default	0	0	0	0	0	1	0	1

Bits	Name	Description
7:4	_	Reserved
3:2	XSP_SPSIZE	XSP sample bit size. 00 32 bits 01 (Default) 24 bits 10–11 Reserved
1:0	ASP_SPSIZE	ASP sample bit size. 00 32 bits 01 (Default) 24 bits 10 16 bits 11 8 bits

#### **Pad Interface Configuration** 7.1.9

#### R/W 7 5 6 4 3 2 1 0 XSP\_3ST ASP\_3ST Default 0 0 0 0 0 0 1 1 Bits Name Description 7:2 Reserved \_

Address 0x1000C

Address 0x1000B

Address 0x1000D



Bits	Name	Description
1	XSP_3ST	Determines the state of the XSP clock drivers when in Master Mode. When in Slave Mode, the serial port clocks are inputs, whose function is not affected by this bit. Before setting an xSP_3ST bit, the associated serial port must be powered down and not powered up until the xSP_3ST bit is cleared.
		0 When in Master Mode, serial port clocks are active. 1 (Default) When in Master Mode, serial port clocks are Hi-Z.
0	ASP_3ST	Determines the state of the ASP clock drivers when in Master Mode. When in Slave Mode, the serial port clock pins are inputs, whose function is not affected by this bit. Before setting an xSP_3ST bit, the associated serial port must be powered down and not powered up until the xSP_3ST bit is cleared.
		0 When in Master Mode, serial port clocks are active. 1 (Default) When in Master Mode, serial port clocks are Hi-Z.

## 7.1.10 Power Down Control

Address 0x20000

R/V	V 7	6	5	4	3	2	1	0	
	PDN_XSF	PDN_ASP	PDN_DSDIF	PDN_HP	PDN_XTAL	PDN_PLL	PDN_CLKOUT	_	
Defaul	t 1	1	1	1	1	1	1	0	
Bits	Name				Description				
7	PDN_XSP	XSP input path pov	ver control. Confi	gures XSP SDIN	I path power state	э.			
		0 Powered up. 1 (Default) Powe	red down.						
6	PDN_ASP	ASP input path pov	ver control. Confi	gures ASP SDIN	I path power state	э.			
		0 Powered up. 1 (Default) Powe	red down.						
5	PDN_DSDIF	DSD interface pow	er control. Sets tl	ne power state o	f the DSD interfac	ce block.			
		0 Powered up. 1 (Default) Powe	red down.						
4	PDN_HP	Power down HPOL	JTx.						
		0 Powered up. Th 1 (Default) Powe soft ramped to	he HP driver and red down. The H mute.	DACx are powe P driver and DA	red up. Cx are powered d	own. When this	bit is set, the audi	o outputs are	
3	PDN_XTAL	Power down crysta	l oscillator.						
		0 Powered up. The 1 (Default) Powe	he XTAL driver is red down. The X	powered up to s TAL driver is pow	start generating N vered down.	ICLK.			
2	PDN_PLL	PLL output power of 0 Powered up. 1 (Default) Powe	LL output power control. Sets the power state of the PLL block. 0 Powered up. 1 (Default) Powered down. PLL block is powered down.						
1	PDN_	CLKOUT output po	ower control. Sets	the power state	of the CLOCKO	JT output.			
	CLKOUT	0 Powered up 1 (Default) Powe	red down. CLKO	UT are driven lov	<i>N</i> .				
0	_	Reserved							

## 7.1.11 Crystal Setting

	<b>J</b> =	J							
R/	W 7	6	5	4	3	2	1	0	
			_				XTAL_IBIAS		
Defau	ult O	0	0	0	0	1	0	0	
Bits	Name		Description						
7:3	_	Reserved							
2:0	XTAL_IBIAS	Crystal bias current 010 15.0 μA 100 (Default) 12.5 110 7.5 μA Others Reserved	strength. μΑ						



# 7.2 PLL Registers

	U							
7.2.1		etting 1					A	ddress 0x30001
R/\	N 7	6	5	4	3	2	1	0
				—				PLL_START
Defau	ılt O	0	0	0	0	0	0	0
Bits	Name				Description			
7:1		Reserved						
0	PLL_START	PLL start bit. Enab 0 (Default) PLL i 1 PLL is started	le PLL output afte s not started	er it has been prop	erly configured.			
7.2.2	2 PLL S	etting 2					A	ddress 0x30002
R/\	N 7	6	5	4	3	2	1	0
		-		PLL DIV	FRAC 0			
Defau	ılt O	0	0	0	0	0	0	0
Bits	Name			I	Description			
7:0	PLL_DIV_ FRAC_0	PLL fractional port e.g., 0xFF means 0000 0000 (Defaul	ion of divide ratio I (2 <sup>-17</sup> + 2 <sup>-18</sup> + …+2 lt)	LSB. There are 3 k 2 <sup>-24</sup> ).	oytes of PLL feed	dback divider fra	ction portion and	this is LSB byte;
7.2.3	B PLL S	etting 3					A	ddress 0x30003
R/\	N 7	6	5	4	3	2	1	0
				PLL_DIV_	FRAC_1			
Defau	ılt O	0	0	0	0	0	0	0
Bits	Name				Description			
7:0	PLL_DIV_ FRAC_1	PLL fractional port 0000 0000 (Defau	ion of divide ratio lt)	middle byte; e.g.,	0xFF means (2	<sup>-9</sup> + 2 <sup>-10</sup> ++2 <sup>-1</sup>	6).	
7.2.4	4 PLL S	etting 4					A	ddress 0x30004
R/\	N 7	6	5	4	3	2	1	0
				PLL_DIV_	FRAC_2			
Defau	ılt O	0	0	0	0	0	0	0
Bits	Name				Description			
7:0	PLL_DIV_ FRAC_2	PLL fractional port 0000 0000 (Defaul	ion of divide ratio lt)	MSB; e.g., 0xFF ı	means (2 <sup>-1</sup> + 2 <sup>-2</sup>	<sup>2</sup> ++2 <sup>-8</sup> ).		
7.2.	5 PLL S	etting 5					A	ddress 0x30005
R/\	N 7	6	5	4	3	2	1	0
				PLL_DI	/_INT			
Defau	ılt O	1	0	0	0	0	0	0
Bits	Name			I	Description			
7:0	PLL_DIV_INT	PLL integer portion 0100 0000 (Defaul	n of divide ratio. Ir lt)	nteger portion of P	LL feedback div	rider.		



7.2.6	6 PLL S	etting 6					Ad	dress 0x30008
R/\	N 7	6	5	4	3	2	1	0
				PLL_OI	JT_DIV			
Defau	lt O	0	0	1	0	0	0	0
Bits	Name				Description			
7:0	PLL_OUT_ DIV	Final PLL clock ou 0001 0000 (Defa	tput divide value. ult)					
7.2.7	7 PLL S	etting 7					Ado	dress 0x3000A
R/\	N 7	6	5	4	3	2	1	0
				PLL_CAI	RATIO			
Defau	ılt 1	0	0	0	0	0	0	0
Bits	Name				Description			
7:0	PLL_CAL_ RATIO	PLL calibration rati 1000 0000 (Defa	o. See Section 4. ult)	7.2 for configurat	ion details. Targe	et value for PL	L VCO calibration.	
7.2.8	B PLL S	etting 8					Add	dress 0x3001B
R/\	N 7	6	5	4	3	2	1	0
				_			PLL_MODE	
Defau	ilt 0	0	0	1	0	0	1	1
Bits	Name				Description			
7:2		Reserved						
1	PLL_MODE	500/512 factor use	d in PLL frequend	cy calculation equ	uation, <mark>Eq</mark> . 4-1.			
		0 No bypass 1 (Default) Bypas	SS					
0		Reserved						
7.2.9	PLL S	etting 9					Ad	dress 0x40002
R/\	N 7	6	5	4	3	2	1	0
			-	_			PLL_REF_	PREDIV
Defau	ılt O	0	0	0	0	0	1	0
Bits	Name				Description			
7:2		Reserved						
1:0	PLL_REF_ PREDIV	PLL reference divid 00 Divide by 1 01 Divide by 2 10 (Default) Divid 11 Divide by 8	de select. de by 4					



Address 0x40004

Address 0x40010

Address 0x40011

Address 0x40012

# 7.3 ASP and XSP Registers

## 7.3.1 CLKOUT Control

R/	W 7	6	5	4	3	2	1	0
		—			CLKOUT_DIV		CLKOU	JT_SEL
Defa	ult O	0	0	0	0	0	0	0
Bits	Name				Description			
7:5	_	Reserved						
4:2	CLKOUT_DIV	Divider setting on inf	ernal MCLK pat	th to CLKOUT.				
		000 (Default) Divic 001 Divide by 3 010 Divide by 4 011 Divide by 8 100–111 Reserved	le by 2 d					
1:0	CLKOUT_SEL	Select the source of 00 (Default) XTAL 01 PLL output path 10–11 Reserved	CLKOUT. /MCLK path า					

## 7.3.2 ASP Numerator 1

R/\	N 7	6	5	4	3	2	1	0	
				ASP_I	N_LSB				
Defau	ılt O	0	0	0	0	0	0	1	
		-			•				
Bits	Name		Description						
7:0	ASP_N_LSB	The value in this re	egister cannot be	changed while th	ne serial port is p	owered up.			
		ASP sample rate fi setting the SCLK fi	ASP sample rate fractional divide numerator LSB. Along with ASP_M_MSB/LSB, selects the fractional divide value for setting the SCLK frequency.						
		(Default) ASP_N = 1							

## 7.3.3 ASP Numerator 2

R/	N 7	6	5	4	3	2	1	0			
			ASP_N_MSB								
Defau	ılt O	0	0 0 0 0 0 0 0								
Bits	Name		Description								
7:0	ASP_N_MSB	The value in this reg	gister cannot be	changed while th	e serial port is p	owered up.					
		ASP sample rate fra setting the SCLK fre (Default) ASP_N =	actional divide nu equency. 1	umerator MSB. A	long with ASP_N	1_MSB/LSB, sele	cts the fractional	divide value for			

## 7.3.4 ASP Denominator 1

R/	N 7	6	5	4	3	2	1	0	
				ASP_N	/LSB				
Defau	ılt O	0 0 0 1 0 0 0							
Bits	Name		Description						
7:0	ASP_M_LSB	The value in this re	gister cannot be	changed while th	e serial port is p	owered up.			
		ASP sample rate fractional divide denominator LSB. Along with ASP_N_MSB/LSB, selects the fractional divide value for setting the SCLK frequency. Default) ASP_M = 8							



Address 0x40013

Address 0x40014

Address 0x40015

Address 0x40016

Address 0x40017

## 7.3.5 ASP Denominator 2

R/	N 7	6	5	4	3	2	1	0			
			ASP_M_MSB								
Defau	ılt O	0	0	0	0	0	0	0			
Bits	Name		Description								
7:0	ASP_M_MSB	The value in this reg	ister cannot be	changed while th	ie serial port is p	owered up.					
		ASP sample rate fra- setting the SCLK fre (Default) ASP_M = 8	ctional divide de quency. 3	enominator LSB. A	Along with ASP_I	N_MSB/LSB, sele	cts the fractional	divide value for			

## 7.3.6 ASP LRCK High Time 1

R/	N 7	6	5	4	3	2	1	0			
			ASP_LCHI_LSB								
Defau	ılt O	0	0	1	1	1	1	1			
Bits	Name		Description								
7:0	ASP_LCHI_ LSB	The value in this reg ASP LRCK high dur ASP_LCPR. (Default) ASP_LCH	he value in this register cannot be changed while the serial port is powered up. SP LRCK high duration, in units of ASP_SCLK periods stored in ASP_LCHI_MSB/LSB. This value must be less than SP_LCPR. Default) ASP_LCHI = 31								

## 7.3.7 ASP LRCK High Time 2

R/	N 7	6	5	4	3	2	1	0	
				ASP_LC	HI_MSB				
Defau	ılt O	0	0	0	0	0	0	0	
Bits	Name		Description						
7:0	ASP_LCHI_ MSB	The value in this rea ASP LRCK high du ASP_LCPR. (Default) ASP_LCH	he value in this register cannot be changed while the serial port is powered up. SP LRCK high duration, in units of ASP_SCLK periods stored in ASP_LCHI_MSB/LSB. This value must be less than SP_LCPR. Default) ASP_LCHI = 31						

## 7.3.8 ASP LRCK Period 1

R/W	7	6	5	4	3	2	1	0
				ASP_LC	PR_LSB			
Default	0	0	1	1	1	1	1	1

Bits	Name	Description
7:0	ASP_LCPR_ LSB	The value in this register cannot be changed while the serial port is powered up. ASP LRCK period, in units of ASP_SCLK periods stored in ASP_LCPR_MSB/LSB. (Default) ASP_LCPR = 63

## 7.3.9 ASP LRCK Period 2

R/\	N 7	6	5	4	3	2	1	0	
				ASP_LC	PR_MSB				
Defau	ılt O	0	0	0	0	0	0	0	
Bits	Nomo		Description						
	Name				Description				



## 7.3.10 ASP Clock Configuration

		0						
R/W	7	6	5	4	3	2	1	0
		_		ASP_M/SB	ASP_SCPOL_ OUT	ASP_SCPOL_ IN	ASP_LCPOL_ OUT	ASP_LCPOL_ IN
Default	0	0	0	0	1	1	0	0

Bits	Name	Description
7:5	—	Reserved
4	ASP_M/SB	ASP port master or slave configuration.
		0 (Default) Slave Mode (input) 1 Master Mode (output)
3	ASP_SCPOL_	ASP SCLK output drive polarity.
	OUT	0 Normal 1 (Default) Inverted
2	ASP_SCPOL_	ASP SCLK input polarity (pad to logic).
	IN	0 Normal 1 (Default) Inverted
1	ASP_LCPOL_	ASP LRCK output drive polarity.
	OUT	0 (Default) Normal 1 Inverted
0	ASP_LCPOL_	ASP LRCK input polarity (pad to logic).
	IN	0 (Default) Normal 1 Inverted

## 7.3.11 ASP Frame Configuration

R/W	7	6	5	4	3	2	1	0
		—		ASP_STP	ASP_5050		ASP_FSD	
Default	0	0	0	0	1	0	1	0

Bits	Name	Description
7:5		Reserved
4	ASP_STP	ASP start phase. Controls which LRCK/FSYNC phase starts a frame. 0 (Default) The frame begins when LRCK/FSYNC transitions from high to low 1 The frame begins when LRCK/FSYNC transitions from low to high
3	ASP_5050	ASP LRCK fixed 50/50 duty cycle. 0 Programmable duty cycle per ASP_LCHI and ASP_LCPR. 1 (Default) Fixed 50% duty cycle
2:0	ASP_FSD	ASP frame start delay (units of ASP_SCLK periods). 000 0 delay 001 0.5 delay 010 (Default) 1.0 delay  101 2.5 delay 110–111 Reserved

## 7.3.12 XSP Numerator 1

R/W	7	6	5	4	3	2	1	0
				XSP_N	N_LSB			
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:0	XSP_N_LSB	The value in this register cannot be changed while the serial port is powered up.
		XSP sample rate fractional divide numerator LSB. Along with XSP_M_MSB/LSB, selects the fractional divide value for setting the SCLK frequency. (Default) XSP_N = 1

Address 0x40018

#### Address 0x40019

Address 0x40020



Address 0x40021

Address 0x40022

Address 0x40023

Address 0x40024

Address 0x40025

### 7.3.13 XSP Numerator 2

R/	N 7	6	5	4	3	2	1	0
				XSP_N	I_MSB			
Defau	ılt O	0	0	0	0	0	0	0
Bits	Name				Description			
7:0	XSP_N_MSB	The value in this reg XSP sample rate fra setting the SCLK fre (Default) XSP_N = 1	ister cannot be ctional divide nu equency.	changed while th umerator MSB. A	e serial port is p long with XSP_N	owered up. 1_MSB/LSB, sele	cts the fractional	divide value for

## 7.3.14 XSP Denominator 1

R/	W 7	6	5	4	3	2	1	0		
				XSP_I	M_LSB					
Defau	ult O	0	0	0	0	0	1	0		
Bits	Name		Description							
7:0	XSP_M_LSB	The value in this reg	jister cannot be	changed while th	ne serial port is p	owered up.				
		XSP sample rate fractional divide denominator LSB. Along with XSP_N_MSB/LSB, selects the fractional divide value for setting the SCLK frequency. (Default) XSP_M = 2								

## 7.3.15 XSP Denominator 2

R/	N 7	6	5	4	3	2	1	0
				XSP_N	1_MSB			
Defau	ılt O	0	0	0	0	0	0	0
Bits	Name				Description			
7:0	XSP_M_MSB	The value in this reg	gister cannot be	changed while th	e serial port is po	owered up.		
		XSP sample rate fra for setting the SCLK	actional divide de Cfrequency.	enominator MSB.	Along with XSP	_N_MSB/LSB, se	elects the fractior	nal divide value

### (Default) XSP\_M = 2

## 7.3.16 XSP LRCK High Time 1

R/W	7	6	5	4	3	2	1	0	
	XSP_LCHI_LSB								
Default	0	0	0	1	1	1	1	1	

Bits	Name	Description
7:0	XSP_LCHI_ LSB	The value in this register cannot be changed while the serial port is powered up. XSP LRCK high duration, in units of XSP_SCLK periods stored in XSP_LCHI_LSB/MSB. This value must be less than XSP_LCPR. (Default) XSP_LCHI = 31

## 7.3.17 XSP LRCK High Time 2

R/\	N 7	6	5	4	3	2	1	0
				XSP_LC	HI_MSB			
Defau	ılt O	0	0	0	0	0	0	0
Bits	Name				Description			
7:0	XSP_LCHI_ MSB	The value in this rea XSP LRCK high du XSP_LCPR. (Default) XSP_LCHI	gister cannot be ration, in units of = 31	changed while th f XSP_SCLK peri	ne serial port is p ods stored in XS	owered up. ፡P_LCHI_LSB/M§	SB. This value m	ust be less than

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## 7.3.18 XSP LRCK Period 1

Address 0x40027

Address 0x40028

R/	N 7	6	5	4	3	2	1	0				
		XSP_LCPR_LSB										
Defau	ılt O	0	1	1	1	1	1	1				
Bits	Name		Description									
7:0	XSP_LCPR_ LSB	SP_LCPR_       The value in this register cannot be changed while the serial port is powered up.         LSB       XSP LRCK period, in units of XSP_SCLK periods stored in XSP_LCPR_LSB/MSB.         (Default) XSP_LCPR = 63										

## 7.3.19 XSP LRCK Period 2

R/	W 7	6	5	4	3	2	1	0		
		XSP_LCPR_MSB								
Defa	ult O	0	0	0	0	0	0	0		
Bits	Name		Description							
7:0	XSP_LCPR_ MSB	The value in this register cannot be changed while the serial port is powered up. XSP LRCK period, in units of XSP_SCLK periods stored in XSP_LCPR_LSB/MSB. (Default) XSP_LCPR = 63								

## 7.3.20 XSP Clock Configuration

R/W	7	6	5	4	3	2	1	0
		_		XSP_M/SB	XSP_SCPOL_ OUT	XSP_SCPOL_ IN	XSP_LCPOL_ OUT	XSP_LCPOL_ IN
Default	0	0	0	0	1	1	0	0

Bits	Name	Description
7:5	—	Reserved
4	XSP_M/SB	XSP port master or slave configuration. 0 (Default) Slave Mode (input)
3	XSP_SCPOL_ OUT	XSP SCLK output drive polarity. 0 Normal 1 (Default) Inverted
2	XSP_SCPOL_ IN	XSP SCLK input polarity (pad to logic). 0 Normal 1 (Default) Inverted
1	XSP_LCPOL_ OUT	XSP LRCK output drive polarity. 0 (Default) Normal 1 Inverted
0	XSP_LCPOL_ IN	XSP LRCK input polarity (pad to logic). 0 (Default) Normal 1 Inverted

## 7.3.21 XSP Frame Configuration

R/W	7	6	5	4	3	2	1	0
		—		XSP_STP	XSP_5050		XSP_FSD	
Default	0	0	0	0	1	0	1	0

Bits	Name	Description
7:5	_	Reserved
4	XSP_STP	XSP start phase. Controls which LRCK/FSYNC phase starts a frame. 0 (Default) The frame begins when LRCK/FSYNC transitions from high to low 1 The frame begins when LRCK/FSYNC transitions from low to high
3	XSP_5050	XSP LRCK fixed 50/50 duty cycle. 0 Programmable duty cycle per XSP_LCHI and XSP_LCPR 1 (Default) Fixed 50% duty cycle

Address 0x40029



Bits	Name				Description							
2:0	XSP_FSD	XSP frame start del	ay (units of XSP	_SCLK periods).								
		000 0 delay 001 0.5 delay 010 (Default) 1.0 d	delay									
		 101 2.5 delay 110–111 Reserve	d									
7.3.	22 ASP C	hannel 1 and	2 Location	1			Address 0x	50000, 0x50001				
R/	W 7	6	5	4	3	2	1	0				
		ASP_RX_CH1										
		ASP_RX_CH2										
Defa	ult O	0	0	0	0	0	0	0				
Bits	Name				Description							
7:0	ASP_RX_CHn	ASP Rx channel <i>n</i> lo frame. 0x00 Start on SCI  0xFF Start on SCI Defaults are 0x00.	ocation. Sets the LK 0 LK 255	e location in ASP	_SCLK periods o	f the ASP Rx ch	nannel <i>n</i> from the s	start of the TDM				
<b>7.3.</b>	23 ASP C	hannel 1 Size	and Enabl	e	3	2	Ad	Idress 0x5000A				

7 2 24		onnol 2 Siza	- and Enchl	•	, , , , , , , , , , , , , , , , , , ,			ddross 0x5000B
Default	0	0	0	0	0	1	1	0
		-	_		ASP_RX_CH1_ AP	ASP_RX_CH1_ EN	ASP_RX_	CH1_RES
R/W	7	6	5	4	3	2	1	0

## 7.3.24 ASP Channel 2 Size and Enable

R/W	7	6	5	4	3	2	1	0
		_	_		ASP_RX_CH2_ AP	ASP_RX_CH2_ EN	ASP_RX_	CH2_RES
Default	0	0	0	0	1	1	1	0

Bits	Name	Description
7:4	_	Reserved
3	ASP_RX_ CH <i>n</i> _AP	ASP RX channel <i>n</i> active phase. Valid only in 50/50 mode (ASP_5050 = 1). 0 (Default when $n = 1$ ) In 50/50 mode, channel data is input when LRCK/FSYNC is low 1 (Default when $n = 2$ ) In 50/50 mode, channel data is input when LRCK/FSYNC is high
2	ASP_RX_ CHn_EN	ASP RX channel <i>n</i> enable. Configures the state of the data for the ASP on channel <i>n</i> . The same rule applies to CHx_EN. 0 (Default) Input channel data is not propagated to the internal data path 1 Input channel data is propagated to the internal data path
1:0	ASP_RX_ CHn_RES	ASP RX channel <i>n</i> size (in bits). Sets the output resolution of the ASP RX channel <i>n</i> samples. 00 8 bits per sample 01 16 bits per sample 10 (Default) 24 bits per sample 11 32 bits per sample



7.3.2	25 XSP C	hannel 1 and	2 Location				Address 0x	60000, 0x60001		
R/\	N 7	6	5	4	3	2	1	0		
				XSP_	RX_CH1					
				XSP_	RX_CH2					
Defau	iit 0	0	0	0	0	0	0	0		
Bits	Name				Description					
7:0	XSP_RX_CHn	XSP Rx channel <i>n</i> I frame. 0x00 Start on SC	ocation. Sets the LK 0	location in XSF	SCLK periods c	f the XSP Rx char	nel <i>n</i> from the s	tart of the TDM		
		0xFF Start on SC Defaults are 0x00.	LK 255							
7.3.2	26 XSP C	hannel 1 Size	and Enable	e			Ad	dress 0x6000A		
R/\	N 7	6	5	4	3	2	1	0		
		_	_		XSP_RX_CH1_ AP	XSP_RX_CH1_ EN	XSP_RX_0	CH1_RES		
Defau	ılt O	0	0	0	0	1	1	0		
7.3.2	27 XSP C	hannel 2 Size	and Enable	e			Ad	dress 0x6000B		
R/\	N 7	6	5	4	3	2	1	1		
		-	_		XSP_RX_CH2_ AP	XSP_RX_CH2_ EN	XSP_RX_0	CH2_RES		
Defau	lt O	0	0	0	1	1	1	0		
Bits	Name				Description					
7:4	_	Reserved								
3	XSP_RX_	XSP Rx channel n	active phase. Val	id only in 50/50	mode (XSP_505	0 = 1).				
	CHn_AP	0 (Default when r 1 (Default when r	n = 1) ln 50/50 m n = 2) ln 50/50 m n	ode, channel da ode, channel da	ata is input when L ata is input when L	RCK/FSYNC is lo RCK/FSYNC is hi	w gh			
2	XSP_RX_	XSP Rx channel <i>n</i> enable. Configures the state of the data for the XSP on channel <i>n</i> . The same rule applies to CHx_EN.								
		0 Input channel d 1 (Default) Input d	ata is not propag channel data is p	ated to the inte ropagated to th	rnal data path e internal data pai	h				
1:0	XSP_RX_	XSP Rx channel n	size (in bits). Sets	s the output res	olution of the XSF	? Rx channel <i>n</i> san	nples.			
	CHn_RES	RES 00 8 bits per sample 10 (Default) 24 bits per sample 11 32 bits per sample								

# 7.4 DSD Registers

7.4.1	DSD V	/olume B					A	ddress 0x70000			
R/V	V 7	6	5	4	3	2	1	0			
DSD_VOLUME_B											
Defau	lt O	1	1	1	1	0	0	0			
Bits	Name		Description								
7:0	DSD_ VOLUME_B	Digital volume cont increments from 0 SZC bit. The same 0000 0000 0 dB 0000 0001 -0.5 0  01111000 -60 c  1111 1110 -127 1111 1111 Digita	rol registers for I dB. Volume settii condition applie dB IB (Default) dB al mute	DSD processor ch ngs are decoded s to DSD_VOLUN	nannel B. It allow as shown below. /IE_A setting.	s independent co The volume cha	ontrol of the signa	al level in 1/2 dB d by the DSD_			



Address 0x70001

Address 0x70002

### 7.4.2 DSD Volume A

R/	W 7	6	5	4	3	2	1	0	
	DSD_VOLUME_A								
Defa	ult O	1	1	1	1	0	0	0	
Bits	Name		Description						
7:0	DSD_ VOLUME_A	Digital volume control registers for channel A. See DSD_VOLUME_B for description.							

## 7.4.3 DSD Processor Path Signal Control 1

R/\	V 7	6	5	4	3	2	1	0	
	_	DSD_VOL_ BEQA	DSD_SZC	_	DSD_AMUTE	DSD_AMUTE_ BEQA	DSD_MUTE_A	DSD_MUTE_B	
Defau	ilt 1	0	1	0	1	0	0	0	
Bits	Name		Description						
7	—	Reserved							
6	DSD_VOL_	DSD_VOLUME_B	equals DSD_VO	LUME_A.					
	BEQA	0 (Default) Volur 1 Volume setting	<ul> <li>0 (Default) Volume setting of both channels in DSD processor are controlled independently</li> <li>1 Volume setting of both channels are controlled by DSD_VOLUME_A. DSD_VOLUME_B is ignored</li> </ul>						
5	DSD_SZC	Soft ramp control.							
		0 Immediate char 1 (Default) Soft ra	0 Immediate change 1 (Default) Soft ramp						
4	—	Reserved							
3	DSD_AMUTE	DSD auto mute.							
		0 Function disabl 1 (Default) Mute of pattern releases	<ul> <li>0 Function disabled</li> <li>1 (Default) Mute occurs after reception of 256 repeated 8-bit DSD mute patterns. A single bit not fitting the repeated pattern releases the mute. Detection and muting is done independently for each channel.</li> </ul>						
2	DSD_	DSD Processor Au	to mute channel	B equals channe	el A.				
	AMUTE_ BEQA	0 (Default) Functi 1 Only mute whe	on disabled n both channels	AMUTE condition	ns are detected				
1	DSD_MUTE_	DSD Processor Ch	annel A mute.						
	A	0 (Default) Functi 1 Channel output	on is disabled is muted. Muting	g function is affeo	cted by the DSD_	SZC bit			
0	DSD_MUTE_	DSD Processor Ch	annel B mute.						
	В	0 (Default) Functi 1 Channel output	on is disabled. is muted. Muting	g function is affeo	cted by the DSD_	SZC bit.			

## 7.4.4 DSD Interface Configuration

Address	0x70003

R/W	7	6	5	4	3	2	1	0
			_			DSD_M/SB	DSD_PM_EN	DSD_PM_SEL
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:3	—	Reserved
2	DSD_M/SB	DSD clock master or Slave Mode.
		0 (Default) Slave Mode 1 Master Mode
1	DSD_PM_EN	DSD phase modulation mode. Can only be used when DSD_SPEED = 0 (64•Fs).
		<ol> <li>(Default) this function is disabled (DSD normal mode)</li> <li>DSD phase modulation input mode is enabled, and the DSD_PM_SEL bit must be set accordingly.</li> </ol>
0	DSD_PM_SEL	DSD phase modulation mode select.
		0 (Default) The 128•Fs (BCKA) clock must be input to DSD_SCLK for phase modulation mode. 1 The 64•Fs (BCKD) clock must be input to DSD_SCLK for phase modulation mode.



7.4.5	DSD P	rocessor Pa	th Signal C	ontrol 2				Address 0x70004
R/V	V 7	6	5	4	3	2	1	0
	—	DSD_F	PRC_SRC	DSD_EN	_	DSD_SPEED	STA_DSD_DE	T INV_DSD_DET
Defau	lt O	0	0	0	0	0	1	0
Bits	Name				Description			
7	_	Reserved						
6:5	DSD_PRC_ SRC	Select the source 00 (Default) DSI 01 Reserved 10 ASP 11 XSP	for DSD process D interface	SOF.				
4	DSD_EN	Enable DSD playt 0 (Default) Func 1 DSD playback	back. tion disabled is enabled					
3	—	Reserved						
2	DSD_SPEED	Setup DSD clock : 0 (Default) 64•F 1 128•Fs	speed. s					
1	STA_DSD_ DET	Static DSD detecti 0 Function disat 1 (Default) Statio detected, sets	ion. bled c DSD detection the DSD_STUC	is enabled. The DS K INT interrupt sta	D processor tus bit and mi	checks for 28 cons utes the output unt	ecutive zeros c	or ones and, if dition is cleared.

- 0 (Default) Function disabled
   1 Invalid DSD detection is enabled. The DSD processor checks for 25 out of 28 bits of the same value and, if detected, sets the DSD\_INVAL\_A\_INT and/or DSD\_INVAL\_B\_INT interrupt status bits.

#### **DSD and PCM Mixing Control** 7.4.6

Invalid DSD detection.

INV\_DSD\_

DET

0

#### Address 0x70005

Address 0x70006

R/W	7	6	5	4	3	2	1	0
			-	_			MIX_PCM_ PREP	MIX_PCM_ DSD
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:2	—	Reserved
1	MIX_PCM_ PREP	Enable PCM playback path for PCM and DSD mixing. This bit must be set prior to setting MIX_PCM_DSD. Disable this bit after disabling MIX_PCM_DSD. This mode requires DSD_EN to be enabled and DSD_PRC_SRC set to receive DSD through either the DSD interface or XSP. 0 (Default) Function disabled 1 Enable PCM playback path for PCM and DSD mixing
0	MIX_PCM_ DSD	Enable PCM stream mixing into DSD stream. This bit must be set only after MIX_PCM_PREP is enabled. Disable this bit prior to disabling MIX_PCM_PREP bit. This mode requires DSD_EN to be enabled and DSD_PRC_SRC set to receive DSD through either the DSD interface or XSP. 0 (Default) Function disabled 1 Enable PCM stream mixing into the DSD stream

#### **DSD Processor Path Signal Control 3** 7.4.7

R/V	V 7	6	5	4	3	2	1	0
	DSD_ZEROI	DB DSD_HPF_EN	_	SIGCTL_ DSDEQPCM	DSD_INV_A	DSD_INV_B	DSD_SWAP_ CHAN	DSD_COPY_ CHAN
Defau	lt O	1	0	0	0	0	0	0
Bits	Name		Description					
7	DSD_ ZERODB	Setting on DSD stro 0 (Default) The S 1 The SACD 0-d	etting on DSD stream volume to match PCM stream volume. 0 (Default) The SACD +3.1-dB level (71% modulation index) matches PCM 0 dB full scale. 1 The SACD 0-dB reference level (50% modulation index) matches PCM 0 dB full scale.					
6 [	DSD_HPF_EN	Enable the high part 0 HPF disabled 1 (Default) Enable	ss filter in the DS e HPF in the DS	SD processor. D processor				


Bits	Name	Description
5	—	Reserved
4	SIGCTL_ DSDEQPCM	Enable DSD signal path control register bits to be controlled by PCM setting. DSD setting is ignored. Register bits affected are the following:
		DSD_VOL_BEQA, DSD_SZC, DSD_AMUTE, DSD_AMUTE_BEQA, DSD_MUTE_A, DSD_MUTE_B, DSD_INV_A, DSD_INV_B, DSD_SWAP_CHAN, DSD_COPY_CHAN
		After set, each DSD_x register bit is equal to setting of PCM_x register bit.
		0 (Default) Function is disabled 1 Function is enabled
3	DSD_INV_A	DSD Processor Channel A signal invert.
		0 (Default) Function is disabled 1 Signal polarity of channel A is inverted
2	DSD_INV_B	DSD Processor Channel B signal invert
		0 (Default) the function is disabled 1 Signal polarity of channel B is inverted
1	DSD_SWAP_	Swap channels A and B at the input. This bit takes effect before DSD_COPY_CHAN and DSD_INV_x.
	CHAN	1 Enable channel A and B swapping
0	DSD_COPY_ CHAN	Copy channel A to channel B. This bit takes effect after DSD_SWAP_CHAN, but before DSD_INV_x. 0 (Default) Function disabled 1 Enable copy A to B function

## 7.5 Headphone and PCM Registers

## 7.5.1 HP Output Control 1

Address 0x80000

Address 0x90000

R/W	7	6	5	4	3	2	1	0
	HP_CLAMPA	HP_CLAMPB	OU	T_FS	HP_IN_EN		—	
Default	0	0	1	1	0	0	0	0

-		
Bits	Name	Description
7	HP_CLAMPA	Opt-out on clamping HPOUTA output to ground when PDN_HP is enabled.
		<ul> <li>0 (Default) Function disabled. HPOUTA is clamped when PDN_HP is set and HP_IN_EN is cleared. HPOUT is not clamped when PDN_HP is cleared.</li> <li>1 HPOUTA clamp is released if and only if PDN_HP is set.</li> </ul>
6	HP_CLAMPB	Opt-out on clamping HPOUTB output to ground when PDN_HP is enabled.
		<ul> <li>0 (Default) Function disabled. HPOUTB is clamped when PDN_HP is set and HP_IN_EN is cleared. HPOUT is not clamped when PDN_HP is cleared.</li> <li>1 HPOUTB clamp is released if and only if PDN_HP is set.</li> </ul>
5:4	OUT_FS	Output full scale setting. This setting must only be updated when PDN_HP is set.
		00 0.5 V 01 1 V 10 1.41 V 11 (Default) 1.73 V
3	HP_IN_EN	HPIN switches enable.
		0 (Default) Switch open 1 Switch closed
2:0	_	Reserved

#### 7.5.2 PCM Filter Option

R/W	7	6	5	4	3	2	1	0
	FILTER_ SLOW_FAS	PHCOMP_ TB LOWLATB	NOS		_		HIGH_PASS	DEEMP_ON
Default	0	0	0	0	0	0	1	0
Bits	Name				Description			
7	FILTER_ SLOW_ FASTB	ast and slow filter selection. 0 (Default) Fast filter is selected. 1 Slow filter is selected.						



-		
Bits	Name	Description
6	PHCOMP_ LOWLATB	Low-latency and phase-compensated filter selection 0 (Default) Low-latency is selected. 1 Phase-compensated filter is selected.
5	NOS	Nonoversampling emulation mode on. When enabled, FILTER_SLOW_FASTB and PHCOMP_LOWLATB are ignored. 0 (Default) NOS emulation mode is off. 1 NOS emulation mode is on.
4:2	—	Reserved
1	HIGH_PASS	High-pass filter enable. 0 High-pass filter is disabled. 1 (Default) High-pass filter is selected.
0	DEEMP_ON	Deemphasis filter on. 0 (Default) Deemphasis for 44.1 kHz is disabled. 1 Deemphasis for 44.1 kHz is enabled.

#### 7.5.3 PCM Volume B

#### Address 0x90001

R/\	V 7	6	5	4	3	2	1	0
				PCM_VC	LUME_B			
Defau	lt O	1	1	1	1	0	0	0
Bits	Name				Description			
7:0	PCM_ VOLUME_B	Digital volume cont from 0 to -127 dB. bits. The same rule 0000 0000 0 dB 0000 0001 -0.5  01111000 -60 d  1111 1110 -127 1111 1111 Digita	trol registers for F Volume settings applies to PCM dB dB (Default) dB al mute	PCM channel B. It are decoded as VOLUME_A set	allows independ shown below. Th ting.	ent control of the e volume change	signal level in 1/ s are dictated by	2 dB increments / the PCM_SZC

#### 7.5.4 PCM Volume A

		•••••						
R/	W 7	6	5	4	3	2	1	0
				PCM_VO	LUME_A			
Defa	ult 0	1	1	1	1	0	0	0
Bits	Name		Description					
7:0	PCM_ VOLUME_A	Digital volume cont	igital volume control registers for channel A. See PCM_VOLUME_B for description.					

#### 7.5.5 PCM Path Signal Control 1

#### Address 0x90003

Address 0x90002

R/W	7	6	5	4	3	2	1	0
	PCM_RAMP_ DOWN	PCM_VOL_ BEQA	PCM	_SZC	PCM_AMUTE	PCM_ AMUTEBEQA	PCM_MUTE_A	PCM_MUTE_B
Default	1	0	1	0	1	0	0	0

Bits	Name	Description
7	PCM_RAMP_ DOWN	Soft volume ramp-down before filter mode change. A mute is performed before filter mode change and an unmute is performed after executing the filter mode change.
		<ul> <li>0 Immediate mute is performed prior to executing a filter mode change</li> <li>1 (Default) This mute and unmute is controlled by PCM_SZC.</li> </ul>
6	PCM_VOL_ BEQA	PCM_VOLUME_B equals PCM_VOLUME_A. 0 (Default) Volume setting of both channels are controlled independently. 1 Volume setting of both channels are controlled by PCM_VOLUME_A. PCM_VOLUME_B is ignored.
5:4	PCM_SZC	Soft ramp and zero cross control. 00 Immediate change 01 In PCM mode, zero cross change 10 (Default) Soft ramp 11 In PCM mode, soft ramp and zero crossings



Bits	Name	Description
3	PCM_AMUTE	PCM auto mute.
		0 Function disabled 1 (Default) Mute occurs after reception of 8,192 consecutive audio samples of static 0 or –1. A single sample of non-static data releases the mute. Detection and muting is done independently for each channel.
2	PCM_	Auto mute channel B equals channel A.
	AMUTEBEQA	0 (Default) Function disabled. 1 Only mute when both channels AMUTE conditions are detected.
1	PCM_MUTE_	Channel A mute.
	A	0 (Default) Function is disabled. 1 Channel output is muted. Muting function is affected by the PCM_SZC bits.
0	PCM_MUTE_	Channel A mute.
	В	0 (Default) Function is disabled. 1 Channel output is muted. Muting function is affected by the PCM_SZC bits.

## 7.5.6 PCM Path Signal Control 2

R/W	7	6	5	4	3	2	1	0
		_	_		PCM_INV_A	PCM_INV_B	PCM_SWAP_ CHAN	PCM_COPY_ CHAN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description			
7:4	_	Reserved			
3	PCM_INV_A	Channel A signal invert.			
		0 (Default) Function is disabled 1 Signal polarity of channel A is inverted			
2	PCM_INV_B Channel B signal invert.				
		0 (Default) the function is disabled 1 Signal polarity of channel B is inverted			
1	PCM_SWAP_	Swap channels A and B at the input. This bit takes effect before PCM_COPY_CHAN.			
	CHAN	0 (Default) Function disabled 1 Enable channel A and B swapping			
0	PCM_COPY_	Copy channel A to channel B. This bit takes effect after PCM_SWAP_CHAN.			
	CHAN	0 (Default) Function disabled 1 Enable copy A to B function			

### 7.5.7 Class H Control

#### Address 0xB0000

Address 0x90004

R/W	7	6	5	4	3	2	1	0
		—			ADPT_PWR	HV_EN	EXT_VCPFILT	
Default	0	0	0	1	1	1	1	0

Bits	Name	Description
7:5	—	Reserved
4:2	ADPT_PWR	Adaptive power adjustment. Configures how power to HP amplifiers adapts to the output signal level. 000 Reserved 001 Fixed, Mode 0 (±VP_LDO) 010 Fixed, Mode 1 (±VCP) 011–110 Reserved 111 (Default) Adapt to signal. The output signal dynamically determines the voltage level.
1	HV_EN	<ul> <li>High voltage mode enable.</li> <li>0 Function disabled (VP_LDO = 2.6V)</li> <li>1 (Default) Function enabled (VP_LDO = 3.0 V). This requires VP min to be 3.3 V. Also, this mode only applies to load 600 Ω and above.</li> </ul>
0	EXT_VCPFILT	<ul> <li>External VCP_FILT± voltage mode.</li> <li>0 (Default) Function disabled</li> <li>1 When enabled, VCP_FILT± voltages can be provided externally at ±3.0 V. See power sequencing/timing requirement in related functional description.</li> </ul>



#### 7.5.8 HP Detect

Address 0xD0000

R/V	V 7	6	5	4	3	2	1	0		
	HPDE	TECT_CTRL	HPDETECT_ INV	HPDETECT_R	ISE_DBC_TIME	HPDETECT_F	ALL_DBC_TIME	—		
Defau	Default 0 0 0 0 0 1 0									
Bits	Name				Description					
7:6	HPDETECT_ CTRL	HP detect control. ( all modes. 00 (Default) Disal (HPDETECT_	1P detect control. Configures operation of the HP detect circuit. The internal weak current source pull-up is enabled in all modes. 00 (Default) Disabled. The HP detect digital circuit is powered down and does not report to the status registers (HPDETECT_PLUG_INT and HPDETECT_UNPLUG_INT are also cleared)							
		01–10 Reserved 11 Enabled								
5	HPDETECT_ INV	HP detect invert. C 0 (Default) Not in 1 Inverted	an be used to inv verted	vert the signal fro	m the HP detect	circuit.				
4:3	HPDETECT_ RISE_DBC_ TIME	Tip sense rising del 00 (Default) 0 ms 01 250 ms 10 500 ms 11 1.0 s	sense rising debounce time. 0 (Default) 0 ms 1 250 ms 0 500 ms 1 1 0 s							
2:1	HPDETECT_ FALL_DBC_ TIME	Tip sense falling de 00 0 ms 01 250 ms 10 (Default) 500 n 11 1.0 s	sense falling debounce time. 0 0 ms 1 250 ms 0 (Default) 500 ms 1 1.0 s							
0	_	Reserved								

#### 7.5.9 HP Status

#### R/O 0 7 2 4 3 1 6 5 HPDETECT\_ PLUG\_DBC HPDETECT\_ UNPLUG\_DNC \_\_\_ \_\_\_ Default 0 0 0 0 0 0 0 0

	-	-
Bits	Name	Description
7	—	Reserved
6	HPDETECT_ PLUG_DBC	HPDETECT plug debounce status. Setting HPDETECT_INV reverses the meaning of this bit. 0 (Default) Condition is not present 1 Condition is present
5	HPDETECT_ UNPLUG_ DBC	HPDETECT unplug debounce status. Setting HPDETECT_INV reverses the meaning of this bit. 0 (Default) Condition is not present 1 Condition is present
4:0	—	Reserved

#### 7.5.10 HP Load 1

#### Address 0xE0000

Address 0xD0001

R/W	7	6	5	4	3	2	1	0
	HPLOAD_EN	-	_	HPLOAD_ CHN_SEL		_	HPLOAD_AC_ START	HPLOAD_DC_ START
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	HPLOAD_EN	HP load enable.
		0 (Default) Function disabled 1 Function enabled
6:5		Reserved
4	HPLOAD_ CHN_SEL	Select channel to perform HP load measurement. 0 (Default) HPOUTA 1 HPOUTB
3:2		Reserved



Bits	Name	Description
1	HPLOAD_AC_ START	HP load AC measurement trigger. A change from 0 to 1 initiates the measurement process. After the measurement completes, this bit must be manually changed back to 0 before initiating another process. (Default) HPLOAD_AC_START = 0
0	HPLOAD_ DC_START	HP load DC measurement trigger. A change from 0 to 1 initiates the measurement process. After measurement complete, this bit must be manually changed back to 0 before initiating another process. (Default) HPLOAD_DC_START = 0

#### 7.5.11 HP Load Measurement 1

Address 0	xE0003
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Address 0xE0004

Address 0xE000D

Address 0xE000E

R/\	N 7	6	5	4	3	2	1	0
				HPLOAD_MEA	S_FREQ_LSB			
Defau	ılt O	0	0	0	0	0	0	0
Bits Name Desc					Description			
7:0 HPLOAD LSB of HP load measurement frequency selection for AC detect (5.8					Hz/lsb when M	CLK_INT = 24.57	6 MHz. 5.94 Hz/	
	MEAS	Ish when MCLK_IN	T = 22 5792 MI	Hz) Érequency rai	nae is 20 Hz to 2	0 kHz	-	

#### 7.5.12 HP Load Measurement 2

Default: 0000 0000

FREQ\_LSB

R/	N 7	6	5	4	3	2	1	0
				HPLOAD_MEA	S_FREQ_MSB			
Default 0 0 0 0 0 0 0						0	0	
Bits	Name				Description			
7:0	HPLOAD_ MEAS_ FREQ_MSB	MSB of HP load me lsb when MCLK_IN Default: 0000 0000	easurement freq T = 22.5792 MH	uency selection fo Iz). Frequency rai	r AC detect (5.86 nge is 20 Hz to 20	Hz/Isb when MC ) kHz.	CLK_INT = 24.57	6 MHz. 5.94 Hz/

#### 7.5.13 HP DC Load Status 0

#### R/O 6 0 7 5 2 4 3 RL\_DC\_STAT\_0 0 0 0 0 0 0 0 0 Default Bits Name Description 7:0 RL DC Byte 0 of HP DC load measured in Ω.RL\_DC\_STAT\_1[7:0] and RL\_DC\_STAT\_0[7:3] represent integer portion of STAT\_0 impedance value. RL\_DC\_STAT\_0[2:0] represent fractional portion, with fractional weighting as follows: [2]: 0.5 11: 0.25 01: 0.125 Default: 0000000

#### 7.5.14 HP DC Load Status 1

R/C	R/O         7         6         5         4         3         2         1           RL_DC_STAT_1         RL_DC_STAT_1         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0 </th <th>0</th>			0				
				RL_DC_	STAT_1			
Default 0 0 0 0 0 0 0							0	0
Bits	Name				Description			
7:0	RL_DC_ STAT_1	Byte 1 of HP DC loa Default: 0000000	ad measured in <b>G</b>	2.Refer to RL_DC	C_STAT_0 for de	tails of measuren	nent interpretatio	n.



#### ~ \_

7.5.	15 HP AC	Load Status	<b>; 0</b>				A	ddress 0xE0010
R/	0 7	6	5	4	3	2	1	0
				RL_AC_	_STAT_0			
Defau	ult O	0	0	0	0	0	0	0
Bits	Name				Description			
7:0	RL_AC_ STAT_0	Byte 0 of HP AC lo RL_AC_STAT_1[7 RL_AC_STAT_0[2 [2]: 0.5 [1]: 0.25 [0]: 0.125 Default: 0000000	ad measured in :0] and RL_AC_3 :0] represent frac	Ω. STAT_0[7:3] repre	esent integer port	tion of impedance hting as follows:	e value.	
7.5.′	16 HP AC	Load Status	<b>; 1</b>				A	ddress 0xE0011
R/	0 7	6	5	4	3	2	1	0
				RL_AC_	_STAT_1			
Defau	ult O	0	0	0	0	0	0	0
Bits	Name				Description			
7:0	RL_AC_ STAT_1	Byte 1 of HP AC lo Default: 0000000	ad measured in	Ω.Refer to RL_A	C_STAT_0 for de	tails of measurer	nent interpretatio	on.
7.5.′	17 HP Lo	ad Status					A	ddress 0xE001 <i>A</i>
R/	0 7	6	5	4	3	2	1	0
	HPLOAD_DO	C_ HPLOAD_			HPLOAD_AC_	HPLOAD_AC_	HPLOAD_DC_	HPLOAD_DC_
Defai			0	0	DONE 0	0	DONE 0	0
Dite	Nama	-	-	-	Description	-		-
	Name		20		Description			
1	DC_ONCE	0 Condition is no 1 Condition is pr	ot present esent	it been performed	at least once.			
6	HPLOAD_ BUSY	Status of HP load 0 State machine 1 State machine	measurement blo is not busy is busy	ock state machine	l.			
5:4	_	Reserved						
3	HPLOAD_AC_ DONE	HP load AC mease 0 Condition is no 1 Condition is pr	urement is done ot present esent	status.				
2	HPLOAD_AC_ BUSY	HP AC load mease 0 Condition is no 1 Condition is pr	urement is "in pro ot present esent	ocess" status.				
1	HPLOAD_ DC_DONE	HP load DC mease 0 Condition is no 1 Condition is pr	urement is done ot present esent	status.				
0	HPLOAD_ DC_BUSY	HP DC load meas 0 Condition is no 1 Condition is pr	urement is "in pro ot present esent	ocess" status.				



Address 0xF0000

# 7.6 Interrupt Status and Mask Registers

### 7.6.1 Interrupt Status 1

-	<u>_</u>	•			I				
R/	0 7	6	5	4	3	2	1	0	
	DAC_OVFL	_ HPDETECT_	HPDETECT_	XTAL_READY_	XTAL_	PLL_READY_	PLL_ERROR_	PDN_DONE_	
	INI	PLUG_IN1	UNPLUG_INT	INI	ERROR_INT	INI	INI	INI	
Defau	ult O	0	0	0	0	0	0	0	
Bits	Name				Description				
7	DAC_OVFL_	Status indicating D	AC modulator ov	erflow condition i	s detected.				
	INT	0 Condition is no 1 Condition is pre	t present esent						
6	HPDETECT_	Status indicating H	P plug event is d	etected.					
	PLUG_INT	0 Condition is no 1 Condition is pre	t present esent						
5	HPDETECT_	Status indicating H	P unplug event is	s detected.					
	UNPLUG_INT	0 Condition is no 1 Condition is pre	t present esent						
4	XTAL_	Status indicating X	TAL is ready afte	r PDN_XTAL is c	leared.				
	READY_INT	0 Condition is no 1 Condition is pre	t present esent						
3	XTAL_	Status indicating X	TAL error condition	on is detected aft	er PDN_XTAL is	cleared.			
	ERROR_INT	0 Condition is no 1 Condition is pre	t present esent						
2	PLL_READY_	Status indicating P	LL ready condition	on is detected after	er PLL_START is	set.			
	INI	0 Condition is no 1 Condition is pre	0 Condition is not present 1 Condition is present						
1	PLL_ERROR_	Status indicating PLL error condition is detected after PLL_START is set.							
	INT	0 Condition is no 1 Condition is pre	0 Condition is not present 1 Condition is present						
0	PDN_DONE_	Status indicating P	DN_HP process	is completed afte	r a request.				
	INT	INT 0 Condition is not present 1 Condition is present							

#### 7.6.2 Interrupt Status 2

#### Address 0xF0001

R/O	7	6	5	4	3	2	1	0
	ASP_OVFL_ INT	ASP_ERROR_ INT	ASP_LATE_ INT	ASP_EARLY_ INT	ASP_ NOLRCK_INT		_	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	ASP_OVFL_ INT	ASP RX request overload. 0 Condition is not present 1 Condition is present
6	ASP_ ERROR_INT	ASP RX LRCK error. Logical OR of LRCK early and LRCK late errors. 0 Condition is not present 1 Condition is present
5	ASP_LATE_ INT	ASP RX LRCK late. 0 Condition is not present 1 Condition is present
4	ASP_EARLY_ INT	ASP RX LRCK early. 0 Condition is not present 1 Condition is present
3	ASP_ NOLRCK_INT	ASP RX no LRCK. 0 Condition is not present 1 Condition is present
2:0	—	Reserved



#### 7.6.3 Interrupt Status 3

Address 0xF0002

Address 0xF0003

R/0	7 C	6	5	4	3	2	1	0	
	XSP_OVFL INT	_ XSP_ERROR_ INT	XSP_LATE_ INT	XSP_EARLY_ INT	XSP_ NOLRCK_INT		_		
Defau	lt 0	0	0	0	0	0	0	0	
Bits	Name				Description				
7	XSP_OVFL_ INT	XSP RX request ov 0 Condition is no 1 Condition is pre	SP RX request overload. 0 Condition is not present 1 Condition is present						
6	XSP_ ERROR_INT	XSP RX LRCK error 0 Condition is no 1 Condition is pre	SP RX LRCK error. Logical OR of LRCK early and LRCK late errors. 0 Condition is not present 1 Condition is present						
5	XSP_LATE_ INT	XSP RX LRCK late 0 Condition is no 1 Condition is pre	e. t present esent						

		r Condition is present
4	XSP_EARLY_ INT	XSP RX LRCK early. 0 Condition is not present 1 Condition is present
3	XSP_ NOLRCK_INT	XSP RX no LRCK. 0 Condition is not present 1 Condition is present
2:0	—	Reserved

### 7.6.4 Interrupt Status 4

		•						
R/	0 7	6	5	4	3	2	1	0
	HPLOAD_N DC_INT	O_ HPLOAD_ UNPLUG_INT		HPLOAD_ OOR_INT	HPLOAD_AC_ DONE_INT	HPLOAD_DC_ DONE_INT	HPLOAD_ OFF_INT	HPLOAD_ON_ INT
Defa	ult O	0	0	0	0	0	0	0
Bits	Name				Description			
7	HPLOAD_ NO_DC_INT	HP load error cond 0 Condition is not	ition: AC load de	tection is perform	ned without DC Ic	ad detection don	e first.	

	NO_DC_INT	0 Condition is not present 1 Condition is present
6	HPLOAD_ UNPLUG_INT	HP load error condition: Unplug event happened during load detection process. 0 Condition is not present 1 Condition is present
5	—	Reserved
4	HPLOAD_ OOR_INT	HP load error condition: HPLOAD out of range result is measured. 0 Condition is not present 1 Condition is present
3	HPLOAD_AC_ DONE_INT	Status indicating HP AC load measurement is completed. 0 Condition is not present 1 Condition is present
2	HPLOAD_ DC_DONE_ INT	Status indicating HP DC load measurement is completed. 0 Condition is not present 1 Condition is present
1	HPLOAD_ OFF_INT	HP load state machine is properly shut down after HPLOAD_EN is cleared. 0 Condition is not present 1 Condition is present
0	HPLOAD_ ON_INT	HP load state machine is properly turned on after HPLOAD_EN is set. 0 Condition is not present 1 Condition is present



Address 0xF0004

Address 0xF0010

#### 7.6.5 Interrupt Status 5

R/	0 7	6	5	4	3	2	1	0	
	DSD_STUCI INT	K_ DSD_INVAL_ A_INT	DSD_INVAL_ B_INT	DSD_ SILENCE_A_ INT	DSD_ SILENCE_B_ INT	DSD_RATE_ ERROR_INT	DOP_MRK_ DET_INT	DOP_ON_INT	
Defau	ılt O	0	0	0	0	0	0	0	
Bits	Name				Description				
7	DSD_STUCK_ INT	At least one DSD i 0 Condition is no 1 Condition is pro	nput channel is s t present esent	tuck at 0 or 1.					
6	DSD_INVAL_ A_INT	Channel A input ex 0 Condition is no 1 Condition is pre	ceeds the max p t present esent	eak level of +3.1	-dB SACD.				
5	DSD_INVAL_ B_INT	Channel B input ex 0 Condition is no 1 Condition is pre	hannel B input exceeds the max peak level of +3.1-dB SACD. 0 Condition is not present 1 Condition is present						
4	DSD_ SILENCE_A_ INT	Channel A contain 0 Condition is no 1 Condition is pre	s DSD silence pa t present esent	ttern.					
3	DSD_ SILENCE_B_ INT	Channel B contains 0 Condition is no 1 Condition is pre	s DSD silence pa t present esent	ttern.					
2	DSD_RATE_ ERROR_INT	DSD data rate-rela 0 Condition is no 1 Condition is pre	SD data rate-related error is detected. The rate of the input DSD stream is not as described in DSD_SPEED setting. 0 Condition is not present 1 Condition is present						
1	DOP_MRK_ DET_INT	A valid sequence of 0 Condition is no 1 Condition is pre-	of DoP markers h t present esent	as been detected	1.				
0	DOP_ON_INT	The DoP decoder i 0 Condition is no 1 Condition is pre	is powered up. t present esent						

## 7.6.6 Interrupt Mask 1

R/W	7	6	5	4	3	2	1	0
	DAC_OVFL_ INT_MASK	HPDETECT_ PLUG_INT_ MASK	HPDETECT_ UNPLUG_INT_ MASK	XTAL_READY_ INT_MASK	XTAL_ ERROR_INT_ MASK	PLL_READY_ INT_MASK	PLL_ERROR_ INT_MASK	PDN_DONE_ INT_MASK
Default	1	1	1	1	1	1	1	1

Bits	Name	Description
7	DAC_OVFL_ INT_MASK	DAC_OVFL_INT mask. 0 Unmasked 1 (Default) Masked
6	HPDETECT_ PLUG_INT_ MASK	HP_DETECT_PLUG_INT mask. 0 Unmasked 1 (Default) Masked
5	HPDETECT_ UNPLUG_ INT_MASK	HP_DETECT_UNPLUG_INT mask. 0 Unmasked 1 (Default) Masked
4	XTAL_ READY_INT_ MASK	XTAL_READY_INT mask. 0 Unmasked 1 (Default) Masked
3	XTAL_ ERROR_INT_ MASK	XTAL_ERROR_INT mask. 0 Unmasked 1 (Default) Masked
2	PLL_READY_ INT_MASK	PLL_READY_INT mask. 0 Unmasked 1 (Default) Masked



Bits	Name	Description
1	PLL_ERROR_ INT_MASK	PLL_ERROR_INT mask. 0 Unmasked 1 (Default) Masked
0	PDN_DONE_ INT_MASK	PDN_DONE_INT mask. 0 Unmasked 1 (Default) Masked

### 7.6.7 Interrupt Mask 2

#### Address 0xF0011

R/W	7	6	5	4	3	2	1	0
	ASP_OVFL_ INT_MASK	ASP_ERROR_ INT_MASK	ASP_LATE_ INT_MASK	ASP_EARLY_ INT_MASK	ASP_ NOLRCK_INT_ MASK		_	
Default	1	1	1	1	1	1	1	1

Bits	Name	Description
7	ASP_OVFL_	ASP_OVFL_INT mask.
		1 (Default) Masked
6	ASP_	ASP_ERROR_INT mask.
	ERROR_INT_ MASK	0 Unmasked 1 (Default) Masked
5	ASP_LATE_	ASP_LATE_INT mask.
	INT_MASK	0 Unmasked 1 (Default) Masked
4	ASP_EARLY_	ASP_EARLY_INT mask.
	INT_MASK	0 Unmasked 1 (Default) Masked
3	ASP_	ASP_NOLRCK_INT mask.
	NOLRCK_ INT_MASK	0 Unmasked 1 (Default) Masked
2:0		Reserved

#### 7.6.8 Interrupt Mask 3

### Address 0xF0012

R/W	7	6	5	4	3	2	1	0
	XSP_OVFL_ INT_MASK	XSP_ERROR_ INT_MASK	XSP_LATE_ INT_MASK	XSP_EARLY_ INT_MASK	XSP_ NOLRCK_INT_ MASK		_	
Default	1	1	1	1	1	0	0	0

Bits	Name	Description
7	XSP_OVFL_ INT_MASK	XSP_OVFL_INT mask. 0 Unmasked
		1 (Default) Masked
6	XSP_ ERROR_INT_ MASK	XSP_ERROR_INT mask. 0 Unmasked 1 (Default) Masked
5	XSP_LATE_ INT_MASK	XSP_LATE_INT mask. 0 Unmasked 1 (Default) Masked
4	XSP_EARLY_ INT_MASK	XSP_EARLY_INT mask. 0 Unmasked 1 (Default) Masked
3	XSP_ NOLRCK_ INT_MASK	XSP_NOLRCK_INT mask. 0 Unmasked 1 (Default) Masked
2:0		Reserved



#### CS43130 7.6 Interrupt Status and Mask Registers

Address 0xF0013

#### 7.6.9 Interrupt Mask 4

R/\	N 7	6	5	4	3	2	1	0
	HPLOAD_NO	DUNPLUG_INT SKMASK	_	HPLOAD_ OOR_INT_ MASK	HPLOAD_AC_ DONE_INT_ MASK	HPLOAD_DC_ DONE_INT_ MASK	HPLOAD_ OFF_INT_ MASK	HPLOAD_ON_ INT_MASK
Defau	ılt 1	1	1	1	1	1	1	1
Bits	Name				Description			
7	HPLOAD_ NO_DC_INT_ MASK	HPLOAD_NO_DC_ 0 Unmasked 1 (Default) Maske	INT mask. ed					
6	HPLOAD_	HPLOAD_UNPLUC	_INT mask.					
	UNPLUG_ INT_MASK	0 Unmasked 1 (Default) Maske	ed					
5	—	Reserved						
4	HPLOAD_	HPLOAD_OOR_IN	T mask.					
	MASK	0 Unmasked 1 (Default) Maske	ed					
3	HPLOAD_AC_	HPLOAD_AC_DOM	IE_INT mask.					
	MASK	0 Unmasked 1 (Default) Maske	ed					
2	HPLOAD_	HPLOAD_DC_DOM	IE_INT mask.					
	INT_MASK	0 Unmasked 1 (Default) Maske	ed					
1	HPLOAD_	HPLOAD_OFF_IN	⊺mask.					
	MASK	0 Unmasked 1 (Default) Maske	ed					
0	HPLOAD_	HPLOAD_ON_INT	mask.					
	MASK	0 Unmasked 1 (Default) Maske	ed					



#### CS43130 7.6 Interrupt Status and Mask Registers

Address 0xF0014

#### 7.6.10 Interrupt Mask 5

R/W	V 7 6 5		4	3	2	1	0	
	DSD_STUCK_ INT_MASK	DSD_INVAL_ A_INT_MASK	DSD_INVAL_ B_INT_MASK	DSD_ SILENCE_A_ INT_MASK	DSD_ SILENCE_B_ INT_MASK	DSD_RATE_ ERROR_INT_ MASK	DOP_MRK_ DET_INT_ MASK	DOP_ON_INT_ MASK
Default	1	1	1	1	1	1	1	1

	•	· ·
Bits	Name	Description
7	DSD_STUCK_ INT_MASK	DSD_STUCK_INT mask. 0 Unmasked 1 (Default) Masked
6	DSD_INVAL_ A_INT_MASK	DSD_INVAL_A_INT mask. 0 Unmasked 1 (Default) Masked
5	DSD_INVAL_ B_INT_MASK	DSD_INVAL_B_INT mask. 0 Unmasked 1 (Default) Masked
4	DSD_ SILENCE_A_ INT_MASK	DSD_SILENCE_A_INT mask. 0 Unmasked 1 (Default) Masked
3	DSD_ SILENCE_B_ INT_MASK	DSD_SILENCE_B_INT mask. 0 Unmasked 1 (Default) Masked
2	DSD_RATE_ ERROR_INT_ MASK	DSD_RATE_ERROR_INT mask. 0 Unmasked 1 (Default) Masked
1	DOP_MRK_ DET_INT_ MASK	DOP_MRK_DET_INT mask. 0 Unmasked 1 (Default) Masked
0	DOP_ON_ INT_MASK	DOP_ON_INT mask. 0 Unmasked 1 (Default) Masked



### 8 PCB Layout Considerations

The following sections provide general guidelines for PCB layout to ensure the best performance of the CS43130.

#### 8.1 Power Supply

As with any high-resolution converter, the CS43130 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Fig. 2-1 shows the recommended power arrangements with VA and VCP connected to independent clean supplies. VL and VD, which power the digital circuitry, may be run from the shared system logic supply.

#### 8.2 Grounding

Note the following:

- Extensive use of power and ground planes, ground-plane fill in unused areas, and surface-mount decoupling capacitors are recommended.
- Decoupling capacitors must be as close as possible to the CS43130 pins.
- To minimize inductance effects, the low-value ceramic capacitor must be closest to the pin and mounted on the same side of the board as the CS43130.
- To avoid unwanted coupling into the modulators, all signals, especially clocks, must be isolated from the FILT+ and FILT- pins.
- The FILT+ capacitors must be positioned to minimize the electrical path from the pin to VA.
- The FILT– capacitors must be positioned to minimize the electrical path from the pin to –VA.
- The VCP\_FILT+ and VCP\_FILT- capacitors must be positioned to minimize the electrical path from each respective pin to GNDCP.

#### 8.3 HPREFA and HPREFB Routing

For best interchannel isolation performance, HPREFA and HPREFB must be routed independently to the headphone connector reference pin. The HPREFA and HPREFB are electrically connected to system's ground plane through via at the headphone connector ground pin. Fig. 2-1 illustrates the recommended arrangements.

For interfacing the HPREFA and HPREFB pins with an IC that performs alternate pinout headset detect functions, both signals must be routed independently to the CS43130's ground pin connecting the detected headset ground pole. Follow the recommended grounding scheme of the CS43130.

### 8.4 QFN Thermal Pad

The CS43130 comes in a compact QFN package, the underside of which reveals a large metal pad that serves as a thermal relief to provide maximum heat dissipation. This pad must mate with an matching copper pad on the PCB and must be electrically connected to ground. A series of vias must be used to connect this copper pad to one or more larger ground planes on other PCB layers. For best performance in split-ground systems, connect this thermal pad to GNDA.



#### **Performance Plots** 9

#### **Digital Filter Response** 9.1



9.1.1 Combined Filter Response—Single Speed (Fs = 32 kHz, Slow Roll-Off)



### 9.1.2 Combined Filter Response—Single Speed (Fs = 32 kHz, Fast Roll-Off)





### 9.1.3 Combined Filter Response—Single Speed (Fs = 44.1 and 48 kHz, Slow Roll-Off)





### 9.1.4 Combined Filter Response—Single Speed (Fs = 44.1 and 48 kHz, Fast Roll-Off)





### 9.1.5 Combined Filter Response—Double Speed (Slow Roll-Off)





### 9.1.6 Combined Filter Response—Double Speed (Fast Roll-Off)





### 9.1.7 Combined Filter Response—Quad Speed (Slow Roll-Off)





## 9.1.8 Combined Filter Response—Quad Speed (Fast Roll-Off)





#### 9.1.9 Combined Filter Response—Octuple Speed



9.1.10 Combined Filter Response—Single Speed (NOS = 1)

Note: 44.1 kHz and 48 kHz only.







9.1.11 Combined Filter Response—Double Speed (NOS = 1)





### 9.1.12 Combined Filter Response—Quad Speed (NOS = 1)











Figure 9-69. High-pass Filter for PCM and DSD Paths





## **10 Package Dimensions**

### 10.1 40-Pin QFN Package Dimensions



#### Figure 10-1. 40-Pin QFN Package Drawing

#### Table 10-1. 40-Pin QFN Package Dimensions

Description		<b>D</b> '		Millimeters				
		DIM	Minimum	Nominal	Maximum			
Total thickness		A	0.7	0.75	0.8			
Stand off		A1	0	0.035	0.05			
Mold thickness		A2	—	0.55	—			
L/F thickness		A3		0.203 REF				
Lead width		b	0.15	0.2	0.25			
Body size X		D	5 BSC					
	Y	E	5 BSC					
Lead pitch		е	0.4 BSC					
EP size	Х	J	3.4	3.5	3.6			
	Y	K	3.4	3.5	3.6			
Lead length		L	0.35	0.4	0.45			
Package edge tolerand	ce	aaa	0.1					
Mold flatness		bbb		0.1				
Coplanarity		CCC		0.08				
Lead offset		ddd		0.1				
Exposed pad offset		eee		0.1				

Notes:

• Dimensioning and tolerances per ASME Y 14.5M–1995.

• X/Y Dimensions are estimates.

- The Ball 1 location indicator shown above is for illustration purposes only and may not be to scale.
- Dimensioning and tolerances per ASME Y 14.5M–1994.
- Dimension "b" applies to the solder sphere diameter and is measured at the midpoint between the package body and the seating plane.



### 10.2 42-Ball WLCSP Package Dimensions



#### Notes:

- Controlling dimensions are in millimeters.
- Dimensioning and tolerances per ASME Y 14.5M-1994.
- The Ball A1 position indicator is for illustration purposes only and may not be to scale.
- Dimension "b" applies to the solder sphere diameter and is measured at the midpoint between the package body and the seating plane datum Z.
- Dimension A3 describes the thickness of the backside film.

#### Figure 10-2. 42-Ball WLCSP Package Drawing

Table 10-2.	42-Ball WL	CSP Package	Dimensions
-------------	------------	-------------	------------

Dimonsion		Millimeters	
Dimension	Minimum	Nominal	Maximum
A	0.461	0.491	0.521
A1	0.175	0.190	0.205
A2	0.286	0.301	0.316
A3	—	0.022	_
М	—	2.000	—
N	—	2.400	_
b	0.220	0.270	0.320
С	—	0.354	—
d	—	0.391	_
е	—	0.400	_
Х	—	2.707	—
Y	—	3.181	—

Notes: X/Y dimensions are estimates.

• Unless otherwise specified, tolerances are: Linear ±0.05 mm, Angular ±1 deg



### **11 Thermal Characteristics**

Table 11.1	Typical JEDEC Four L	war 2c2n Board	Thormal Charactoric	tice
	Typical JEDEC Foul-La	ayei, zszp buaiu	Thermal Characteris	lics

Parameter	Symbol	WLCSP	QFN	Units
Junction-to-ambient thermal resistance	$\theta_{JA}$	42.3	32.7	°C/W
Junction-to-board thermal resistance	$\theta_{JB}$	11.1	8.8	°C/W
Junction-to-case thermal resistance	θJC	0.22	0.92	°C/W
Junction-to-board thermal-characterization parameter	$\Psi_{JB}$	11.0	8.8	°C/W
Junction-to-package-top thermal-characterization parameter	$\Psi_{JT}$	0.09	0.23	°C/W

#### Notes:

• Natural convection at the maximum recommended operating temperature T<sub>A</sub> (see Table 3-2)

• Four-layer, 2s2p PCB as specified by JESD51-9 and JESD51-11; dimensions: 101.5 x 114.5 x 1.6 mm

• Thermal parameters as defined by JESD51-12

# 12 Ordering Information

#### Table 12-1. Ordering Information

Product	Description	Package	Halogen Free	Pb Free	Grade	Temperature Range	Container	Order Number
CS43130	CS43130 130-dB, 32-Bit High-Performance DAC	42-ball WLCSP	Yes	Yes	Commercial	–10°C to +70°C	Tape and Reel	CS43130-CWZR
	with Integrated Headphone Driver and Impedance Detection	40-pin QFN	Yes	Yes	Commercial	–10°C to +70°C	Tray Tape and Reel	CS43130-CNZ CS43130-CNZR

### **13 References**

• NXP Semiconductors, The I<sup>2</sup>C-Bus Specification and User Manual (UM10204). http://www.nxp.com/

# 14 Revision History

#### Table 14-1. Revision History

Revision	Changes
F1	Initial release
DEC '16	

**Important**: Please check with your Cirrus Logic sales representative to confirm that you are using the latest revision of this document and to determine whether there are errata associated with this device.



#### **Contacting Cirrus Logic Support**

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