

General Description

The MAX16008/MAX16009 are adjustable quad window voltage detectors in a small thin QFN package. These devices are designed to provide a higher level of system reliability by monitoring multiple supply voltages and providing a fault signal when any of the voltages exceed their overvoltage thresholds or fall below their undervoltage thresholds.

These devices offer user-adjustable thresholds that allow voltages to be monitored down to 0.4V. These devices allow the upper and lower trip thresholds of each window detector to be set externally with the use of three external resistors.

Each monitored threshold has an independent opendrain output for signaling a fault condition. The outputs can be wire OR'ed together to provide a single fault output. The open-drain outputs are internally pulled up with a 30µA current, but can be externally driven to other voltage levels for interfacing to other logic levels.

Both devices feature a margin input to disable the outputs during margin testing or any other time after power-up operations. The MAX16009 offers a reset output that deasserts after a reset timeout period after all voltages are within their threshold specifications. The reset timeout is internally set to 140ms (min), but can be externally adjusted to other reset timeouts using an external capacitor. In addition, the MAX16009 offers a manual reset input.

All devices are offered in a 4mm x 4mm TQFN package and are fully specified from -40°C to +125°C.

Applications

Storage Equipment Networking/Telecommunications Equipment Multivoltage ASICs Servers

Features

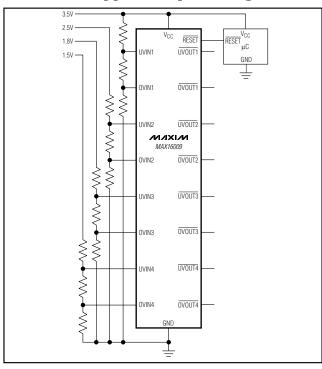
- ♦ Monitor Four Undervoltage/Overvoltage Conditions
- **♦** 1.5% Accuracy Over Temperature
- ♦ User-Adjustable Thresholds (Down to 0.4V)
- ♦ Open-Drain Outputs with Internal Pullups Reduce the Number of External Components
- ♦ Manual Reset Input (MAX16009)
- ♦ Margin Enable Input
- ♦ Fixed or Adjustable RESET Timeout (MAX16009)
- ♦ Guaranteed Correct Output Logic State Down to Vcc = 1V
- ♦ Fully Specified from -40°C to +125°C
- ♦ Small, 4mm x 4mm TQFN Package

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX16008TP+	-40°C to +125°C	20 TQFN
MAX16009TG+	-40°C to +125°C	24 TQFN

+Denotes a lead(Pb)-free/RoHS-compliant package. For tape-and-reel, add a "T" after the "+." Tape-and-reel are offered in 2.5k increments.

Typical Operating Circuit



Pin Configurations and Selector Guide appear at end of data sheet.

Maxim Integrated Products 1

ABSOLUTE MAXIMUM RATINGS

V _{CC} , OVOUT_, UVOUT_, RESET,	Оре
UVIN_, OVIN_ to GND0.3V to +6V	Jun
$\overline{\text{MARGIN}}$, $\overline{\text{MR}}$, TOL, SRT to GND0.3V to (V _{CC} + 0.3V)	Stor
Input/Output Current	Lea
(RESET, MARGIN, SRT, MR, UVOUT_, OVOUT_)±20mA	Solo
Continuous Power Dissipation ($T_A = +70^{\circ}C$)	
20-Pin Thin QFN (derate 16.9mW/°C above +70°C) 1355mW	
24-Pin Thin QFN (derate 16.9mW/°C above +70°C)1666mW	

Operating Temperature Range	40°C to +125°C
Junction Temperature	+150°C
Storage Temperature Range	65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow)	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

 $(V_{CC} = 2.0 \text{V to } 5.5 \text{V}, \text{ TOL} = \text{GND}, \text{ T}_{A} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}, \text{ unless otherwise specified. Typical values are at } V_{CC} = 3.3 \text{V}, \text{ T}_{A} = +25 ^{\circ}\text{C}.)$ (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Operating Voltage Range	V _{CC}	(Note 2)	1.0		5.5	V	
Cupply Current (Note 2)	la a	V _{CC} = 3.3V, outputs deasserted		45	65		
Supply Current (Note 3)	Range		45	70	μΑ		
UVLO (Undervoltage Lockout)	Vuvlo	V _{CC} rising	1.62	1.8	1.98	V	
UVIN_/OVIN_							
Adjustable Threshold (UVIN_ Falling/OVIN_ Rising)	V _{TH}		0.388	0.394	0.400	V	
UVIN_/OVIN_ Hysteresis	V _{TH} _HYS	_	ercentage of 0.5			% V _{TH}	
UVIN_/OVIN_ Input Current	I _{IB}		-100		+100	nA	
RESET							
		SRT = V _{CC}	140	200	280		
Reset Timeout	too	C _{SRT} = 1500pF (Note 4)	2.43	3.09	3.92	1	
Reset Timeout	IRP	C _{SRT} = 100pF	0.206		ms		
		C _{SRT} = open		0.05			
SRT Ramp Current I _{SRT} V _{SRT} = 0V		V _{SRT} = 0V	460	600	740	nA	
SRT Threshold V _{TH_SRT}		1.173	1.235	1.293	V		
SRT Hysteresis				100		mV	
UVIN_/OVIN_ to Reset Delay	t _{RD}	UVIN_ falling/OVIN_ rising		20		μs	

ELECTRICAL CHARACTERISTICS (continued)

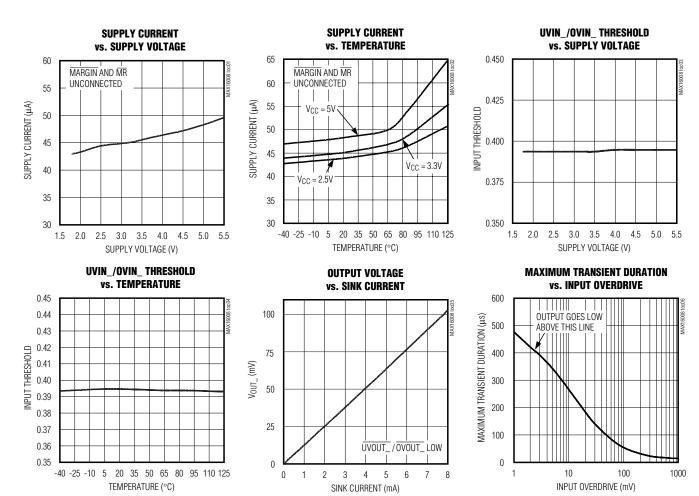
 $(V_{CC} = 2.0V \text{ to } 5.5V, TOL = GND, T_A = -40^{\circ}C \text{ to } +125^{\circ}C, \text{ unless otherwise specified. Typical values are at } V_{CC} = 3.3V, T_A = +25^{\circ}C.)$ (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		V _{CC} = 3.3V, I _{SINK} = 10mA, RESET asserted			0.30	
RESET Output-Voltage Low	VoL	V _{CC} = 2.5V, I _{SINK} = 6mA, RESET asserted			0.30	V
		V _{CC} = 1.2V, I _{SINK} = 50μA, RESET asserted			0.30	
RESET Output-Voltage High	Voh	V _{CC} ≥ 2.0V, I _{SOURCE} = 6µA, RESET deasserted	0.8 x V _C C			V
MR Input-Voltage Low	V _{IL}				0.3 x V _C C	V
MR Input-Voltage High	VIH		0.7 x V _{CC}			V
MR Minimum Pulse Width			1			μs
MR Glitch Rejection				100		ns
MR to RESET Delay				200		ns
MR Pullup Resistance			12	20	28	kΩ
OUTPUTS (UVOUT_/OVOUT_)	,		1			
UVOUT_, OVOUT_ Output- Voltage Low	V _{OL}	$V_{CC} = 3.3V$, $I_{SINK} = 2mA$ $V_{CC} = 2.5V$, $I_{SINK} = 1.2mA$			0.30	V
OVOUT_, OVOUT_ Output- Voltage High	Voh	V _{CC} ≥ 2.0V, I _{SOURCE} = 6µA	0.8 x V _{CC}			V
UVIN_/OVIN_ to UVOUT_/ OVOUT_ Propagation Delay	t _D	(V _{TH} - 100mV) to (V _{TH} + 100mV)		20		μs
DIGITAL LOGIC						
TOL Input-Voltage Low	V _{IL}				0.3 x V _C C	V
TOL Input-Voltage High	VIH		0.7 x V _C C			V
TOL Input Current		TOL = VCC			100	nA
MARGIN Input-Voltage Low	VIL				0.3 x V _C C	V
MARGIN Input-Voltage High	VIH		0.7 x V _C C	_	_	V
MARGIN Pullup Resistance		Pulled up to V _{CC}	12	20	28	kΩ
MARGIN Delay Time	t _{MD}	Rising or falling (Note 5)		50		μs

- Note 1: Devices are tested at $T_A = +25^{\circ}C$ and guaranteed by design for $T_A = T_{MIN}$ to T_{MAX} .
- **Note 2:** The outputs are guaranteed to be in the correct logic state down to $V_{CC} = 1V$.
- Note 3: Measured with MR and MARGIN unconnected.
- **Note 4:** The minimum and maximum specifications for this parameter are guaranteed by using the worse case of the SRT current and SRT threshold specifications. Do not set the reset timeout period to more than 1.12s.
- Note 5: Amount of time required for logic to lock/unlock outputs from margin testing

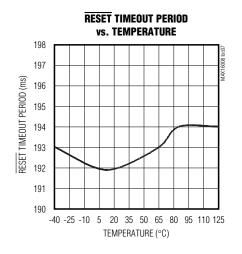
Typical Operating Characteristics

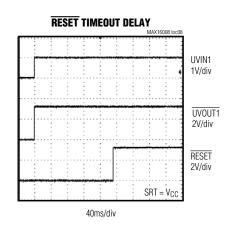
($V_{CC} = 3.3V$, $T_A = +25$ °C, unless otherwise noted.)

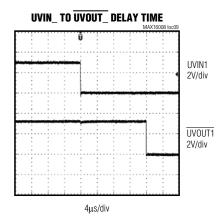


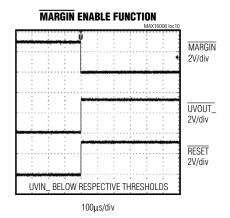
Typical Operating Characteristics (continued)

 $(V_{CC} = 3.3V, T_A = +25^{\circ}C, unless otherwise noted.)$









Pin Description

PI	N		
MAX16008	MAX16009	NAME	FUNCTION
1	1	UVIN3	Undervoltage Threshold Input 3. When the voltage on UVIN3 falls below its threshold, UVOUT3 asserts low.
2	2	OVIN3	Overvoltage Threshold Input 3. When the voltage on OVIN3 rises above its threshold, OVOUT3 asserts low.
3	3	UVIN4	Undervoltage Threshold Input 4. When the voltage on UVIN4 falls below its threshold, UVOUT4 asserts low.
4	4	OVIN4	Overvoltage Threshold Input 4. When the voltage on OVIN4 rises above its threshold, OVOUT4 asserts low.
5	6	GND	Ground
6, 20	7, 24	Vcc	Unmonitored Power to the Device
7	8	ŪVOUT3	Active-Low Undervoltage Output 3. When the voltage at UVIN3 falls below its threshold, UVOUT3 asserts low and stays asserted until the voltage at UVIN3 exceeds its threshold. The open-drain output has a 30µA internal pullup to VCC.
8	9	OVOUT3	Active-Low Overvoltage Output 3. When the voltage at OVIN3 rises above its threshold, $\overline{\text{OVOUT3}}$ asserts low and stays asserted until the voltage at OVIN3 falls below its threshold. The open-drain output has a 30µA internal pullup to VCC.
9	10	ŪVOUT4	Active-Low Undervoltage Output 4. When the voltage at UVIN4 falls below its threshold, UVOUT4 asserts low and stays asserted until the voltage at UVIN4 exceeds its threshold. The open-drain output has a 30µA internal pullup to VCC.
10	11	OVOUT4	Active-Low Overvoltage Output 4. When the voltage at OVIN4 rises above its threshold, OVOUT4 asserts low and stays asserted until the voltage at OVIN4 falls below its threshold. The open-drain output has a 30µA internal pullup to VCC.
11	14	MARGIN	Active-Low Margin Enable Input. Pull MARGIN low to deassert all outputs (go into high state) regardless of the voltage at any monitored input.
12	15	OVOUT2	Active-Low Overvoltage Output 2. When the voltage at OVIN2 rises above its threshold, OVOUT2 asserts low and stays asserted until the voltage at OVIN2 falls below its threshold. The open-drain output has a 30µA internal pullup to VCC.

_Pin Description (continued)

PI	N		
MAX16008	MAX16009	NAME	FUNCTION
13	16	UVOUT2	Active-Low Undervoltage Output 2. When the voltage at UVIN2 falls below its threshold, UVOUT2 asserts low and stays asserted until the voltage at UVIN2 exceeds its threshold. The open-drain output has a 30µA internal pullup to VCC.
14	17	OVOUT1	Active-Low Overvoltage Output 1. When the voltage at OVIN1 rises above its threshold, OVOUT1 asserts low and stays asserted until the voltage at OVIN1 falls below its threshold. The open-drain output has a 30µA internal pullup to VCC.
15	18	UVOUT1	Active-Low Undervoltage Output 1. When the voltage at UVIN1 falls below its threshold, UVOUT1 asserts low and stays asserted until the voltage at UVIN1 exceeds its threshold. The open-drain output has a 30µA internal pullup to VCC.
16	20	UVIN1	Undervoltage Threshold Input 1. When the voltage on UVIN1 falls below its threshold, UVOUT1 asserts low.
17	21	OVIN1	Overvoltage Threshold Input 1. When the voltage on OVIN1 rises above its threshold, OVOUT1 asserts low.
18	22	UVIN2	Undervoltage Threshold Input 2. When the voltages on UVIN2 falls below its threshold, UVOUT2 asserts low.
19	23	OVIN2	Overvoltage Threshold Input 2. When the voltage on OVIN2 rises above its threshold, OVOUT2 asserts low.
_	5	N.C.	Not Internally Connected
_	12	MR	Active-Low Manual Reset Input. Pull $\overline{\text{MR}}$ low to assert $\overline{\text{RESET}}$ low. $\overline{\text{RESET}}$ remains low for the reset timeout period after $\overline{\text{MR}}$ is deasserted. $\overline{\text{MR}}$ is pulled up to V_{CC} through a $20\text{k}\Omega$ resistor.
_	13	SRT	Set Reset Timeout Input. Connect a capacitor from SRT to GND to set the reset timeout period. The reset timeout period can be calculated as follows: Reset Timeout (s) = $2.06 \times 10^6 (\Omega) \times C_{SRT}$ (F). Do not set the reset timeout period to more than 1.12s. For the internal timeout period of 140ms (min), connect SRT to V_{CC} .
_	19	RESET	Active-Low Reset Output. RESET asserts low when the voltage on any of the UVIN_ inputs falls below their respective thresholds, the voltage on any of the OVIN_ inputs goes above its respective threshold, or MR is asserted. RESET remains asserted for at least the minimum reset timeout after all monitored UVIN_ inputs exceed their respective thresholds, all OVIN_ inputs fall below their respective thresholds, and MR is deasserted. This open-drain output has a 30µA internal pullup.
_	_	EP	Exposed Pad. EP is internally connected to GND. Connect EP to the ground plane to provide a low thermal resistance path from the IC junction to the PC board. Do not use as the only electrical connection to GND.

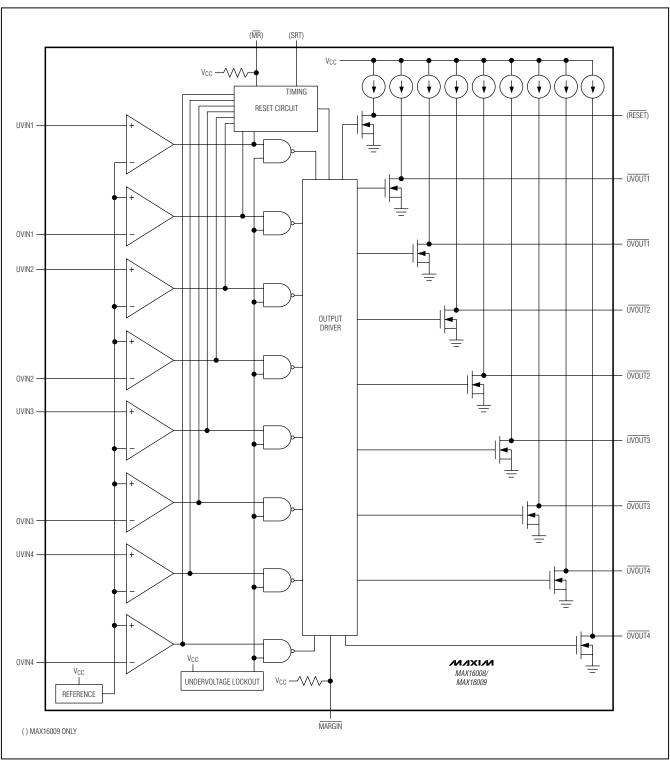


Figure 1. Functional Diagram

Detailed Description

The MAX16008/MAX16009 are adjustable quad window voltage detectors in a small thin QFN package. These devices are designed to provide a higher level of system reliability by monitoring multiple supply voltages and providing a fault signal when any of the voltages exceeds its overvoltage threshold or falls below its undervoltage threshold.

These devices offer user-adjustable thresholds that allow voltages to be monitored down to 0.4V. The devices allow the upper and lower trip thresholds of each window detector to be set externally with the use of three external resistors.

Each monitored threshold has an independent opendrain output for signaling a fault condition. The outputs can be wire OR'ed together to provide a single fault output. The open-drain outputs are internally pulled up with a 30µA current, but can be externally driven to other voltage levels for interfacing to other logic levels.

Both devices feature a margin input to disable the outputs during margin testing or any other time after power-up operations. The MAX16009 offers a reset output that deasserts after a reset timeout period after all voltages are within their threshold specification. The reset timeout is internally set to 140ms (min), but can be externally adjusted to other reset timeouts using an external capacitor. In addition, the MAX16009 offers a manual reset input.

Applications Information

Voltage Monitoring

The MAX16008/MAX16009 feature undervoltage and overvoltage comparators for window detection (see Figure 2). UVOUT_/OVOUT_ deassert high when the monitored voltage is within the "selected window." When the monitored voltage falls below the lower limit of the window (VTRIPLOW), UVOUT_ asserts low; or if the monitored voltage exceeds the upper limit (VTRIPHIGH), OVOUT_ asserts low. The application in Figure 2 shows the MAX16008/MAX16009 enabling the DC-DC converter when the monitored voltage is in the selected window.

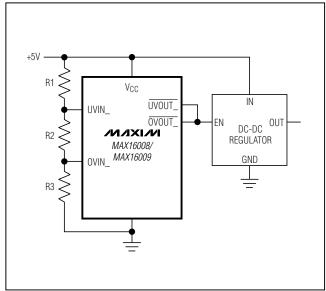


Figure 2. MAX16008/MAX16009 Monitor Circuit

The resistor values R1, R2, and R3 can be calculated as shown:

$$V_{TRIPLOW} = V_{TH} \left(\frac{R_{TOTAL}}{R2 + R3} \right)$$
 $V_{TRIPHIGH} = V_{TH} \left(\frac{R_{TOTAL}}{R3} \right)$

where RTOTAL = R1 + R2 + R3.

Use the following steps to determine the values for R1, R2, and R3:

1) Choose a value for R_{TOTAL} , the sum of R1, R2, and R3. Because the MAX16008/MAX16009 have very low input bias current (2nA typ), R_{TOTAL} can be up to $2M\Omega$. Large-value resistors help minimize power consumption. Lower-value resistors can be used to maintain overall accuracy.

Use the following formulas to calculate the error:

$$E_{UV}(\%) = \frac{I_{IB}\left(R_1 + \frac{R_1 R_3}{R_2 + R_3}\right)}{V_{TRIPLOW}} \times 100$$

$$E_{OV}(\%) = \frac{I_{IB}(R_2 + (2 \times R_1))}{V_{TRIPHIGH}} \times 100$$

where E_{UV} and E_{OV} are the undervoltage and overvoltage error (in %), respectively.

2) Calculate R3 based on R_{TOTAL} and the desired upper trip point:

$$R3 = \frac{V_{TH} \times R_{TOTAL}}{V_{TRIPHIGH}}$$

Calculate R2 based on RTOTAL, R3, and the desired lower trip point:

$$R2 = \frac{V_{TH} \times R_{TOTAL}}{V_{TRIPLOW}} - R3$$

4) Calculate R1 based on RTOTAL, R3, and R2:

$$R1 = R_{TOTAL} - R2 - R3$$

Overvoltage Shutdown

The MAX16008/MAX16009 are ideal for overvoltage-shutdown applications. Figure 3 shows a typical circuit for this application using a pass p-channel MOSFET.

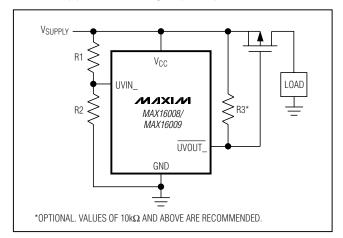


Figure 3. Overvoltage Shutdown Circuit (with External Pass MOSFET)

The MAX16008/MAX16009 are powered directly from the system voltage supply. Select R1 and R2 to set the trip voltage. When the supply voltage remains below the selected threshold, a low logic level on $\overline{\text{UVOUT}}_{-}$ turns on the p-channel MOSFET. In the case of an overvoltage event, $\overline{\text{UVOUT}}_{-}$ goes high turning off the MOSFET, and shuts down the power to the load.

Figure 4 shows a similar application using a fuse and a silicon-controlled rectifier (SCR). An overvoltage event turns on the SCR and shorts the supply to ground. The surge of current through the short circuit blows the fuse and terminates the current to the load. Select R3 so that the gate of the SCR is properly biased when UVOUT_goes high.

Unused Inputs

Any unused UVIN_ inputs must be connected to V_{CC}, and any unused OVIN_ inputs must be connected to GND.

UVOUT_/OVOUT_ Outputs

UVOUT_ and OVOUT_ outputs assert low when UVIN_ and OVIN_, respectively, drop below or exceed their specified thresholds. The undervoltage/overvoltage outputs are open-drain with a (30μA) internal pullup to V_{CC}. For many applications, no external pullup resistor is required to interface with other logic devices. An external pullup resistor to any voltage up to 5.5V overdrives the internal pullup if interfacing to different logic supply voltages. Internal circuitry prevents reverse current flow from the external pullup voltage to V_{CC} (Figure 5). When choosing the external pullup resistor, the resistance value should be large enough to ensure that the output can sink the necessary current during a logic-low condition and small enough to be able to overdrive the internal pullup current and meet output high specifications

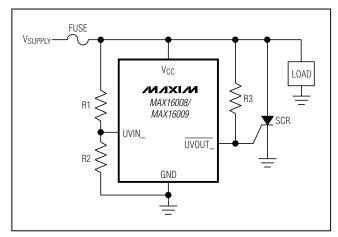


Figure 4. Overvoltage Shutdown Circuit (with SCR Fuse)

(VOH). Resistor values of $50 \text{k}\Omega$ to $200 \text{k}\Omega$ can generally be used.

RESET Output (MAX16009 Only)

RESET asserts low when the voltage on any of the UVIN_ inputs falls below its respective threshold, the voltage on any of the OVIN_ inputs goes above its respective threshold, or MR is asserted. RESET remains asserted for the reset timeout period after all monitored UVIN_ inputs exceed their respective thresholds, all OVIN_ inputs fall below their respective thresholds, and MR is deasserted (see Figure 6). This open-drain output has a 30µA internal pullup.

Reset Timeout Capacitor

The reset timeout period can be adjusted to accommodate a variety of microprocessor (μ P) applications from 50 μ s to 1.12s. Adjust the reset timeout period (t_{RP}) by connecting a capacitor (t_{RP}) between SRT and GND. Calculate the reset timeout capacitor as follows:

$$C_{SRT}(F) = \frac{t_{RP}(s)}{\left(\frac{V_{TH_SRT}}{I_{SRT}}\right)}$$

Do not use capacitor (C_{SRT}) values higher than 390nF. Connect SRT to V_{CC} for a factory-programmed reset timeout of 140ms (min).

Manual Reset Input (MR) (MAX16009 Only) Many μP-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. A logic-low on $\overline{\text{MR}}$ asserts $\overline{\text{RESET}}$ low. $\overline{\text{RESET}}$ remains asserted while $\overline{\text{MR}}$ is low, and during the reset timeout period (140ms min) after $\overline{\text{MR}}$ returns high. The $\overline{\text{MR}}$ input has an internal $20\text{k}\Omega$ pullup resistor to VCC, so it can be left open if it is

after $\overline{\text{MR}}$ returns high. The $\overline{\text{MR}}$ input has an internal $20\text{k}\Omega$ pullup resistor to VCC, so it can be left open if it is not used. $\overline{\text{MR}}$ can be driven with TTL or CMOS-logic levels, or with open-drain/collector outputs. Connect a normally open momentary switch from $\overline{\text{MR}}$ to GND to create a manual reset function; external debounce circuitry is not required. If $\overline{\text{MR}}$ is driven from long cables or if the device is used in a noisy environment, connecting a $0.1\mu\text{F}$ capacitor from $\overline{\text{MR}}$ to GND provides additional noise immunity.

Margin Output Disable (MARGIN)

MARGIN allows system-level testing while power supplies are adjusted from their nominal voltages. Drive MARGIN low to deassert all outputs (UVOUT_,

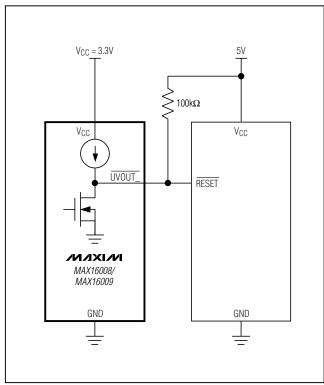


Figure 5. Interfacing to a Different Logic Supply Voltage

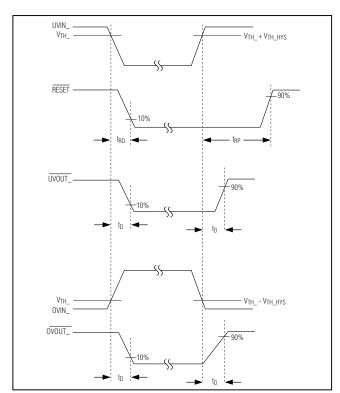


Figure 6. Output Timing Diagram

OVOUT_, and RESET) regardless of the voltage at any monitored input. The state of each output does not change while MARGIN = GND. While MARGIN is low, the IC continues to monitor all voltages. When MARGIN is deasserted, the outputs go to their monitored states after a short propagation delay. The MARGIN input is internally pulled up to VCC. Leave unconnected or connect to VCC if unused.

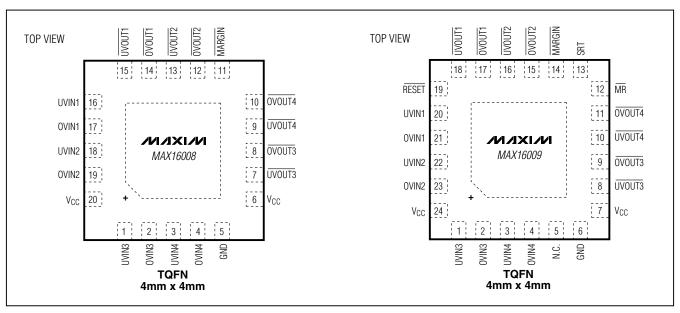
Power-Supply Bypassing

The MAX16008/MAX16009 operate from a 2.0V to 5.5V supply. An undervoltage lockout ensures that the outputs are in the correct states when the UVLO is exceeded. In noisy applications, bypass V_{CC} to ground with a 0.1µF capacitor as close to the device as possible. In addition, the additional capacitor improves transient immunity. For fast-rising V_{CC} transients, additional capacitance may be required.

Selector Guide

PART	NUMBER OF MONITORED LEVELS	UNDERVOLTAGE/ OVERVOLTAGE THRESHOLDS	RESET	ADJUSTABLE RESET TIMEOUT	MR
MAX16008	4	Adjustable	_	_	_
MAX16009	4	Adjustable	V	V	~

Pin Configurations



Package Information

For the latest package outline information and land patterns (footprints), go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 TQFN-EP	T2044+3	<u>21-0139</u>	<u>90-0037</u>
24 TQFN-EP	T2444+4	<u>21-0139</u>	90-0022

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/05	Initial release	_
1	1/11	Added soldering temperature in the <i>Absolute Maximum Rating</i> section and added symbol in <i>Electrical Characteristics</i> table	2

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ПОСТАВКА ЭЛЕКТРОННЫХ КОМПОНЕНТОВ

многоканальный

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Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

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