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November 2013

FDP030N06B_F102

N-Channel PowerTrench[®] MOSFET 60 V, 195 A, 3.1 m Ω

Features

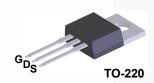
- $R_{DS(on)}$ = 2.67 m Ω (Typ.) @ V_{GS} = 10 V, I_D = 100 A
- Low FOM R_{DS(on)} * Q_G
- Low Reverse-Recovery Charge, Q_{rr} = 78 nC
- · Soft Reverse-Recovery Body Diode
- Enables High Efficiency in Synchronous Rectification
- · Fast Switching Speed
- · 100% UIL Tested
- · RoHS Compliant

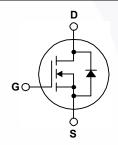
Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Applications

- · Synchronous Rectification for ATX / Server / Telecom PSU
- · Battery Protection Circuit
- · Motor Drives and Uninterruptible Power Supplies
- Renewable System





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol		Parameter	FDP030N06B_F102	Unit
V _{DSS}	Drain to Source Voltage		60	V
V_{GSS}	Gate to Source Voltage		±20	V
		- Continuous (T _C = 25°C, Silicon Limited)	195*	
I _D	Drain Current	ent - Continuous (T _C = 100°C, Silicon Limited)		
		- Continuous (T _C = 25°C, Package Limited)	120	
I _{DM}	Drain Current	- Pulsed (Note 1)	780	Α
E _{AS}	Single Pulsed Avalanche Energy	(Note 2)	600	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	6.0	V/ns
D	Power Dissipation	$(T_C = 25^{\circ}C)$	205	W
P _D Power Dissipation		- Derate Above 25°C	1.37	W/°C
T _J , T _{STG}	Operating and Storage Tempera	Operating and Storage Temperature Range		
T _L	Maximum Lead Temperature for	Soldering, 1/8" from Case for 5 Seconds	300	°C

^{*} Package limitation current is 120A.

Thermal Characteristics

Symbol	Parameter FDP030N06B_F102		Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.73	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. 62.5		C/VV

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDP030N06B_F102	FDP030N06B	TO-220	Tube	N/A	N/A	50 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	eteristics					
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	60	-	-	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	-	0.03	-	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 48 V, V _{GS} = 0 V	-	-	1	μΑ
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	±100	nA

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	2	-	4	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 100 A	-	2.67	3.1	mΩ
9 _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 100 A	-	206	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V = 20 V V = 0 V	-	6035	8030	pF
Coss	Output Capacitance	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz	-	1685	2240	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1/11/12	-	55	-	pF
C _{oss(er)}	Energy Related Output Capacitance	V _{DS} = 30 V, V _{GS} = 0 V	-	2619	-	pF
Q _{g(tot)}	Total Gate Charge at 10V		-	76	99	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DS} = 30 \text{ V}, I_{D} = 100 \text{ A},$		29	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	V _{GS} = 10 V	-	12	-	nC
V _{plateau}	Gate Plateau Volatge	(Note 4)	-	5.2	-	V
Q _{oss}	Output Charge	V _{DS} = 30V, V _{GS} = 0V	-	92.4	-	nC
ESR	Equivalent Series Resistance (G-S)	f = 1 MHz	-	2.0	-	Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time		-	32	74	ns
t _r		$V_{DD} = 30 \text{ V}, I_{D} = 100 \text{ A},$	-/	33	76	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_G = 4.7 \Omega$	-	56	122	ns
t _f	Turn-Off Fall Time	(Note 4)	-	23	56	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Dio	Maximum Continuous Drain to Source Diode Forward Current			195*	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	780	Α
V_{SD}	Drain to Source Diode Forward Voltage V _{GS} = 0V, I _{SD} = 100 A		-		1.25	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 100 A,	-	71	-	ns
Q _{rr}	Reverse Recovery Charge	$dI_F/dt = 100A/\mu s$	-	78	/-	nC

Notes

- 1. Repetitive rating: pulse-width limited by maximum junction temperature.
- 2. L = 3 mH, I_{AS} = 20 A, starting T_J = 25°C.
- 3. I $_{SD}$ \leq 100 A, di/dt \leq 200 A/ μ s, V $_{DD}$ \leq BV $_{DSS},$ starting T $_{J}$ = 25°C.
- 4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

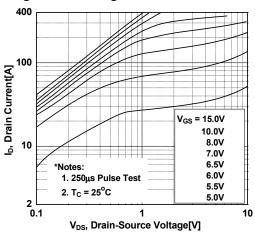


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

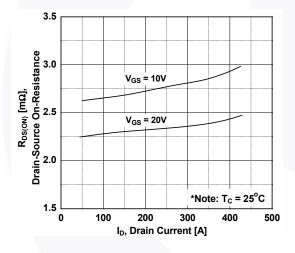


Figure 5. Capacitance Characteristics

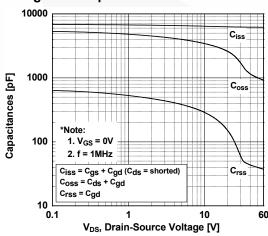


Figure 2. Transfer Characteristics

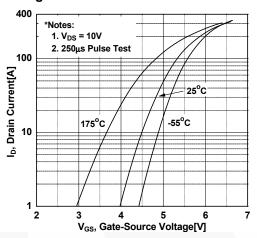


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

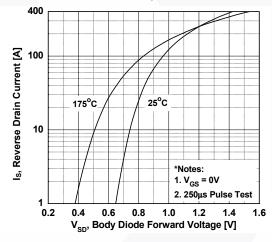
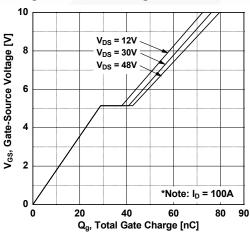


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

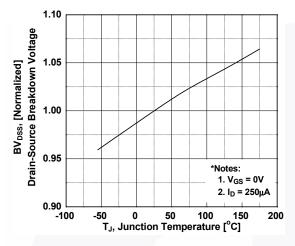


Figure 9. Maximum Safe Operating Area

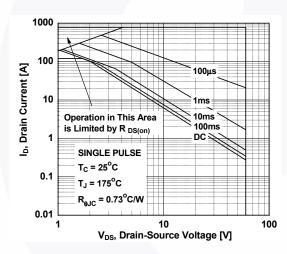


Figure 11. Eoss vs. Drain to Source Voltage

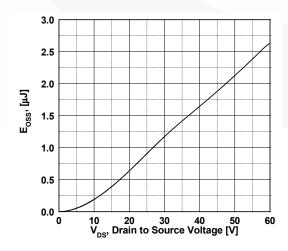


Figure 8. On-Resistance Variation vs. Temperature

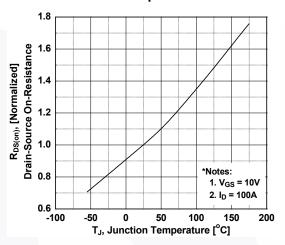


Figure 10. Maximum Drain Current vs. Case Temperature

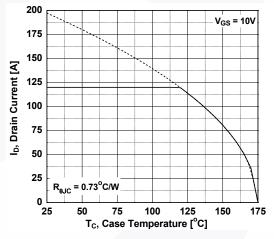
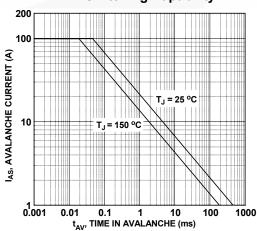
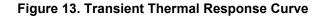
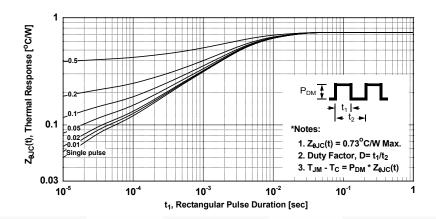


Figure 12. Unclamped Inductive Switching Capability



Typical Performance Characteristics (Continued)





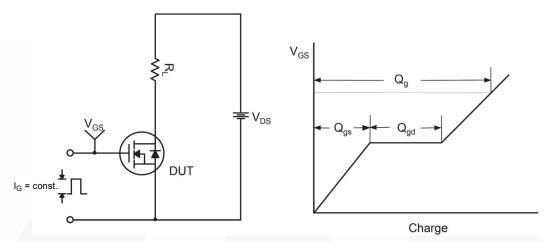


Figure 14. Gate Charge Test Circuit & Waveform

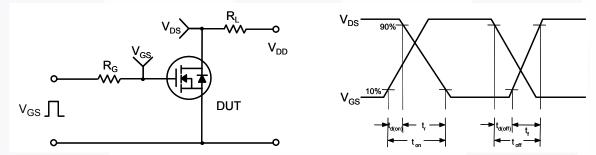


Figure 15. Resistive Switching Test Circuit & Waveforms

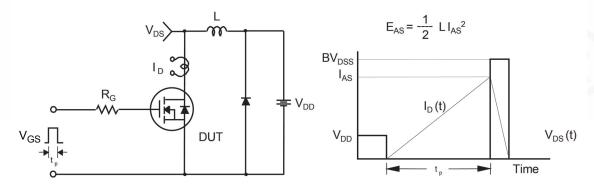


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

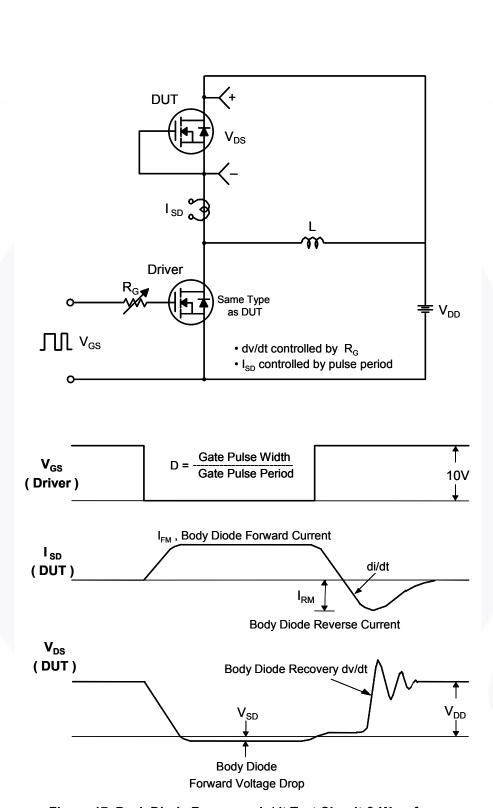


Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

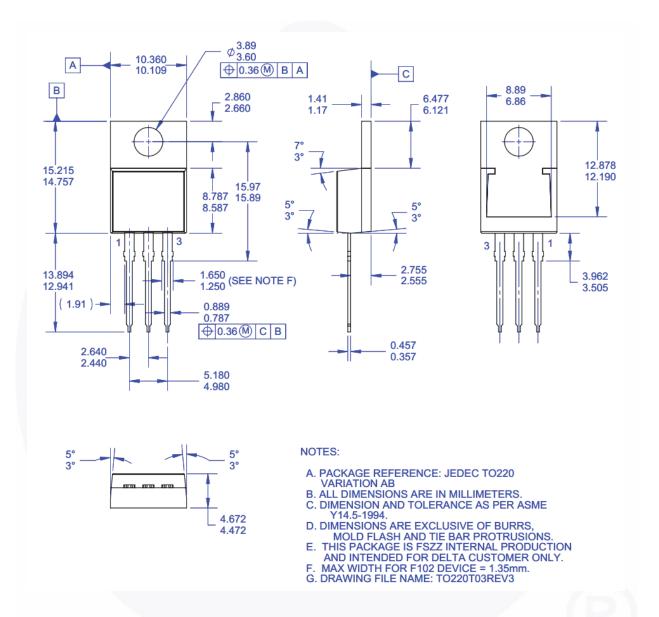


Figure 18. TO-220, Molded, 3-Lead, Jedec Variation AB (Delta)

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