

# ACPL-796J

## Optically Isolated Sigma-Delta Modulator



### Data Sheet

#### Description

The ACPL-796J is a 1-bit, second-order sigma-delta ( $\Sigma$ - $\Delta$ ) modulator converts an analog input signal into a high-speed data stream with galvanic isolation based on optical coupling technology. The ACPL-796J operates from a 5 V power supply with dynamic range of 80 dB with an appropriate digital filter. The differential inputs of  $\pm 200$  mV (full scale  $\pm 320$  mV) are ideal for direct connection to shunt resistors or other low-level signal sources in applications such as motor phase current measurement.

The analog input is continuously sampled by means of sigma-delta over-sampling using external clock, coupled across the isolation barrier, which allows synchronous operation with any digital controller. The signal information is contained in the modulator data, as a density of ones with data rate up to 20 MHz, and the data are encoded and transmitted across the isolation boundary where they are recovered and decoded into high-speed data stream of digital ones and zeros. The original signal information can be reconstructed with a digital filter. The serial interface has a wide supply range of 3 V to 5.5 V.

Combined with superior optical coupling technology, the modulator delivers high noise margins and excellent immunity against isolation-mode transients. With 0.5 mm minimum distance through insulation (DTI), the ACPL-796J provides reliable double protection and high working insulation voltage, which is suitable for fail-safe designs. This outstanding isolation performance is superior to alternatives including devices based on capacitive- or magnetic-coupling with DTI in micro-meter range. Offered in an SO-16 package, the isolated ADC delivers the reliability, small size, superior isolation and over-temperature performance motor drive designers need to accurately measure current at much lower price compared to traditional current transducers.

The internal clock version modulators, HCPL-7860 (DIP-8/ gull wing surface mount package) and HCPL-786J (SO-16 package), are also available.

#### Features

- 5 MHz to 20 MHz external clock input range
- 1-bit, second-order sigma-delta modulator
- 16 bits resolution no missing codes (12 bits ENOB)
- 74 dB minimum SNR
- 3.5  $\mu\text{V}/^\circ\text{C}$  maximum offset drift
- $\pm 1\%$  maximum gain error
- Internal reference voltage
- $\pm 200$  mV linear range with single 5 V supply
- 3 V to 5.5 V wide supply range for digital interface
- $-40^\circ\text{C}$  to  $+105^\circ\text{C}$  operating temperature range
- SO-16 package
- 25 kV/ $\mu\text{s}$  common-mode transient immunity
- Safety and regulatory approval (pending):
  - IEC/EN/DIN EN 60747-5-5: 1140 Vpeak working insulation voltage
  - UL 1577: 5000 Vrms/1min double protection rating
  - CSA: Component Acceptance Notice #5

#### Applications

- Motor phase and rail current sensing
- Power inverter current and voltage sensing
- Industrial process control
- Data acquisition systems
- General purpose current and voltage sensing
- Traditional current transducer replacements

#### Functional Block Diagram

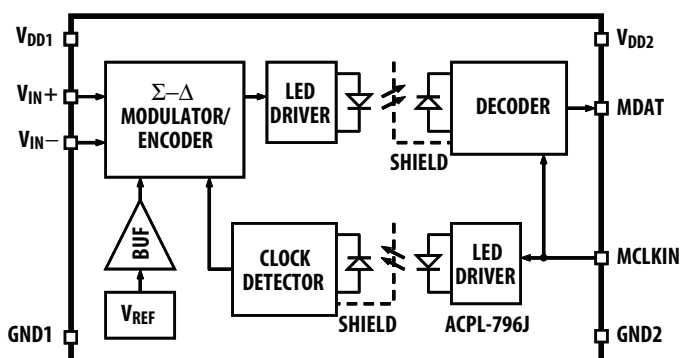


Figure 1.

**CAUTION:** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

## Pin Configuration and Descriptions

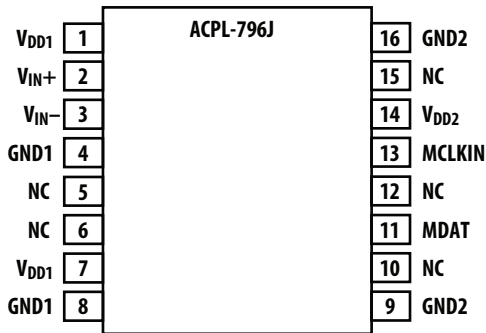


Figure 2. Pin configuration.

Table 1. Pin descriptions.

Pin No.	Symbol	Description
1, 7	V <sub>DD1</sub>	Supply voltage for signal input side (analog side), relative to GND1
2	V <sub>IN+</sub>	Positive analog input, recommended input range $\pm 200$ mV
3	V <sub>IN-</sub>	Negative analog input, recommended input range $\pm 200$ mV (normally connected to GND1)
4, 8	GND1	Supply ground for signal input side
5, 6, 10, 12, 15	NC	No connection. Leave floating
9, 16	GND2	Supply ground for data output side (digital side)
11	MDAT	Modulator data output
13	MCLKIN	Modulator clock input, 5 MHz to 20 MHz
14	V <sub>DD2</sub>	Supply voltage for data output side, relative to GND2

Table 2. Ordering Information

ACPL-796J is UL recognized with 5000 Vrms/1 minute rating per UL 1577 (pending).

Part number	Option (RoHS Compliant)	Package	Surface Mount	Tape & Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-796J	-000E	SO-16	X			45 per tube
	-060E		X		X	45 per tube
	-500E		X	X		850 per reel
	-560E		X	X	X	850 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

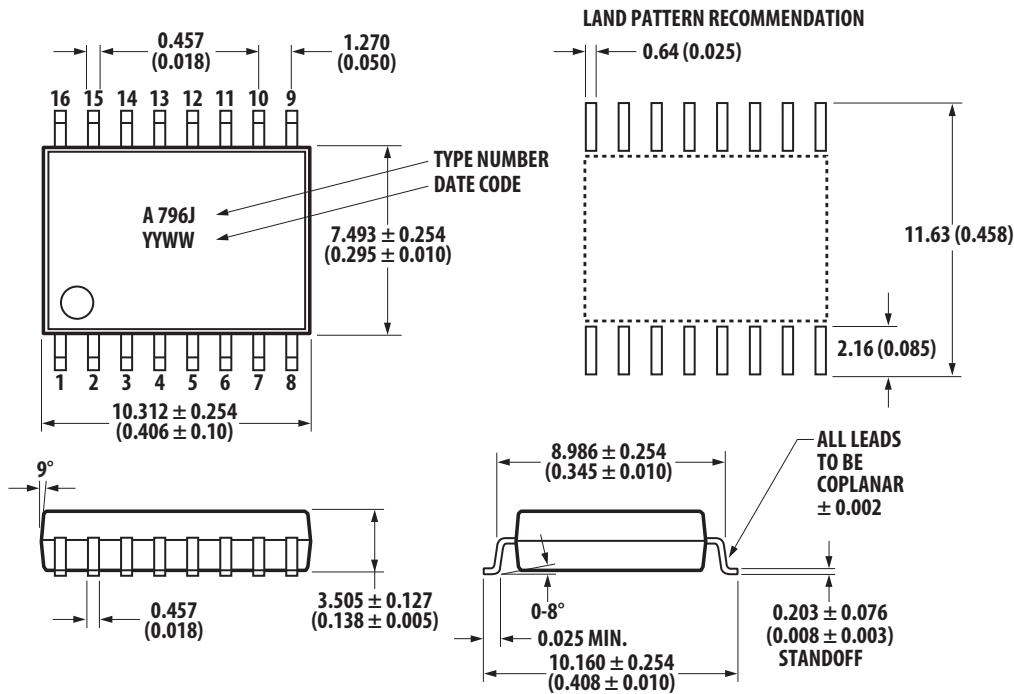
Example:

ACPL-796J-560E to order product of Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval and RoHS compliance.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

## Package Outline Drawings

### 16-Lead Surface Mount (S0-16)



Dimensions in millimeters and (inches).

Note: Floating lead protrusion is 0.15 mm (6 mils) max.

Note: Initial and continued variation in color of the white mold compound is normal and does not affect performance or reliability of the device.

Figure 3. 16-Lead Surface Mount.

### Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

### Regulatory Information

The ACPL-796J is pending for approvals by the following organizations:

#### IEC/EN/DIN EN 60747-5-5

Approved with Maximum Working Insulation Voltage  
 $V_{IORM} = 1140 V_{peak}$ .

#### CSA

Approval under CSA Component Acceptance Notice #5,  
 File CA 88324.

#### UL

Approval under UL 1577, component recognition program  
 up to  $V_{ISO} = 5000 V_{rms}/1min$ . File E55361.

**Table 3. IEC/EN/DIN EN 60747-5-5 Insulation Characteristics<sup>[1]</sup>**

Description	Symbol	Value	Units
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 150 Vrms for rated mains voltage ≤ 300 Vrms for rated mains voltage ≤ 450 V rms for rated mains voltage ≤ 600 Vrms for rated mains voltage ≤ 1000 Vrms		I-IV I-IV I-III I-III I-II	
Climatic Classification		55/105/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	$V_{IORM}$	1140	Vpeak
Input to Output Test Voltage, Method b $V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test with $t_m = 1$ sec, Partial Discharge < 5 pC	$V_{PR}$	2137	Vpeak
Input to Output Test Voltage, Method a $V_{IORM} \times 1.6 = V_{PR}$ , Type and Sample Test, $t_m = 10$ sec, Partial Discharge < 5 pC	$V_{PR}$	1824	Vpeak
Highest Allowable Overvoltage (Transient Overvoltage, $t_{ini} = 60$ sec)	$V_{IOTM}$	6000	Vpeak
Safety-limiting values (Maximum values allowed in the event of a failure)			
Case Temperature	$T_S$	175	°C
Input Current <sup>[2]</sup>	$I_{S,INPUT}$	400	mA
Output Power <sup>[2]</sup>	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at $T_S$ , $V_{IO} = 500$ V	$R_S$	$\geq 10^9$	$\Omega$

Notes:

- Insulation characteristics are guaranteed only within the safety maximum ratings, which must be ensured by protective circuits within the application.
- Safety-limiting parameters are dependent on ambient temperature. Refer to the following figure for dependence of  $P_S$  and  $I_S$  on ambient temperature.

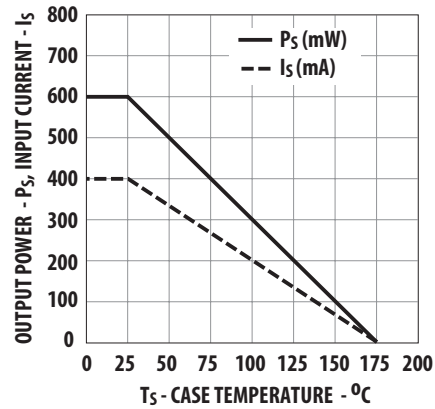


Figure 4.

**Table 4. Insulation and Safety Related Specifications**

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (External Creepage)	L(102)	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

**Table 5. Absolute Maximum Ratings**

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	$T_S$	-55	+125	°C
Ambient Operating Temperature	$T_A$	-40	+105	°C
Supply voltage	$V_{DD1}, V_{DD2}$	-0.5	6.0	V
Steady-State Input Voltage <sup>[1,3]</sup>	$V_{IN+}, V_{IN-}$	-2	$V_{DD1} + 0.5$	V
Two-Second Transient Input Voltage <sup>[2]</sup>	$V_{IN+}, V_{IN-}$	-6	$V_{DD1} + 0.5$	V
Digital Input/Output Voltages	MCLKIN, MDAT	-0.5	$V_{DD2} + 0.5$	V
Lead Solder Temperature	260°C for 10 sec., 1.6 mm below seating plane			

Notes:

1. DC voltage of up to -2 V on the inputs does not cause latch-up or damage to the device; tested at typical operating conditions.
2. Transient voltage of 2 seconds up to -6 V on the inputs does not cause latch-up or damage to the device; tested at typical operating conditions.
3. Absolute maximum DC current on the inputs = 100 mA, no latch-up or device damage occurs.

**Table 6. Recommended Operating Conditions**

Parameter	Symbol	Min.	Max.	Units
Ambient Operating Temperature	$T_A$	-40	+105	°C
$V_{DD1}$ Supply Voltage	$V_{DD1}$	4.5	5.5	V
$V_{DD2}$ Supply Voltage	$V_{DD2}$	3	5.5	V
Analog Input Voltage <sup>[1]</sup>	$V_{IN+}, V_{IN-}$	-200	+200	mV

Notes:

1. Full scale signal input range  $\pm 320$  mV.

**Table 7. Electrical Specifications**

Unless otherwise noted,  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ ,  $V_{DD1} = 4.5\text{ V}$  to  $5.5\text{ V}$ ,  $V_{DD2} = 3\text{ V}$  to  $5.5\text{ V}$ ,  $V_{IN+} = -200\text{ mV}$  to  $+200\text{ mV}$ , and  $V_{IN-} = 0\text{ V}$  (single-ended connection); tested with Sinc<sup>3</sup> filter, 256 decimation ratio,  $f_{MCLKIN} = 10\text{ MHz}$ .

Parameter	Symbol	Min.	Typ. <sup>[1]</sup>	Max.	Units	Test Conditions/Notes	Fig.
<b>STATIC CHARACTERISTICS</b>							
Resolution		16			Bits	Decimation filter output set to 16 bits	
Integral Nonlinearity	INL	-15	3	15	LSB	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ ; see Definitions section	
		-25	3	25	LSB	$T_A = 85^\circ\text{C}$ to $105^\circ\text{C}$	
		-25		25		$V_{IN+} = -250\text{ mV}$ to $+250\text{ mV}$	
Differential Nonlinearity	DNL	-0.9		0.9	LSB	No missing codes, guaranteed by design; see Definitions section	
Offset Error	$V_{OS}$	-1	3	4.5	mV	$T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ ; see Definitions section	
Offset Drift vs. Temperature	$TCV_{OS}$			3.5	$\mu\text{V}/^\circ\text{C}$		
Offset Drift vs. $V_{DD1}$			120		$\mu\text{V}/\text{V}$		
Gain Error	$G_E$	-2		2	%	$T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ , $V_{IN+} = -250$ to $+250\text{ mV}$ ; see Definitions section	
		-1		1	%	$T_A = 25^\circ\text{C}$ , $V_{IN+} = -250$ to $+250\text{ mV}$	
Gain Error Drift vs. Temperature	$TCG_E$		60		ppm/ $^\circ\text{C}$		
Gain Error Drift vs. $V_{DD1}$			110		$\mu\text{V}/\text{V}$		
<b>ANALOG INPUTS</b>							
Full-Scale Differential Voltage Input Range	FSR		$\pm 320$		mV	$V_{IN} = V_{IN+} - V_{IN-}$ ; Note 2	
Average Input Bias Current	$I_{INA}$		-0.5		$\mu\text{A}$	$V_{DD1} = 5\text{ V}$ , $V_{DD2} = 5\text{ V}$ , $V_{IN+} = 0\text{ V}$ ; Note 3	6
Average Input Resistance	$R_{IN}$		33		$\text{k}\Omega$	Across $V_{IN+}$ or $V_{IN-}$ to GND1; Note 3	
Input Capacitance	$C_{INA}$		8		pF	Across $V_{IN+}$ or $V_{IN-}$ to GND1	
<b>DYNAMIC CHARACTERISTICS</b>							
Signal-to-Noise Ratio	SNR	74	80		dB	$T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ ; see Definitions section	
Signal-to-(Noise + Distortion) Ratio	SNDR	65	75		dB	$T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ ; see Definitions section	7, 8
		68	75		dB	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	7, 8
		65				$T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ , $V_{IN+} = -250\text{ mV}$ to $+250\text{ mV}$	7
Effective Number of Bits	ENOB		12		Bits	see Definitions section	
Isolation Transient Immunity	CMR		25		$\text{kV}/\mu\text{V}$	$V_{CM} = 1\text{ kV}$ ; See Definitions section	
Common-Mode Rejection Ratio	CMRR		74		dB		
<b>DIGITAL INPUTS AND OUTPUTS</b>							
Input High Voltage	$V_{IH}$	$0.8 \times V_{DD2}$			V	Note 5	
Input Low Voltage	$V_{IL}$			$0.2 \times V_{DD2}$	V	Note 5	
Input Current	$I_{IND}$		$\pm 0.5$		$\mu\text{A}$		
Input Capacitance	$C_{IND}$		6		pF		
Output High Voltage	$V_{OH}$	$V_{DD2} - 0.2$	$V_{DD2} - 0.1$		V	$V_{DD2} = 5\text{ V}$ supply, $I_{OUT} = -200\text{ }\mu\text{A}$	
		$V_{DD2} - 0.15$	$V_{DD2} - 0.1$		V	$V_{DD2} = 3.3\text{ V}$ supply, $I_{OUT} = -200\text{ }\mu\text{A}$	
Output Low Voltage	$V_{OL}$			0.4	V	$I_{OUT} = +200\text{ }\mu\text{A}$	
<b>POWER SUPPLY</b>							
$V_{DD1}$ Supply Current	$I_{DD1}$		14	19	mA		9, 10
$V_{DD2}$ Supply Current	$I_{DD2}$		6	8	mA	$V_{DD2} = 5\text{ V}$ supply	11, 12
			5	7	mA	$V_{DD2} = 3.3\text{ V}$ supply	

Notes:

1. All Typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = 5\text{ V}$ ,  $V_{DD2} = 5\text{ V}$ .
2. Beyond the full-scale input range the data output is either all zeroes or all ones.
3. Because of the switched-capacitor nature of the isolated modulator, time averaged values are shown.
4. Signal frequency of 543 Hz is used as a reference frequency for coherent sampling.
5. Ensured by design.

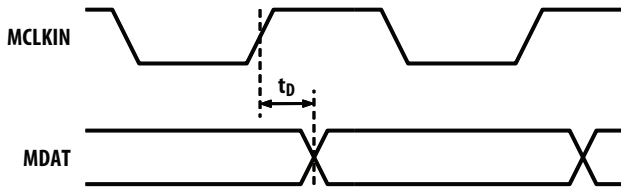
**Table 8. Timing Specifications**

Unless otherwise noted,  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ ,  $V_{DD1} = 4.5\text{ V}$  to  $5.5\text{ V}$ ,  $V_{DD2} = 3\text{ V}$  to  $5.5\text{ V}$ .

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions/Notes	Fig.
Modulator Clock Input Frequency	$f_{\text{MCLKIN}}$	5	10	20	MHz	Clock duty cycle 40% to 60%	
Data Delay After Rising Edge of MCLKIN <sup>[1]</sup>	$t_D$	3		15	ns	$C_L = 15\text{ pF}$	5

Notes:

1. Data changes at the clock rising edge so it can be safely read at the falling edge, although it can be read at the rising edge if preferred.

**Figure 5. Data timing.****Table 9. Package Characteristics**

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Note
Input-Output Momentary Withstand Voltage	$V_{\text{ISO}}$	5000			Vrms	$RH \leq 50\%$ , $t = 1\text{ min}$ ; $T_A = 25^\circ\text{C}$	1, 2
Input-Output Resistance	$R_{\text{I-O}}$	$10^{12}$	$10^{13}$		$\Omega$	$V_{\text{I-O}} = 500\text{ Vdc}$	2
		$10^{11}$			$\Omega$	$T_A = 100^\circ\text{C}$	2
Input-Output Capacitance	$C_{\text{I-O}}$		1.4		pF	$f = 1\text{ MHz}$	2
Input IC Junction-to-Ambient Thermal Resistance	$\theta_{\text{JAI}}$		83		$^\circ\text{C/W}$	1 oz. trace, 2-layer PCB, still air, $T_A = 25^\circ\text{C}$	3
Output IC Junction-to- Ambient Thermal Resistance	$\theta_{\text{JAO}}$		85		$^\circ\text{C/W}$	1 oz. trace, 2-layer PCB, still air, $T_A = 25^\circ\text{C}$	3

Notes:

1. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage  $\geq 6000\text{ Vrms}$  for 1 second (leakage detection current limit,  $I_{\text{I-O}} \leq 5\text{ }\mu\text{A}$ ). This test is performed before the 100% production test for partial discharge (method b) shown in IEC/EN/DIN EN 60747-5-5 Insulation Characteristic Table.
2. This is a two-terminal measurement: pins 1-8 are shorted together and pins 9-16 are shorted together.
3. Maximum power dissipation in analog side and digital side IC's needs to be limited to ensure that their respective junction temperature is less than  $125^\circ\text{C}$ . The maximum permissible power dissipation is dependent on the thermal impedance and the ambient temperature.

## Typical Performance Plots

Unless otherwise noted,  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = 5\text{ V}$ ,  $V_{DD2} = 5\text{ V}$ ,  $V_{IN+} = -200\text{ mV to } +200\text{ mV}$ , and  $V_{IN-} = 0\text{ V}$ ,  $f_{MCLKIN} = 10\text{ MHz}$ , with Sinc<sup>3</sup> filter, 256 decimation ratio.

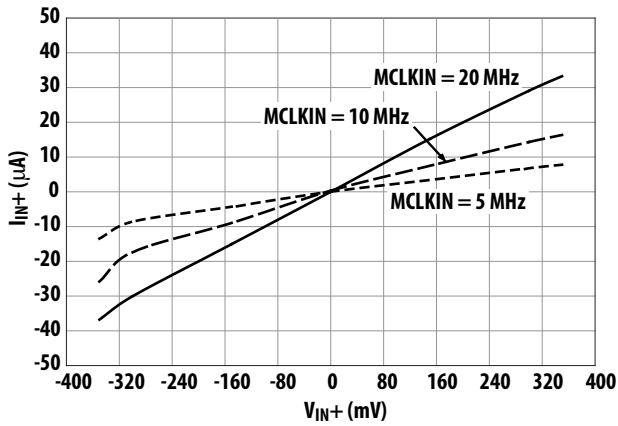


Figure 6. Input current vs. input voltage.

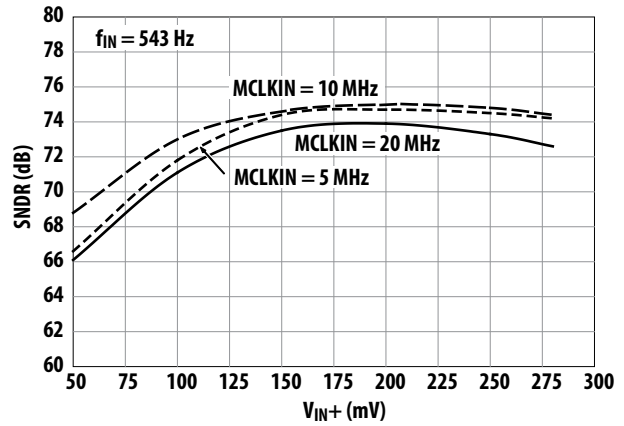


Figure 7. SNDR vs. input voltage  $V_{IN+}$ .

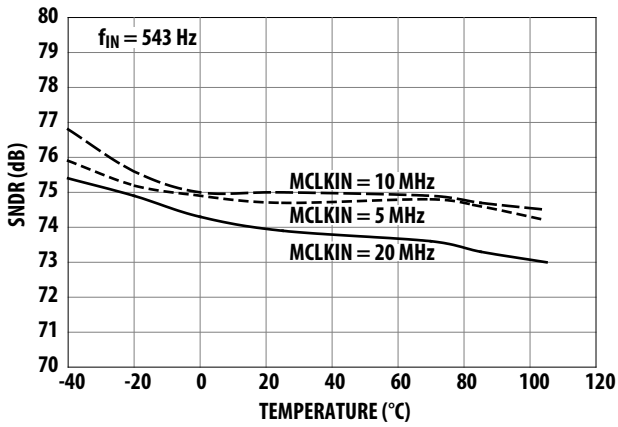


Figure 8. SNDR vs. temperature.

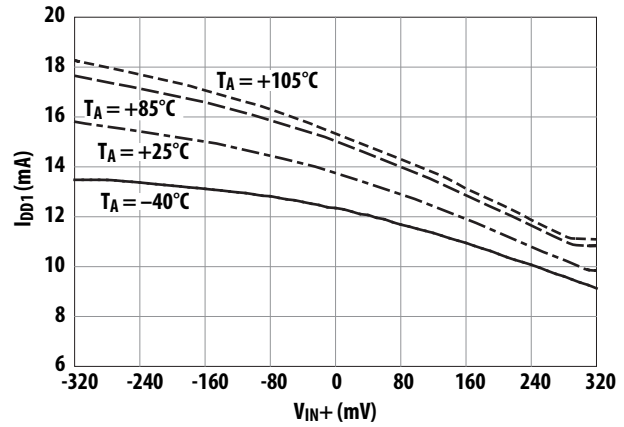


Figure 9.  $I_{DD1}$  vs.  $V_{IN}$  DC input at various temperatures.

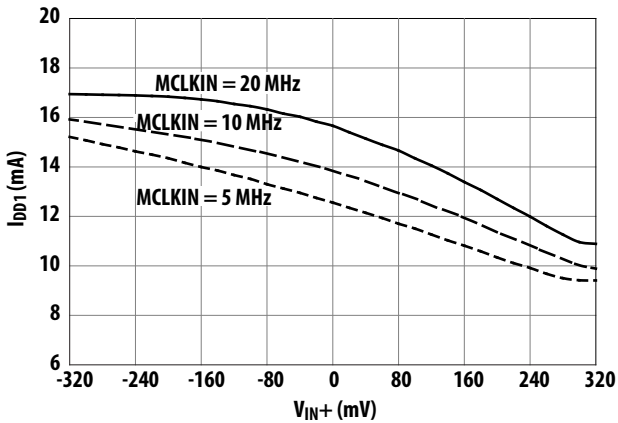


Figure 10.  $I_{DD1}$  vs.  $V_{IN}$  DC input for various frequencies.



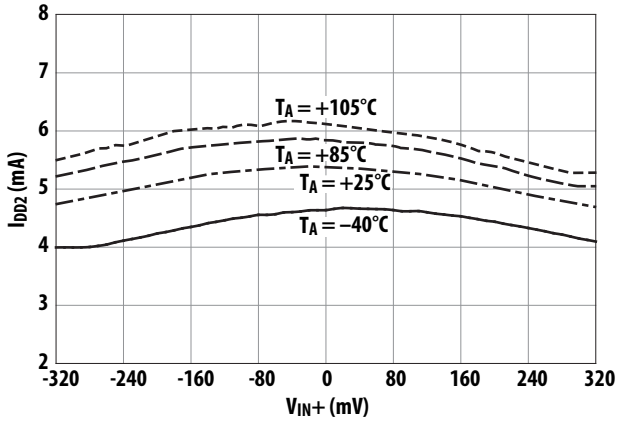


Figure 11.  $I_{DD2}$  vs.  $V_{IN}$  DC input at various temperatures.

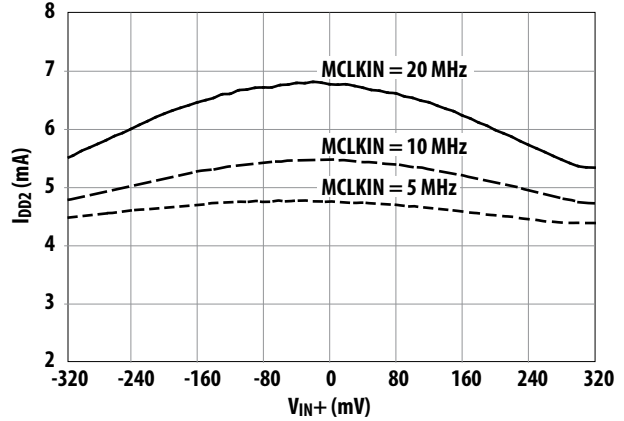


Figure 12.  $I_{DD2}$  vs.  $V_{IN}$  DC input for various frequencies.

## Definitions

### Integral Nonlinearity (INL)

INL is the maximum deviation of a transfer curve from a straight line passing through the endpoints of the ADC transfer function, with offset and gain errors adjusted out.

### Differential Nonlinearity (DNL)

DNL is the deviation of an actual code width from the ideal value of 1 LSB between any two adjacent codes in the ADC transfer curve. DNL is a critical specification in closed-loop applications. A DNL error of less than  $\pm 1$  LSB guarantees no missing codes and a monotonic transfer function.

### Offset Error

Offset error is the deviation of the actual input voltage corresponding to the mid-scale code (32,768 for a 16-bit system with an unsigned decimation filter) from 0V. Offset error can be corrected by software or hardware.

### Gain Error

Gain error is the the difference between the ideal gain slope and the actual gain slope, with offset error adjusted out. Gain error includes reference error. Gain error can be corrected by software or hardware.

### Signal-to-Noise Ratio (SNR)

The SNR is the measured ratio of AC signal power to noise power below half of the sampling frequency. The noise power excludes harmonic signals and DC.

### Signal-to-(Noise + Distortion) Ratio (SNDR)

The SNDR is the measured ratio of AC signal power to noise plus distortion power at the output of the ADC. The signal power is the rms amplitude of the fundamental input signal. Noise plus distortion power is the rms sum of all non-fundamental signals up to half the sampling frequency (excluding DC).

### Effective Number of Bits (ENOB)

The ENOB determines the effective resolution of an ADC, expressed in bits, defined by  $ENOB = (SNDR - 1.76)/6.02$

### Isolation Transient Immunity (CMR)

The isolation transient immunity (also known as Common-Mode Rejection or CMR) specifies the minimum rate-of-rise/fall of a common-mode signal applied across the isolation boundary beyond which the modulator clock or data is corrupted.

## Product Overview

### Description

The ACPL-796J isolated sigma-delta ( $\Sigma-\Delta$ ) modulator converts an analog input signal into a high-speed (up to 20 MHz) single-bit data stream by means of a sigma-delta over-sampling modulator. The time average of the modulator data is directly proportional to the input signal voltage. The modulator uses external clock ranges from 5 MHz to 20 MHz that is coupled across the isolation barrier. This arrangement allows synchronous operation of data acquisition to any digital controller, and adjustable clock for speed requirements of the application. The modulator data are encoded and transmitted across the isolation boundary where they are recovered and decoded into high-speed data stream of digital ones and zeros. The original signal information is represented by the density of ones in the data output.

The other main function of the modulator (optocoupler) is to provide galvanic isolation between the analog signal input and the digital data output. It provides high noise margins and excellent immunity against isolation-mode transients that allows direct measurement of low-level signals in highly noisy environments, for example measurement of motor phase currents in power inverters.

With 0.5 mm minimum DTI, the ACPL-796J provides reliable double protection and high working insulation voltage, which is suitable for fail-safe designs. This outstanding isolation performance is superior to alternatives including devices based on capacitive- or magnetic-coupling with DTI in micro-meter range. Offered in an SO-16 package, the isolated ADC delivers the reliability, small size, superior isolation and over-temperature performance motor drive designers need to accurately measure current at much lower price compared to traditional current transducers.

### Analog Input

The differential analog inputs of the ACPL-796J are implemented with a fully-differential, switched-capacitor circuit. The ACPL-796J accepts signal of  $\pm 200$  mV (full scale  $\pm 320$  mV), which is ideal for direct connection to shunt based current sensing or other low-level signal sources applications such as motor phase current measurement. An internal voltage reference determines the full-scale analog input range of the modulator ( $\pm 320$  mV); an input range of  $\pm 200$  mV is recommended to achieve optimal performance. Users are able to use higher input range, for example  $\pm 250$  mV, as long as within full-scale range, for purpose of over-current or overload detection. Figure 13 shows the simplified equivalent circuit of the analog input.

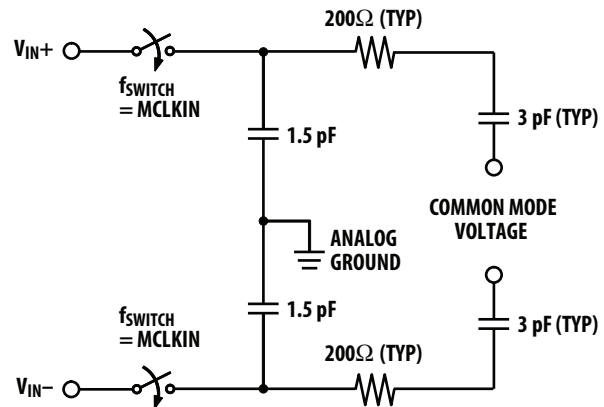


Figure 13. Analog input equivalent circuit.

In the typical application circuit (Figure 18), the ACPL-796J is connected in a single-ended input mode. Given the fully differential input structure, a differential input connection method (balanced input mode as shown in Figure 14) is recommended to achieve better performance. The input currents created by the switching actions on both of the pins are balanced on the filter resistors and cancelled out each other. Any noise induced on one pin will be coupled to the other pin by the capacitor C and creates only common mode noise which is rejected by the device. Typical value for Ra and Rb is 22  $\Omega$  and 10 nF for C.

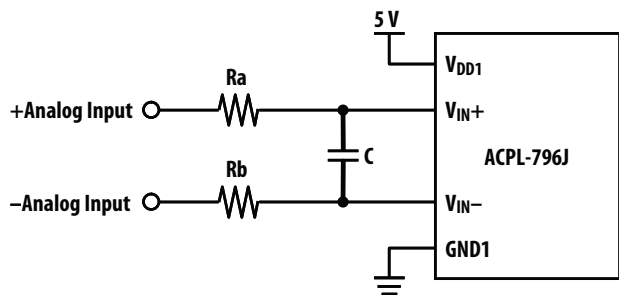


Figure 14. Simplified differential input connection diagram.

## Latch-up Consideration

Latch-up risk of CMOS devices needs careful consideration, especially in applications with direct connection to signal source that is subject to frequent transient noise. The analog input structure of the ACPL-796J is designed to be resilient to transients and surges, which are often encountered in highly noisy application environments such as motor drive and other power inverter systems. Other situations could cause transient voltages to the inputs include short circuit and overload conditions. The ACPL-796J is tested with DC voltage of up to  $-2\text{ V}$  and 2-second transient voltage of up to  $-6\text{ V}$  to the analog inputs and there is no latch-up or damage to the device.

## Modulator Data Output

Input signal information is contained in the modulator output data stream, represented by the density of ones and zeros. The density of ones is proportional to the input signal voltage, as shown in Figure 15. A differential input signal of  $0\text{ V}$  ideally produces a data stream of ones 50% of the time and zeros 50% of the time. A differential input of  $-200\text{ mV}$  corresponds to 18.75% density of ones, and a differential input of  $+200\text{ mV}$  is represented by 81.25% density of ones in the data stream. A differential input of  $+320\text{ mV}$  or higher results in ideally all ones in the data stream, while input of  $-320\text{ mV}$  or lower will result in all zeros ideally. Table 10 shows this relationship.

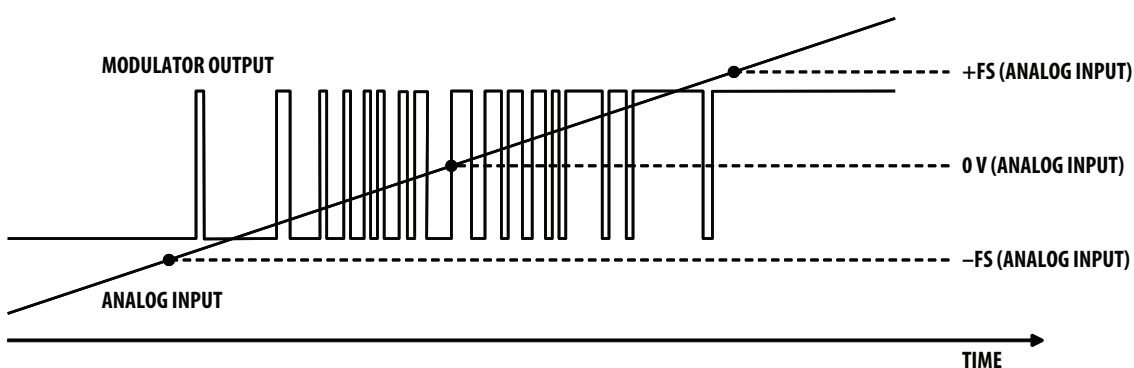


Figure 15. Modulator output vs. analog input.

Table 10. Input voltage with ideal corresponding density of 1s at modulator data output, and ADC code.

Analog Input	Voltage Input	Density of 1s	ADC Code (16-bit unsigned decimation)
Full-Scale Range	640 mV		
+Full-Scale	+320 mV	100%	65,535
+Recommended Input Range	+200 mV	81.25%	53,248
Zero	0 mV	50%	32,768
-Recommended Input Range	-200 mV	18.75%	12,288
-Full-Scale	-320 mV	0%	0

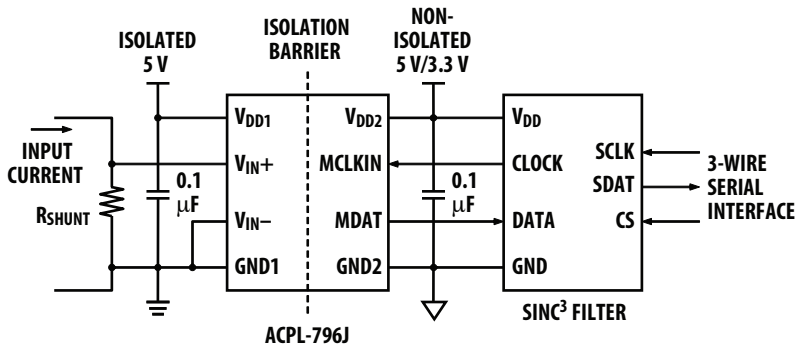
Notes:

1. With bipolar offset binary coding scheme, the digital code begins with digital 0 at  $-FS$  input and increases proportionally to the analog input until the full-scale code is reached at the  $+FS$  input. The zero crossing occurs at the mid-scale input.
2. Ideal density of 1s at modulator data output can be calculated with  $V_{IN}/640\text{ mV} + 50\%$ ; similarly, the ADC code can be calculated with  $(V_{IN}/640\text{ mV}) \times 65,536 + 32,768$ , assuming a 16-bit unsigned decimation filter.

## Digital Filter

A digital filter converts the single-bit data stream from the modulator into a multi-bit output word similar to the digital output of a conventional A/D converter. With this conversion, the data rate of the word output is also reduced (decimation). A Sinc<sup>3</sup> filter is recommended to work together with the ACPL-796J. With a 10 MHz external

clock frequency, 256 decimation ratio and 16-bit word settings, the output data rate is 39 kHz (= 10 MHz/256). This filter can be implemented in an ASIC, an FPGA or a DSP. Some of the ADC codes with corresponding input voltages are shown in Table 10.



Note: In applications, a 0.1 µF bypass capacitor must be connected between pins V<sub>DD1</sub> and GND1, and between pins V<sub>DD2</sub> and GND2 of the ACPL-796J.

Figure 16. Typical application circuit with a Sinc<sup>3</sup> filter.

## Digital Interface IC

The HCPL-0872 Digital Interface IC (SO-16 package) is a digital filter that converts the single-bit data stream from the modulator into 15-bit output words and provides a serial output interface that is compatible with SPI®, QSPI®, and Microwire® protocols, allowing direct connection to a

microcontroller. Instead of a digital filter implemented in software, the HCPL-0872 can be used together with the ACPL-796J to form an isolated programmable two-chip A/D converter (see Figure 17).

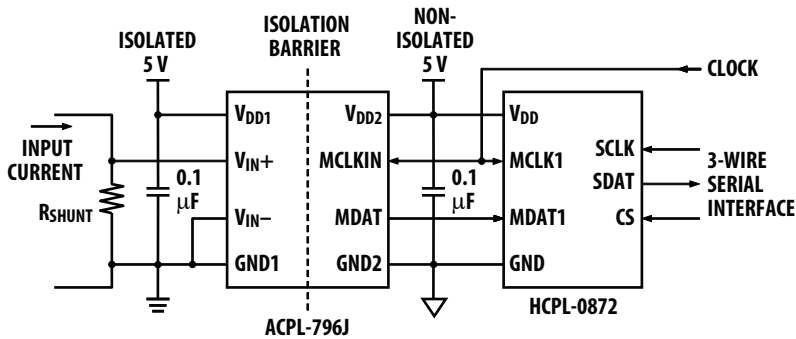


Figure 17. Typical application circuit with the HCPL-0872.

Available in an SO-16 surface-mount package, the Digital Interface IC has features include five different conversion modes (combinations of speed and resolution), three different pre-trigger modes (allows conversion time <1 µs), offset calibration, fast over-range (over-current, or short circuits) detection, and adjustable threshold detection. Programmable features are configured via the

Serial Configuration port. A second multiplexed input is available to allow measurements with a second isolated modulator without additional hardware. Refer to the HCPL-0872 data sheet for details.

Notes:

SPI and QSPI are trademarks of Motorola Corp.

Microwire is a trademark of National Semiconductor Inc.

## Application Information

### Digital Current Sensing Circuit

Figure 18 shows a typical application circuit for motor control phase current sensing. By choosing the appropriate shunt resistance, any range of current can be monitored, from less than 1 A to more than 100 A.

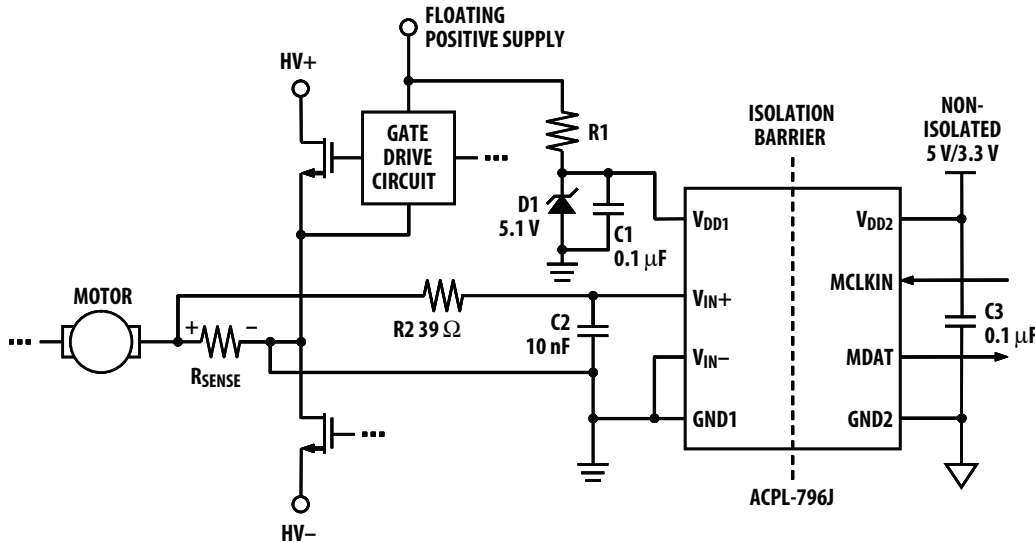


Figure 18. Typical application circuit for motor phase current sensing.

### Power Supplies and Bypassing

As shown in Figure 18, a floating power supply (which in many applications could be the same supply that is used to drive the high-side power transistor) is regulated to 5 V using a simple zener diode ( $D_1$ ); the value of resistor  $R_1$  should be chosen to supply sufficient current from the existing floating supply. The voltage from the current sensing resistor or shunt ( $R_{SENSE}$ ) is applied to the input of the ACPL-796J through an RC anti-aliasing filter ( $R_2$  and  $C_2$ ). And finally, a clock is connected to the ACPL-796J and data are connected to the digital filter. Although the application circuit is relatively simple, a few recommendations should be followed to ensure optimal performance.

The power supply for the isolated modulator is most often obtained from the same supply used to power the power transistor gate drive circuit. If a dedicated supply is required, in many cases it is possible to add an additional winding on an existing transformer. Otherwise, some sort of simple isolated supply can be used, such as a line powered transformer or a high-frequency DC-DC converter.

An inexpensive 78L05 three terminal regulator can also be used to reduce the floating supply voltage to 5 V. To help attenuate high-frequency power supply noise or ripple, a resistor or inductor can be used in series with the input of the regulator to form a low-pass filter with the regulator's input bypass capacitor.

As shown in Figure 18, 0.1  $\mu F$  bypass capacitors ( $C_1$  and  $C_3$ ) should be located as close as possible to the input and output power-supply pins of the isolated modulator. The bypass capacitors are required because of the high-speed digital nature of the signals inside the isolated modulator. A 10 nF bypass capacitor ( $C_2$ ) is also recommended at the input due to the switched-capacitor nature of the input circuit. The input bypass capacitor also forms part of the anti-aliasing filter, which is recommended to prevent high frequency noise from aliasing down to lower frequencies and interfering with the input signal.

### PC Board Layout

The design of the printed circuit board (PCB) should follow good layout practices, such as keeping bypass capacitors close to the supply pins, keeping output signals away from input signals, the use of ground and power planes, etc. In addition, the layout of the PCB can also affect the isolation transient immunity (CMR) of the isolated modulator, due primarily to stray capacitive coupling between the input and the output circuits. To obtain optimal CMR performance, the layout of the PC board should minimize any stray coupling by maintaining the maximum possible distance between the input and output sides of the circuit and ensuring that any ground or power plane on the PC board does not pass directly below or extend much wider than the body of the isolated modulator.

## Shunt Resistors

The current-sensing shunt resistor should have low resistance (to minimize power dissipation), low inductance (to minimize di/dt induced voltage spikes which could adversely affect operation), and reasonable tolerance (to maintain overall circuit accuracy). Choosing a particular value for the shunt is usually a compromise between minimizing power dissipation and maximizing accuracy. Smaller shunt resistances decrease power dissipation, while larger shunt resistances can improve circuit accuracy by utilizing the full input range of the isolated modulator.

The first step in selecting a shunt is determining how much current the shunt will be sensing. The graph in Figure 19 shows the RMS current in each phase of a three-phase induction motor as a function of average motor output power (in horsepower, hp) and motor drive supply voltage. The maximum value of the shunt is determined by the current being measured and the maximum recommended input voltage of the isolated modulator. The maximum shunt resistance can be calculated by taking the maximum recommended input voltage and dividing by the peak current that the shunt should see during normal operation. For example, if a motor will have a maximum RMS current of 10 A and can experience up to 50% overloads during normal operation, then the peak current is 21.1 A ( $= 10 \times 1.414 \times 1.5$ ). Assuming a maximum input voltage of 200 mV, the maximum value of shunt resistance in this case would be about 10 mΩ.

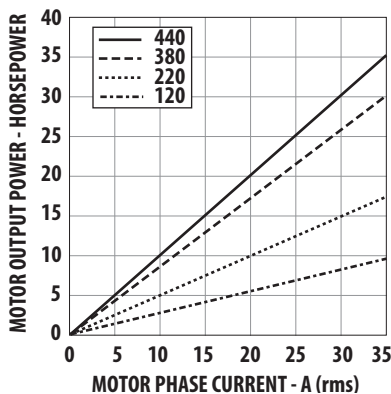


Figure 19. Motor Output Horsepower vs. Motor Phase Current and Supply.

The maximum average power dissipation in the shunt can also be easily calculated by multiplying the shunt resistance times the square of the maximum RMS current, which is about 1 W in the previous example.

If the power dissipation in the shunt is too high, the resistance of the shunt can be decreased below the maximum

value to decrease power dissipation. The minimum value of the shunt is limited by precision and accuracy requirements of the design. As the shunt value is reduced, the output voltage across the shunt is also reduced, which means that the offset and noise, which are fixed, become a larger percentage of the signal amplitude. The selected value of the shunt will fall somewhere between the minimum and maximum values, depending on the particular requirements of a specific design.

When sensing currents large enough to cause significant heating of the shunt, the temperature coefficient (tempco) of the shunt can introduce nonlinearity due to the signal dependent temperature rise of the shunt. The effect increases as the shunt-to-ambient thermal resistance increases. This effect can be minimized either by reducing the thermal resistance of the shunt or by using a shunt with a lower tempco. Lowering the thermal resistance can be accomplished by repositioning the shunt on the PC board, by using larger PC board traces to carry away more heat, or by using a heat sink.

For a two-terminal shunt, as the value of shunt resistance decreases, the resistance of the leads becomes a significant percentage of the total shunt resistance. This has two primary effects on shunt accuracy. First, the effective resistance of the shunt can become dependent on factors such as how long the leads are, how they are bent, how far they are inserted into the board, and how far solder wicks up the lead during assembly (these issues will be discussed in more detail shortly). Second, the leads are typically made from a material such as copper, which has a much higher tempco than the material from which the resistive element itself is made, resulting in a higher tempco for the shunt overall. Both of these effects are eliminated when a four-terminal shunt is used. A four-terminal shunt has two additional terminals that are Kelvin-connected directly across the resistive element itself; these two terminals are used to monitor the voltage across the resistive element while the other two terminals are used to carry the load current. Because of the Kelvin connection, any voltage drops across the leads carrying the load current should have no impact on the measured voltage.

Several four-terminal shunts from Isotek (Isabellenhütte) suitable for sensing currents in motor drives up to 71 Arms (71 hp or 53 kW) are shown in Table 11; the maximum current and motor power range for each of the PBV series shunts are indicated. For shunt resistances from 50 mΩ down to 10 mΩ, the maximum current is limited by the input voltage range of the isolated modulator. For the 5 mΩ and 2 mΩ shunts, a heat sink may be required due to the increased power dissipation at higher currents.

**Table 11. Isotek (Isabellenhütte) four-terminal shunt summary.**

Shunt Resistor Part Number	Shunt Resistance	Tol.	Maximum RMS Current	Motor Power Range 120 V <sub>AC</sub> - 440 V <sub>AC</sub>	
	mΩ	%	A	hp	kW
PBV-R050-0.5	50	0.5	3	0.8 - 3	0.6 - 2
PBV-R020-0.5	20	0.5	7	2 - 7	0.6 - 2
PBV-R010-0.5	10	0.5	14	4 - 14	3 - 10
PBV-R005-0.5	5	0.5	25 [28]	7 - 25 [8 - 28]	5 - 19 [6 - 21]
PBV-R002-0.5	2	0.5	39 [71]	11 - 39 [19 - 71]	8 - 29 [14 - 53]

Note: Values in brackets are with a heatsink for the shunt.

When laying out a PC board for the shunts, a couple of points should be kept in mind. The Kelvin connections to the shunt should be brought together under the body of the shunt and then run very close to each other to the input of the isolated modulator; this minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal. If the shunt is not located on the same PC board as the isolated modulator circuit, a tightly twisted pair of wires can accomplish the same thing.

Also, multiple layers of the PC board can be used to increase current carrying capacity. Numerous plated-through vias should surround each non-Kelvin terminal of the shunt to help distribute the current between the layers of the PC board. The PC board should use 2 or 4 oz. copper for the layers, resulting in a current carrying capacity in excess of 20 A. Making the current carrying traces on the PC board fairly large can also improve the shunt's power dissipation capability by acting as a heat sink. Liberal use of vias where the load current enters and exits the PC board is also recommended.

### Shunt Connections

The recommended method for connecting the isolated modulator to the shunt resistor is shown in Figure 18.  $V_{IN+}$  of the ACPL-796J is connected to the positive terminal of the shunt resistor, while  $V_{IN-}$  is shorted to GND1, with the power-supply return path functioning as the sense line to the negative terminal of the current shunt. This allows a single pair of wires or PC board traces to connect the isolated modulator circuit to the shunt resistor. By referencing the input circuit to the negative side of the sense resistor, any load current induced noise transients on the shunt are seen as a common-mode signal and will not interfere with the current-sense signal. This is important because the large load currents flowing through the motor drive, along with the parasitic inductances inherent

in the wiring of the circuit, can generate both noise spikes and offsets that are relatively large compared to the small voltages that are being measured across the current shunt.

If the same power supply is used both for the gate drive circuit and for the current sensing circuit, it is very important that the connection from GND1 of the isolated modulator to the sense resistor be the only return path for supply current to the gate drive power supply in order to eliminate potential ground loop problems. The only direct connection between the isolated modulator circuit and the gate drive circuit should be the positive power supply line.

In some applications, however, supply currents flowing through the power-supply return path may cause offset or noise problems. In this case, better performance may be obtained by connecting  $V_{IN+}$  and  $V_{IN-}$  directly across the shunt resistor with two conductors, and connecting GND1 to the shunt resistor with a third conductor for the power-supply return path, as shown in Figure 20. When connected this way, both input pins should be bypassed. To minimize electromagnetic interference of the sense signal, all of the conductors (whether two or three are used) connecting the isolated modulator to the sense resistor should be either twisted pair wire or closely spaced traces on a PC board.

The 39 Ω resistor in series with the input lead (R2) forms a low pass anti-aliasing filter with the 10 nF input bypass capacitor (C2) with a 400 kHz bandwidth. The resistor performs another important function as well; it dampens any ringing which might be present in the circuit formed by the shunt, the input bypass capacitor, and the inductance of wires or traces connecting the two. Undamped ringing of the input circuit near the input sampling frequency can alias into the baseband producing what might appear to be noise at the output of the device.

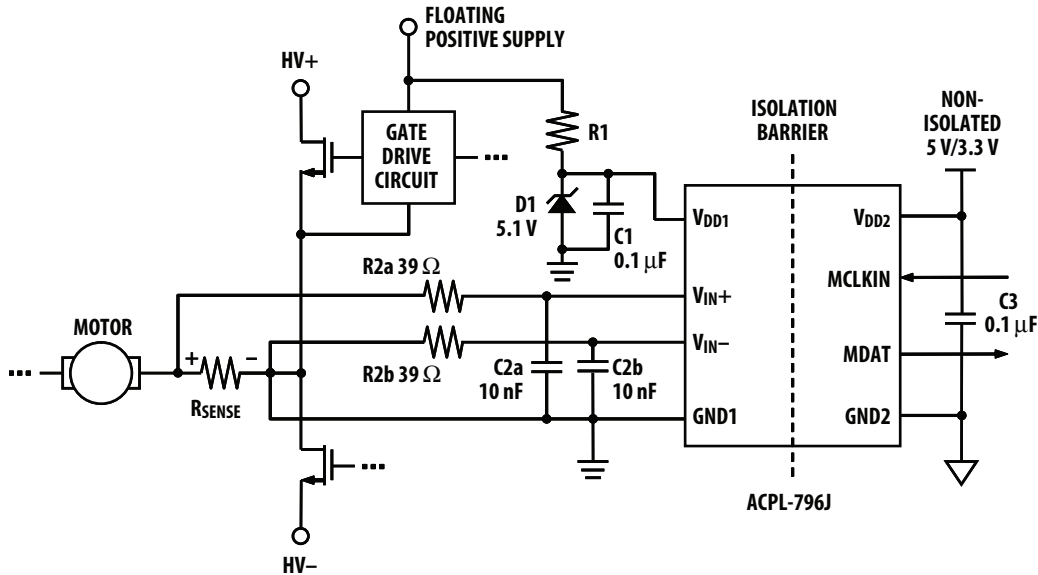


Figure 20. Schematic for three conductor shunt connection.

## Voltage Sensing

The ACPL-796J can also be used to isolate signals with amplitudes larger than its recommended input range with the use of a resistive voltage divider at its input. The only restrictions are that the impedance of the divider be relatively small (less than 1 k $\Omega$ ) so that the input resistance (33 k $\Omega$ ) and input bias current (0.5  $\mu$ A) do not affect the accuracy of the measurement. An input bypass capacitor is still required, although the 39  $\Omega$  series damping resistor

is not (the resistance of the voltage divider provides the same function). The low-pass filter formed by the divider resistance and the input bypass capacitor may limit the achievable bandwidth. To obtain higher bandwidth, the input bypass capacitor (C2) can be reduced, but it should not be reduced much below 1000 pF to maintain adequate input bypassing of the isolated modulator.

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