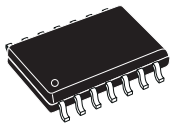
L9669

FAULT TOLERANT CAN TRANSCEIVER

- FAULT TOLERANT DIFFERENTIAL CAN TRANSCEIVER
- OPERATING SUPPLY VOLTAGE 6V TO 28V, TRANSIENTS UP TO 40V
- LOW QUIESCENT CURRENT IN STANDBY MODE (100µA) AND SLEEP MODE (37µA)
- ON CHIP DIAGNOSIS FOR ERRORS ON THE PHYSICAL BUSLINES WITH MICRO CONTROLLER INTERFACE
- OPTIMIZED EMI BEHAVIOUR DUE TO LIMITED AND SYMMETRIC SLOPES OF CAN SIGNALS
- AUTOMATIC SWITCHING TO SINGLE WIRE MODE UPON BUS FAILURES
- TWO-EDGE SENSITIVE WAKE-UP PIN
- SUPPORTS TRANSMISSION WITH GROUND SHIFT VOLTAGES ACCORDING TO GIFT SPECIFICATION:
  - SINGLE WIRE: 1.5V
  - DIFFERENTIAL WIRE: 3V
- AN UNPOWERED NODE OR UNSUFFICIENT SUPPLIES DO NOT DISTURB THE BUS LINES



SO14

ORDERING NUMBER: L9669

DESCRIPTION

The L9669 is an integrated circuit which contains a CAN physical line interface. It integrates all main local functions for automotive body electronic applications connected to a CAN bus.

Obsolete Product(s) - Obsolete Product(s)

Figure 1. Block Diagram

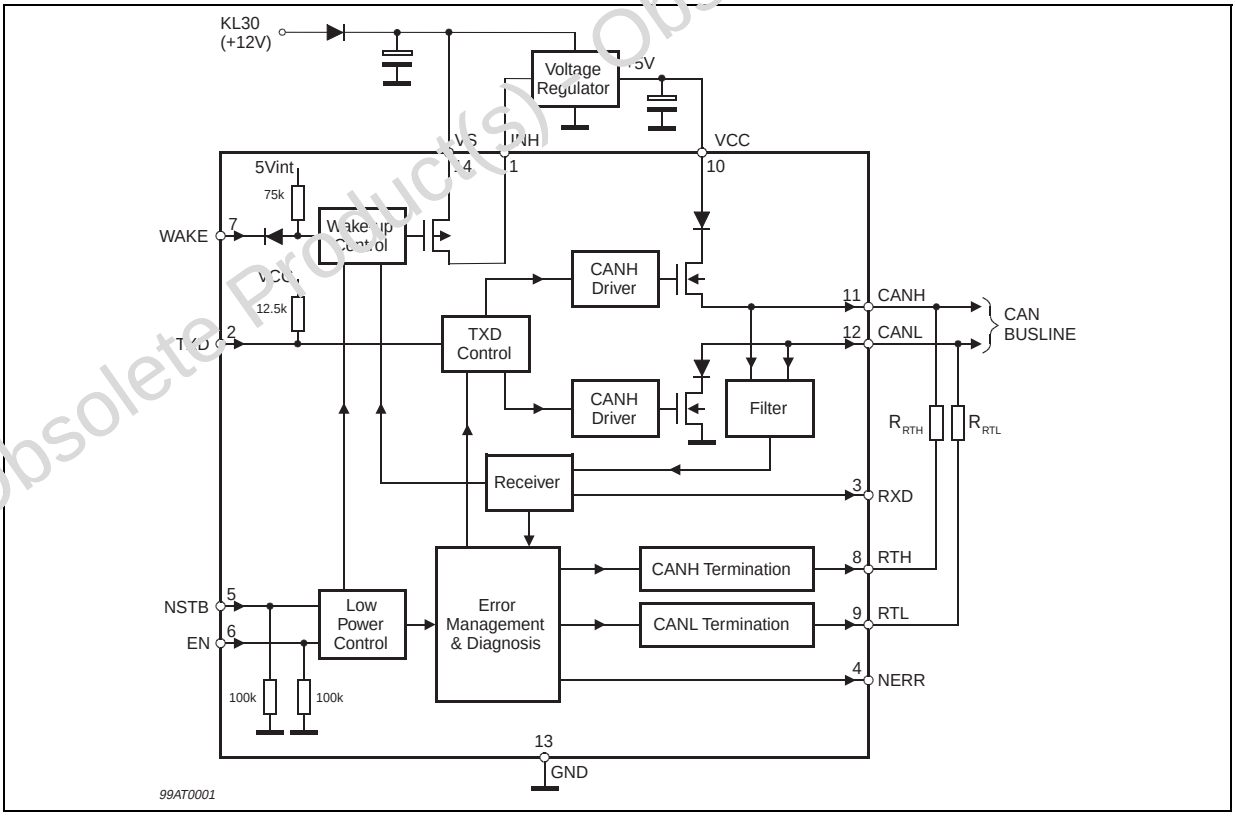


Figure 2. Pin Connection top view.

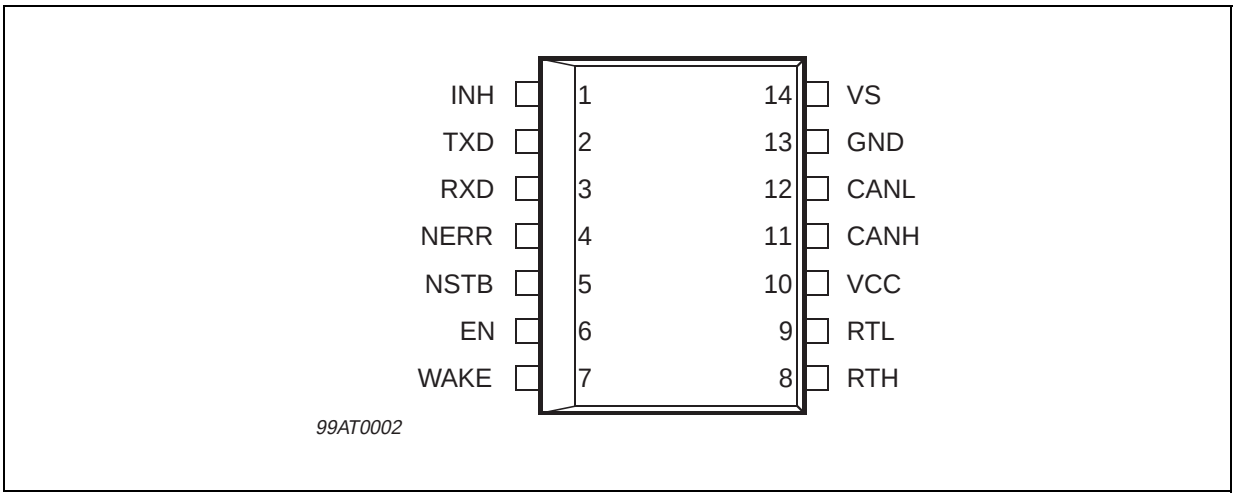


Table 1. Pin Functions

N°	Pin	Function
1	INH	**Inhibit Output** - for switching external 5V Regulator
2	TXD	**Transmit Data Input** - active LOW dominant Bit transmission
3	RXD	**Receive Data Output** - active LOW dominant Bit reception
4	NERR	**Error/Diagnostic Output** - active LOW error/Wake-up and Diagnostic output
5	NSTB	**Not Standby Input** - Digital control signal for low power modes
6	EN	**Enable Input/Diagnostic Clock** - Digital control signal for low power modes/Diagnostic clock
7	WAKE	**Wake-Up Input** - If level of V_{WAKE} changes the device initiates a wake-up from sleep mode by switching INH to VS
8	RTH	**Termination Resistor for CANH** - controlled by internal error management
9	RTL	**Termination Resistor for CANL** - controlled by internal error management
10	VCC	**Supply Voltage Input** - +5V
11	CANH	**High Voltage Bus Line** - High: dominant state
12	CANL	**Low Voltage Bus Line** - Low: dominant state
13	GND	**Ground**
14	VS	**Battery Voltage Input** - +12V

Table 2. Thermal Data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}amb}$	Thermal resistance junction to ambient	120	°C/W

Obsolete Product(s) - Obsolete Product(s)

Table 3. Absolute Maximum Ratings

For externally applied voltages or currents exceeding these limits damage of the circuit may occur!

Symbol	Parameter	Value	Unit
V_{S-DC}	DC operating battery voltage	-0.3 to +28	V
V_{S-P}	Pulse operating battery voltage (t<400ms)	-0.3 to +40	V
V_{CC}	Supply voltage	-0.3 to +6	V
$V_{CANH,L-DC}$	DC voltage CANH, CANL	-28 to +40	V
V_X	Voltage TXD, RXD, NERR, NSTB, EN	-0.3 to V_{CC}+0.3	V
V_{WAKE}	Voltage WAKE	-0.3 to V_S+0.3	V
T_{STG}	Storage temperature	-55 to +150	°C
T_j	Operating junction temperature	-40 to +150	°C

Notes: 1. All pins of the IC are protected against ESD. The verification is performed according to MIL 883C, human body model with R = 1.5kΩ, C = 100pF and discharge voltage ±2kV, corresponding to a maximum discharge energy of 0.2mJ.
2. Voltage forced means voltage limited to specified values while current is not limited. Current forced means voltage unlimited but current limited to specified value.

Table 4. Electrical Characteristcs

V_{CC} = 4.75V to 5.25V, V_S = 6V to 28V, T_j = -40°C to 150°C unless otherwise specified.

Item	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
1	**Supplies**						
1.1	I_{SSL}	Supply current in sleep mode ($I_{SSL} = I_{VS}$)	V_{CC} = 0V, V_S = 14V	15	37	65	µA
1.2	I_{VSSB}	Battery current on pin VS in standby mode	V_{CC} = 5V, V_S = 14V I_{INH} = 0	15	80	135	µA
1.3	I_{VCCSB}	Supply current on pin VCC in standby mode	V_{CC} = 5V, V_S = 14V I_{INH} = 0	10	30	160	µA
1.4	I_{SSB}	Supply current in standby mode ($I_{SSB} = I_{VS} + I_{VCC}$)	V_{CC} = 5V, V_S = 14V I_{INH} = 0	25	110	160	µA
1.5	I_{VSNR}	Battery current on pin VS in normal mode (recessive state)	V_{CC} = 5V, V_S =14V V_{TXD}=V_{CC} no load at CAN	0.1	0.5	3	mA
1.6	I_{VCCNR}	Supply current on pin VCC in normal mode (recessive state)	V_{CC} = 5V, V_S =14V V_{TXD}=V_{CC} no load at CAN	0.4	2.1	8	mA
1.7	I_{SNR}	Supply current in normal mode (recessive state) ($I_{SNR} = I_{VS} + I_{VCC}$)	V_{CC} = 5V, V_S=14V V_{TXD}=V_{CC} no load at CAN	0.5	2.6	10	mA
1.8	I_{VSND}	Battery current on pin VS in normal mode (dominant state)	V_{CC} = 5V, V_S = 14V V_{TXD} = 0 no load at CAN	0.1	0.8	3	mA

Obsolete Product(s) - Obsolete Product(s)

Table 4. Electrical Characteristcs (continued)
V_{CC} = 4.75V to 5.25V, V_S = 6V to 28V, T_j = -40°C to 150°C unless otherwise specified.

Item	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
1.9	I_{VCCND}	Supply current on pin VCC in normal mode (dominant state)	V_{CC} = 5V, V_S = 14V V_{TXD} = 0 no load at CAN	0.2	2.4	7	mA
1.10	I_{SND}	Supply current in normal mode (dominant state) (I_{SND} = I_{VS} + I_{VCC})	V_{CC} = 5V, V_S = 14V V_{TXD} = 0 no load at CAN	0.3	3.4	10	mA
2	**CAN Line Interface**						
2.1	V_{r-d}	Differential receiver recessive to dominant threshold V_{CANH} - V_{CANL}	No bus errors. V_{CC} = 5V	-3.50		-2.20	V
2.2	V_{d-r}	Differential receiver dominant to recessive threshold V_{CANH} - V_{CANL}	No bus errors. V_{CC} = 5V	-3.80		-2.40	V
2.3	V_{CANHr}	CANH recessive output voltage	V_{TXD} = V_{CC} R_{RTH} < 4kΩ			0.35	V
2.4	V_{CANHd}	CANH dominant output voltage	V_{TXD} = 0V I_{CANH} = -40mA	V_{CC}-1.4			V
2.5	V_{CANLr}	CANL recessive output voltage	V_{TXD} = V_{CC} R_{RTH} < 4kΩ	V_{CC}-0.2			V
2.6	V_{CANLd}	CANL dominant output voltage	V_{TXD} = 0V I_{CANL} = 40mA			1.4	V
2.7	I_{CANH}	CANH output current	V_{CANH} = 0V V_{TXD} = 0V	-160	-110	-60	mA
2.8	I_{CANL}	CANL output current	V_{CANL} = 5V V_{TXD} = 0V	60	110	160	mA
2.9	I_{CANHl}	CANH leakage current	V_{CANH} = 14V Sleep mode.	-10	0	10	µA
2.10	I_{CANLl}	CANL leakage current	V_{CANL} = 0V Sleep mode.	-10	0	10	µA
2.11	V_{CANHWK}	CANH wake-up voltage	Sleep/standby mode.	1.2	1.9	2.7	V
2.12	V_{CANLWK}	CANL wake-up voltage	Sleep/standby mode.	2.4	3.1	3.8	V
2.13	V_{CANHs}	CANH single ended receiver threshold	Normal mode. V_{CC} = 5V	1.5	1.8	2.15	V
2.14	V_{CANLs}	CANL single ended receiver threshold	Normal mode. V_{CC} = 5V	2.7	3.1	3.4	V

Obsolete Product(s) - Obsolete Product(s)

Table 4. Electrical Characteristcs (continued)
V_{CC} = 4.75V to 5.25V, V_S = 6V to 28V, T_j = -40°C to 150°C unless otherwise specified.

Item	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
2.15	V_{CANHOV}	CANH overvoltage detection threshold	Normal mode. V_{CC} = 5V	6.6	7.2	7.8	V
2.16	V_{CANLOV}	CANL overvoltage detection threshold	Normal mode. V_{CC} = 5V	6.6	7.2	7.8	V
2.17	t_{drd}	Propagation delay TXD to RXD recessive to dominant	10% to 90% $C_1 = C_2$ = 3.3nF R_1 = 100Ω		1	1.6	µs
2.18	t_{ddr}	Propagation delay TXD to RXD recessive to dominant	10% to 90% $C_1 = C_2$ = 3.3nF R_1 = 100Ω			2.2	µs
2.19	$t_{r,f}$	CANH, CANL output rise/fall time dominant to recessive	10% to 90% $C_1 = C_2$ = 3.3nF R_1 = 100Ω		0.6	1.5	µs
2.20	$t_{r,f}$	CANH, CANL output rise/fall time dominant to recessive	10% to 90% $C_1 = C_2$ = 3.3nF R_1 = 100Ω		2.6	6	µs
2.21	t_{wuCAN}	Minimum dominant time for wake-up on CANH or CANL	Sleep/standby mode.	3		38	µs
2.22	t_{wuWK}	Minimum pulse time for wake-up on WAKE	Sleep/standby mode	4		38	µs
2.23	$C_{CANH-GND}$	Parasitic Capacitance between CANH and GND	Values of Capacitors are not measured in production test, parameters are guaranteed by design		20	40	pF
2.24	$C_{CANL-GND}$	Parasitic Capacitance between CANL and GND			20	40	pF
2.25	$C_{CANH-CANL}$	Parasitic Capacitance between CANH and CANL			5	10	pF
3	**Termination RTH, RTL**						
3.1	R_{RTH}	Internal RTH to GND switch-on resistance	Normal mode. No errors. V_{RTH} = 1V	25	45	100	Ω
3.2	I_{RTH}	Internal RTH to GND pull down current	Normal mode. Error 3. V_{RTH} = 1V	30	65	100	µA
3.3	R_{RTL}	Internal RTL to V_{CC} switch-on resistance	Normal mode. No errors. $V_{RTL} = V_{CC}$ - 1V	25	45	100	Ω

Obsolete Product(s) - Obsolete Product(s)

Table 4. Electrical Characteristcs (continued)
V_{CC} = 4.75V to 5.25V, V_S = 6V to 28V, T_j = -40°C to 150°C unless otherwise specified.

Item	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
3.4	I_{RTL}	Internal RTL to V_{CC} pull up current	Normal mode. Error 4, 6 or 7. $V_{RTL} = V_{CC}$ - 1.5V	-100	-65	-30	µA
3.5	R_{RTL-VS}	Internal RTL to V_S termination resistance	Sleep/standby mode. V_{RTL} = 1V, 5V	8	13	26	kΩ
3.6	V_{RTH}	RTH output voltage	Sleep/standby mode I_{RTH} = 1mA			1	V
3.7	$R_{RTH, RTL}$	External termination resistance	Guaranteed by design	0.5		16	kΩ
4	**Input TXD**						
4.1	V_{TXDh}	TXD high level input voltage		V_{CC}-0.9		V_{CC}	V
4.2	V_{TXDl}	TXD low level input voltage		0		0.9	V
4.3	I_{TXDh}	TXD high level input current	V_{TXD} = 4 V	-200		-25	µA
4.4	I_{TXDl}	TXD low level input current	V_{TXD} = 1 V	-800		-100	µA
5	**Outputs RXD, NERR**						
5.1	V_{Xh}	High level output voltage	I_X = -100µA	V_{CC}-0.9		V_{CC}	V
5.2	V_{Xl}	Low level output voltage	I_X = 100µA	0		0.9	V
5.3	I_{RXDl}	RXD low level output current	$V_{RXD} = V_{VCC}$		1.5		mA
5.4	I_{RXDh}	RXD high level output current	V_{RXD} =0		-1.5		mA
5.5	I_{NERRl}	NERR low level output current	$V_{NERR} = V_{VCC}$		17		mA
5.6	I_{NERRh}	NERR high level output current	V_{NERR} = 0		-0.5		mA
6	**Output INH**						
6.1	V_{dropl}	High level voltage drop ($V_{dropl} = V_S - V_{INH}$)	I_{INH} = -0.18mA Not sleep mode.			1	V
6.2	I_{Il}	Leakage current	V_{INH} = 0V Sleep mode.	-5		5	µA
7	**Inputs NSTB, EN**						
7.1	V_{Xh}	High level input voltage		V_{CC}-0.9		V_{CC}	V
7.2	V_{Xl}	Low level input voltage		0		0.9	V

Obsolete Product(s) - Obsolete Product(s)

Table 4. Electrical Characteristcs (continued)
V_{CC} = 4.75V to 5.25V, V_S = 6V to 28V, T_j = -40°C to 150°C unless otherwise specified.

Item	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
7.3	I_{Xh}	High level input current	V_X = 4 V	10		150	µA
7.4	I_{Xl}	Low level input current	V_X = 1 V	2		40	µA
8	**Input WAKE**						
8.1	V_{WAKEh}	WAKE high level input voltage		3		V_S	V
8.2	V_{WAKEl}	WAKE low level input voltage		0		0.9	V
8.3	$I_{WAKEleak}$	WAKE input leakage current	V_{WAKE} = 5V	-5	0	5	µA
8.4	I_{WAKEl}	WAKE input current	V_{WAKE} = 0	-75	-35	-10	µA
9	**Thermal shutdown**						
9.1	T_{jsd}	Shutdown junction temperature			170		°C
10	**CAN Error detection**						
10.1	$t_{fail38d}$	Error 3, 8 detection time	Normal/RXonly mode.	1.6		3.6	ms
10.2	$t_{fail46710d}$	Error 4, 6, 7, 10 detection time	Normal/RXonly mode.	0.4		1.6	ms
10.3	$t_{fail38r}$	Error 3, 8 recovery time	Normal/RXonly mode.	0.4		1.6	ms
10.4	$t_{fail47r}$	Error 4, 7 recovery time	Normal/RXonly mode.	10		50	µs
10.5	t_{fail6r}	Error 6 recovery time	Normal/RXonly mode.	0.2		0.75	ms
10.6	$t_{fail10r}$	Error 10 recovery time	Normal/RXonly mode.	0.7		4	µs
10.7	$t_{fail38ds}$	Error 3, 8 detection time	Sleep/standby mode.	1.6		3.6	ms
10.8	$t_{fail4rs}$	Error 4 recovery time	Sleep/standby mode.	0.4		1.6	ms
10.9	$t_{fail348rs}$	Error 3, 4, 8 recovery time	Sleep/standby mode.	0.4		1.6	ms
10.10	N_{edge-d}	Edge count difference between CANH and CANL for detection	Normal/RXonly mode. Error 1, 2, 5 or 9.		3		Edges
10.11	N_{edge-r}	Edge count difference between CANH and CANL for recovery	Normal/RXonly mode. Error 1, 2, 5 or 9.		3		Edges
10.12	t_{Dmax}	Diagnostic timeout		15		80	µs
10.13	t_{Hmin}	minimum hold time go to sleep				60	µs

Obsolete Product(s) - Obsolete Product(s)

1. FUNCTIONAL DESCRIPTION

The L9669 is a monolithic integrated circuit which provides all main functions for an automotive body CAN system. The device guarantees a clearly defined behavior in case of failure to avoid permanent CAN bus errors. It is primarily intended for low speed applications in passenger cars.

1.1 Transceiver

– Supports double wire unshielded busses
– Baud rates up to 125 kBaud
– Single wire operation possible (automatic switching to single wire upon bus failures)
– Bus not loaded in case of unpowered transceiver

The CAN transceiver stage is able to transfer serial data on two independent communication wires either differentially (normal operation) or in case of a single wire fault on the remaining line. The physical bitcoding is done using dominant (transmitter active) and overwritable recessive states. Too long dominant phases are detected internally and further transmission is automatically disabled (malfunction of protocol unit does not affect communication on the bus (“fail safe mechanism”)).

1.2 Modes of Operation

Five different functional modes exist to enable or establish the usage of low power or receive only operation.

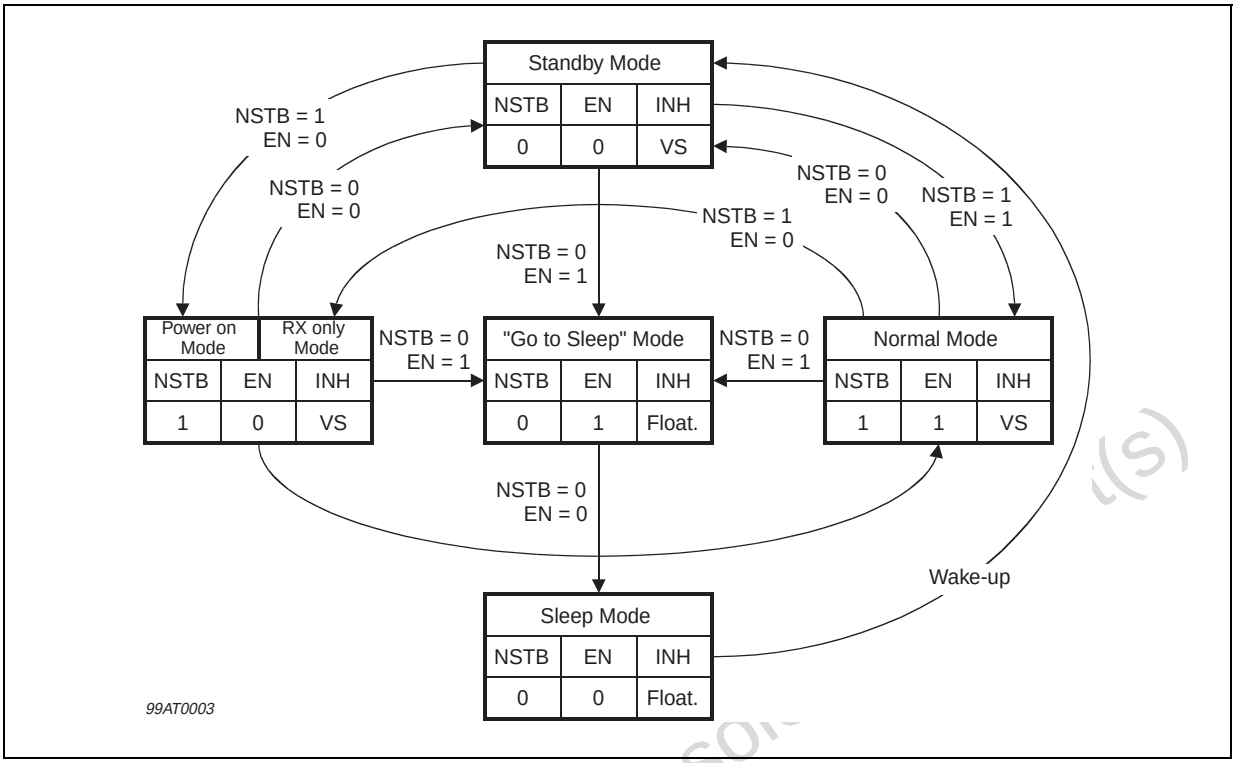
<table>
<tr><th>NSTB</th><th>EN</th><th>Mode</th><th>INH</th><th>NERR</th><th>RXD</th><th>RTL</th></tr>
<tr><td>0</td><td>0</td><td>standby</td><td>VS</td><td colspan="2" rowspan="3">active LOW wake-up interrupt signal (if VCC is present)</td><td rowspan="3">switched to VS (typ. 13kΩ)</td></tr>
<tr><td>0</td><td>0</td><td>sleep</td><td rowspan="2">floating</td></tr>
<tr><td>0</td><td>1</td><td>“go to sleep”</td></tr>
<tr><td>1</td><td>1</td><td>normal</td><td rowspan="3">VS</td><td rowspan="2">active LOW error flag</td><td rowspan="2">HIGH=recessive LOW=dominant received data</td><td rowspan="2">switched to VCC</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">0</td><td>RXonly</td></tr>
<tr><td>Power on</td><td>active LOW VS power-on flag if VCC is present</td><td>active LOW wake-up interrupt signal if VCC is present</td><td>switched to VS</td></tr>
</table>

Note: Wake-up interrupts are released when entering RXonly or normal mode.

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The following state diagram shows these modes and the possible state interactions depending on the input signals NSTB and EN.

Figure 3.



1.3 Error Management

Ten different errors on the physical buslines can be distinguished:

N	Type of Errors	Severity	
		RX	TX
Errors caused by damage of the datalines or isolation			
1	CANH wire interrupted (floating or tied to termination)	0	0
2	CANL wire interrupted (floating or tied to termination)	0	0
3	CANH short circuit to VS (overvoltage condition)	1	1
4	CANL short circuit to GND (permanently dominant)	2	0
5	CANH short circuit to GND (permanently recessive)	0	2
6	CANL short circuit to VS (overvoltage condition)	1	1
7	CANL shorted to CANH	2	2
Errors caused by misbehaviour of transceiver stage			
8	CANH short circuit to VCC (permanently dominant)	2	0
9	CANL short circuit to VCC (permanently recessive)	0	2
Errors caused by defective protocol unit			
10	CANH, CANL driven dominant for more than 1.3 ms	2	2

Not all of these errors leads to a breakdown of the whole communication. So the errors can be categorized into “negligible” (severity 0), “problematic” (severity 1) and “severe” (severity 2).

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Negligible Errors
Transmitter
Error 1, 2, 4 or 8: In all cases data still can be transmitted in differential mode.
Receiver
Error 1, 2, 5 or 9: In all cases data still can be received in differential mode.

Problematic Errors
Transmitter
Error 3 or 6: Data are transmitted using the remaining dataline (single wire).
Receiver
Error 3 or 6: Data are received using the remaining dataline (single wire).

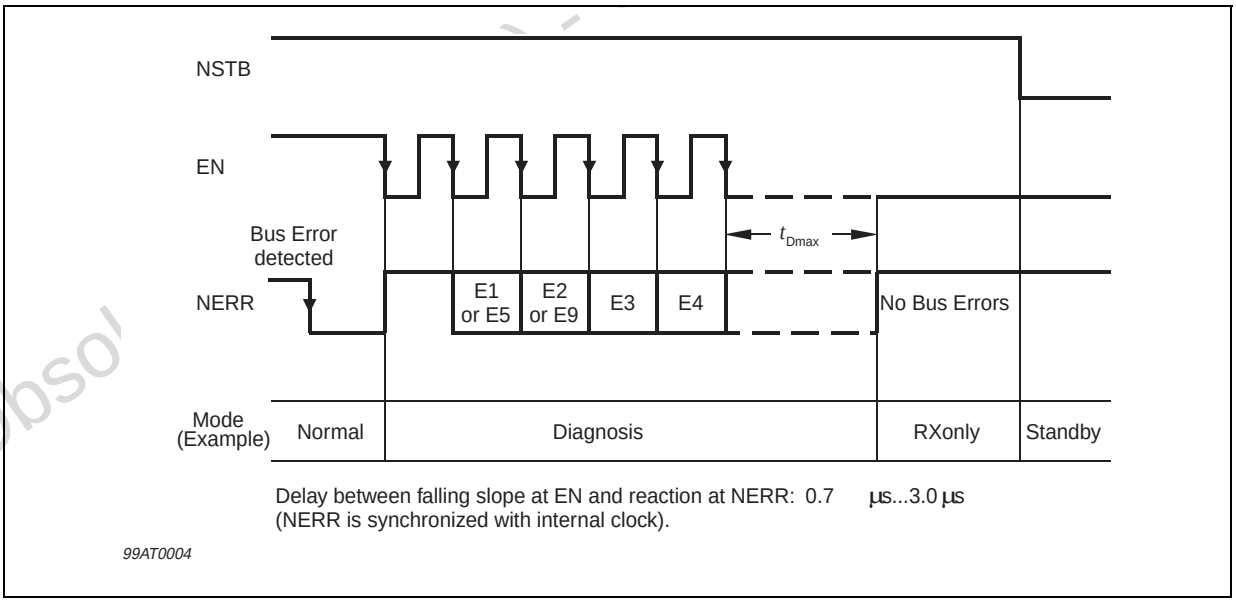
Severe Errors
Transmitter
Error 5 or 9: Data are transmitted using the remaining dataline after short circuit detection.
Error 7: Data are transmitted on CANH or CANL after overcurrent was detected.
Error 10: Transmission is terminated (fail safe).
Receiver
Error 7: Data are received on CANH or CANL after detection of permanent dominant state.
Error 4 or 8: Data are received on CANH or CANL after short circuit was detected.
Error 10: Data are received normally, error is detected by protocol unit.

Upon any error in normal or RXonly mode the NERR output will be forced LOW and released after error recovery.

1.4 Diagnosis

A serial interface is available to retrieve diagnostic informations. Diagnostic data can be requested by using EN as serial clock and evaluating NERR.

Figure 4.



Readout is initialized by a negative edge on EN and acknowledged by NERR entering HIGH state. Following the next negative edge the first error status bit is displayed on NERR according to the data table below. If no

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edge on EN is detected for a time longer than t_{Dmax} diagnosis is disabled and operation continuous in the mode given by NSTB and EN with NERR showing bus errors or wake-up correspondingly. If the clock continues, the readout sequence starts over again with the initial bit set HIGH.

The following errors are displayable (sequence listed in chronological order):

– error status bit 1 (LSB): HIGH if Error 1 or 5
– error status bit 2: HIGH if Error 2 or 9
– error status bit 3: HIGH if Error 3
– error status bit 4: HIGH if Error 4
– error status bit 5: HIGH if Error 6
– error status bit 6: HIGH if Error 8
– error status bit 7: HIGH if Error 10
– error status bit 8: HIGH if Thermal shutdown of Transceiver

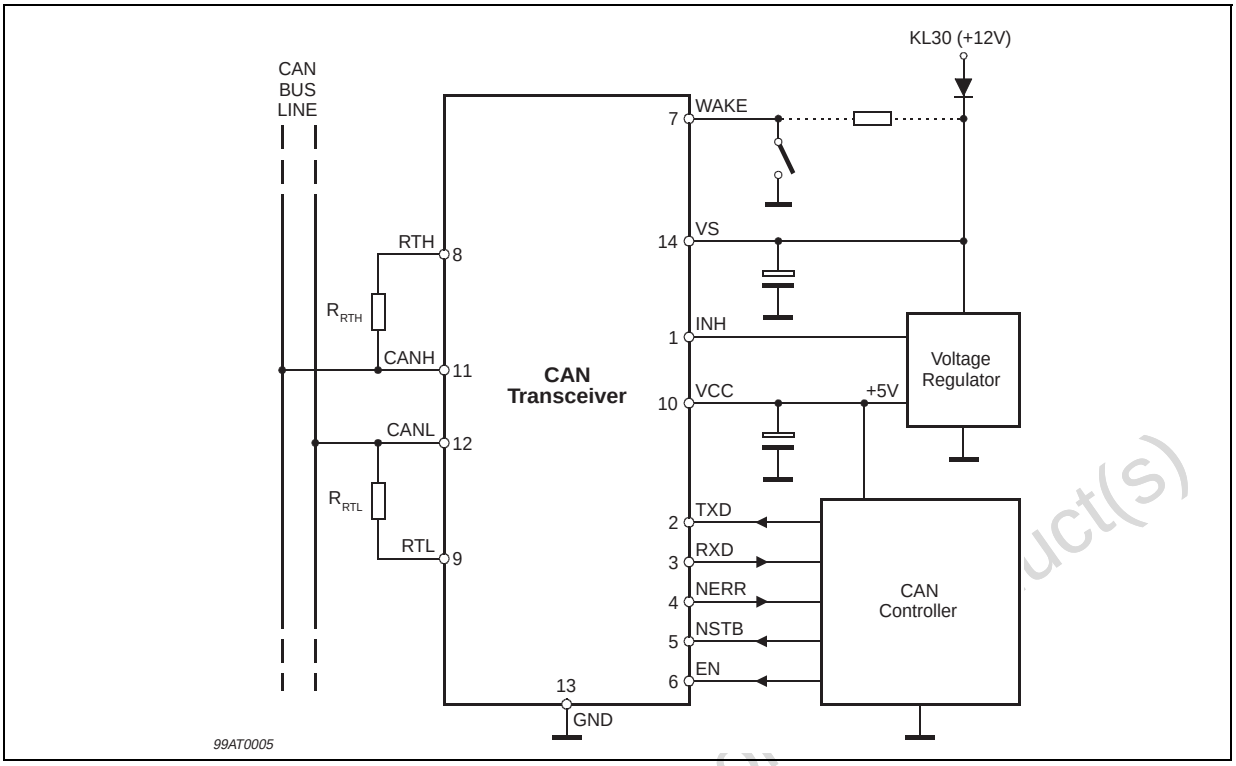
1.5 Protections

A current limiting circuit protects the transmitter outputs against short-circuit to battery, ground and shorted wires.
If the junction temperature exceeds a maximum value, the transmitter output stages are disabled.

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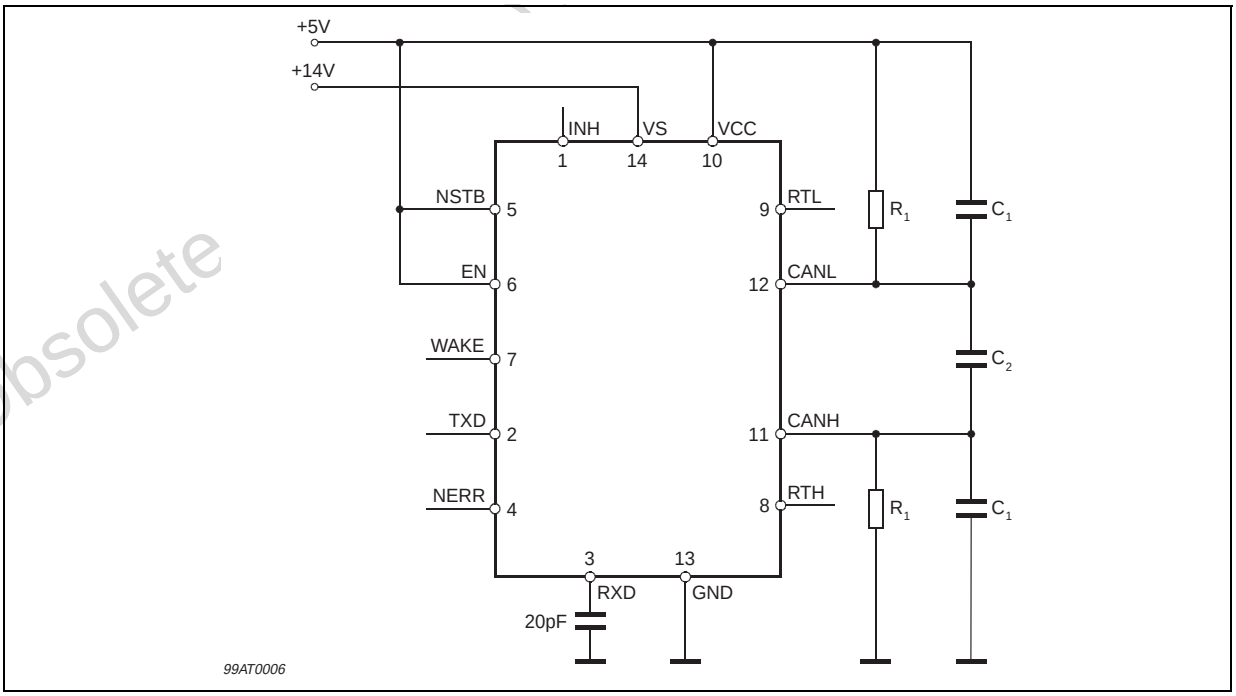
2. APPLICATION CIRCUIT DIAGRAM

Figure 5.



3. TEST CIRCUIT FOR DYNAMIC CHARACTERISTICS

Figure 6.

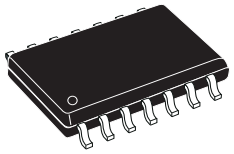


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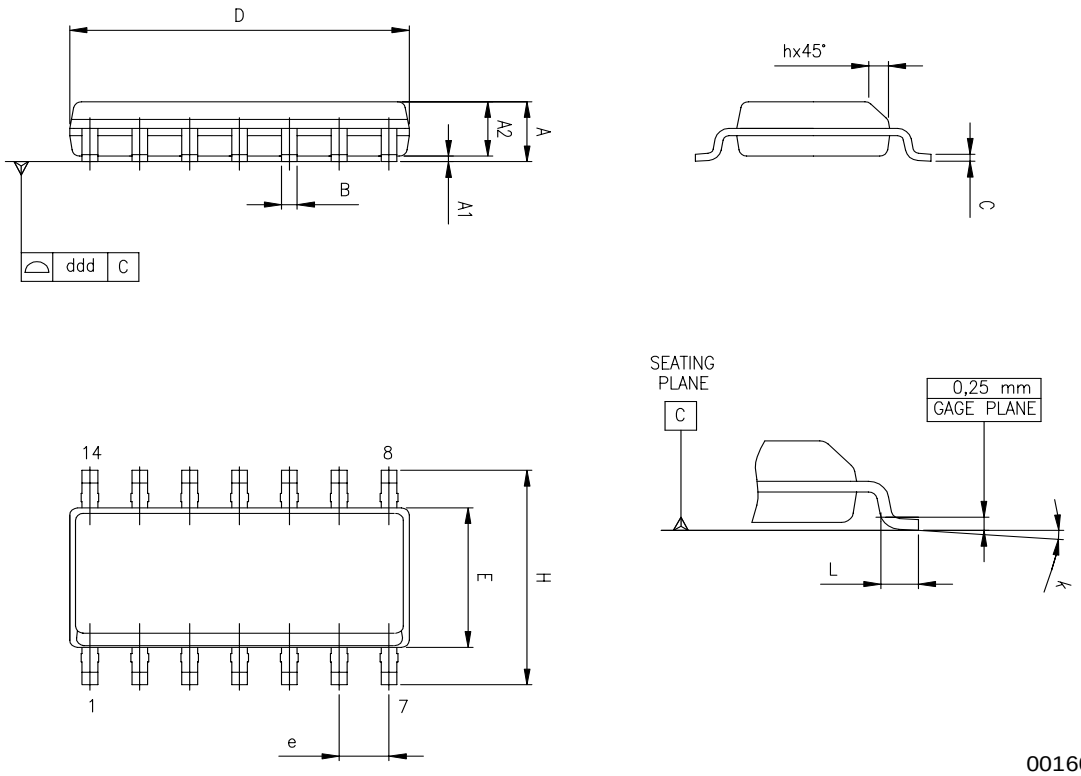
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.30	0.004		0.012
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.01
D (1)	8.55		8.75	0.337		0.344
E	3.80		4.0	0.150		0.157
e		1.27			0.050	
H	5.8		6.20	0.228		0.244
h	0.25		0.50	0.01		0.02
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA



SO14



0016019 D

Obsolete Product(s) - Obsolete Product(s)

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