# MCP1501

## High-Precision Buffered Voltage Reference

### Features

- Maximum Temperature Coefficient: 50 ppm/°C from –40°C to +125°C
- Initial Accuracy: 0.1%
- Operating Temperature Range: –40 to +125°C
- Low Typical Operating Current: 140 µA
- Line Regulation: 50 ppm/V Maximum
- Load Regulation: 40 ppm/mA Maximum
- 8 Voltage Variants Available:
  - 1.024V
  - 1.250V
  - 1.800V
  - 2.048V
  - 2.500V
  - 3.000V
  - 3.300V
  - 4.096V
- Output Noise: 27 µVRMS, 10 Hz to 10 kHz (1.024V)

### Applications

- Precision Data Acquisition Systems
- High-Resolution Data Converters
- Medical Equipment Applications
- Industrial Controls
- Battery-Powered Devices

### General Description

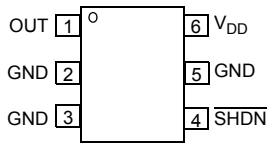
The MCP1501 is a buffered voltage reference capable of sinking and sourcing 20 mA of current. The voltage reference is a low-drift bandgap-based reference. The bandgap uses chopper-based amplifiers, effectively reducing the drift to zero.

The MCP1501 is available in the following packages:

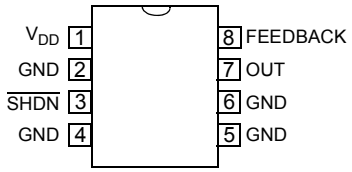
- 6-Lead SOT-23
- 8-Lead SOIC
- 8-Lead 2 mm x 2 mm WDFN

### Package Types

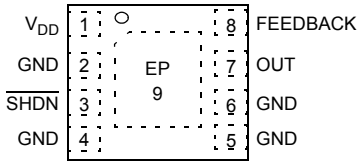
MCP1501
6-Lead SOT-23




MCP1501
8-Lead SOIC




MCP1501
2x2 WDFN*




*Includes Exposed Thermal Pad (EP). See Table 3-1

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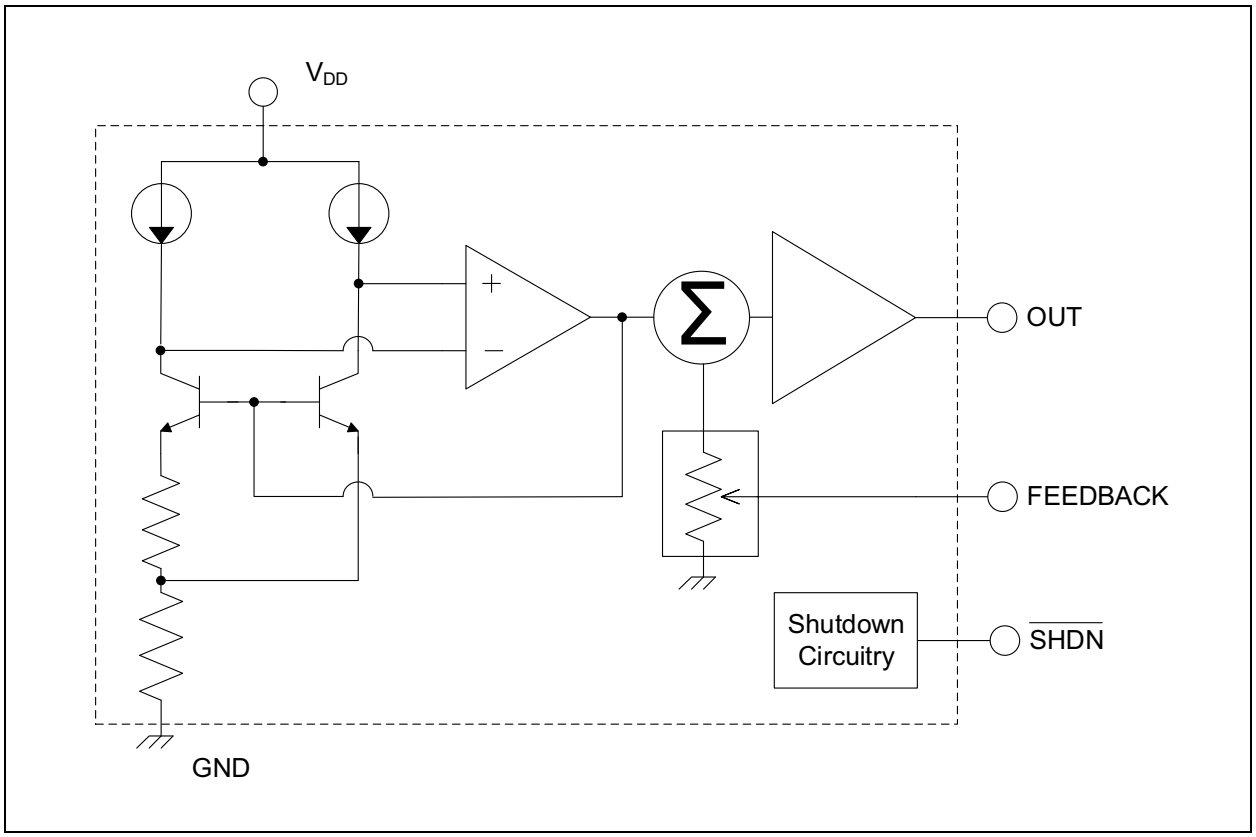
## BLOCK DIAGRAM





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# 1.0 ELECTRICAL CHARACTERISTICS

## Absolute Maximum Ratings(†)

$V_{DD}$ ..... 5.5V
Maximum current into $V_{DD}$ pin ..... 30 mA
Clamp current, $I_K$ ($V_{PIN}$ < 0 or $V_{PIN}$ > $V_{DD}$) ..... ±20 mA
Maximum output current sunk by OUTPUT pin ..... 30 mA
Maximum output current sourced by OUTPUT pin ..... 30 mA
(HBM:CDM:MM) ..... (2 kV:±1.5 kV:200V)

† **Notice**: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

**TABLE 1-1: DC CHARACTERISTICS**

| **Electrical Characteristics:** Unless otherwise specified, $V_{DD(MIN)} \le V_{DD} \le 5.5V$ at –40°C ≤ $T_A$ ≤ +125°C. | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Characteristic** | | **Sym.** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| Supply Voltage | | $V_{DD}$ | 1.65 | — | 5.5 | V | MCP1501-10 |
| | | $V_{DD}$ | 1.65 | — | 5.5 | V | MCP1501-12 |
| | | $V_{DD}$ | 2.0 | — | 5.5 | V | MCP1501-18 |
| | | $V_{DD}$ | 2.25 | — | 5.5 | V | MCP1501-20 |
| | | $V_{DD}$ | 2.70 | — | 5.5 | V | MCP1501-25 |
| | | $V_{DD}$ | 3.2 | — | 5.5 | V | MCP1501-30 |
| | | $V_{DD}$ | 3.5 | — | 5.5 | V | MCP1501-33 |
| | | $V_{DD}$ | 4.3 | — | 5.5 | V | MCP1501-40 |
| Power-on-Reset Release Voltage | | $V_{POR}$ | — | 1.45 | — | V | |
| Power-on-Reset Rearm Voltage | | — | — | 0.8 | — | V | |
| Output Voltage | MCP1501-10 | $V_{OUT}$ | 1.0230 | 1.0240 | 1.0250 | V | |
| | MCP1501-12 | | 1.2488 | 1.2500 | 1.2513 | V | |
| | MCP1501-18 | | 1.7982 | 1.800 | 1.8018 | V | |
| | MCP1501-20 | | 2.0460 | 2.0480 | 2.0500 | V | |
| | MCP1501-25 | | 2.4975 | 2.500 | 2.5025 | V | |
| | MCP1501-30 | | 2.9970 | 3.000 | 3.0030 | V | |
| | MCP1501-33 | | 3.2967 | 3.300 | 3.3033 | V | |
| | MCP1501-40 | | 4.0919 | 4.0960 | 4.1001 | V | |
| Temperature Coefficient | MCP1501-XX | $T_C$ | — | 10 | 50 | ppm/°C | |
| Line Regulation | | $\Delta V_{OUT}$ / $\Delta V_{IN}$ | — | 5 | 50 | ppm/V | |
| Load Regulation | | $\Delta V_{OUT}$ / $\Delta I_{OUT}$ | — | 10 ppm – sink<br>15 ppm – source | 40 ppm – sink<br>70 ppm – source | ppm/mA | –5 mA < $I_{LOAD}$ < +5 mA |
| Dropout Voltage | | $V_{DO}$ | — | — | 200 | mV | –5 mA < $I_{LOAD}$ < +2 mA |
| Power Supply Rejection Ratio | | PSRR | | 94 dB | | | 1.024V option, $V_{IN}$ = 5.5V, 60 Hz at 100 $mV_{P-P}$ |

**TABLE 1-1: DC CHARACTERISTICS (CONTINUED)**

| Electrical Characteristics: Unless otherwise specified, $V_{DD(MIN)} \le V_{DD} \le 5.5V$ at –40°C ≤ $T_A$ ≤ +125°C. | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Characteristic** | | **Sym.** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| Shutdown | | $V_{IL}$ | | 1.35 | | | $V_{IN}$ = 5.5V |
| | | $V_{IH}$ | | 3.80 | | | |
| Output Voltage Hysteresis | | $\Delta V_{OUT_HYST}$ | | 300 µV | | | Refer to **Section 1.1.10 "Output Voltage Hysteresis"** for additional details on testing conditions. |
| Output Noise | MCP1501-10 | $e_N$ | — | 14 | — | µVRMS | 0.1 Hz to 10 Hz, $T_A$ = +25°C |
| | | | — | 27 | — | | 10 Hz to 10 kHz, $T_A$ = +25°C |
| | MCP1501-40 | $e_N$ | — | 20 | — | µVRMS | 0.1 Hz to 10 Hz, $T_A$ = +25°C |
| | | | — | 110 | — | | 10 Hz to 10 kHz, $T_A$ = +25°C |
| Maximum Load Current | | $I_{LOAD}$ | — | ±20 | — | mA | $T_A$ = +25°C<br>2.048V option |
| Supply Current | | $I_{DD}$ | — | 140 | 550 | µA | No Load |
| | | | — | — | 350 | | No Load, $T_A$ = +25°C |
| Shutdown Current | MCP1501-10 | $I_{SHDN}$ | | 205 | | nA | $T_A$ = +25°C |
| | MCP1501-20 | | | 185 | | | |
| | MCP1501-40 | | | 185 | | | |

**TABLE 1-2: TEMPERATURE SPECIFICATIONS**

| Electrical Specifications: Unless otherwise indicated, all parameters apply at $AV_{DD}$, $DV_{DD}$ = 2.7 to 3.6V. | | | | | | |
|---|---|---|---|---|---|---|
| **Parameters** | **Sym.** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| **Temperature Ranges** | | | | | | |
| Operating Temperature Range | $T_A$ | –40 | — | +125 | °C | |
| Storage Temperature Range | $T_A$ | –65 | — | +150 | °C | |
| **Thermal Package Resistance** | | | | | | |
| Thermal Resistance for SOT-23-6 | $\theta_{JA}$ | — | +190.5 | — | °C/W | |
| Thermal Resistance for SOIC-8 | $\theta_{JA}$ | — | +149.5 | — | °C/W | |
| Thermal Resistance for DFN-8 | $\theta_{JA}$ | — | +141.3 | — | °C/W | |


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## 1.1 Terminology

### 1.1.1 OUTPUT VOLTAGE

Output voltage is the reference voltage that is available on the OUT pin.

### 1.1.2 INPUT VOLTAGE

The input voltage ($V_{IN}$) is the range of voltage that can be applied to the $V_{DD}$ pin and still have the device produce the designated output voltage on the OUT pin.

### 1.1.3 TEMPERATURE COEFFICIENT ($TC_{OUT}$)

The output temperature coefficient or voltage drift is a measure of how much the output voltage will vary from its initial value with changes in ambient temperature. The value specified in the electrical specifications is measured as shown in Equation 1-1.

**EQUATION 1-1: $TC_{OUTPUT}$ CALCULATION**

$$TC_{OUT} = \frac{V_{OUT(MAX)} - V_{OUT(MIN)}}{\Delta T \times V_{OUT(NOM)}} \times 10^6 \; ppm/°C$$

Where:

| | | |
|---|---|---|
| $V_{OUT(MAX)}$ | = | Maximum output voltage over the temperature range |
| $V_{OUT(MIN)}$ | = | Minimum output voltage over the temperature range |
| $V_{OUT(NOM)}$ | = | Average output voltage over the temperature range |
| $\Delta T$ | = | Temperature range over which the data was collected |

### 1.1.4 DROPOUT VOLTAGE

The dropout voltage is defined as the voltage difference between $V_{DD}$ and $V_{OUT}$ under load. Equation 1-2 is used to calculate the dropout voltage.

**EQUATION 1-2:**

$$V_{DO} = V_{IN} - V_{OUT} \mid I_{OUT} = Constant$$

### 1.1.5 LINE REGULATION

An ideal voltage reference will maintain a constant output voltage regardless of any changes to the input voltage. However, when real devices are considered, a small error may be measured on the output when an input voltage change occurs.

Line regulation is defined as the change in output voltage ($\Delta V_{OUT}$) as a function of a change in input voltage ($\Delta V_{IN}$), and expressed as a percentage, as shown in Equation 1-3.

**EQUATION 1-3:**

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} \times 100\% = \%\ Line\ Regulation$$

Line regulation may also be expressed as %/V or in ppm/V, as shown in Equation 1-4 and Equation 1-5, respectively.

**EQUATION 1-4:**

$$\frac{\left(\frac{\Delta V_{OUT}}{V_{OUT(NOM)}}\right)}{\Delta V_{IN}} \times 100\% = \frac{\%}{V}\ Line\ Regulation$$

**EQUATION 1-5:**

$$\frac{\left(\frac{\Delta V_{OUT}}{V_{OUT(NOM)}}\right)}{\Delta V_{IN}} \times 10^6 = \frac{ppm}{V}\ Line\ Regulation$$

As an example, if the MCP1501-20 is implemented in a design and a 2 µV change in output voltage is measured from a 250 mV change on the input, then the error in percent, ppm, percent/volt, and ppm/volt, as shown in Equation 1-6 – Equation 1-9.

**EQUATION 1-6:**

$$\left(\frac{\Delta V_{OUT}}{\Delta V_{IN}} \times 100\%\right) \times \left(\frac{2\ \mu V}{250\ mV} \times 100\%\right) = .0008\%$$

**EQUATION 1-7:**

$$\left(\frac{\Delta V_{OUT}}{\Delta V_{IN}} \times 10^6\right) \times \left(\frac{2\ \mu V}{250\ mV} \times 10^6\right) = 8\ ppm$$

**EQUATION 1-8:**

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} \times 100\% = \left(\frac{\left(\frac{2\ \mu V}{2.048 V}\right)}{250\ mV}\right) \times 100\% = 0.000390625\ \frac{\%}{V}$$

**EQUATION 1-9:**

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} \times 10^6 = \left(\frac{\left(\frac{2\ \mu V}{2.048 V}\right)}{250\ mV}\right) \times 10^6 = 3.90625\ \frac{ppm}{V}$$

### 1.1.6 LOAD REGULATION

An ideal voltage reference will maintain the specified output voltage regardless of the load's current demand. However, real devices experience a small error voltage that deviates from the specified output voltage when a load is present.

Load regulation is defined as the voltage difference when under no load ($V_{OUT}$ @ $I_{OUT|0}$) and under maximum load ($V_{OUT}$ @ $I_{OUT|MAX}$), and is expressed as a percentage, as shown in Equation 1-10.

**EQUATION 1-10:**

$$\frac{V_{OUT}\ @\ I_{OUT|0} - V_{OUT}\ @\ I_{OUT|MAX}}{V_{OUT}\ @\ I_{OUT|0}} \times 100\% = \%\ Load\ Regulation$$

Similar to line regulation, load regulation may also be expressed as %/mA or in ppm/mA as shown in Equation 1-11 and Equation 1-12, respectively.

**EQUATION 1-11:**

$$\frac{\left(\frac{\Delta V_{OUT}}{V_{OUT(NOM)}}\right)}{\Delta I_{OUT}} \times 100\% = \frac{\%}{mA}\ Load\ Regulation$$

**EQUATION 1-12:**

$$\frac{\left(\frac{\Delta V_{OUT}}{V_{OUT(NOM)}}\right)}{\Delta I_{OUT}} \times 10^6 = \frac{ppm}{mA}\ Load\ Regulation$$

As an example, if the MCP1501-20 is implemented in a design and a 10 µV change in output voltage is measured from a 2 mA change on the input, then the error in percent, ppm, percent/volt, ppm/volt, as shown in Equation 1-13 – Equation 1-16.

**EQUATION 1-13:**

$$\frac{2.048V - 2.04799V}{2.04799V} \times 100\% = .0004882\%$$

**EQUATION 1-14:**

$$\frac{2.048V - 2.04799V}{2.04799V} \times 10^6 = \left(\frac{2.048V - 2.04799V}{2.04799V} \times 10^6\right) = 4.882\ ppm$$

**EQUATION 1-15:**

$$\frac{\left(\frac{\Delta V_{OUT}}{V_{OUT(NOM)}}\right)}{\Delta I_{OUT}} \times 100\% = \left(\frac{\left(\frac{10\ \mu V}{2.048V}\right)}{2\ mA}\right) \times 100\% = 0.2441\ \frac{\%}{mA}$$

**EQUATION 1-16:**

$$\frac{\left(\frac{\Delta V_{OUT}}{V_{OUT(NOM)}}\right)}{\Delta I_{OUT}} \times 10^6 = \left(\frac{\left(\frac{10\ \mu V}{2.048V}\right)}{2\ mA}\right) \times 10^6 = 2.441\ \frac{ppm}{mA}$$


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### 1.1.7 INPUT CURRENT

The input current (operating current) is the current that sinks from $V_{IN}$ to GND without a load current on the output pin. This current is affected by temperature, input voltage, output voltage, and the load current.

### 1.1.8 POWER SUPPLY REJECTION RATIO

Power supply rejection ratio (PSRR) is a measure of the change in output voltage ($\Delta V_{OUT}$) relative to the change in input voltage ($\Delta V_{IN}$) over frequency.

### 1.1.9 LONG-TERM DRIFT

The long-term output stability is measured by exposing the devices to an ambient temperature of +125°C, as shown in Figure 2-18 while configured in the circuit shown in Figure 1-1. In this test, all electrical specifications of the devices are measured periodically at +25°C.

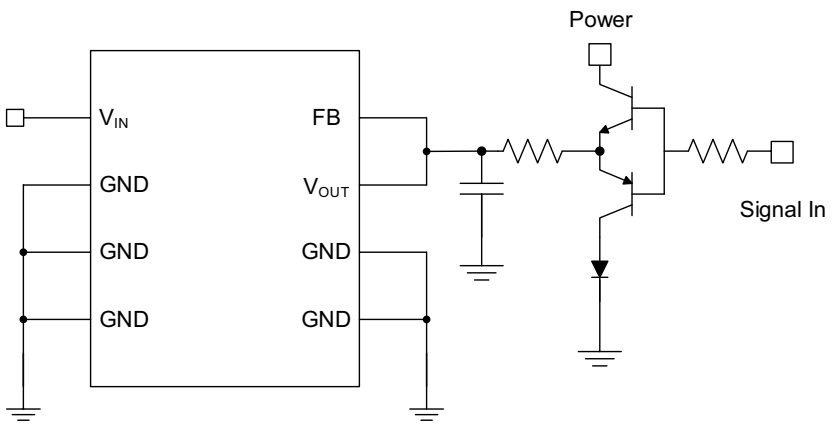


***FIGURE 1-1:*** *Long-Term Drift Test Circuit.*

### 1.1.10 OUTPUT VOLTAGE HYSTERESIS

The output voltage hysteresis is a measure of the output voltage error after the powered devices are cycled over the entire operating temperature range. The amount of hysteresis can be quantified by measuring the change in the +25°C output voltage after temperature excursions from +25°C to +125°C to +25°C, and also from +25°C to –40°C to +25°C.

## 2.0 TYPICAL OPERATING CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

**Note:** Unless otherwise specified, maximum values are: $V_{DD(MIN)} \leq V_{DD} \leq 5.5V$ at $-40°C \leq T_A \leq +125°C$.

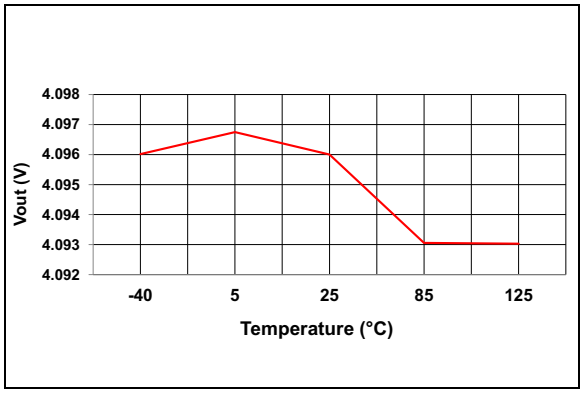


***FIGURE 2-1:*** *$V_{OUT}$ vs. Temperature, No Load, 4.096V Option.*

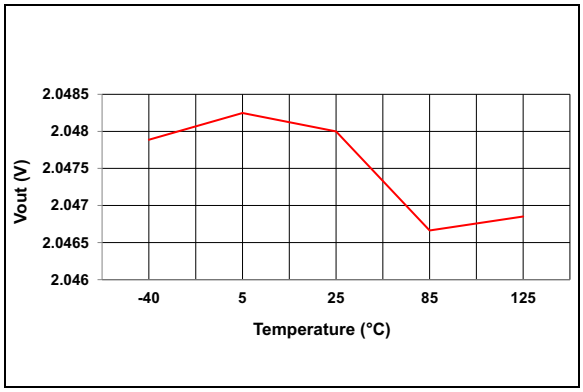


***FIGURE 2-2:*** *$V_{OUT}$ vs. Temperature, No Load, 2.048V Option.*

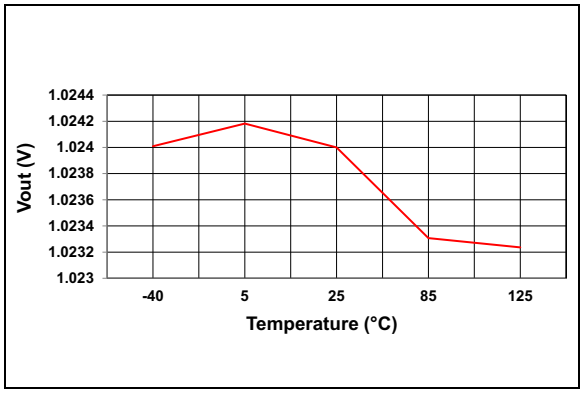


***FIGURE 2-3:*** *$V_{OUT}$ vs. Temperature, No Load, 1.024V Option.*

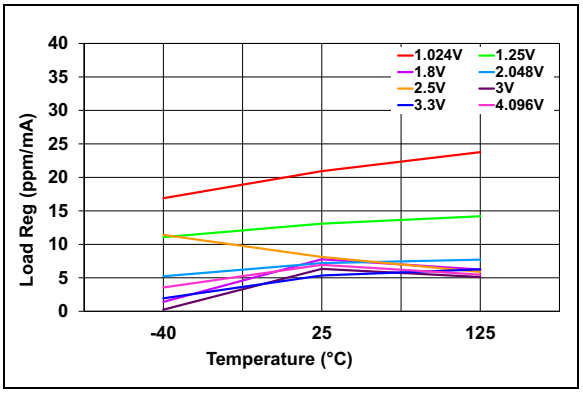


***FIGURE 2-4:*** *Load Regulation vs. Temperature, $I_{LOAD}$ 5mA Sink.*

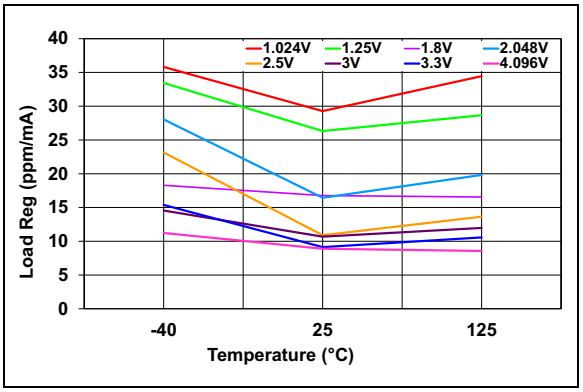


***FIGURE 2-5:*** *Load Regulation vs. Temperature, $I_{LOAD}$ 5mA Source.*

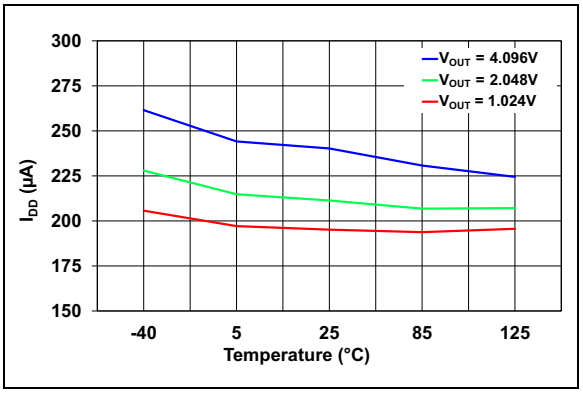


***FIGURE 2-6:*** *$I_{DD}$ vs. Temperature, All Options.*


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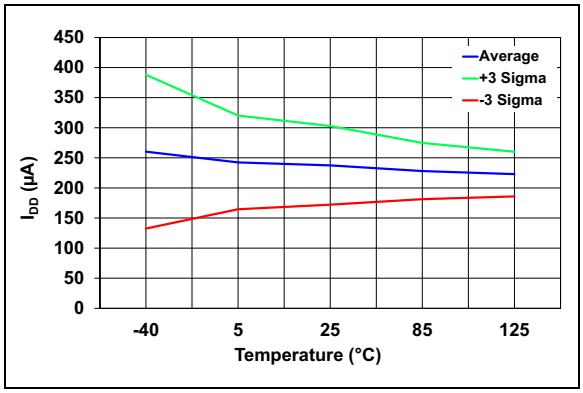


***FIGURE 2-7:*** *$I_{DD}$ vs. Temperature for $V_{OUT}$, 50 Units, No Load, 4.096V Option.*

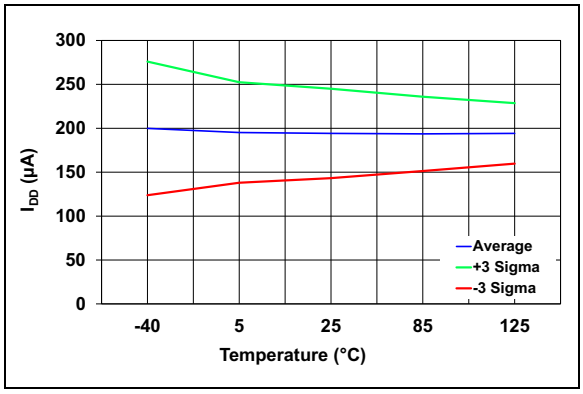


***FIGURE 2-8:*** *$I_{DD}$ vs. Temperature for $V_{OUT}$, 50 Units, No Load, 1.024V Option.*

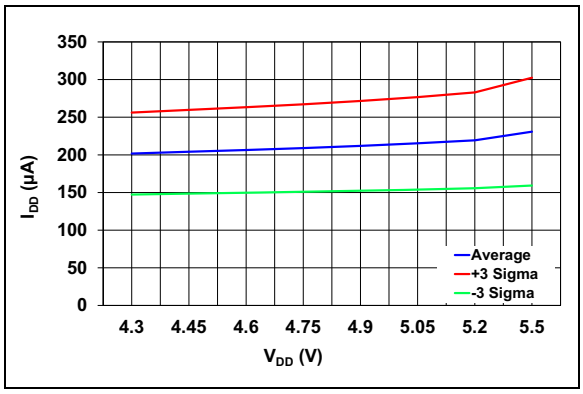


***FIGURE 2-9:*** *$I_{DD}$ vs. $V_{DD}$, $V_{OUT}$ = 4.096V, 50 Units, No Load.*

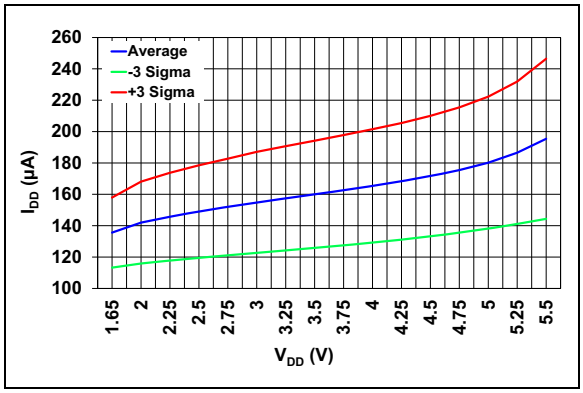


***FIGURE 2-10:*** *$I_{DD}$ vs. $V_{DD}$, $V_{OUT}$ = 1.024V, 50 Units, No Load.*

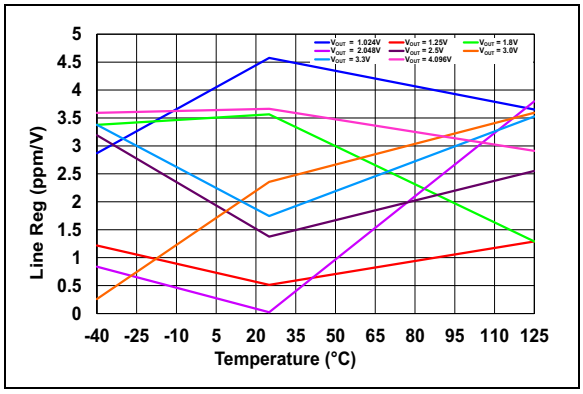


***FIGURE 2-11:*** *Line Regulation vs. Temperature.*

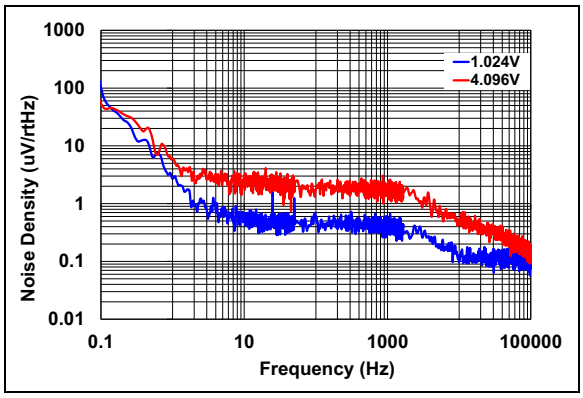


***FIGURE 2-12:*** *Noise vs. Frequency, No Load, $T_A$ = +25°C.*

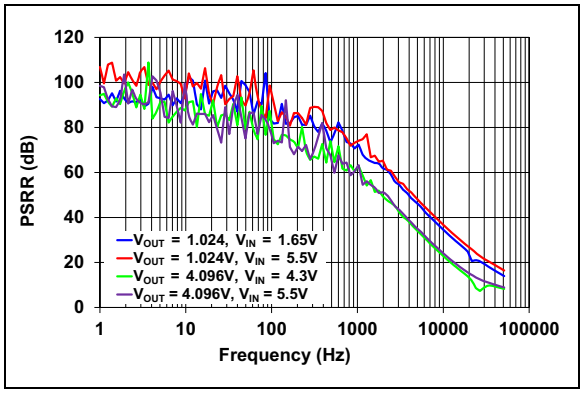


***FIGURE 2-13:*** *PSRR vs. Frequency, No Load, $T_A$ = +25°C.*

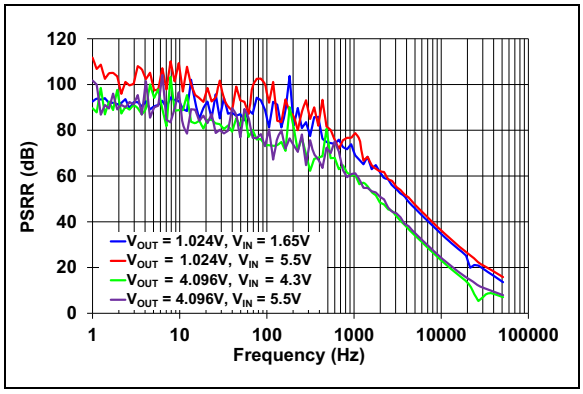


***FIGURE 2-14:*** *PSRR vs. Frequency, 1 kΩ Load, $T_A$ = +25°C.*

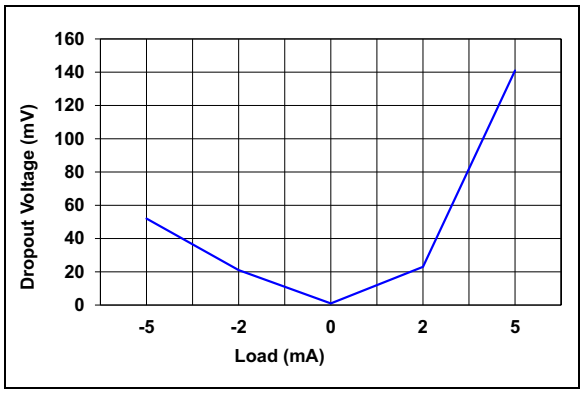


***FIGURE 2-15:*** *Dropout Voltage vs. Load, $T_A$ = +25°C, 2.048V Option.*

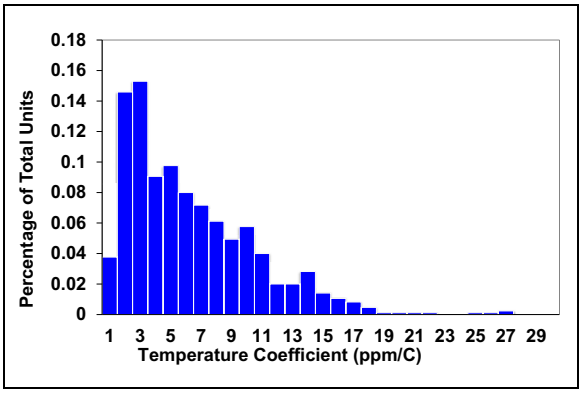


***FIGURE 2-16:*** *Tempco Distribution, No Load, $T_A$ = +25°C, $V_{DD}$ = 2.7V, 50 Units.*

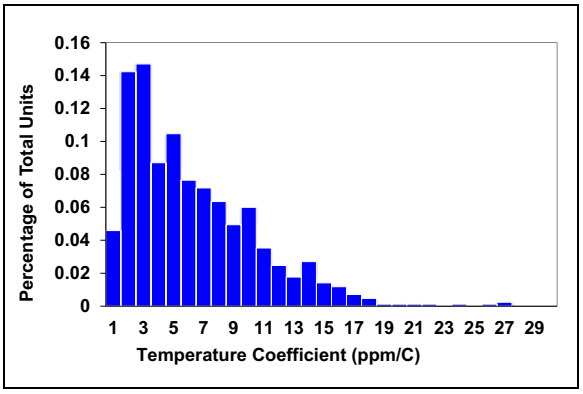


***FIGURE 2-17:*** *Tempco Distribution, No Load, $T_A$ = +25°C, $V_{DD}$ = 5.5V, 50 Units.*

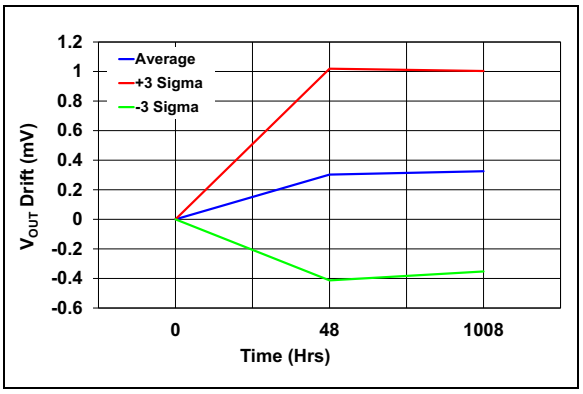


***FIGURE 2-18:*** *$V_{OUT}$ Drift vs. Time, $T_A$ = +25°C, No Load, 800 Units.*


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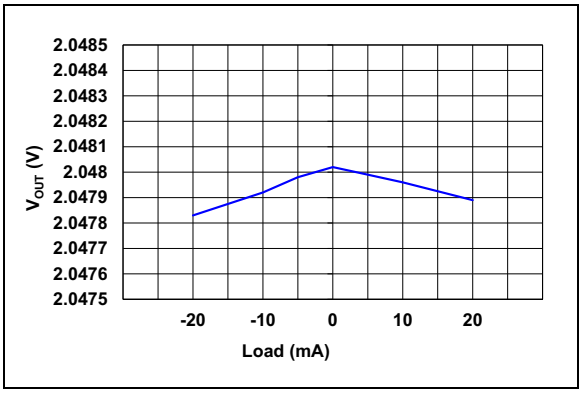


***FIGURE 2-19:*** *$V_{OUT}$ vs. Load, $T_A$ = +25°C, 2.048V Option.*

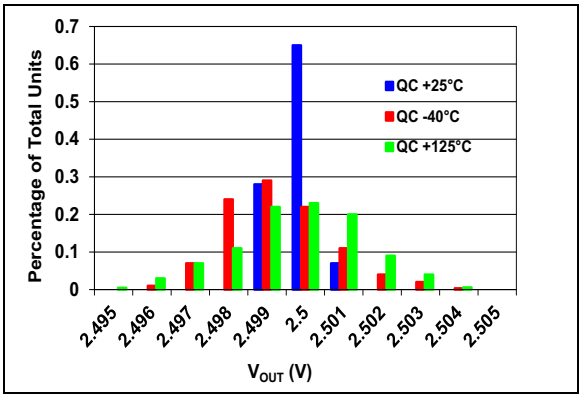


***FIGURE 2-20:*** *$V_{OUT}$ at $V_{DDMIN}$, $V_{DD}$ = 2.7V, 800 Units, 2.5V Option, No Load.*

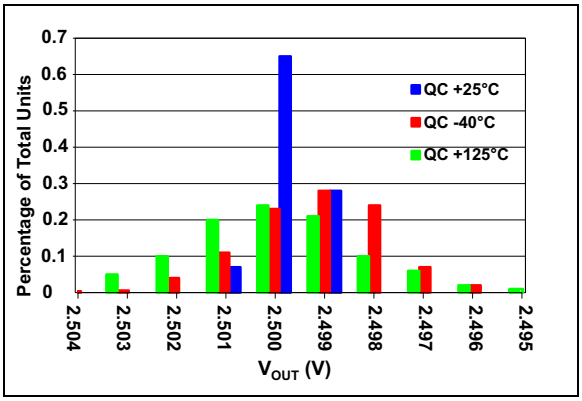


***FIGURE 2-21:*** *$V_{OUT}$ Distribution at $V_{DDMAX}$, $V_{DD}$ = 5.5V, 800 Units, 2.5V Option, No Load.*

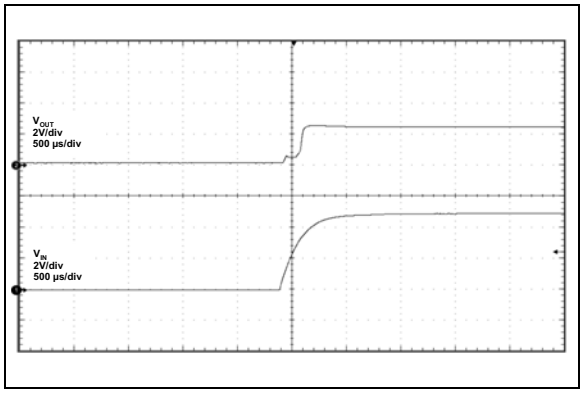


***FIGURE 2-22:*** *Turn On Transient, $V_{DD}$ = 5/5V, $V_{IN}$ = 2.048V Option, No Load.*

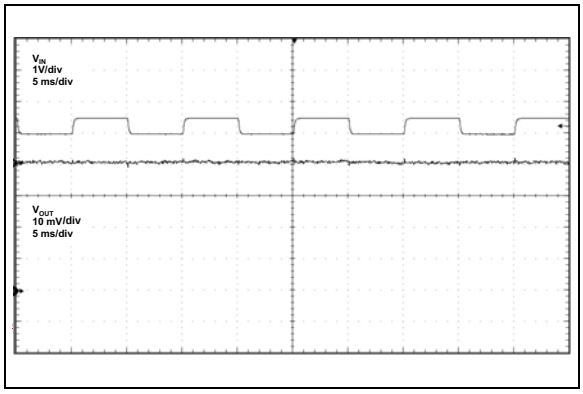


***FIGURE 2-23:*** *Line Transient, $V_{DD}$ = 5.5V, $V_{IN}$ = 500 $mV_{PP}$ @ 5$V_{DC}$, 2.048V Option, No Load.*

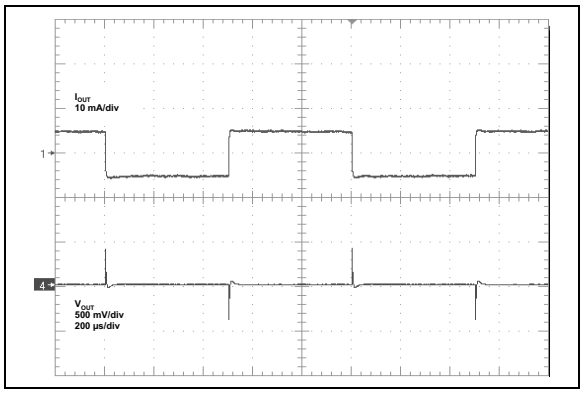


***FIGURE 2-24:*** *Load Transient, $V_{DD}$ = 5.5, $V_{IN}$ = 2.5, 2.048V Option.*

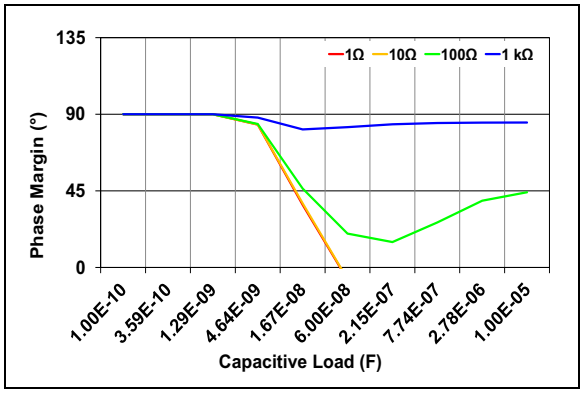


***FIGURE 2-25:*** *$R_{ISO}$ vs. $C_{LOAD}$, 4.096V Option Unloaded.*

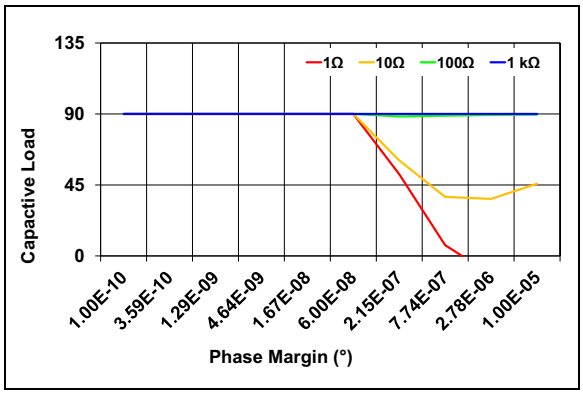


***FIGURE 2-26:*** *$R_{ISO}$ vs. $C_{LOAD}$, 4.096V Option Loaded.*


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## 3.0 PIN FUNCTION TABLE

The pin functions are described in Table 3-1.

**TABLE 3-1: PIN FUNCTION TABLE**

| SOT-23 | SOIC | 2 x 2 WDFN | Symbol | Function |
|---|---|---|---|---|
| 1 | 7 | 7 | OUT | Buffered $V_{REF}$ Output |
| — | 8 | 8 | FEEDBACK | Buffered $V_{REF}$ Feedback |
| 2, 3, 5 | 2, 4, 5, 6 | 2, 4, 5, 6 | GND | System Ground |
| 4 | 3 | 3 | $\overline{SHDN}$ | Shutdown Pin Active Low |
| 6 | 1 | 1 | $V_{DD}$ | Power Supply Input |
| — | — | 9 | EP | Exposed Thermal Pad |

### 3.1 Buffered $V_{REF}$ Output (OUT)

This is the Buffered Reference Output. On the WDFN and SOIC package, this should be connected to the FEEDBACK pin at the device. The output driver is tristated when in shutdown.

### 3.2 Buffered $V_{REF}$ Feedback (FEEDBACK)

This is the buffer amplifier feedback pin. On the WDFN and SOIC package, this should be connected to the OUT pin at the device. This connection is internal on the SOT-23 package. Note that if there is routing impedance or IR-drop between the OUT and FEEDBACK pins, it is the FEEDBACK pin which accurately holds the output voltage. This can be used in an application to remove IR-drop effects on output voltage caused by the Printed Circuit Board (PCB) or interconnect resistance with a high-current load.

### 3.3 System Ground (GND)

This is the power supply return and should be connected to system ground.

### 3.4 Shutdown Pin ($\overline{SHDN}$)

This is a digital input that will place the device in Shutdown. The device should be allowed to power up before using this feature. This pin is active low.

### 3.5 Power Supply Input ($V_{DD}$)

This power pin also serves as the input voltage for the voltage reference. Refer to the Electrical Tables to determine minimum voltage, based on the device.

### 3.6 Exposed Thermal Pad (EP)

Not internally connected, but recommend grounding.

## 4.0 THEORY OF OPERATION

The MCP1501 is a buffered voltage reference that is capable of operating over a wide input supply range while providing a stable output across the input supply range. The fundamental building block (see **Block Diagram**) of the MCP1501 is an internal bandgap reference circuit. As with all bandgap circuits, the internal reference sums together two voltages having an opposite temperature coefficient which allows a voltage reference that is practically independent from temperature.

The bandgap of the MCP1501 is based on a second order temperature coefficient (TC) compensated bandgap circuit that allows the MCP1501 to achieve high initial accuracy and low temperature coefficient operation across supply and ambient temperature. The bandgap curvature compensation is determined during device characterization and is trimmed for optimal accuracy.

The MCP1501 also includes a chopper-based amplifier architecture that ensures excellent low-noise operation, further reduces temperature dependent offsets that would otherwise increase the temperature coefficient of the MCP1501, and significantly improves long-term drift performance. Additional circuitry is included to eliminate the chopping frequency from the output of the device.

After the bandgap voltage is compensated, it is amplified, buffered, and provided to the output drive circuit which has excellent performance when sinking or sourcing load currents (±5 mA).


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# 5.0 APPLICATION CIRCUITS

## 5.1 Application Tips

### 5.1.1 BASIC APPLICATION CIRCUIT

Figure 5-1 illustrates a basic circuit configuration of the MCP1501.

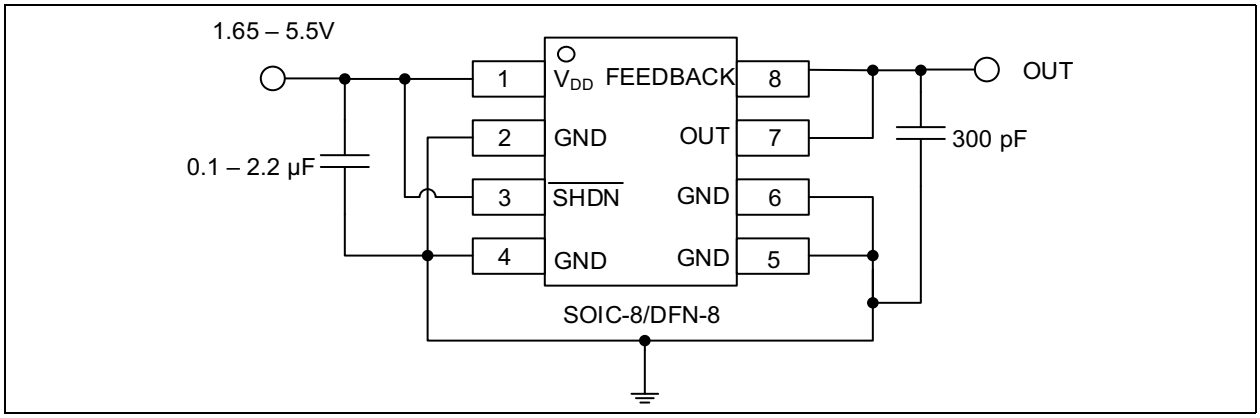


***FIGURE 5-1:*** *Basic Circuit Configuration.*

An output capacitor is not required for stability of the voltage reference, but may be optionally added to provide noise filtering or act as a charge-reservoir for switching loads, e.g., successive approximation register (SAR) analog-to-digital converter (ADC). As shown, the input voltage is connected to the device at the $V_{IN}$ input, with an optional 2.2 µf ceramic capacitor. This capacitor would be required if the input voltage has excessive noise. A 2.2 µf capacitor would reject input voltage noise at approximately 1 to 2 MHz. Noise below this frequency will be amply rejected by the input voltage rejection of the voltage reference. Noise at frequencies above 2 MHz will be beyond the bandwidth of the voltage reference and, consequently, not transmitted from the input pin through the device to the output.

If the noise at the output of these voltage references is too high for the particular application, it can be easily filtered with an external RC filter and op-amp buffer (see Figure 5-2).

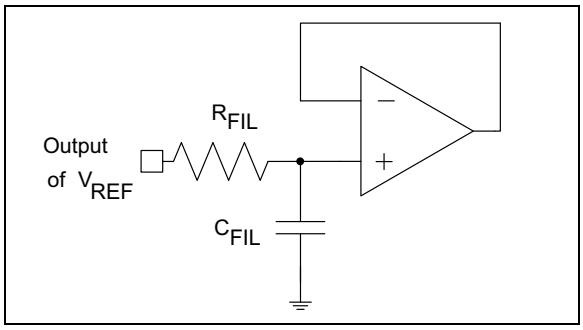


***FIGURE 5-2:*** *Output Noise-Reducing Filter.*

The RC filter values are selected for a desired cutoff frequency, as shown in Equation 5-1.

**EQUATION 5-1:**

$$f_C = \frac{1}{2\pi(R_{FIL}C_{FIL})}$$

The values that are shown in Figure 5-2 (10 kΩ and 1 µF) will create a first-order, low-pass filter at the output of the amplifier. The cutoff frequency of this filter is 15.9 Hz, and the attenuation slope is 20 dB/decade. The MCP6021 amplifier isolates the loading of this low-pass filter from the remainder of the application circuit. This amplifier also provides additional drive, with a faster response time than the voltage reference.

### 5.1.2 LOAD CAPACITOR

The maximum capacitive load is 300 pF. However, larger capacitors may be implemented if a resistor is used in series with a larger load capacitor. Refer to Figure 2-25 and Figure 2-26 to ensure adequate phase margin when selecting a resistor/capacitor combination.

### 5.1.3 PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

Mechanical stress due to Printed Circuit Board (PCB) mounting can cause the output voltage to shift from its initial value. Devices in the SOT-23-6 package are generally more prone to assembly stress than devices in the WDFN package. To reduce stress-related output voltage shifts, mount the reference on low-stress areas of the PCB (i.e., away from PCB edges, screw holes and large components).


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## 5.2 Typical Applications Circuits

### 5.2.1 NEGATIVE VOLTAGE REFERENCE

A negative voltage reference can be generated using any of the devices in the MCP1501 family. A typical application is shown in Figure 5-3. In this circuit, the voltage inversion is implemented using the MCP6061 and two equal resistors. The voltage at the output of the MCP1501 voltage reference drives R1, which is connected to the inverting input of the MCP6061 amplifier. Since the noninverting input of the amplifier is biased to ground, the inverting input will also be close to ground potential. The second 10 kΩ resistor is placed around the feedback loop of the amplifier. Since the inverting input of the amplifier is high-impedance, the current generated through R1 will also flow through R2. As a consequence, the output voltage of the amplifier is equal to –2.5V for the MCP1501-25 and –4.096V for the MCP1501-40.

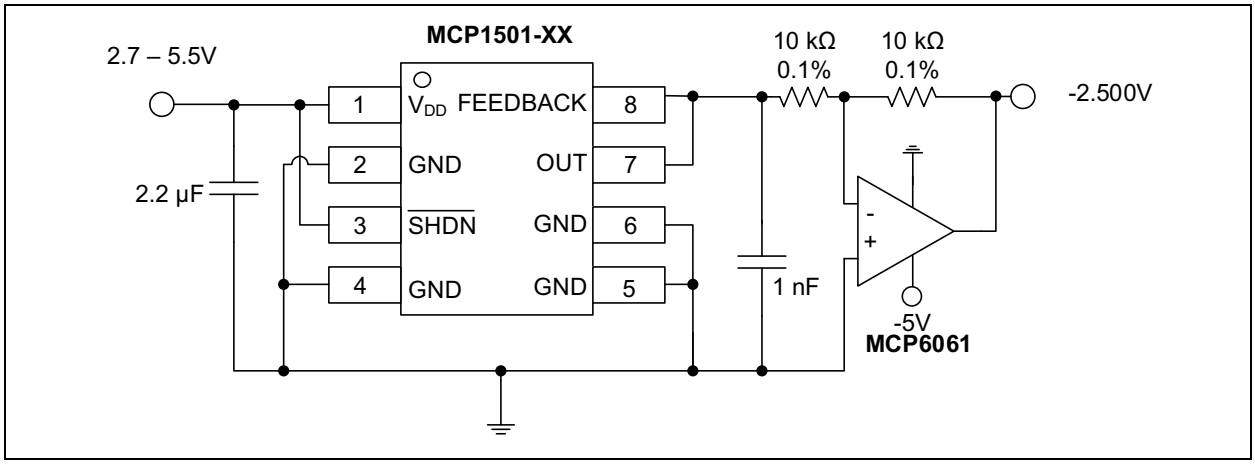


***FIGURE 5-3:*** *Negative Voltage Reference.*

### 5.2.2 A/D CONVERTER REFERENCE

The MCP1501 product family was carefully designed to provide a precision, low noise voltage reference for the Microchip families of ADCs. The circuit shown in Figure 5-4 shows a MCP1501-25 configured to provide the reference to the MCP3201, a 12-bit ADC.

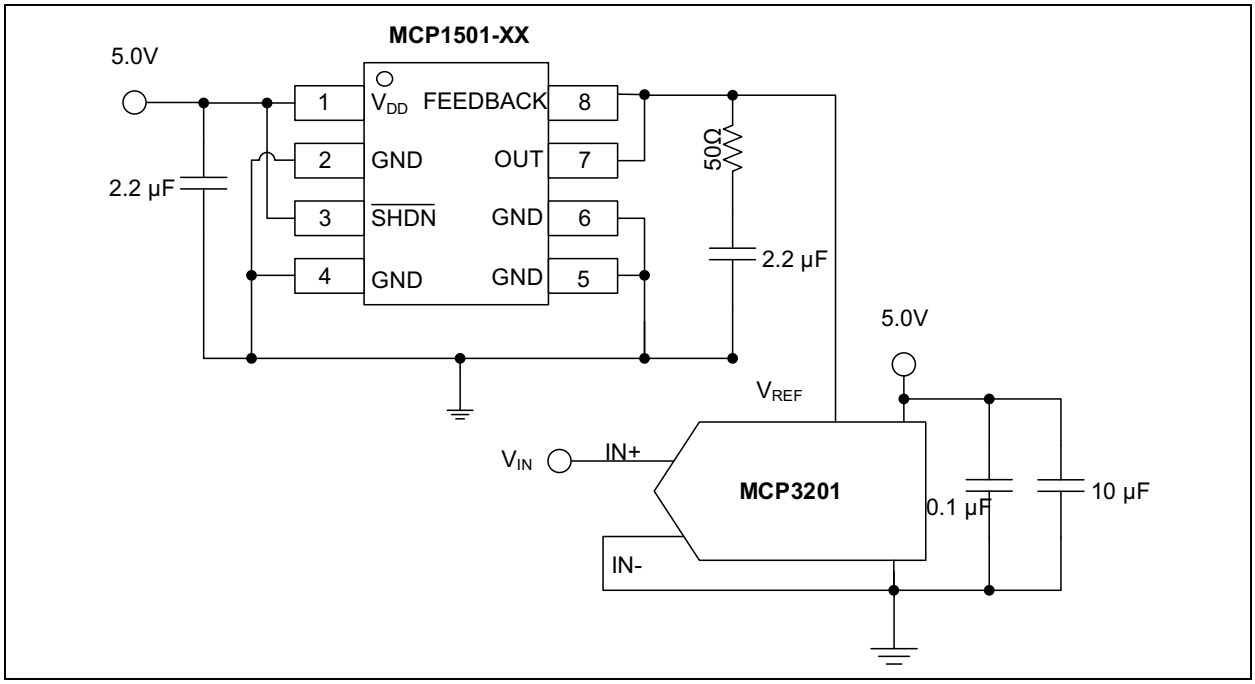


***FIGURE 5-4:*** *ADC Example Circuit.*

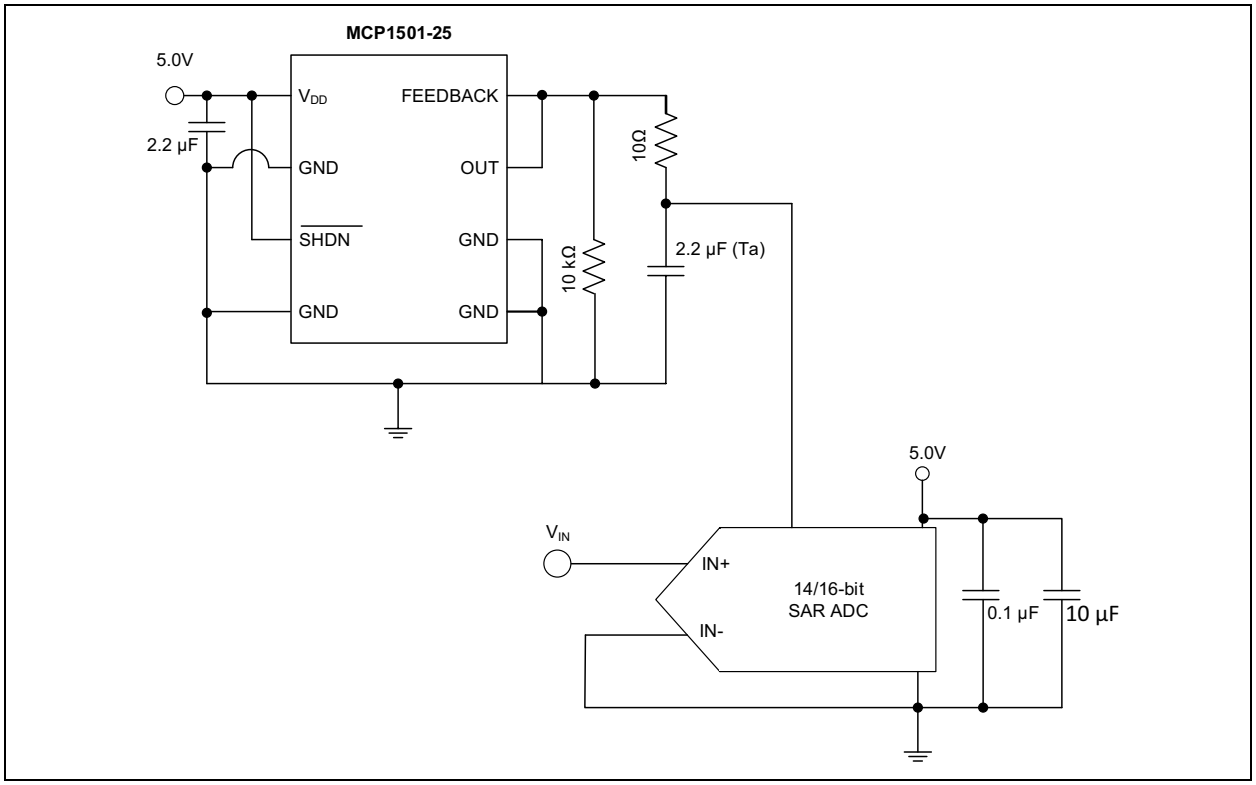


***FIGURE 5-5:*** *SAR ADC Example Circuit.*

The circuit shown in Figure 5-5 shows a MCP1501-25 configured to provide the reference to a 14-bit or 16-bit SAR ADC.


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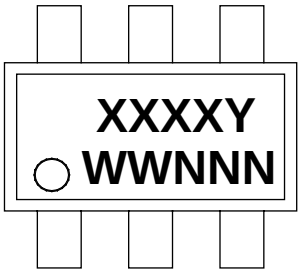
# 6.0 PACKAGE INFORMATION

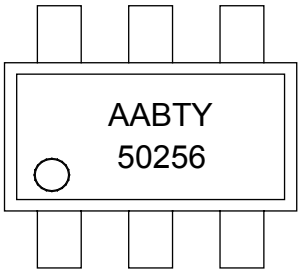
## 6.1 Package Markings

6-Lead SOT-23

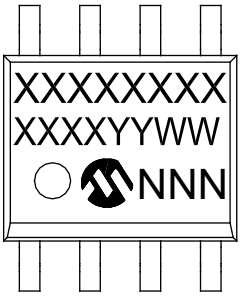



| Device | Code |
|---|---|
| MCP1501T-10E/CHY | AABTY |
| MCP1501T-12E/CHY | AABUY |
| MCP1501T-18E/CHY | AABVY |
| MCP1501T-20E/CHY | AABWY |
| MCP1501T-25E/CHY | AABXY |
| MCP1501T-30E/CHY | AABYY |
| MCP1501T-33E/CHY | AABZY |
| MCP1501T-40E/CHY | AACAY |

Example

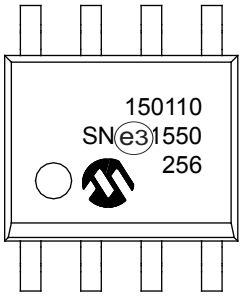



8-Lead SOIC

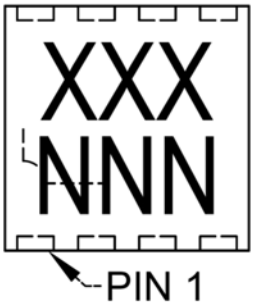



| Device | Code |
|---|---|
| MCP1501T-10E/SN | 150110 |
| MCP1501T-12E/SN | 150112 |
| MCP1501-18E/SN | 150118 |
| MCP1501-20E/SN | 150120 |
| MCP1501T-25E/SN | 150125 |
| MCP1501T-30E/SN | 150130 |
| MCP1501T-33E/SN | 150133 |
| MCP1501T-40E/SN | 150140 |

Example

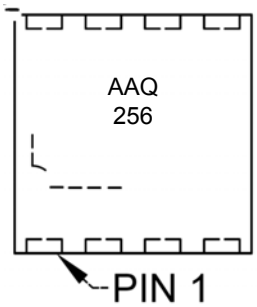



8-Lead WDFN (2 x2 mm)




| Device | Code |
|---|---|
| MCP1501T-10E/RW | AAQ |
| MCP1501T-12E/RW | AAR |
| MCP1501-18E/RW | AAS |
| MCP1501-20E/RW | AAT |
| MCP1501T-25E/RW | AAU |
| MCP1501T-30E/RW | AAV |
| MCP1501T-33E/RW | AAW |
| MCP1501T-40E/RW | AAX |

Example

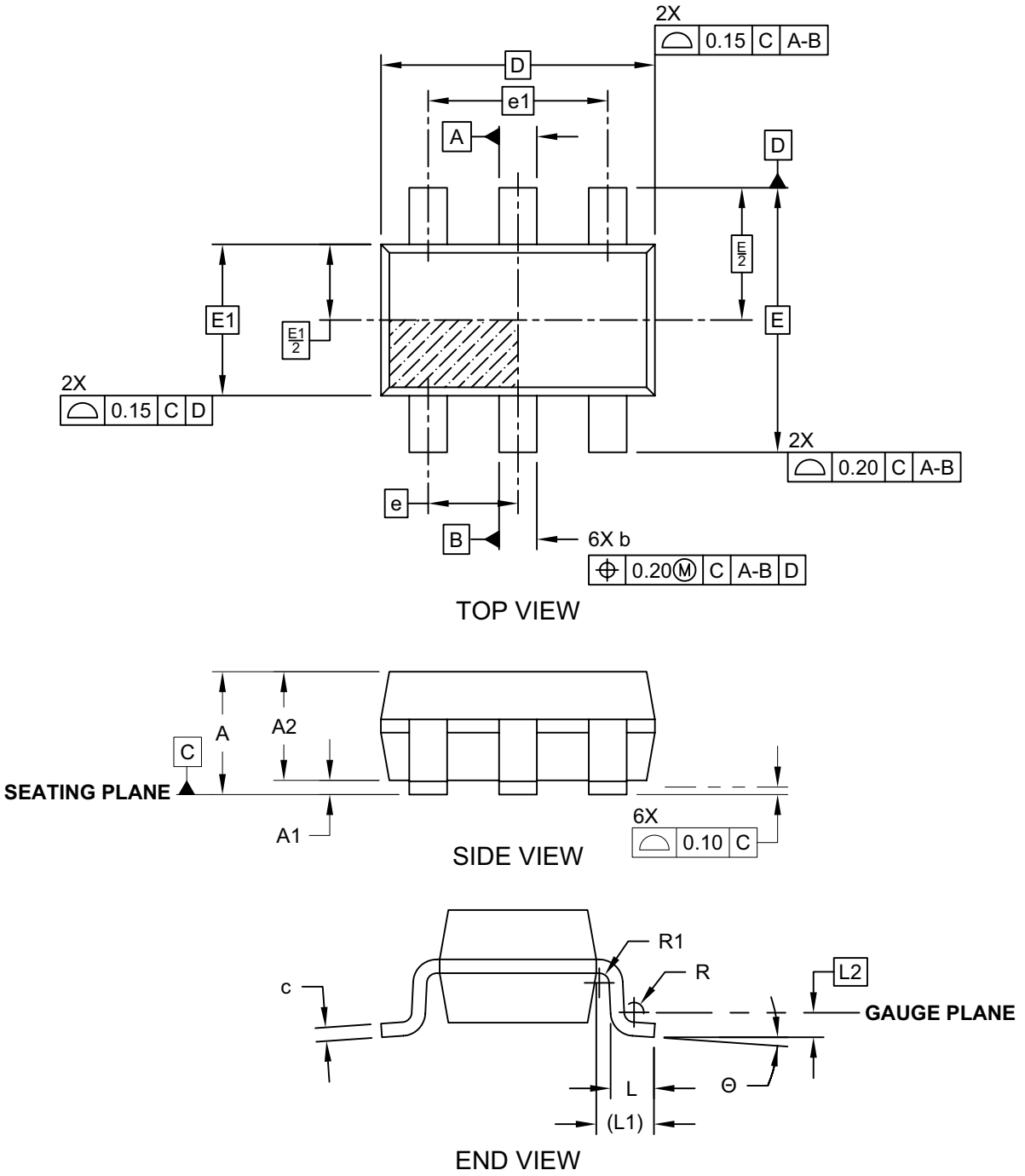



| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | e3 | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

## 6-Lead Plastic Small Outline Transistor (CH, CHY) [SOT-23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-028C (CH) Sheet 1 of 2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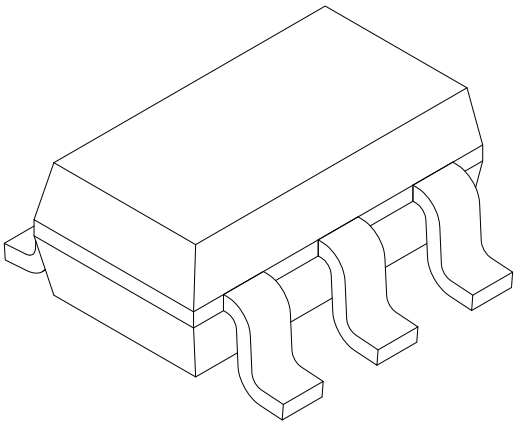
## 6-Lead Plastic Small Outline Transistor (OT, OTY) [SOT-23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Leads | N | 6 | | |
| Pitch | e | 0.95 BSC | | |
| Outside lead pitch | e1 | 1.90 BSC | | |
| Overall Height | A | 0.90 | - | 1.45 |
| Molded Package Thickness | A2 | 0.89 | 1.15 | 1.30 |
| Standoff | A1 | 0.00 | - | 0.15 |
| Overall Width | E | 2.80 BSC | | |
| Molded Package Width | E1 | 1.60 BSC | | |
| Overall Length | D | 2.90 BSC | | |
| Foot Length | L | 0.30 | 0.45 | 0.60 |
| Footprint | L1 | 0.60 REF | | |
| Seating Plane to Gauge Plane | L1 | 0.25 BSC | | |
| Foot Angle | ϕ | 0° | - | 10° |
| Lead Thickness | c | 0.08 | - | 0.26 |
| Lead Width | b | 0.20 | - | 0.51 |

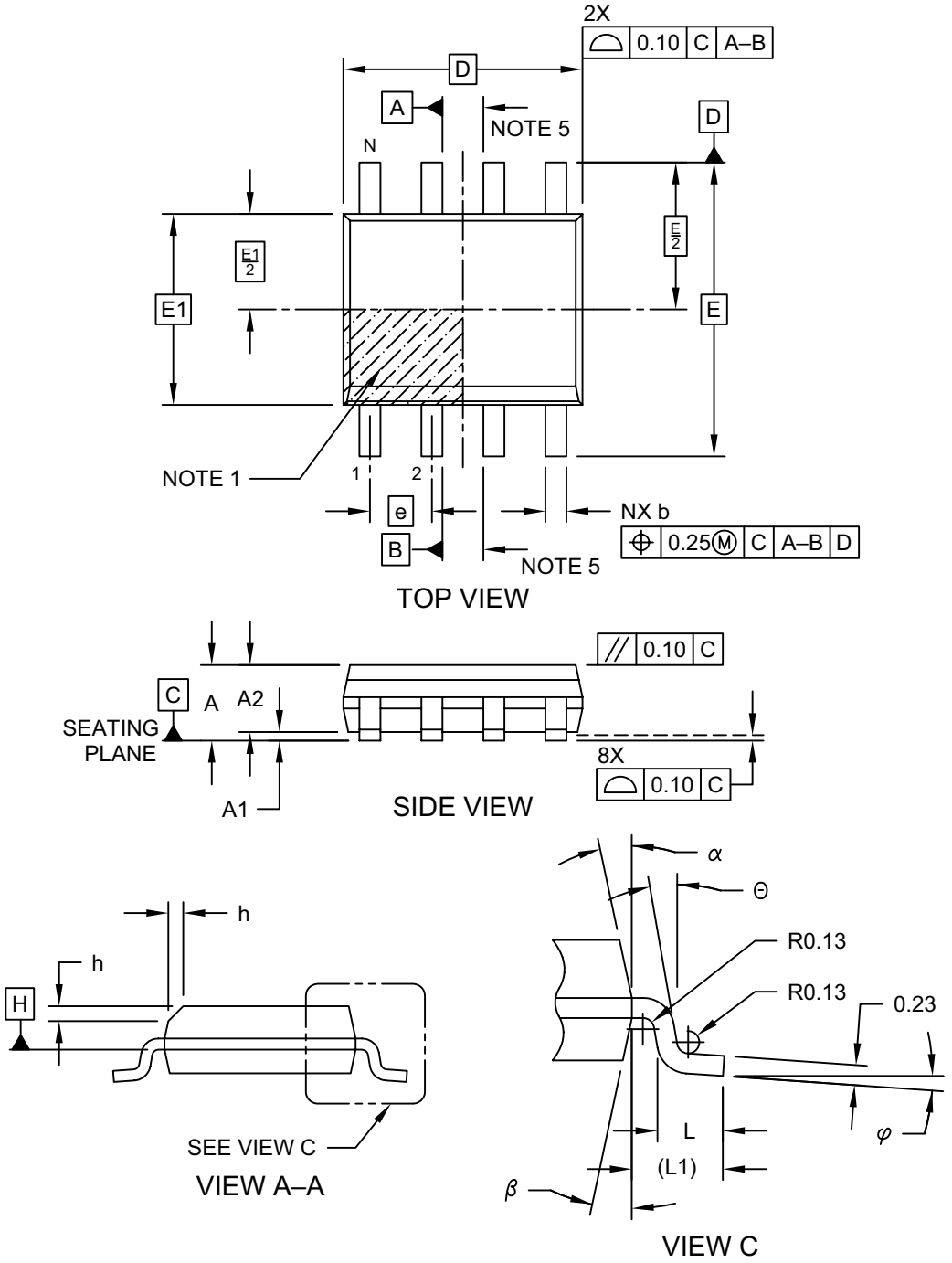
Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-028C (OT) Sheet 2 of 2

### 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing No. C04-057-SN Rev D Sheet 1 of 2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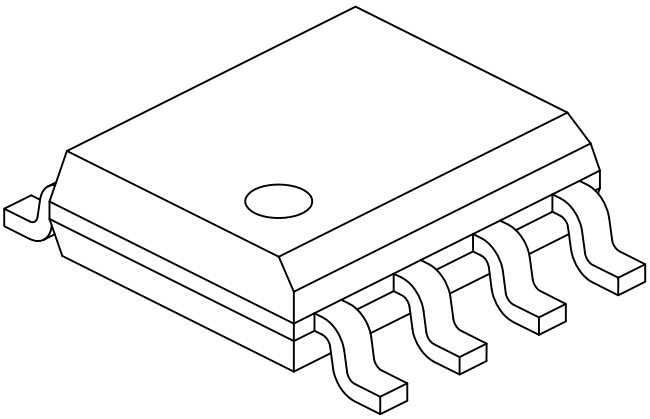
## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | 8 | | |
| Pitch | e | 1.27 BSC | | |
| Overall Height | A | - | - | 1.75 |
| Molded Package Thickness | A2 | 1.25 | - | - |
| Standoff § | A1 | 0.10 | - | 0.25 |
| Overall Width | E | 6.00 BSC | | |
| Molded Package Width | E1 | 3.90 BSC | | |
| Overall Length | D | 4.90 BSC | | |
| Chamfer (Optional) | h | 0.25 | - | 0.50 |
| Foot Length | L | 0.40 | - | 1.27 |
| Footprint | L1 | 1.04 REF | | |
| Foot Angle | $\varphi$ | 0° | - | 8° |
| Lead Thickness | c | 0.17 | - | 0.25 |
| Lead Width | b | 0.31 | - | 0.51 |
| Mold Draft Angle Top | $\alpha$ | 5° | - | 15° |
| Mold Draft Angle Bottom | $\beta$ | 5° | - | 15° |

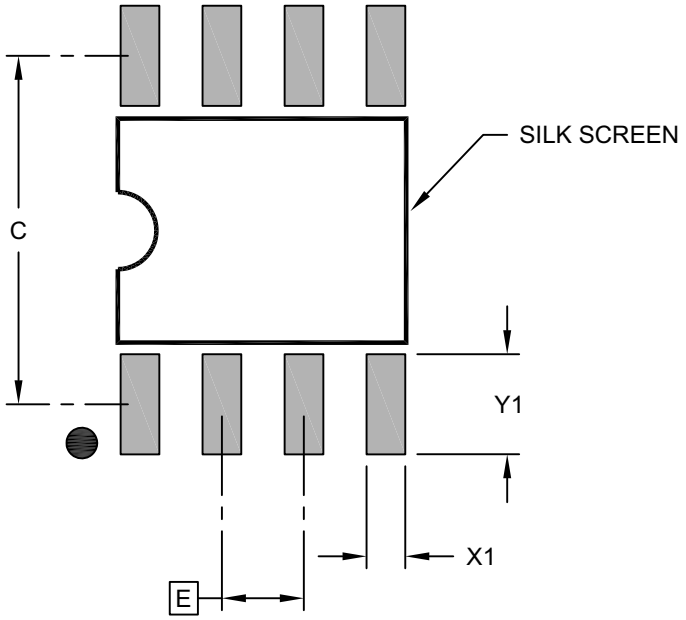
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev D Sheet 2 of 2

## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 1.27 BSC | | |
| Contact Pad Spacing | C | | 5.40 | |
| Contact Pad Width (X8) | X1 | | | 0.60 |
| Contact Pad Length (X8) | Y1 | | | 1.55 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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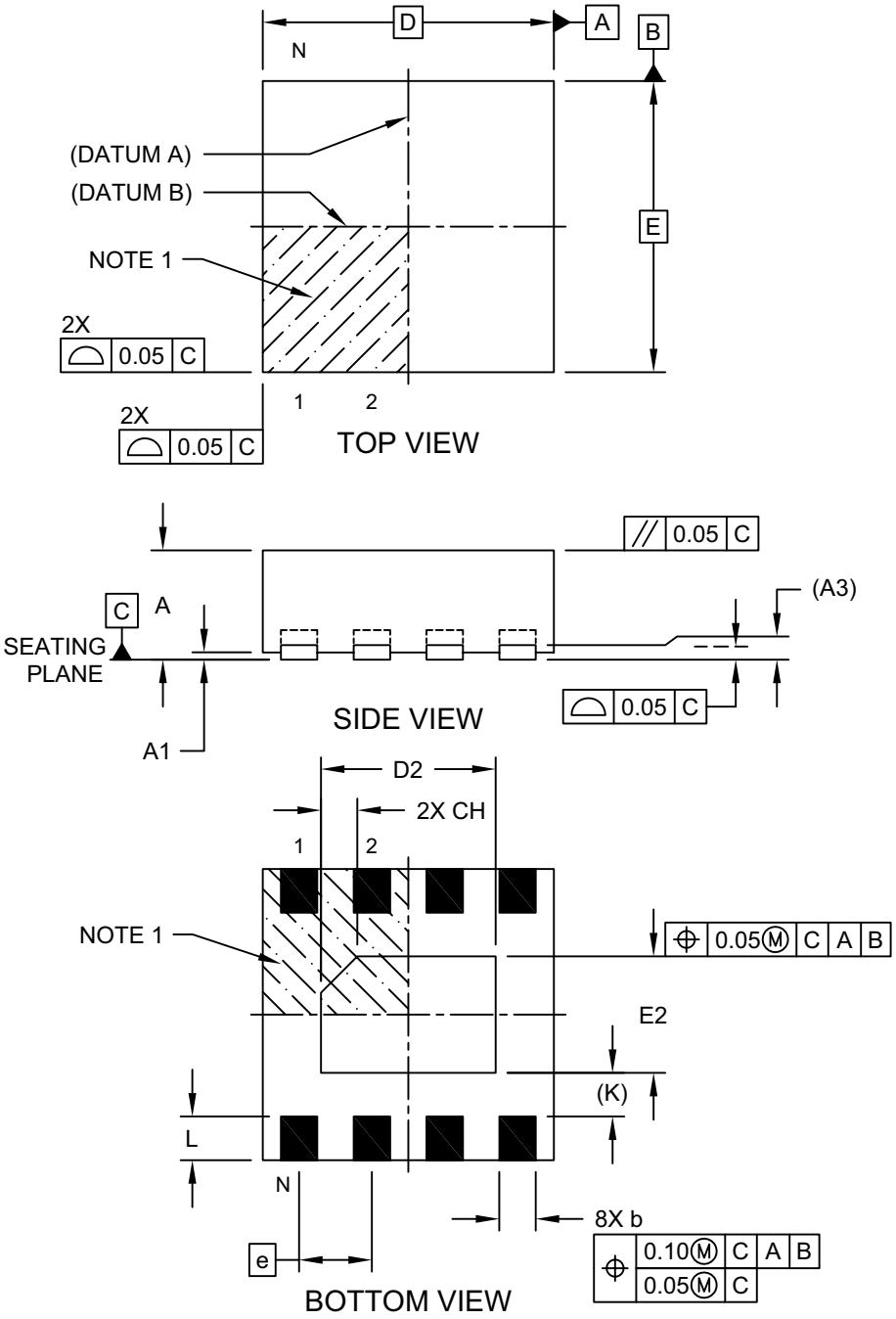
## 8-Lead Very, Very Thin Plastic Dual Flat, No Lead Package (RW) - 2x2 mm Body [WDFN]

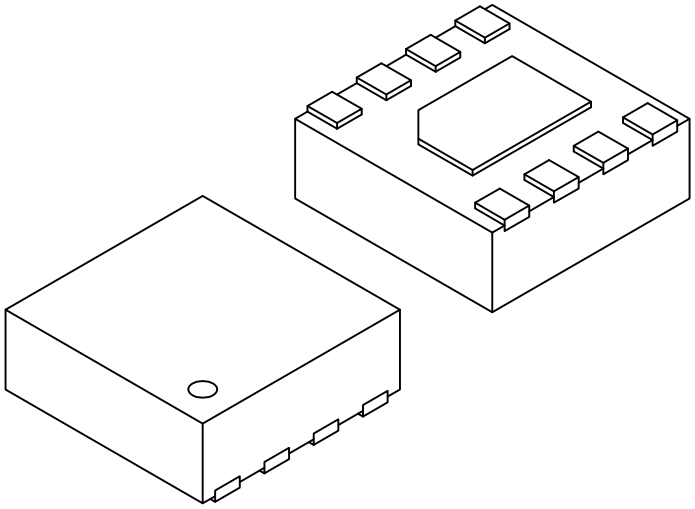
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-261A Sheet 1 of 2

## 8-Lead Very, Very Thin Plastic Dual Flat, No Lead Package (RW) - 2x2 mm Body [WDFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | 8 | | |
| Pitch | e | 0.50 BSC | | |
| Overall Height | A | 0.70 | 0.75 | 0.80 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | (A3) | 0.10 REF | | |
| Overall Width | E | 2.00 BSC | | |
| Exposed Pad Width | E2 | 0.70 | 0.80 | 0.90 |
| Overall Length | D | 2.00 BSC | | |
| Exposed Pad Length | D2 | 1.10 | 1.20 | 1.30 |
| Exposed Pad Chamfer | CH | - | 0.25 | - |
| Terminal Width | b | 0.20 | 0.25 | 0.30 |
| Terminal Length | L | 0.25 | 0.30 | 0.35 |
| Terminal-to-Exposed-Pad | (K) | 0.30 | - | - |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-261A Sheet 2 of 2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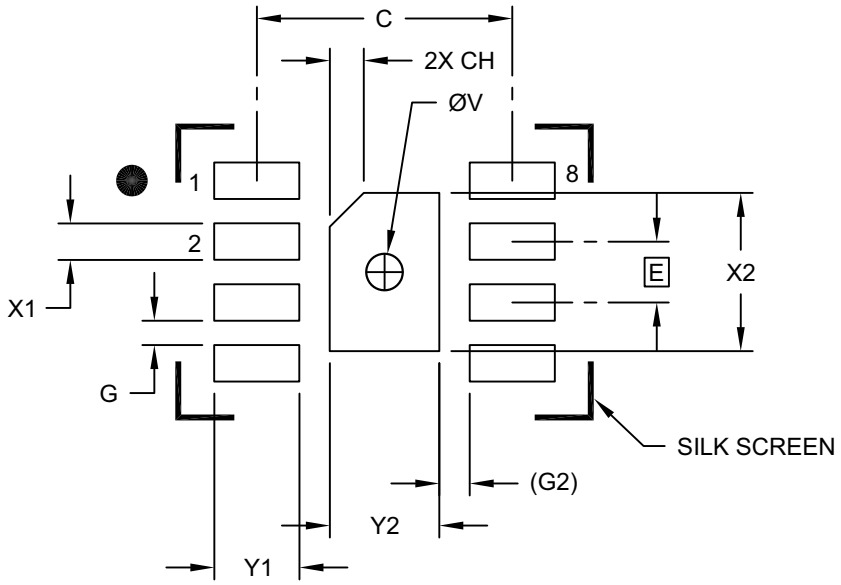
## 8-Lead Very, Very Thin Plastic Dual Flat, No Lead Package (RW) - 2x2 mm Body [WDFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Optional Center Pad Width | Y2 | | | 0.90 |
| Optional Center Pad Length | X2 | | | 1.30 |
| Contact Pad Spacing | C | | 2.10 | |
| Center Pad Chamfer | CH | | 0.28 | |
| Contact Pad Width (X8) | X1 | | | 0.30 |
| Contact Pad Length (X8) | Y1 | | | 0.70 |
| Contact Pad to Contact Pad (X6) | G1 | 0.20 | | |
| Contact Pad to Center Pad (X8) | G1 | | 0.25 REF | |
| Thermal Via Diameter | V | | 0.30 | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerances, for reference only.

Microchip Technology Drawing C04-2261A

**NOTES:**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# APPENDIX A: REVISION HISTORY

## Revision E (August 2017)

The following is the list of modifications:

- Updated Features.
- Updated Package Types.
- Updated Section 1.0, Electrical Characteristics, Table 1-1.
- Updated Figure 2-12, Figure 2-20 and Figure 2-21.
- Updated Table 3-1.
- Updated Section 3.4, Shutdown Pin (SHDN).
- Updated Section 5.1.2, LOAD CAPACITOR.
- Corrected Figure 5-3 and Figure 5-4.
- Added Figure 5-5.
- Minor typographical corrections.

## Revision D (March 2017)

The following is the list of modifications:

- Updated Table 1-1.
- Updated Equation 1-1, Equation 1-4, Equation 1-5, Equation 1-10, Equation 1-11, Equation 1-12 and Equation 1-16.
- Updated Figure 2-11, Figure 2-20, Figure 2-21, Figure 2-25 and Figure 2-26.
- Updated Figure 5-1 and Figure 5-4.
- Updated **"Product Identification System"** section.
- Minor typographical corrections.

## Revision C (May 2016)

The following is the list of modifications:

- Updated Section 1.0, Electrical Characteristics, Section 4.0, Theory of Operation, Section 5.0, Application Circuits.
- Updated Features section, General Description section, Section 3.1, Buffered $V_{REF}$ Output (OUT).
- Updated **"Product Identification System"** section.
- Updated Figure 2-12, Figure 2-20, Figure 2-21, Figure 5-1 and Figure 5-4.
- Updated Equation 1-10 and Equation 1-16.
- Minor typographical corrections.

## Revision B (January 2016)

The following is the list of modifications:

- Updated Section 6.0, Package Information.
- Updated **"Product Identification System"** section.
- Minor typographical corrections.

## Revision A (December 2015)

Original Release of this Document.

**NOTES:**


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## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO.- | [X](1) | X | /XX |
|---|---|---|---|
| Device | Tape and Reel | Output Voltage Option | Package |

| | | | |
|---|---|---|---|
| **Device:** | MCP1501 – 50 ppm maximum thermal drift buffered reference | | |
| **Tape and Reel Option:** | Blank | = | Standard packaging (tube or tray) |
| | T | = | Tape and Reel (1) |
| **Output Voltage Option:** | 10 | = | 1.024V |
| | 12 | = | 1.200V |
| | 18 | = | 1.800V |
| | 20 | = | 2.048V |
| | 25 | = | 2.500V |
| | 30 | = | 3.000V |
| | 33 | = | 3.300V |
| | 40 | = | 4.096V |
| **Package:** | CHY* | = | 6-Lead Plastic Small Outline Transistor (SOT-23) |
| | SN | = | 8-Lead Plastic Small Outline – Narrow, 3.90 mm Body (SOIC) |
| | RW | = | 8-Lead Very, Very Thin Plastic Dual Flat, No Lead Package – 2 x 2 mm Body (WDFN) |
| | *Y | = | Nickel palladium gold manufacturing designator. Only available on the SOT-23 package. |

**Examples:**

| | | |
|---|---|---|
| a) | MCP1501T-10E/CHY: | 1.024V, 6-lead SOT-23 package, Tape and Reel |
| b) | MCP1501-12E/SN: | 1.2V, 8-lead SOIC package |
| c) | MCP1501T-18E/SN: | 1.8V, 8-lead SOIC package, Tape and Reel |
| d) | MCP1501T-20E/RW: | 2.048V, 8-lead WDFN package, Tape and Reel |

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip sales office for package availability for the Tape and Reel option.

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