# 80C186EC/80C188EC AND 80L186EC/80L188EC 16-BIT HIGH-INTEGRATION EMBEDDED PROCESSORS

- **Fully Static Operation**
- **True CMOS Inputs and Outputs**

- **Integrated Feature Set:**
  - **Low-Power, Static, Enhanced 8086 CPU Core**
  - **Two Independent DMA Supported UARTs, each with an Integral Baud Rate Generator**
  - **Four Independent DMA Channels**
  - **22 Multiplexed I/O Port Pins**
  - **Two 8259A Compatible Programmable Interrupt Controllers**
  - **Three Programmable 16-Bit Timer/ Counters**
  - **32-Bit Watchdog Timer**
  - **Ten Programmable Chip Selects with Integral Wait-State Generator**
  - **Memory Refresh Control Unit**
  - **Power Management Unit**
  - **On-Chip Oscillator**
  - **System Level Testing Support (ONCE Mode)**
- **Direct Addressing Capability to 1 Mbyte Memory and 64 Kbyte I/O**
- **Low-Power Operating Modes:**
  - **Idle Mode Freezes CPU Clocks but Keeps Peripherals Active**
  - **Powerdown Mode Freezes All Internal Clocks**
  - **Powersave Mode Divides All Clocks by Programmable Prescalar**
- **Available in Extended Temperature Range (−40°C to +85°C)**
- **Supports 80C187 Numerics Processor Extension (80C186EC only)**
- **Package Types:**
  - **100-Pin EIAJ Quad Flat Pack (QFP)**
  - **100-Pin Plastic Quad Flat Pack (PQFP)**
  - **100-Pin Shrink Quad Flat Pack (SQFP)**
- **Speed Versions Available (5V):**
  - **25 MHz (80C186EC25/80C188EC25)**
  - **20 MHz (80C186EC20/80C188EC20)**
  - **13 MHz (80C186EC13/80C188EC13)**
- **Speed Version Available (3V):**
  - **16 MHz (80L186EC16/80L188EC16)**
  - **13 MHz (80L186EC13/80L188EC13)**

The 80C186EC is a member of the 186 Integrated Processor Family. The 186 Integrated Processor Family incorporates several different VLSI devices all of which share a common CPU architecture: the 8086/8088. The 80C186EC uses the latest high density CHMOS technology to integrate several of the most common system peripherals with an enhanced 8086 CPU core to create a powerful system on a single monolithic silicon die.

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# 80C186EC/80C188EC and 80L186EC/80L188EC 16-BIT HIGH-INTEGRATION EMBEDDED PROCESSOR

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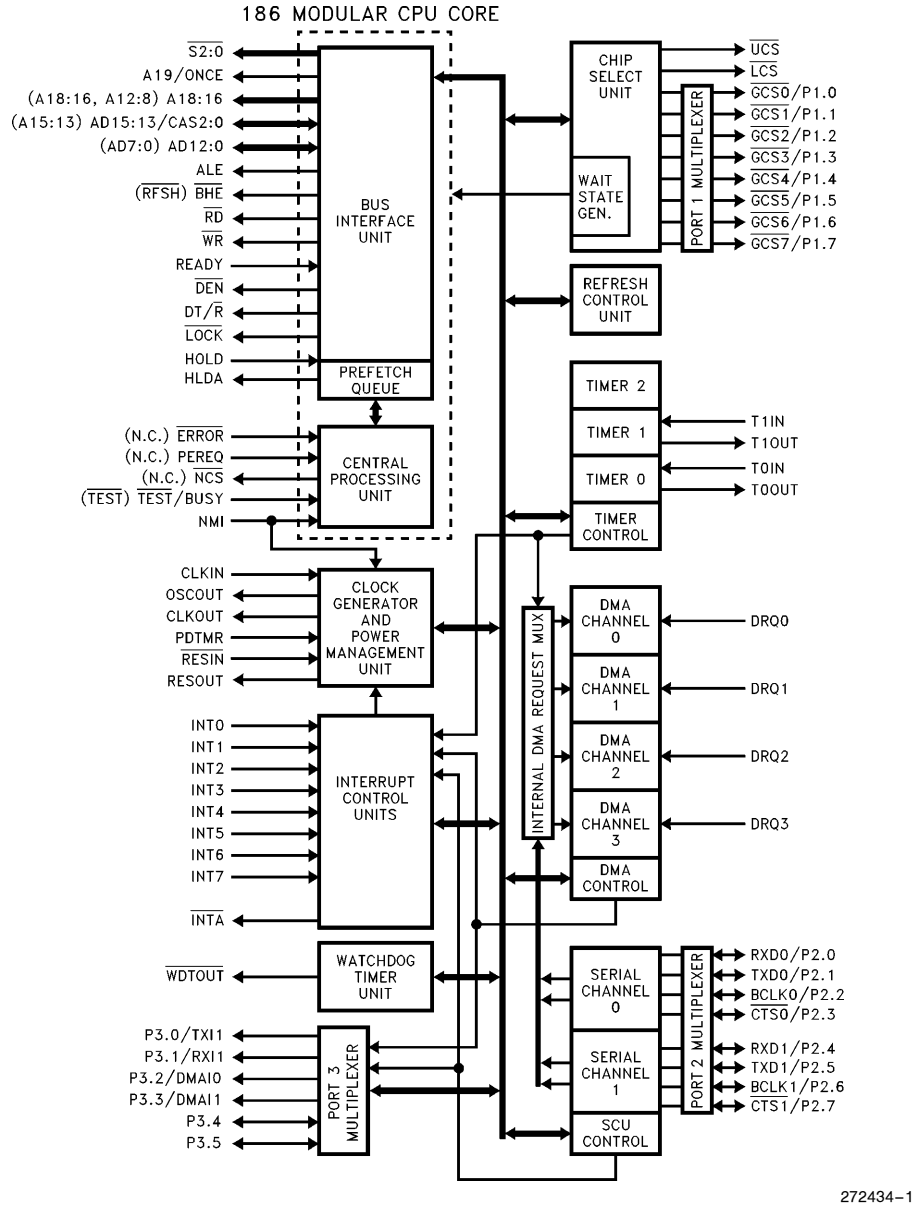
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**NOTE:**
Pin names in parentheses apply to the 80C188EC/80L188EC

**Figure 1. 80C186EC/80L186EC Block Diagram**

## INTRODUCTION

Unless specifically noted, all references to the 80C186EC apply to the 80C188EC, 80L186EC, and 80L188EC. References to pins that differ between the 80C186EC/80L186EC and the 80C188EC/80L188EC are given in parentheses. The "L" in the part number denotes low voltage operation. Physically and functionally, the "C" and "L" devices are identical.

The 80C186EC is one of the highest integration members of the 186 Integrated Processor Family. Two serial ports are provided for services such as interprocessor communication, diagnostics and modem interfacing. Four DMA channels allow for high speed data movement as well as support of the onboard serial ports. A flexible chip select unit simplifies memory and peripheral interfacing. The three general purpose timer/counters can be used for a variety of time measurement and waveform generation tasks. A watchdog timer is provided to insure system integrity even in the most hostile of environments. Two 8259A compatible interrupt controllers handle internal interrupts, and, up to 57 external interrupt requests. A DRAM refresh unit and 24 multiplexed I/O ports round out the feature set of the 80C186EC.

The future set of the 80C186EC meets the needs of low-power, space-critical applications. Low-power applications benefit from the static design of the CPU and the integrated peripherals as well as low voltage operation. Minimum current consumption is achieved by providing a powerdown mode that halts operaton of the device and freezes the clock circuits. Peripheral design enhancements ensure that non-initialized peripherals consume little current.

The 80L186EC is the 3V version of the 80C186EC. The 80L186EC is functionally identical to the 80C186EC embedded processor. Current 80C186EC users can easily upgrade their designs to use the 80L186EC and benefit from the reduced power consumption inherent in 3V operation.

Figure 1 shows a block diagram of the 80C186EC/80C188EC. The execution unit (EU) is an enhanced 8086 CPU core that includes: dedicated hardware to speed up effective address calculations, enhanced execution speed for multiple-bit shift and rotate instructions and for multiply and divide instructions, string move instructions that operate at full bus bandwidth, ten new instructions and fully static operation. The bus interface unit (BIU) is the same as that found on the original 186 family products, except the queue-status mode has been deleted and buffer interface control has been changed to ease system design timings. An independent internal bus is used for communication between the BIU and on-chip peripherals.

## 80C186EC CORE ARCHITECTURE

### Bus Interface Unit

The 80C186EC core incorporates a bus controller that generates local bus control signals. In addition, it employs a HOLD/HLDA protocol to share the local bus with other bus masters.

The bus controller is responsible for generating 20 bits of address, read and write strobes, bus cycle status information and data (for write operations) information. It is also responsible for reading data from the local bus during a read operation. A ready input pin is provided to extend a bus cycle beyond the minimum four states (clocks).

The bus controller also generates two control signals ($\overline{DEN}$ and DT/$\overline{R}$) when interfacing to external transceiver chips. This capability allows the addition of transceivers for simple buffering of the multiplexed address/data bus.

### Clock Generator

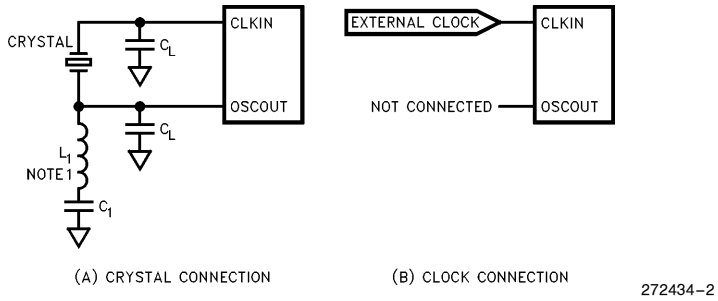
The 80C186EC provides an on-chip clock generator for both internal and external clock generation. The clock generator features a crystal oscillator, a divide-by-two counter and three low-power operating modes.

The oscillator circuit is designed to be used with either a parallel resonant fundamental or third-overtone mode crystal network. Alternatively, the oscillator circuit may be driven from an external clock source. Figure 2 shows the various operating modes of the oscillator circuit.

The crystal or clock frequency chosen must be twice the required processor operating frequency due to the internal divide-by-two counter. This counter is used to drive all internal phase clocks and the external CLKOUT signal. CLKOUT is a 50% duty cycle processor clock and can be used to drive other system components. All AC timings are referenced to CLKOUT.

The following parameters are recommended when choosing a crystal:

| | |
|---|---|
| Temperature Range: | Application Specific |
| ESR (Equivalent Series Res.): | 40Ω max |
| C0 (Shunt Capacitance of Crystal): | 7.0 pF max |
| $C_L$ (Load Capacitance): | 20 pF ±2 pF |
| Drive Level: | 1 mW (max) |




**NOTE:**
1. The LC network is only required when using a third overtone crystal.

**Figure 2. 80C186EC Clock Connections**

## 80C186EC PERIPHERAL ARCHITECTURE

The 80C186EC integrates several common system peripherals with a CPU core to create a compact, yet powerful system. The integrated peripherals are designed to be flexbile and provide logical interconnections between supporting units (e.g., the DMA unit can accept requests from the Serial Communications Unit).

The list of integrated peripherals includes:

— Two cascaded, 8259A compatible, Programmable Interrupt Controllers
— 3-Channel Timer/Counter Unit
— 2-Channel Serial Communications Unit
— 4-Channel DMA Unit
— 10-Output Chip-Select Unit
— 32-bit Watchdog Timer Unit
— I/O Port Unit
— Refresh Control Unit
— Power Management Unit

The registers associated with each integrated peripheral are contained within a 128 x 16-bit register file called the Peripheral Control Block (PCB). The base address of the PCB is programmable and can be located on any 256 byte address boundary in either memory or I/O space.

Figure 3 provides a list of the registers associated with the PCB. The Register Bit Summary individually lists all of the registers and identifies each of their programming attributes.

| PCB Offset | Function |
|---|---|
| 00H | Master PIC Port 0 |
| 02H | Master PIC Port 1 |
| 04H | Slave PIC Port 0 |
| 06H | Slave PIC Port 1 |
| 08H | Reserved |
| 0AH | SCU Int. Req. Ltch. |
| 0CH | DMA Int. Req. Ltch. |
| 0EH | TCU Int. Req. Ltch. |
| 10H | Reserved |
| 12H | Reserved |
| 14H | Reserved |
| 16H | Reserved |
| 18H | Reserved |
| 1AH | Reserved |
| 1CH | Reserved |
| 1EH | Reserved |
| 20H | WDT Reload High |
| 22H | WDT Reload Low |
| 24H | WDT Count High |
| 26H | WDT Count Low |
| 28H | WDT Clear |
| 2AH | WDT Disable |
| 2CH | Reserved |
| 2EH | Reserved |
| 30H | T0 Count |
| 32H | T0 Compare A |
| 34H | T0 Compare B |
| 46H | T0 Control |
| 38H | T1 Count |
| 3AH | T1 Compare A |
| 3CH | T1 Compare B |
| 3EH | T1 Control |

| PCB Offset | Function |
|---|---|
| 40H | T2 Count |
| 42H | T2 Compare |
| 44H | Reserved |
| 46H | T2 Control |
| 48H | Port 3 Direction |
| 4AH | Port 3 Pin State |
| 4CH | Port 3 Mux Control |
| 4EH | Port 3 Data Latch |
| 50H | Port 1 Direction |
| 52H | Port 1 Pin State |
| 54H | Port 1 Mux Control |
| 56H | Port 1 Data Latch |
| 58H | Port 2 Direction |
| 5AH | Port 2 Pin State |
| 5CH | Port 2 Mux Control |
| 5EH | Port 2 Data Latch |
| 60H | SCU 0 Baud |
| 62H | SCU 0 Count |
| 64H | SCU 0 Control |
| 66H | SCU 0 Status |
| 68H | SCU 0 RBUF |
| 6AH | SCU 0 TBUF |
| 6CH | Reserved |
| 6EH | Reserved |
| 70H | SCU 1 Baud |
| 72H | SCU 1 Count |
| 74H | SCU 1 Control |
| 76H | SCU 1 Status |
| 78H | SCU 1 RBUF |
| 7AH | SCU 1 TBUF |
| 7CH | Reserved |
| 7EH | Reserved |

| PCB Offset | Function |
|---|---|
| 80H | GCS0 Start |
| 82H | GCS0 Stop |
| 84H | GCS1 Start |
| 86H | GCS1 Stop |
| 88H | GCS2 Start |
| 8AH | GCS2 Stop |
| 8CH | GCS3 Start |
| 8EH | GCS3 Stop |
| 90H | GCS4 Start |
| 92H | GCS4 Stop |
| 94H | GCS5 Start |
| 96H | GCS5 Stop |
| 98H | GCS6 Start |
| 9AH | GCS6 Stop |
| 9CH | GCS7 Start |
| 9EH | GCS7 Stop |
| A0H | LCS Start |
| A2H | LCS Stop |
| A4H | UCS Start |
| A6H | UCS Stop |
| A8H | Relocation Register |
| AAH | Reserved |
| ACH | Reserved |
| AEH | Reserved |
| B0H | Refresh Base Addr. |
| B2H | Refresh Time |
| B4H | Refresh Control |
| B6H | Refresh Address |
| B8H | Power Control |
| BAH | Reserved |
| BCH | Step ID |
| BEH | Powersave |

| PCB Offset | Function |
|---|---|
| C0H | DMA 0 Source Low |
| C2H | DMA 0 Source High |
| C4H | DMA 0 Dest. Low |
| C6H | DMA 0 Dest. High |
| C8H | DMA 0 Count |
| CAH | DMA 0 Control |
| CCH | DMA Module Pri. |
| CEH | DMA Halt |
| D0H | DMA 1 Source Low |
| D2H | DMA 1 Source High |
| D4H | DMA 1 Dest. Low |
| D6H | DMA 1 Dest. High |
| D8H | DMA 1 Count |
| DAH | DMA 1 Control |
| DCH | Reserved |
| DEH | Reserved |
| E0H | DMA 2 Source Low |
| E2H | DMA 2 Source High |
| E4H | DMA 2 Dest. Low |
| E6H | DMA 2 Dest. High |
| E8H | DMA 2 Count |
| EAH | DMA 2 Control |
| ECH | Reserved |
| EEH | Reserved |
| F0H | DMA 3 Source Low |
| F2H | DMA 3 Source High |
| F4H | DMA 3 Dest. Low |
| F6H | DMA 3 Dest. High |
| F8H | DMA 3 Count |
| FAH | DMA 3 Control |
| FCH | Reserved |
| FEH | Reserved |

**Figure 3. Peripheral Control Block Registers**

## Programmable Interrupt Controllers

The 80C186EC utilizes two 8259A compatible Programmable Interrupt Controllers (PIC) to manage both internal and external interrupts. The 8259A modules are configured in a master/slave arrangement.

Seven of the external interrupt pins, INT0 through INT6, are connected to the master 8259A module. The eighth external interrupt pin, INT7, is connected to the slave 8259A module.

There are a total of 11 internal interrupt sources from the integrated peripherals: 4 Serial, 4 DMA and 3 Timer/Counter.

## Timer/Counter Unit

The 80C186EC Timer/Counter Unit (TCU) provides three 16-bit programmable timers. Two of these are highly flexible and are connected to external pins for external control or clocking. The third timer is not connected to any external pins and can only be clocked internally. However, it can be used to clock the other two timer channels. The TCU can be used to count external events, time external events, generate non-repetitive waveforms or generate timed interrupts.

## Serial Communications Unit

The 80C186EC Serial Communications Unit (SCU) contains two independent channels. Each channel is identical in operation except that only channel 0 is directly supported by the integrated interrupt controller (the channel 1 interrupts are routed to external interrupt pins). Each channel has its own baud rate generator and can be internally or externally clocked up to one half the processor operating frequency. Both serial channels can request service from the DMA unit thus providing block reception and transmission without CPU intervention.

Independent baud rate generators are provided for each of the serial channels. For the asynchronous modes, the generator supplies an 8x baud clock to both the receive and transmit shifting register logic. A 1x baud clock is provided in the synchronous mode.

## DMA Unit

The four channel Direct Memory Access (DMA) Unit is comprised of two modules with two channels each. All four channels are identical in operation. DMA transfers can take place from memory to memory, I/O to memory, memory to I/O or I/O to I/O. DMA requests can be external (on the DRQ pins), internal (from Timer 2 or a serial channel) or software initiated.

The DMA Unit transfers data as bytes only. Each data transfer requires at least two bus cycles, one to fetch data and one to deposit. The minimum clock count for each transfer is 8, but this will vary depending on synchronization and wait states.

## Chip-Select Unit

The 80C186EC Chip-Select Unit (CSU) integrates logic which provides up to ten programmable chip-selects to access both memories and peripherals. In addition, each chip-select can be programmed to automatically insert additional clocks (wait states) into the current bus cycle, and/or automatically terminate a bus cycle independent of the condition of the READY input pin.

## I/O Port Unit

The I/O Port Unit on the 80C186EC supports two 8-bit channels and one 6-bit channel of input, output or input/output operation. Port 1 is multiplexed with the chip select pins and is output only. Port 2 is multiplexed with the pins for serial channels 1 and 2. All Port 2 pins are input/output. Port 3 has a total of 6 pins: four that are multiplexed with DMA and serial port interrupts and two that are non-multiplexed, open drain I/O.

## Refresh Control Unit

The Refresh Control Unit (RCU) automatically generates a periodic memory read bus cycle to keep dynamic or pseudo-static memory refreshed. A 9-bit counter controls the number of clocks between refresh requests.

A 12-bit address generator is maintained by the RCU and is presented on the A12:1 address lines during the refresh bus cycle. Address bits A19:13 are programmable to allow the refresh address block to be located on any 8 Kbyte boundary.

## Watchdog Timer Unit

The Watchdog Timer Unit (WDT) allows for graceful recovery from unexpected hardware and software upsets. The WDT consists of a 32-bit counter that decrements every clock cycle. If the counter reaches zero before being reset, the $\overline{\text{WDTOUT}}$ pin is

pulled low for four clock cycles. Logically ANDing the WDTOUT pin with the power-on reset signal allows the WDT to reset the device in the event of a WDT timeout. If a less drastic method of recovery is desired. WDTOUT can be connected directly to NMI or one of the INT input pins. The WDT may also be used as a general purpose timer.

## Power Management Unit

The 80C186EC Power Management Unit (PMU) is provided to control the power consumption of the device. The PMU provides four power management modes: Active, Powersave, Idle and Powerdown.

Active Mode indicates that all units on the 80C186EC are operating at ½ the CLKIN frequency.

Idle Mode freezes the clocks of the Execution and Bus units at a logic zero state (all peripherals continue to operate normally).

The Powerdown Mode freezes all internal clocks at a logic zero level and disables the crystal oscillator.

In Powersave Mode, all internal clock signals are divided by a programmable prescalar (up to 1/64 the normal frequency). Powersave Mode can be used with Idle Mode as well as during normal (Active Mode) operation.

## 80C187 Interface (80C186EC only)

The 80C186EC supports the direct connection of the 80C187 Numerics Processor Extension. The 80C187 can dramatically improve the performance of calculation intensive applications.

## ONCE Test Mode

To facilitate testing and inspection of devices when fixed into a target system, the 80C186EC has a test mode available which forces all output and input/output pins to be placed in the high-impedance state. ONCE stands for ''ON Circuit Emulation'', The ONCE mode is selected by forcing the A19/S6/ONCE pin low during a processor reset (this pin is weakly held high during reset to prevent inadvertant entrance into ONCE Mode).

# PACKAGE INFORMATION

This section describes the pin functions, pinout and thermal characteristics for the 80C186EC in the Plastic Quad Flat Pack (JEDEC PQFP), the EIAJ Quad Flat Pack (QFP) and the Shrink Quad Flat Pack (SQFP). For complete package specifications and information, see the Intel Packaging Outlines and Dimensions Guide (Order Number: 231369).

## Prefix Identification

Table 1 lists the prefix identifications.

**Table 1: Prefix Identification**

| Prefix | Note | Package Type | Temperature Range |
|---|---|---|---|
| x | | QFP (EIAJ) | Extended |
| x | 1 | PQFP | Extended/Commercial |
| x | 1 | SQFP | Extended/Commercial |
| x | 1 | QFP (EIAJ) | Commercial |

**NOTE:**

1. The 5V 25 MHz version is only available in commercial temperature range corresponding to 0°C to a 70°C ambient.
1. To address the fact that many of the package prefix variables have changed, all package prefix variables in this document are now indicated with an "x".

## Pin Descriptions

Each pin or logical set of pins is described in Table 2, There are four columns for each entry in the Pin Description Table. The following sections describe each column.

Column 1. Pin Name

In this column is a mnemonic that describes the pin function. Negation of the signal name (i.e. RESIN) implies that the signal is active low.

Column 2. Pin Type

A pin may be either power (P), ground (G), input only (I), output only (O) or input/output (I/O). Please note that some pins have more than 1 function. A19/S6/ONCE, for example, is normally an output but functions as an input during reset. For this reason A19/S6/ONCE is classified as an input/output pin.

**Column 3. Input Type (for I and I/O types only)**

There are two different types of input pins on the 80C186EC: asynchronous and synchronous. **Asynchronous** pins require that setup and hold times be met only to *guarantee recognition*. **Synchronous** input pins require that the setup and hold times be met to *guarantee proper operation*. Stated simply, missing a setup or hold on an asynchronous pin will result in something minor (i.e. a timer count will be missed) whereas missing a setup or hold on a synchronous pin will result in system failure (the system will ''lock up'').

An input pin may also be edge or level sensitive.

**Column 4: Output States (for O and I/O types only)**

The state of an output or I/O pin is dependent on the operating mode of the device. There are four modes of operation that are different from normal active mode: Bus Hold, Reset, Idle Mode, Powerdown Mode. This column describes the output pin state in each of these modes.

The legend for interpreting the information in the Pin Descriptions is shown in Table 1.

As an example, please refer to the table entry for AD12:0. The ''I/O'' signifies that the pins are bidirectional (i.e. have both an input and output function). The ''S'' indicates that, as an input the signal must be synchronized to CLKOUT for proper operation. The ''H(Z)'' indicates that these pins will float while the processor is in the Hold Acknowledge state. R(Z) indicates that these pins will float while $\overline{\text{RESIN}}$ is low. P(0) and I(0) indicate that these pins will drive 0 when the device is in either Powerdown or Idle Mode.

Some pins, the I/O Ports for example, can be programmed to perform more than one function. Multifunction pins have a ''/'' in their signal name between the different functions (i.e. P3.0/RXI1). If the input pin type or output pin state differ between functions, then that will be indicated by separating the state (or type) with a ''/'' (i.e. H(X)/H(Q)). In this example when the pin is configured as P3.0 then its hold output state is H(X); when configured as RXI1 its output state is H(Q).

All pins float while the processor is in the ONCE Mode (with the exception of OSCOUT).

**Table 1. Pin Description Nomenclature**

| Symbol | Description |
|---|---|
| P | Power Pin (apply + $V_{CC}$ voltage) |
| G | Ground (connect to $V_{SS}$) |
| I | Input only pin |
| O | Output only pin |
| I/O | Input/Output pin |
| S(E) | Synchronous, edge sensitive |
| S(L) | Synchronous, level sensitive |
| A(E) | Asynchronous, edge sensitive |
| A(L) | Asynchronous, level sensitive |
| H(1) | Output driven to $V_{CC}$ during bus hold |
| H(0) | Output driven to $V_{SS}$ during bus hold |
| H(Z) | Output floats during bus hold |
| H(Q) | Output remains active during bus hold |
| H(X) | Output retains current state during bus hold |
| R(WH) | Output weakly held at $V_{CC}$ during reset |
| R(1) | Output driven to $V_{CC}$ during reset |
| R(0) | Output driven to $V_{SS}$ during reset |
| R(Z) | Output floats during reset |
| R(Q) | Output remains active during reset |
| R(X) | Output retains current state during reset |
| I(1) | Output driven to $V_{CC}$ during Idle Mode |
| I(0) | Output driven to $V_{SS}$ during Idle Mode |
| I(Z) | Output floats during Idle Mode |
| I(Q) | Output remains active during Idle Mode |
| I(X) | Output retains current state during Idle Mode |
| P(1) | Output driven to $V_{CC}$ during Powerdown Mode |
| P(0) | Output driven to $V_{SS}$ during Powerdown Mode |
| P(Z) | Output floats during Powerdown Mode |
| P(Q) | Output remains active during Powerdown Mode |
| P(X) | Output retains current state during Powerdown Mode |

**Table 2. Pin Descriptions**

| Pin Name | Pin Type | Input Type | Output States | Pin Description |
|---|---|---|---|---|
| $V_{CC}$ | P | — | — | **POWER** +5V ±10% power supply connection |
| $V_{SS}$ | G | — | — | **GROUND** |
| CLKIN | I | A(E) | — | **CLocK INput** is the external clock input. An external oscillator operating at two times the required processor operating frequency can be connected to CLKIN. For crystal operation, CLKIN (along with OSCOUT) are the crystal connections to an internal Pierce oscillator. |
| OSCOUT | O | — | H(Q)<br>R(Q)<br>I(Q)<br>P(X) | **OSCillator OUTput** is only used when using a crystal to generate the internal clock. OSCOUT (along with CLKIN) are the crystal connections to an internal Pierce oscillator. This pin can not be used as 2X clock output for non-crystal applications (i.e. this pin is not connected for non-crystal applications). |
| CLKOUT | O | — | H(Q)<br>R(Q)<br>I(Q)<br>P(X) | **CLocK OUTput** provides a timing reference for inputs and outputs of the processor, and is one-half the input clock (CLKIN) frequency. CLKOUT has a 50% duty cycle and transitions every falling edge of CLKIN. |
| $\overline{RESIN}$ | I | A(L) | — | **RESet IN** causes the processor to immediately terminate any bus cycle in progress and assume an initialized state. All pins will be driven to a known state, and RESOUT will also be driven active. The rising edge (low-to-high) transition synchronizes CLKOUT with CLKIN before the processor begins fetching opcodes at memory location 0FFFF0H. |
| RESOUT | O | — | H(0)<br>R(1)<br>I(0)<br>P(0) | **RESet OUTput** that indicates the processor is currently in the reset state. RESOUT will remain active as long as $\overline{RESIN}$ remains active. |
| PDTMR | I/O | A(L) | H(WH)<br>R(Z)<br>P(WH)<br>I(WH) | **Power-Down TiMeR** pin (normally connected to an external capacitor) that determines the amount of time the processors waits after an exit from Powerdown before resuming normal operation. The duration of time required will depend on the startup characteristics of the crystal oscillator. |
| NMI | I | A(E) | — | **Non-Maskable Interrupt** input causes a TYPE-2 interrupt to be serviced by the CPU. NMI is latched internally. |
| $\overline{TEST}$/BUSY (TEST) | I | A(E) | — | **TEST** is used during the execution of the WAIT instruction to suspend CPU operation until the pin is sampled active (LOW). $\overline{TEST}$ is alternately known as **BUSY** when interfacing with an 80C187 numerics coprocessor (80C186EC only). |
| A19/S6/$\overline{ONCE}$ | I/O | A(L) | H(Z)<br>R(WH)<br>I(0)<br>P(0) | This pin drives address bit 19 during the address phase of the bus cycle. During T2 and T3 this pin functions as status bit 6. S6 is low to indicate CPU bus cycles and high to indicate DMA or refresh bus cycles. During a processor reset ($\overline{RESIN}$ active) this pin becomes the ONCE input pin. Holding this pin low during reset will force the part into ONCE Mode. |

**NOTE:**
Pin names in parentheses apply to the 80C188EC/80L188EC.

**Table 2. Pin Descriptions** (Continued)

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Input Type</th><th>Output States</th><th>Pin Description</th></tr>
<tr><td>A18/S5<br>A17/S4<br>A16/S3<br>(A15:8)</td><td>I/O</td><td>A(L)</td><td>H(Z)<br>R(WH)<br>I(0)<br>P(0)</td><td>These pins drive address information during the address phase of the bus cycle. During T2 and T3 these pins drive status information (which is always 0 on the 80C186EC). These pins are used as inputs during factory test; driving these pins low during reset will cause unspecified operation. On the 80C188EC, A15:8 provide valid address information for the entire bus cycle.</td></tr>
<tr><td>AD15/CAS2<br>AD14/CAS1<br>AD13/CAS0</td><td>I/O</td><td>S(L)</td><td>H(Z)<br>R(Z)<br>I(0)<br>P(0)</td><td>These pins are part of the multiplexed ADDRESS and DATA bus. During the address phase of the bus cycle, address bits 15 through 13 are presented on these pins and can be latched using ALE. Data information is transferred during the data phase of the bus cycle. Pins AD15:13/CAS2:0 drive the 82C59 slave address information during interrupt acknowledge cycles.</td></tr>
<tr><td>AD12:0<br>(AD7:0)</td><td>I/O</td><td>S(L)</td><td>H(Z)<br>R(Z)<br>I(0)<br>P(0)</td><td>These pins provide a multiplexed ADDRESS and DATA bus. During the address phase of the bus cycle, address bits 0 through 12 (0 through 7 on the 80C188EC) are presented on the bus and can be latched using ALE. Data information is transferred during the data phase of the bus cycle.</td></tr>
<tr><td>$\overline{S2:0}$</td><td>O</td><td>—</td><td>H(Z)<br>R(1)<br>I(1)<br>P(1)</td><td>Bus cycle Status are encoded on these pins to provide bus transaction information. $\overline{S2:0}$ are encoded as follows:
<table>
<tr><th>$\overline{S2}$</th><th>$\overline{S1}$</th><th>$\overline{S0}$</th><th>Bus Cycle Initiated</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Interrupt Acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read I/O</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write I/O</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Processor HALT</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Instruction Queue Fetch</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read Memory</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write Memory</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Passive (No bus activity)</td></tr>
</table></td></tr>
<tr><td>ALE</td><td>O</td><td>—</td><td>H(0)<br>R(0)<br>I(0)<br>P(0)</td><td>Address Latch Enable output is used to strobe address information into a transparent type latch during the address phase of the bus cycle.</td></tr>
<tr><td>$\overline{BHE}$<br>($\overline{RFSH}$)</td><td>O</td><td>—</td><td>H(Z)<br>R(Z)<br>I(1)<br>P(1)</td><td>Byte High Enable output to indicate that the bus cycle in progress is transferring data over the upper half of the data bus. $\overline{BHE}$ and A0 have the following logical encoding:
<table>
<tr><th>A0</th><th>$\overline{BHE}$</th><th>Encoding (for 80C186EC/80L186EC only)</th></tr>
<tr><td>0</td><td>0</td><td>Word transfer</td></tr>
<tr><td>0</td><td>1</td><td>Even Byte transfer</td></tr>
<tr><td>1</td><td>0</td><td>Odd Byte transfer</td></tr>
<tr><td>1</td><td>1</td><td>Refresh operation</td></tr>
</table>
On the 80C188EC/80L188EC, $\overline{RFSH}$ is asserted low to indicate a refresh bus cycle.</td></tr>
</table>

**NOTE:**
Pin names in parentheses apply to the 80C188EC/80L188EC.

**Table 2. Pin Descriptions** (Continued)

| Pin Name | Pin Type | Input Type | Output States | Pin Description |
|---|---|---|---|---|
| $\overline{RD}$ | O | — | H(Z)<br>R(Z)<br>I(1)<br>P(1) | **ReaD** output signals that the accessed memory or I/O device should drive data information onto the data bus. |
| $\overline{WR}$ | O | — | H(Z)<br>R(Z)<br>I(1)<br>P(1) | **WRite** output signals that data available on the data bus are to be written into the accessed memory or I/O device. |
| READY | I | A(L)<br>S(L)<br>(Note 1) | — | **READY** input to signal the completion of a bus cycle. READY must be active to terminate any 80C186EC bus cycle, unless it is ignored by correctly programming the Chip-Select unit. |
| $\overline{DEN}$ | O | — | H(Z)<br>R(Z)<br>I(1)<br>P(1) | **Data ENable** output to control the enable of bi-directional transceivers in a buffered system. $\overline{DEN}$ is active only when data is to be transferred on the bus. |
| DT/$\overline{R}$ | O | — | H(Z)<br>R(Z)<br>I(X)<br>P(X) | **Data Transmit/Receive** output controls the direction of a bi-directional buffer in a buffered system. |
| $\overline{LOCK}$ | I/O | A(L) | H(Z)<br>R(Z)<br>I(X)<br>P(X) | **LOCK** output indicates that the bus cycle in progress is not interruptable. The processor will not service other bus requests (such as HOLD) while $\overline{LOCK}$ is active. This pin is configured as a weakly held high input while $\overline{RESIN}$ is active and must not be driven low. |
| HOLD | I | A(L) | — | **HOLD** request input to signal that an external bus master wishes to gain control of the local bus. The processor will relinquish control of the local bus between instruction boundaries that are not LOCKed. |
| HLDA | O | — | H(1)<br>R(0)<br>I(0)<br>P(0) | **HoLD Acknowledge** output to indicate that the processor has relinquished control of the local bus. When HLDA is asserted, the processor will (or has) floated its data bus and control signals allowing another bus master to drive the signals directly. |
| $\overline{NCS}$ | O | — | H(1)<br>R(1)<br>I(1)<br>P(1) | **Numerics Coprocessor Select** output is generated when acessing a numerics coprocessor. This signal does not exist on the 80C188EC/80L188EC. |
| $\overline{ERROR}$ | I | A(L) | — | **ERROR** input that indicates the last numerics processor extension operation resulted in an exception condition. An interrupt TYPE 16 is generated if $\overline{ERROR}$ is sampled active at the beginning of a numerics operation. Systems not using an 80C187 must tie $\overline{ERROR}$ to $V_{CC}$. This signal does not exist on the 80C188EC/80L188EC. |

**NOTE:**
Pin names in parentheses apply to the 80C188EC/80L188EC.

**Table 2. Pin Descriptions** (Continued)

| Pin Name | Pin Type | Input Type | Output States | Pin Description |
|---|---|---|---|---|
| PEREQ | I | A(L) | — | **Processor Extension REQuest** signals that a data transfer between an 80C187 Numerics Processor Extension and Memory is pending. Systems not using an 80C187 must tie this pin to $V_{SS}$. This signal does not exist on the 80C188EC/80L188EC. |
| $\overline{UCS}$ | O | — | H(1)<br>R(1)<br>I(1)<br>P(1) | **Upper Chip Select** will go active whenever the address of a memory or I/O bus cycle is within the address range programmed by the user. After reset, $\overline{UCS}$ is configured to be active for memory accesses between 0FFC00H and 0FFFFFH. |
| $\overline{LCS}$ | O | — | H(1)<br>R(1)<br>I(1)<br>P(1) | **Lower Chip Select** will go active whenever the address of a memory or I/O bus cycle is within the address range programmed by the user. $\overline{LCS}$ is inactive after a reset. |
| P1.0/$\overline{GCS0}$<br>P1.1/$\overline{GCS1}$<br>P1.2/$\overline{GCS2}$<br>P1.3/$\overline{GCS3}$<br>P1.4/$\overline{GCS4}$<br>P1.5/$\overline{GCS5}$<br>P1.6/$\overline{GCS6}$<br>P1.7/$\overline{GCS7}$ | O | — | H(X)/H(1)<br>R(1)<br>I(X)/I(1)<br>P(X)/P(1) | These pins provide a multiplexed function. If enabled, each pin can provide a **General purpose Chip Select** output which will go active whenever the address of a memory or I/O bus cycle is within the address limitations programmed by the user. When not programmed as a Chip-Select, each pin may be used as a general purpose output port. |
| T0OUT<br>T1OUT | O | — | H(Q)<br>R(1)<br>I(Q)<br>P(X) | **Timer OUTput** pins can be programmed to provide single clock or continuous waveform generation, depending on the timer mode selected. |
| T0IN<br>T1IN | I | A(L)<br>A(E) | — | **Timer INput** is used either as clock or control signals, depending on the timer mode selected. This pin may be either level or edge sensitive depending on the programming mode. |
| INT7:0 | I | A(L)<br>A(E) | — | **Maskable INTerrupt** input will cause a vector to a specific Type interrupt routine. The INT6:0 pins can be used as cascade inputs from slave 8259A devices. The INT pins can be configured as level or edge sensitive. |
| $\overline{INTA}$ | O | — | H(1)<br>R(1)<br>I(1)<br>P(1) | **INTerrupt Acknowledge** output is a handshaking signal used by external 82C59A Programmable Interrupt Controllers. |
| P3.5<br>P3.4 | I/O | A(L) | H(X)<br>R(Z)<br>I(X)<br>H(X) | Bidirectional, open-drain port pins. |
| P3.3/DMAI1<br>P3.2/DMAI0 | O | — | H(X)<br>R(0)<br>I(Q)<br>P(X) | **DMA Interrupt** output goes active to indicate that the channel has completed a transfer. DMAI1 and DMAI0 are multiplexed with output only port functions. |

**NOTE:**
Pin names in parentheses apply to the 80C188EC/80L188EC.

**Table 2. Pin Descriptions** (Continued)

| Pin Name | Pin Type | Input Type | Output States | Pin Description |
|---|---|---|---|---|
| P3.1/TXI1 | O | — | H(X)/H(Q)<br>R(0)<br>I(Q)<br>P(X) | **Transmit Interrupt** output goes active to indicate that serial channel 1 has completed a transfer. TXI1 is multiplexed with an output only Port function. |
| P3.0/RXI1 | O | — | H(X)/H(Q)<br>R(0)<br>I(Q)<br>P(X) | **Receive Interrupt** output goes active to indicate that serial channel 1 has completed a reception. RXI1 is multiplexed with an output only port function. |
| $\overline{\text{WDTOUT}}$ | O | — | H(Q)<br>R(1)<br>I(Q)<br>P(X) | **WatchDog Timer OUTput** is driven low for four clock cycles when the watchdog timer reaches zero. $\overline{\text{WDTOUT}}$ may be ANDed with the power-on reset signal to reset the processor when the watchdog timer is not properly reset. |
| P2.7/$\overline{\text{CTS1}}$<br>P2.3/$\overline{\text{CTS0}}$ | I/O | A(L) | H(X)<br>R(Z)<br>I(X)<br>P(X) | **Clear-To-Send** input is used to prevent the transmission of serial data on the TXD signal pin. $\overline{\text{CTS1}}$ and $\overline{\text{CTS0}}$ are multiplexed with an I/O Port function. |
| P2.6/BCLK1<br>P2.2/BCLK0 | I/O | A(L)/<br>A(E) | H(X)<br>R(Z)<br>I(X)<br>P(X) | **Baud CLocK** input can be used as an alternate clock source for each of the integrated serial channels. The BCLK inputs are multiplexed with I/O Port functions. The BCLK input frequency cannot exceed ½ the operating frequency of the processor . |
| P2.5/TXD1<br>P2.1/TXD0 | I/O | A(L) | H(Q)<br>R(Z)<br>I(X)/I(Q)<br>P(X) | **Transmit Data** output provides serial data information. The TXD outputs are multiplexed with I/O Port functions. During synchronous serial communications, TXD will function as a clock output. |
| P2.4/RXD1<br>P2.0/RXD0 | I/O | A(L) | H(X)/H(Q)<br>R(Z)<br>I(X)/I(Q)<br>P(X) | **Receive Data** input accepts serial data information. The RXD pins are multiplexed with I/O Port functions. During synchronous serial communications, RXD is bi-directional and will become an output for transmission of data (TXD becomes the clock). |
| DRQ3:0 | I | A(L) | — | **DMA ReQuest** input pins are used to request a DMA transfer. The timing of the request is dependent on the programmed synchronization mode. |

**NOTES:**
1. READY is A(E) for the rising edge of CLKOUT, S(E) for the falling edge of CLKOUT.
2. Pin names in parentheses apply to the 80C188EC/80L188EC.

## Pinout

Tables 3 and 4 list the pin names with package location for the 100-pin Plastic Quad Flat Pack (PQFP) component. Figure 4 depicts the PQFP package as viewed from the top side of the component (i.e. contacts facing down).

Tables 5 and 6 list the pin names with package location for the 100-pin EIAJ Quad Flat Pack (QFP) component. Figure 5 depicts the QFP package as viewed from the top side of the component (i.e. contacts facing down).

Tables 7 and 8 list the pin names with package location for the 100-pin Shrink Quad Flat Pack (SQFP) component. Figure 6 depicts the SQFP package as viewed from the top side of the component (i.e., contacts facing down).

**Table 3. PQFP Pin Functions with Location**

| AD Bus | |
|---|---|
| **Name** | **Pin** |
| AD0 | 73 |
| AD1 | 72 |
| AD2 | 71 |
| AD3 | 70 |
| AD4 | 66 |
| AD5 | 65 |
| AD6 | 64 |
| AD7 | 63 |
| AD8 (A8) | 60 |
| AD9 (A9) | 59 |
| AD10 (A10) | 58 |
| AD11 (A11) | 57 |
| AD12 (A12) | 56 |
| AD13/CAS0 (A13/CAS0) | 55 |
| AD14/CAS1 (A14/CAS1) | 54 |
| AD15/CAS2 (A15/CAS2) | 53 |
| A16/S3 | 77 |
| A17/S4 | 76 |
| A18/S5 | 75 |
| A19/S6/$\overline{\text{ONCE}}$ | 74 |

| Bus Control | |
|---|---|
| **Name** | **Pin** |
| ALE | 52 |
| $\overline{\text{BHE}}$ ($\overline{\text{RFSH}}$) | 51 |
| $\overline{\text{S0}}$ | 78 |
| $\overline{\text{S1}}$ | 79 |
| $\overline{\text{S2}}$ | 80 |
| $\overline{\text{RD}}$ | 50 |
| $\overline{\text{WR}}$ | 49 |
| READY | 85 |
| $\overline{\text{DEN}}$ | 47 |
| DT/$\overline{\text{R}}$ | 46 |
| $\overline{\text{LOCK}}$ | 48 |
| HOLD | 44 |
| HLDA | 45 |
| $\overline{\text{INTA}}$ | 34 |

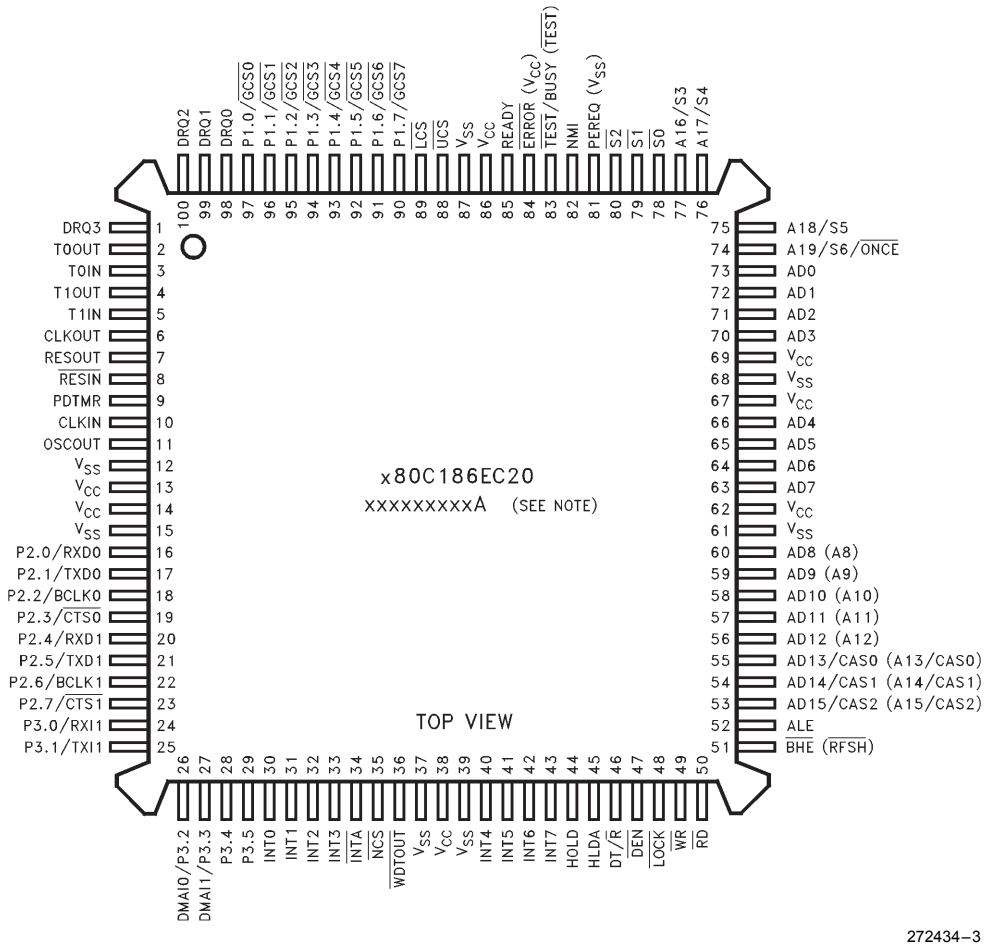
| Power and Ground | |
|---|---|
| **Name** | **Pin** |
| $V_{CC}$ | 13 |
| $V_{CC}$ | 14 |
| $V_{CC}$ | 38 |
| $V_{CC}$ | 62 |
| $V_{CC}$ | 67 |
| $V_{CC}$ | 69 |
| $V_{CC}$ | 86 |
| $V_{SS}$ | 12 |
| $V_{SS}$ | 15 |
| $V_{SS}$ | 37 |
| $V_{SS}$ | 39 |
| $V_{SS}$ | 61 |
| $V_{SS}$ | 68 |
| $V_{SS}$ | 87 |

| Processor Control | |
|---|---|
| **Name** | **Pin** |
| $\overline{\text{RESIN}}$ | 8 |
| RESOUT | 7 |
| CLKIN | 10 |
| OSCOUT | 11 |
| CLKOUT | 6 |
| $\overline{\text{TEST}}$/BUSY ($\overline{\text{TEST}}$) | 83 |
| PEREQ ($V_{SS}$) | 81 |
| $\overline{\text{NCS}}$ (N.C.) | 35 |
| $\overline{\text{ERROR}}$ ($V_{CC}$) | 84 |
| PDTMR | 9 |
| NMI | 82 |
| INT0 | 30 |
| INT1 | 31 |
| INT2 | 32 |
| INT3 | 33 |
| INT4 | 40 |
| INT5 | 41 |
| INT6 | 42 |
| INT7 | 43 |

| I/O | |
|---|---|
| **Name** | **Pin** |
| $\overline{\text{UCS}}$ | 88 |
| $\overline{\text{LCS}}$ | 89 |
| | |
| P1.7/$\overline{\text{GCS7}}$ | 90 |
| P1.6/$\overline{\text{GCS6}}$ | 91 |
| P1.5/$\overline{\text{GCS5}}$ | 92 |
| P1.4/$\overline{\text{GCS4}}$ | 93 |
| P1.3/$\overline{\text{GCS3}}$ | 94 |
| P1.2/$\overline{\text{GCS2}}$ | 95 |
| P1.1/$\overline{\text{GCS1}}$ | 96 |
| P1.0/$\overline{\text{GCS0}}$ | 97 |
| | |
| P2.7/$\overline{\text{CTS1}}$ | 23 |
| P2.6/BCLK1 | 22 |
| P2.5/TXD1 | 21 |
| P2.4/RXD1 | 20 |
| P2.3/$\overline{\text{CTS0}}$ | 19 |
| P2.2/BCLK0 | 18 |
| P2.1/TXD0 | 17 |
| P2.0/RXD0 | 16 |
| | |
| P3.5 | 29 |
| P3.4 | 28 |
| P3.3/DMAI1 | 27 |
| P3.2/DMAI0 | 26 |
| P3.1/TXI1 | 25 |
| P3.0/RXI1 | 24 |
| | |
| T0IN | 3 |
| T0OUT | 2 |
| T1IN | 5 |
| T1OUT | 4 |
| | |
| DRQ0 | 98 |
| DRQ1 | 99 |
| DRQ2 | 100 |
| DRQ3 | 1 |
| | |
| $\overline{\text{WDTOUT}}$ | 36 |

**Table 4. PQFP Pin Locations with Pin Name**

| Pin | Name | Pin | Name | Pin | Name | Pin | Name |
|---|---|---|---|---|---|---|---|
| 1 | DRQ3 | 26 | DMAI0/P3.2 | 51 | $\overline{BHE}$ ($\overline{RFSH}$) | 76 | A17/S4 |
| 2 | T0OUT | 27 | DMAI1/P3.3 | 52 | ALE | 77 | A16/S3 |
| 3 | T0IN | 28 | P3.4 | 53 | AD15 (A15) | 78 | $\overline{S0}$ |
| 4 | T1OUT | 29 | P3.5 | 54 | AD14 (A14) | 79 | $\overline{S1}$ |
| 5 | T1IN | 30 | INT0 | 55 | AD13 (A13) | 80 | $\overline{S2}$ |
| 6 | CLKOUT | 31 | INT1 | 56 | AD12 (A12) | 81 | PEREQ ($V_{SS}$) |
| 7 | RESOUT | 32 | INT2 | 57 | AD11 (A11) | 82 | NMI |
| 8 | $\overline{RESIN}$ | 33 | INT3 | 58 | AD10 (A10) | 83 | $\overline{TEST}$ |
| 9 | PDTMR | 34 | $\overline{INTA}$ | 59 | AD9 (A9) | 84 | $\overline{ERROR}$ ($V_{CC}$) |
| 10 | CLKIN | 35 | $\overline{NCS}$ (N.C.) | 60 | AD8 (A8) | 85 | READY |
| 11 | OSCOUT | 36 | $\overline{WDTOUT}$ | 61 | $V_{SS}$ | 86 | $V_{CC}$ |
| 12 | $V_{SS}$ | 37 | $V_{SS}$ | 62 | $V_{CC}$ | 87 | $V_{SS}$ |
| 13 | $V_{CC}$ | 38 | $V_{CC}$ | 63 | AD7 | 88 | $\overline{UCS}$ |
| 14 | $V_{CC}$ | 39 | $V_{SS}$ | 64 | AD6 | 89 | $\overline{LCS}$ |
| 15 | $V_{SS}$ | 40 | INT4 | 65 | AD5 | 90 | P1.7/$\overline{GCS7}$ |
| 16 | P2.0/RXD0 | 41 | INT5 | 66 | AD4 | 91 | P1.6/$\overline{GCS6}$ |
| 17 | P2.1/TXD0 | 42 | INT6 | 67 | $V_{CC}$ | 92 | P1.5/$\overline{GCS5}$ |
| 18 | P2.2/BCLK0 | 43 | INT7 | 68 | $V_{SS}$ | 93 | P1.4/$\overline{GCS4}$ |
| 19 | P2.3/$\overline{CTS0}$ | 44 | HOLD | 69 | $V_{CC}$ | 94 | P1.3/$\overline{GCS3}$ |
| 20 | P2.4/RXD1 | 45 | HLDA | 70 | AD3 | 95 | P1.2/$\overline{GCS2}$ |
| 21 | P2.5/TXD1 | 46 | DT/$\overline{R}$ | 71 | AD2 | 96 | P1.1/$\overline{GCS1}$ |
| 22 | P2.6/BCLK1 | 47 | $\overline{DEN}$ | 72 | AD1 | 97 | P1.0/$\overline{GCS0}$ |
| 23 | P2.7/$\overline{CTS1}$ | 48 | $\overline{LOCK}$ | 73 | AD0 | 98 | DRQ0 |
| 24 | P3.0/RXI1 | 49 | $\overline{WR}$ | 74 | A19/S6/$\overline{ONCE}$ | 99 | DRQ1 |
| 25 | P3.1/TXI1 | 50 | $\overline{RD}$ | 75 | A18/S5 | 100 | DRQ2 |




NOTE:
This is the FPO number location (indicated by X's).

Figure 4. 100-Pin Plastic Quad Flat Pack Package (PQFP)

**Table 5. QFP Pin Names with Package Location**

| AD Bus | |
|---|---|
| **Name** | **Pin** |
| AD0 | 76 |
| AD1 | 75 |
| AD2 | 74 |
| AD3 | 73 |
| AD4 | 69 |
| AD5 | 68 |
| AD6 | 67 |
| AD7 | 66 |
| AD8 (A8) | 63 |
| AD9 (A9) | 62 |
| AD10 (A10) | 61 |
| AD11 (A11) | 60 |
| AD12 (A12) | 59 |
| AD13/CAS0 (A13/CAS0) | 58 |
| AD14/CAS1 (A14/CAS1) | 57 |
| AD15/CAS2 (A15/CAS2) | 56 |
| A16/S3 | 80 |
| A17/S4 | 79 |
| A18/S5 | 78 |
| A19/S6/$\overline{\text{ONCE}}$ | 77 |

| Bus Control | |
|---|---|
| **Name** | **Pin** |
| ALE | 55 |
| $\overline{\text{BHE}}$ ($\overline{\text{RFSH}}$) | 54 |
| $\overline{\text{S0}}$ | 81 |
| $\overline{\text{S1}}$ | 82 |
| $\overline{\text{S2}}$ | 83 |
| $\overline{\text{RD}}$ | 53 |
| $\overline{\text{WR}}$ | 52 |
| READY | 88 |
| $\overline{\text{DEN}}$ | 50 |
| DT/$\overline{\text{R}}$ | 49 |
| $\overline{\text{LOCK}}$ | 51 |
| HOLD | 47 |
| HLDA | 48 |
| $\overline{\text{INTA}}$ | 37 |

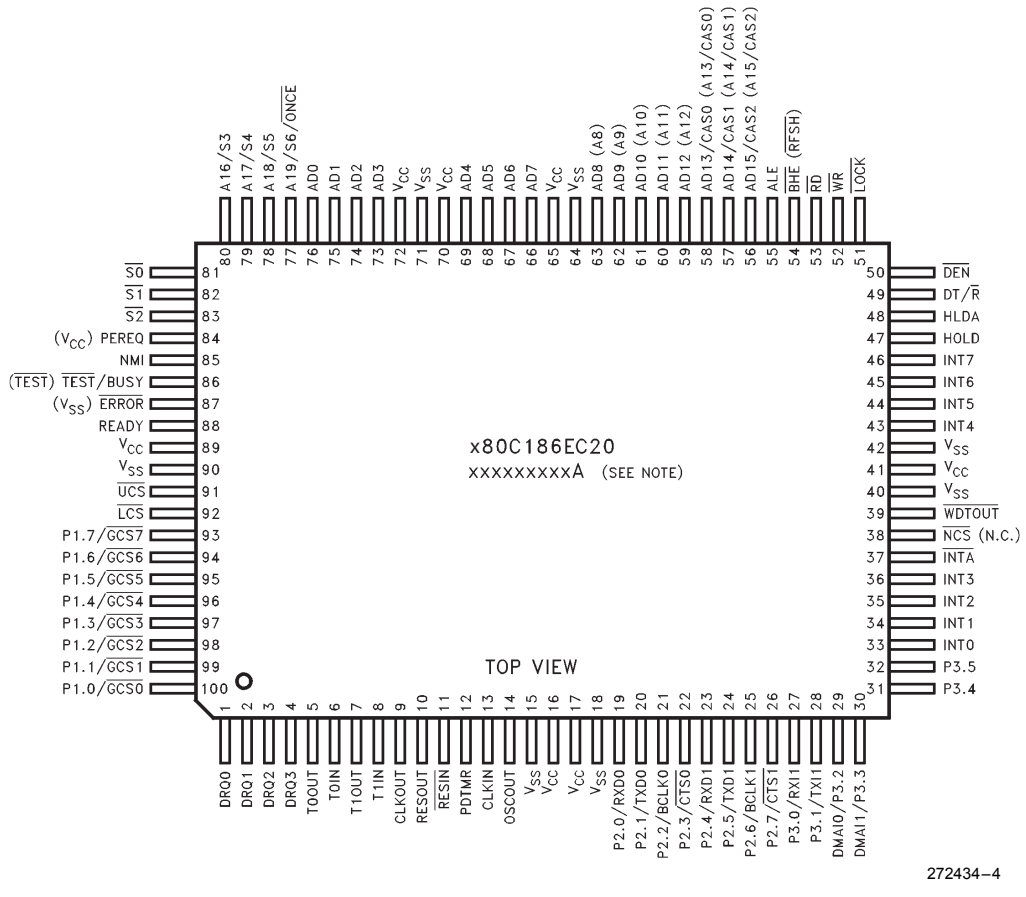
| Power and Ground | |
|---|---|
| **Name** | **Pin** |
| $V_{CC}$ | 16 |
| $V_{CC}$ | 17 |
| $V_{CC}$ | 41 |
| $V_{CC}$ | 65 |
| $V_{CC}$ | 70 |
| $V_{CC}$ | 72 |
| $V_{CC}$ | 89 |
| $V_{SS}$ | 15 |
| $V_{SS}$ | 18 |
| $V_{SS}$ | 40 |
| $V_{SS}$ | 42 |
| $V_{SS}$ | 64 |
| $V_{SS}$ | 71 |
| $V_{SS}$ | 90 |

| Processor Control | |
|---|---|
| **Name** | **Pin** |
| $\overline{\text{RESIN}}$ | 11 |
| RESOUT | 10 |
| CLKIN | 13 |
| OSCOUT | 14 |
| CLKOUT | 9 |
| $\overline{\text{TEST}}$/BUSY ($\overline{\text{TEST}}$) | 86 |
| PEREQ ($V_{SS}$) | 84 |
| $\overline{\text{NCS}}$ (N.C.) | 38 |
| $\overline{\text{ERROR}}$ ($V_{CC}$) | 87 |
| PDTMR | 12 |
| NMI | 85 |
| INT0 | 33 |
| INT1 | 34 |
| INT2 | 35 |
| INT3 | 36 |
| INT4 | 43 |
| INT5 | 44 |
| INT6 | 45 |
| INT7 | 46 |

| I/O | |
|---|---|
| **Name** | **Pin** |
| $\overline{\text{UCS}}$ | 91 |
| $\overline{\text{LCS}}$ | 92 |
| | |
| P1.7/$\overline{\text{GCS7}}$ | 93 |
| P1.6/$\overline{\text{GCS6}}$ | 94 |
| P1.5/$\overline{\text{GCS5}}$ | 95 |
| P1.4/$\overline{\text{GCS4}}$ | 96 |
| P1.3/$\overline{\text{GCS3}}$ | 97 |
| P1.2/$\overline{\text{GCS2}}$ | 98 |
| P1.1/$\overline{\text{GCS1}}$ | 99 |
| P1.0/$\overline{\text{GCS0}}$ | 100 |
| | |
| P2.7/$\overline{\text{CTS1}}$ | 26 |
| P2.6/BCLK1 | 25 |
| P2.5/TXD1 | 24 |
| P2.4/RXD1 | 23 |
| P2.3/$\overline{\text{CTS0}}$ | 22 |
| P2.2/BCLK0 | 21 |
| P2.1/TXD0 | 20 |
| P2.0/RXD0 | 19 |
| | |
| P3.5 | 32 |
| P3.4 | 31 |
| P3.3/DMAI1 | 30 |
| P3.2/DMAI0 | 29 |
| P3.1/TXI1 | 28 |
| P3.0/RXI1 | 27 |
| | |
| T0IN | 6 |
| T0OUT | 5 |
| T1IN | 8 |
| T1OUT | 7 |
| | |
| DRQ0 | 1 |
| DRQ1 | 2 |
| DRQ2 | 3 |
| DRQ3 | 4 |
| | |
| $\overline{\text{WDTOUT}}$ | 39 |

**Table 6. QFP Package Location with Pin Names**

| Pin | Name | Pin | Name | Pin | Name | Pin | Name |
|---|---|---|---|---|---|---|---|
| 1 | DRQ0 | 26 | P2.7/$\overline{\text{CTS1}}$ | 51 | $\overline{\text{LOCK}}$ | 76 | AD0 |
| 2 | DRQ1 | 27 | P3.0/RXI1 | 52 | $\overline{\text{WR}}$ | 77 | A19/S6/$\overline{\text{ONCE}}$ |
| 3 | DRQ2 | 28 | P3.1/TXI1 | 53 | $\overline{\text{RD}}$ | 78 | A18/S5 |
| 4 | DRQ3 | 29 | DMAI0/P3.2 | 54 | $\overline{\text{BHE}}$ ($\overline{\text{RFSH}}$) | 79 | A17/S4 |
| 5 | T0OUT | 30 | DMAI1/P3.3 | 55 | ALE | 80 | A16/S3 |
| 6 | T0IN | 31 | P3.4 | 56 | AD15 (A15) | 81 | $\overline{\text{S0}}$ |
| 7 | T1OUT | 32 | P3.5 | 57 | AD14 (A14) | 82 | $\overline{\text{S1}}$ |
| 8 | T1IN | 33 | INT0 | 58 | AD13 (A13) | 83 | $\overline{\text{S2}}$ |
| 9 | CLKOUT | 34 | INT1 | 59 | AD12 (A12) | 84 | PEREQ ($V_{SS}$) |
| 10 | RESOUT | 35 | INT2 | 60 | AD11 (A11) | 85 | NMI |
| 11 | $\overline{\text{RESIN}}$ | 36 | INT3 | 61 | AD10 (A10) | 86 | $\overline{\text{TEST}}$ |
| 12 | PDTMR | 37 | $\overline{\text{INTA}}$ | 62 | AD9 (A9) | 87 | $\overline{\text{ERROR}}$ ($V_{CC}$) |
| 13 | CLKIN | 38 | $\overline{\text{NCS}}$ (N.C.) | 63 | AD8 (A8) | 88 | READY |
| 14 | OSCOUT | 39 | $\overline{\text{WDTOUT}}$ | 64 | $V_{SS}$ | 89 | $V_{CC}$ |
| 15 | $V_{SS}$ | 40 | $V_{SS}$ | 65 | $V_{CC}$ | 90 | $V_{SS}$ |
| 16 | $V_{CC}$ | 41 | $V_{CC}$ | 66 | AD7 | 91 | $\overline{\text{UCS}}$ |
| 17 | $V_{CC}$ | 42 | $V_{SS}$ | 67 | AD6 | 92 | $\overline{\text{LCS}}$ |
| 18 | $V_{SS}$ | 43 | INT4 | 68 | AD5 | 93 | P1.7/$\overline{\text{GCS7}}$ |
| 19 | P2.0/RXD0 | 44 | INT5 | 69 | AD4 | 94 | P1.6/$\overline{\text{GCS6}}$ |
| 20 | P2.1/TXD0 | 45 | INT6 | 70 | $V_{CC}$ | 95 | P1.5/$\overline{\text{GCS5}}$ |
| 21 | P2.2/BCLK0 | 46 | INT7 | 71 | $V_{SS}$ | 96 | P1.4/$\overline{\text{GCS4}}$ |
| 22 | P2.3/$\overline{\text{CTS0}}$ | 47 | HOLD | 72 | $V_{CC}$ | 97 | P1.3/$\overline{\text{GCS3}}$ |
| 23 | P2.4/RXD1 | 48 | HLDA | 73 | AD3 | 98 | P1.2/$\overline{\text{GCS2}}$ |
| 24 | P2.5/TXD1 | 49 | DT/$\overline{\text{R}}$ | 74 | AD2 | 99 | P1.1/$\overline{\text{GCS1}}$ |
| 25 | P2.6/BCLK1 | 50 | $\overline{\text{DEN}}$ | 75 | AD1 | 100 | P1.0/$\overline{\text{GCS0}}$ |




NOTE:
This is the FPO number location (indicated by X's).

Figure 5: Quad Flat Pack (EIAJ) Pinout Diagram

**Table 7. SQFP Pin Functions with Location**

| AD Bus | |
|---|---|
| AD0 | 73 |
| AD1 | 72 |
| AD2 | 71 |
| AD3 | 70 |
| AD4 | 66 |
| AD5 | 65 |
| AD6 | 64 |
| AD7 | 63 |
| AD8 (A8) | 60 |
| AD9 (A9) | 59 |
| AD10 (A10) | 58 |
| AD11 (A11) | 57 |
| AD12 (A12) | 56 |
| AD13 (A13) | 55 |
| AD14 (A14) | 54 |
| AD15 (A15) | 53 |
| A16 | 77 |
| A17 | 76 |
| A18 | 75 |
| A19/ONCE | 74 |

| Bus Control | |
|---|---|
| ALE | 52 |
| $\overline{BHE}$ ($\overline{RFSH}$) | 51 |
| $\overline{S0}$ | 78 |
| $\overline{S1}$ | 79 |
| $\overline{S2}$ | 80 |
| $\overline{RD}$ | 50 |
| $\overline{WR}$ | 49 |
| READY | 85 |
| DT/$\overline{R}$ | 46 |
| $\overline{DEN}$ | 47 |
| $\overline{LOCK}$ | 48 |
| HOLD | 44 |
| HLDA | 45 |

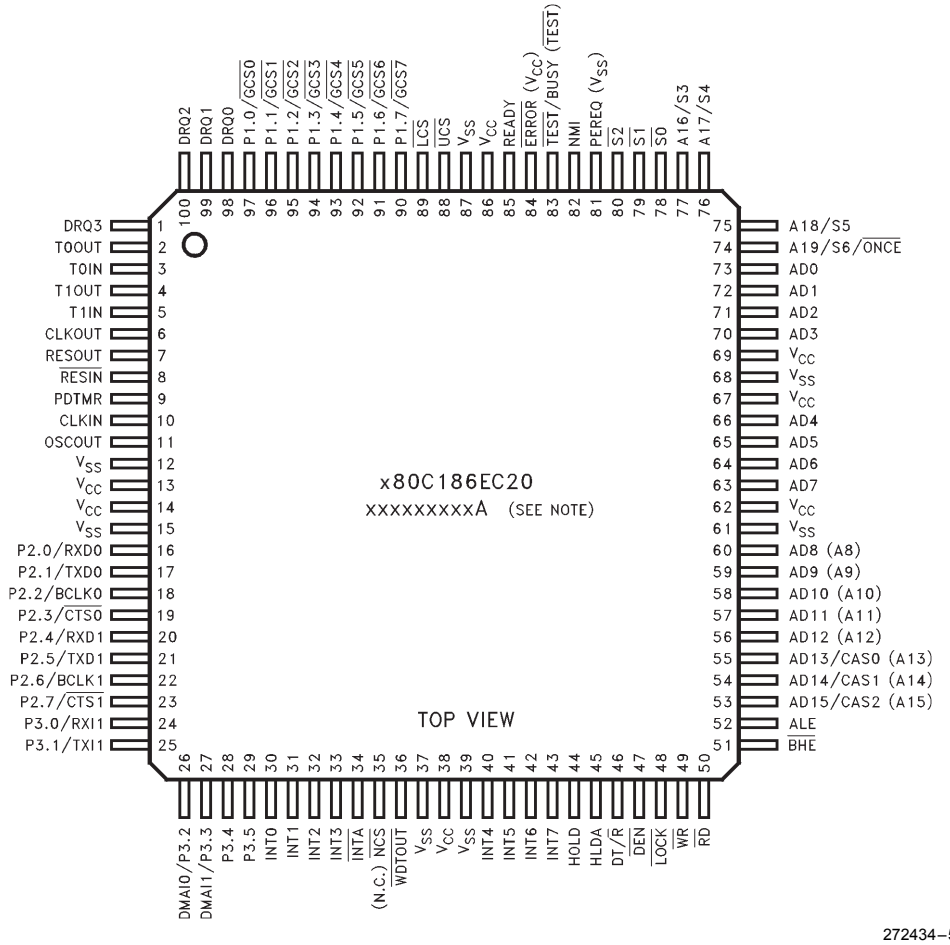
| Processor Control | |
|---|---|
| $\overline{RESIN}$ | 8 |
| RESOUT | 7 |
| CLKIN | 10 |
| OSCOUT | 11 |
| CLKOUT | 6 |
| $\overline{TEST}$/BUSY | 83 |
| NMI | 82 |
| INT0 | 30 |
| INT1 | 31 |
| INT2 | 32 |
| INT3 | 33 |
| INT4 | 40 |
| INT5 | 41 |
| INT6 | 42 |
| INT7 | 43 |
| $\overline{INTA}$ | 34 |
| $\overline{PEREQ}$ ($V_{SS}$) | 81 |
| $\overline{ERROR}$ ($V_{CC}$) | 84 |
| $\overline{NCS}$ (N.C.) | 35 |
| PDTMR | 9 |

| Power and Ground | |
|---|---|
| $V_{CC}$ | 13 |
| $V_{CC}$ | 14 |
| $V_{CC}$ | 38 |
| $V_{CC}$ | 62 |
| $V_{CC}$ | 67 |
| $V_{CC}$ | 69 |
| $V_{CC}$ | 86 |
| $V_{SS}$ | 12 |
| $V_{SS}$ | 15 |
| $V_{SS}$ | 37 |
| $V_{SS}$ | 39 |
| $V_{SS}$ | 61 |
| $V_{SS}$ | 68 |
| $V_{SS}$ | 87 |

| I/O | |
|---|---|
| $\overline{UCS}$ | 88 |
| $\overline{LCS}$ | 89 |
| | |
| P1.0/$\overline{GCS0}$ | 97 |
| P1.1/$\overline{GCS1}$ | 96 |
| P1.2/$\overline{GCS2}$ | 95 |
| P1.3/$\overline{GCS3}$ | 94 |
| P1.4/$\overline{GCS4}$ | 93 |
| P1.5/$\overline{GCS5}$ | 92 |
| P1.6/$\overline{GCS6}$ | 91 |
| P1.7/$\overline{GCS7}$ | 90 |
| | |
| P2.0/RXD0 | 16 |
| P2.1/TXD0 | 17 |
| P2.2/BCLK0 | 18 |
| P2.3/$\overline{CTS0}$ | 19 |
| P2.4/RXD1 | 20 |
| P2.5/TXD1 | 21 |
| P2.6/BCLK1 | 22 |
| P2.7/$\overline{CTS1}$ | 23 |
| | |
| P3.0/RXI1 | 24 |
| P3.1/TXI1 | 25 |
| P3.2/DMAI0 | 26 |
| P3.3/DMAI1 | 27 |
| P3.4 | 28 |
| P3.5 | 29 |
| | |
| DRQ0 | 98 |
| DRQ1 | 99 |
| DRQ2 | 100 |
| DRQ3 | 1 |
| | |
| T0IN | 3 |
| T0OUT | 2 |
| T1IN | 5 |
| T1OUT | 4 |
| $\overline{WDTOUT}$ | 36 |

**Table 8. SQFP Pin Locations with Pin Names**

| Pin | Name | Pin | Name | Pin | Name | Pin | Name |
|---|---|---|---|---|---|---|---|
| 1 | DRQ3 | 26 | P3.2/DMAI0 | 51 | $\overline{BHE}$ ($\overline{RFSH}$) | 76 | A17 |
| 2 | T0OUT | 27 | P3.3/DMAI1 | 52 | ALE | 77 | A16 |
| 3 | T0IN | 28 | P3.4 | 53 | AD15 (A15) | 78 | $\overline{S0}$ |
| 4 | T1OUT | 29 | P3.5 | 54 | AD14 (A14) | 79 | $\overline{S1}$ |
| 5 | T1IN | 30 | INT0 | 55 | AD13 (A13) | 80 | $\overline{S2}$ |
| 6 | CLKOUT | 31 | INT1 | 56 | AD12 (A12) | 81 | PEREQ ($V_{SS}$) |
| 7 | RESOUT | 32 | INT2 | 57 | AD11 (A11) | 82 | MNI |
| 8 | $\overline{RESIN}$ | 33 | INT3 | 58 | AD10 (A10) | 83 | $\overline{TEST}$/BUSY ($\overline{TEST}$) |
| 9 | PDTMR | 34 | $\overline{INTA}$ | 59 | AD9 (A9) | 84 | $\overline{ERROR}$ ($V_{CC}$) |
| 10 | CLKIN | 35 | $\overline{NSC}$ (N.C.) | 60 | AD8 (A8) | 85 | READY |
| 11 | OSCOUT | 36 | $\overline{WDTOUT}$ | 61 | $V_{SS}$ | 86 | $V_{CC}$ |
| 12 | $V_{SS}$ | 37 | $V_{SS}$ | 62 | $V_{CC}$ | 87 | $V_{SS}$ |
| 13 | $V_{CC}$ | 38 | $V_{CC}$ | 63 | AD7 (A7) | 88 | $\overline{UCS}$ |
| 14 | $V_{CC}$ | 39 | $V_{SS}$ | 64 | AD6 (A6) | 89 | $\overline{LCS}$ |
| 15 | $V_{SS}$ | 40 | INT4 | 65 | AD5 | 90 | P1.7/$\overline{GCS7}$ |
| 16 | P2.0/RXD0 | 41 | INT5 | 66 | AD4 | 91 | P1.6/$\overline{GS6}$ |
| 17 | P2.1/TXD0 | 42 | INT6 | 67 | $V_{CC}$ | 92 | P1.5/$\overline{GCS5}$ |
| 18 | P2.2/BCLK0 | 43 | INT7 | 68 | $V_{SS}$ | 93 | P1.4/$\overline{GCS4}$ |
| 19 | P2.3/$\overline{CTS0}$ | 44 | HOLD | 69 | $V_{CC}$ | 94 | P1.3/$\overline{GCS3}$ |
| 20 | P2.4/RXD1 | 45 | HLDA | 70 | AD3 | 95 | P1.2/$\overline{GCS2}$ |
| 21 | P2.5/TXD1 | 46 | DT/$\overline{R}$ | 71 | AD2 | 96 | P1.1/$\overline{GCS1}$ |
| 22 | P2.6/BCLK1 | 47 | $\overline{DEN}$ | 72 | AD1 | 97 | P1.0/$\overline{GCS0}$ |
| 23 | P2.7/$\overline{CTS1}$ | 48 | $\overline{LOCK}$ | 73 | AD0 | 98 | DRQ0 |
| 24 | P3.0/RXI1 | 49 | $\overline{WR}$ | 74 | A19/ONCE | 99 | DRQ1 |
| 25 | P3.1/TXI1 | 50 | $\overline{RD}$ | 75 | AD18 | 100 | DRQ2 |




NOTE:
This is the FPO number location (indicated by X's)

Figure 6: 100-Pin Shrink Quad Flat Pack Package (SQFP)

## Package Thermal Specifications

The 80C186EC/80L186EC is specified for operation when $T_C$ (the case temperature) is within the range of $-40°C$ to $+100°C$. $T_C$ may be measured in any environment to determine whether the processor is within the specified operating range. The case temperature must be measured at the center of the top surface.

$T_A$ (the ambient temperature) can be calculated from $\theta_{CA}$ (thermal resistance from the case to ambient) with the following equation:

$$T_A = T_C - P * \theta_{CA}$$

Typical values for $\theta_{CA}$ at various airflows are given in Table 9. P (the maximum power consumption—specified in Watts) is calculated by using the maximum $I_{CC}$ and $V_{CC}$ of 5.5V.

**Table 9. Thermal Resistance ($\theta_{CA}$) at Various Airflows (in °C/Watt)**

| | Airflow in ft/min (m/sec) | | | | | |
|---|---|---|---|---|---|---|
| | **0 (0)** | **200 (1.01)** | **400 (2.03)** | **600 (3.04)** | **800 (4.06)** | **1000 (5.07)** |
| $\theta_{CA}$ (PQFP) | 27.0 | 22.0 | 18.0 | 15.0 | 14.0 | 13.5 |
| $\theta_{CA}$ (QFP) | 64.5 | 55.5 | 51.0 | TBD | TBD | TBD |
| $\theta_{CA}$ (SQFP) | 62.0 | TBD | TBD | TBD | TBD | TBD |

# ELECTRICAL SPECIFICATIONS

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

## Absolute Maximum Ratings

Storage Temperature . . . . . −65°C to +150°C

Case Temperature Under Bias . . . −65°C to +100°C

Supply Voltage
with Respect to $V_{SS}$ . . . . . −0.5V to +6.5V

Voltage on Other Pins
with Respect to $V_{SS}$ . . . . . −0.5V to $V_{CC}$ + 0.5V

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

## Recommended Connections

Power and ground connections must be made to multiple $V_{CC}$ and $V_{SS}$ pins. Every 80C186EC-based circuit board should include separate power ($V_{CC}$) and ground ($V_{SS}$) planes. Every $V_{CC}$ pin must be connected to the power plane, and every $V_{SS}$ pin must be connected to the ground plane. Liberal decoupling capacitance should be placed near the processor. The processor can cause transient power surges when its output buffers transition, particularly when connected to large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance is reduced by placing the decoupling capacitors as close as possible to the processor $V_{CC}$ and $V_{SS}$ package pins.

Always connect any unused input to an appropriate signal level. In particular, unused interrupt inputs (NMI, INT0:7) should be connected to $V_{SS}$ through a pull-down resistor. Leave any unused output pin unconnected.

## DC SPECIFICATIONS (80C186EC/80C188EC)

| Symbol | Parameter | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 4.5 | 5.5 | V | |
| $V_{IL}$ | Input Low Voltage | −0.5 | 0.3 $V_{CC}$ | V | |
| $V_{IH}$ | Input High Voltage | 0.7 $V_{CC}$ | $V_{CC}$ + 0.5 | V | |
| $V_{OL}$ | Output Low Voltage | | 0.45 | V | $I_{OL}$ = 3 mA (Min) |
| $V_{OH}$ | Output High Voltage | $V_{CC}$ − 0.5 | | V | $I_{OH}$ = −2 mA (Min) |
| $V_{HYR}$ | Input Hysteresis on $\overline{\text{RESIN}}$ | 0.5 | | V | |
| $I_{LI}$ | Input Leakage Current for Pins: AD15:0 (AD7:0, A15:8), READY, HOLD, $\overline{\text{RESIN}}$, CLKIN, $\overline{\text{TEST}}$/BUSY, NMI, INT7:0, T0IN, T1IN, P2.7–P2.0, P3.5–P3.0, DRQ3:0, PEREQ, $\overline{\text{ERROR}}$ | | ±15 | μA | $0 \le V_{IN} \le V_{CC}$ |
| $I_{LIU}$ | Input Leakage for Pins with Pullups Active During Reset: A19:16, $\overline{\text{LOCK}}$ | −0.275 | −5 | mA | $V_{IN}$ = 0.7 $V_{CC}$ (Note 1) |
| $I_{LO}$ | Output Leakage for Floated Output Pins | | ±15 | μA | $0.45 \le V_{OUT} \le V_{CC}$ (Note 2) |
| $I_{CC}$ | Supply Current Cold (in RESET)<br>80C186EC25<br>80C186EC20<br>80C186EC13 | | <br>125<br>100<br>70 | <br>mA<br>mA<br>mA | <br>(Notes 3, 7)<br>(Note 3)<br>(Note 3) |
| $I_{ID}$ | Supply Current in Idle Mode<br>80C186EC25<br>80C186EC20<br>80C186EC13 | | <br>92<br>76<br>50 | <br>mA<br>mA<br>mA | <br>(Notes 4, 7)<br>(Note 4)<br>(Note 4) |
| $I_{PD}$ | Supply Current in Powerdown Mode<br>80C186EC25<br>80C186EC20<br>80C186EC13 | | <br>100<br>100<br>100 | <br>μA<br>μA<br>μA | <br>(Notes 5, 7)<br>(Note 5)<br>(Note 5) |
| $C_{IN}$ | Input Pin Capacitance | 0 | 15 | pF | $T_F$ = 1 MHz |
| $C_{OUT}$ | Output Pin Capacitance | 0 | 15 | pF | $T_F$ = 1 MHz (Note 6) |

**NOTES:**
1. These pins have an internal pull-up device that is active while $\overline{\text{RESIN}}$ is low and ONCE Mode is not active. Sourcing more current than specified (on any of these pins) may invoke a factory test mode.
2. Tested by outputs being floated by invoking ONCE Mode or by asserting HOLD.
3. Measured with the device in RESET and at worst case frequency, $V_{CC}$, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to $V_{CC}$ or GND.
4. Measured with the device in HALT (IDLE Mode active) and at worst case frequency, $V_{CC}$, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to $V_{CC}$ or GND.
5. Measured with the device in HALT (Powerdown Mode active) and at worst case frequency, $V_{CC}$, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to $V_{CC}$ or GND.
6. Output Capacitance is the capacitive load of a floating output pin.
7. Operating conditions for 25 MHz is 0°C to +70°C, $V_{CC}$ = 5.0 ±10%.

## DC SPECIFICATIONS (80L186EC13/80L188EC13)

| Symbol | Parameter | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 2.7 | 5.5 | V | |
| $V_{IL}$ | Input Low Voltage | −0.5 | 0.3 $V_{CC}$ | V | |
| $V_{IH}$ | Input High Voltage | 0.7 $V_{CC}$ | $V_{CC}$ + 0.5 | V | |
| $V_{OL}$ | Output Low Voltage | | 0.45 | V | $I_{OL}$ = 3 mA (Min) |
| $V_{OH}$ | Output High Voltage | $V_{CC}$ − 0.5 | | V | $I_{OH}$ = −2 mA (Min) |
| $V_{HYR}$ | Input Hysteresis on $\overline{RESIN}$ | 0.5 | | V | |
| $I_{LI}$ | Input Leakage Current for Pins: AD15:0 (AD7:0, A15:8), READY, HOLD, $\overline{RESIN}$, CLKIN, $\overline{TEST}$/BUSY, NMI, INT7:0, T0IN, T1IN, P2.7–P2.0, P3.5–P3.0, DRQ3:0, PEREQ, $\overline{ERROR}$ | | ±15 | μA | $0 \leq V_{IN} \leq V_{CC}$ |
| $I_{LIU}$ | Input Leakage for Pins with Pullups Active During Reset: A19:16, $\overline{LOCK}$ | −0.275 | −5 | mA | $V_{IN}$ = 0.7 $V_{CC}$ (Note 1) |
| $I_{LO}$ | Output Leakage for Floated Output Pins | | ±15 | μA | $0.45 \leq V_{OUT} \leq V_{CC}$ (Note 2) |
| $I_{CC}$ | Supply Current Cold (in RESET) 80L186EC-13 | | 36 | mA | (Note 3) |
| $I_{ID}$ | Supply Current in Idle Mode 80L186EC-13 | | 24 | mA | (Note 4) |
| $I_{PD}$ | Supply Current in Powerdown Mode 80L186EC-13 | | 30 | μA | (Note 5) |
| $C_{IN}$ | Input Pin Capacitance | 0 | 15 | pF | $T_F$ = 1 MHz |
| $C_{OUT}$ | Output Pin Capacitance | 0 | 15 | pF | $T_F$ = 1 MHz (Note 6) |

**NOTES:**
1. These pins have an internal pull-up device that is active while $\overline{RESIN}$ is low and ONCE Mode is not active. Sourcing more current than specified (on any of these pins) may invoke a factory test mode.
2. Tested by outputs being floated by invoking ONCE Mode or by asserting HOLD.
3. Measured with the device in RESET and at worst case frequency, $V_{CC}$, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to $V_{CC}$ or GND.
4. Measured with the device in HALT (IDLE Mode active) and at worst case frequency, $V_{CC}$, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to $V_{CC}$ or GND.
5. Measured with the device in HALT (Powerdown Mode active) and at worst case frequency, $V_{CC}$, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to $V_{CC}$ or GND.
6. Output Capacitance is the capacitive load of a floating output pin.

## DC SPECIFICATIONS (80L186EC16/80L188EC16) (Operating Temperature 0°C to 70°C)

| Symbol | Parameter | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 3.0 | 5.5 | V | |
| $V_{IL}$ | Input Low Voltage | −0.5 | 0.3 $V_{CC}$ | V | |
| $V_{IH}$ | Input High Voltage | 0.7 $V_{CC}$ | $V_{CC}$ + 0.5 | V | |
| $V_{OL}$ | Output Low Voltage | | 0.45 | V | $I_{OL}$ = 3 mA (Min) |
| $V_{OH}$ | Output High Voltage | $V_{CC}$ − 0.5 | | V | $I_{OH}$ = −2 mA (Min) |
| $V_{HYR}$ | Input Hysteresis on $\overline{RESIN}$ | 0.5 | | V | |
| $I_{LI}$ | Input Leakage Current for Pins: AD15:0 (AD7:0, A15:8), READY, HOLD, $\overline{RESIN}$, CLKIN, $\overline{TEST}$/BUSY, NMI, INT7:0, T0IN, T1IN, P2.7–P2.0, P3.5–P3.0, DRQ3:0, PEREQ, $\overline{ERROR}$ | | ±15 | μA | $0 \leq V_{IN} \leq V_{CC}$ |
| $I_{LIU}$ | Input Leakage for Pins with Pullups Active During Reset: A19:16, $\overline{LOCK}$ | −0.275 | −5 | mA | $V_{IN}$ = 0.7 $V_{CC}$ (Note 1) |
| $I_{LO}$ | Output Leakage for Floated Output Pins | | ±15 | μA | $0.45 \leq V_{OUT} \leq V_{CC}$ (Note 2) |
| $I_{CC}$ | Supply Current Cold (in RESET) 80L186EC-16 | | 45 | mA | (Note 3) |
| $I_{ID}$ | Supply Current in Idle Mode 80L186EC-16 | | 35 | mA | (Note 4) |
| $I_{PD}$ | Supply Current in Powerdown Mode 80L186EC-16 | | 50 | μA | (Note 5) |
| $C_{IN}$ | Input Pin Capacitance | 0 | 15 | pF | $T_F$ = 1 MHz |
| $C_{OUT}$ | Output Pin Capacitance | 0 | 15 | pF | $T_F$ = 1 MHz (Note 6) |

**NOTES:**
1. These pins have an internal pull-up device that is active while $\overline{RESIN}$ is low and ONCE Mode is not active. Sourcing more current than specified (on any of these pins) may invoke a factory test mode.
2. Tested by outputs being floated by invoking ONCE Mode or by asserting HOLD.
3. Measured with the device in RESET and at worst case frequency, $V_{CC}$, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to $V_{CC}$ or GND.
4. Measured with the device in HALT (IDLE Mode active) and at worst case frequency, $V_{CC}$, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to $V_{CC}$ or GND.
5. Measured with the device in HALT (Powerdown Mode active) and at worst case frequency, $V_{CC}$, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to $V_{CC}$ or GND.
6. Output Capacitance is the capacitive load of a floating output pin.

## $I_{CC}$ versus Frequency and Voltage

The $I_{CC}$ consumed by the processor is composed of two components:

1. $I_{PD}$—The quiescent current that represents internal device leakage. Measured with all inputs at either $V_{CC}$ or ground and no clock applied.
2. $I_{CCS}$—The switching current used to charge and discharge internal parasitic capacitance when changing logic levels. $I_{CCS}$ is related to both the frequency of operation and the device supply voltage ($V_{CC}$). $I_{CCS}$ is given by the formula:

$$\text{Power} = V * I = V^2 * C_{DEV} * f$$
$$\therefore I_{CCS} = V * C_{DEV} * f$$

Where:

$V$ = Supply Voltage ($V_{CC}$)

$C_{DEV}$ = Device Capacitance

$f$ = Operating Frequency

Measuring $C_{PD}$ on a device like the 80C186EC would be difficult. Instead, $C_{PD}$ is calculated using the above formula with $I_{CC}$ values measured at known $V_{CC}$ and frequency. Using the $C_{PD}$ value, the user can calculate $I_{CC}$ at any voltage and frequency within the specified operating range.

**Example.** Calculate typical $I_{CC}$ at 14 MHz, 5.2V $V_{CC}$.

$$I_{CC} = I_{PD} + I_{CCS}$$
$$= 0.1\text{ mA} + 5.2V * 0.77 * 14\text{ MHz}$$
$$= 56.2\text{ mA}$$

## PDTMR Pin Delay Calculation

The PDTMR pin provides a delay between the assertion of NMI and the enabling of the internal clocks when exiting Powerdown Mode. A delay is required only when using the on chip oscillator to allow the crystal or resonator circuit to stabilize.

**NOTE:**
The PDTMR pin function does not apply when $\overline{\text{RESIN}}$ is asserted (i.e. a device reset while in Powerdown is similar to a cold reset and $\overline{\text{RESIN}}$ must remain active until after the oscillator has stabilized.

To calculate the value of capacitor to use to provide a desired delay, use the equation:

$$440 \times t = C_{PD}\ (5V, 25°C)$$

Where:

$t$ = desired delay in **seconds**
$C_{PD}$ = capacitive load on PDTMR in **microfarads**

**Example.** For a delay of 300 $\mu$s, a capacitor value of $C_{PD} = 440 \times (300 \times 10^{-6} = 0.132\ \mu$F is required. Round up to a standard (available) capacitor value.

**NOTE:**
The above equation applies to delay time longer than 10 $\mu$s and will compute the **TYPICAL** capacitance needed to achieve the desired delay. A delay variance of +50% to −25% can occur due to temperature, voltage, and device process extremes. In general, higher $V_{CC}$ and/or lower temperatures will decrease delay time, while lower $V_{CC}$ and/or higher temperature will increase delay time.

| Parameter | Typical | Max | Units | Notes |
|---|---|---|---|---|
| CPD | 0.77 | 1.37 | mA/V*MHz | 1, 2 |
| CPD (Idle Mode) | 0.55 | 0.96 | mA/V*MHz | 1, 2 |

**NOTES:**
1. Maximum $C_{PD}$ is measured at −40°C with all outputs loaded as specified in the AC test conditions and the device in reset (or Idle Mode). Due to tester limitations, CLKOUT and OSCOUT also have 50 pF loads that increase $I_{CC}$ by V*C*F.
2. Typical $C_{PD}$ is calculated at 25°C assuming no loads on CLKOUT or OSCOUT and the device in reset (or Idle Mode).

## AC SPECIFICATIONS

### AC Characteristics—80C186EC25

| Symbol | Parameter | 25 MHz | | Units | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| **INPUT CLOCK** | | | | | |
| $T_F$ | CLKIN Frequency | 0 | 50 | MHz | 1 |
| $T_C$ | CLKIN Period | 20 | ∞ | ns | 1 |
| $T_{CH}$ | CLKIN High Time | 8 | ∞ | ns | 1, 2 |
| $T_{CL}$ | CLKIN Low Time | 8 | ∞ | ns | 1, 2 |
| $T_{CR}$ | CLKIN Rise Time | 1 | 10 | ns | 1, 3 |
| $T_{CF}$ | CLKIN Fall Time | 1 | 10 | ns | 1, 3 |
| **OUTPUT CLOCK** | | | | | |
| $T_{CD}$ | CLKIN to CLKOUT Delay | 0 | 17 | ns | 1, 4 |
| T | CLKOUT Period | | $2*T_C$ | ns | 1 |
| $T_{PH}$ | CLKOUT High Time | (T/2) − 5 | (T/2) + 5 | ns | 1 |
| $T_{PL}$ | CLKOUT Low Time | (T/2) − 5 | (T/2) + 5 | ns | 1 |
| $T_{PR}$ | CLKOUT Rise Time | 1 | 6 | ns | 1, 5 |
| $T_{PF}$ | CLKOUT Fall Time | 1 | 6 | ns | 1, 5 |
| **OUTPUT DELAYS** | | | | | |
| $T_{CHOV1}$ | ALE, $\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{BHE}$ ($\overline{RFSH}$), $\overline{LOCK}$, A19:16 | 3 | 17 | ns | 1, 4, 6, 7 |
| $T_{CHOV2}$ | $\overline{GCS0:7}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{NCS}$, $\overline{RD}$, $\overline{WR}$ | 3 | 20 | ns | 1, 4, 6, 8 |
| $T_{CLOV1}$ | $\overline{BHE}$ ($\overline{RFSH}$), $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16 | 3 | 17 | ns | 1, 4, 6 |
| $T_{CLOV2}$ | $\overline{RD}$, $\overline{WR}$, $\overline{GCS7:0}$, $\overline{LCS}$, $\overline{UCS}$, AD15:0 (AD7:0, A15:8), $\overline{NCS}$, $\overline{INTA1:0}$, $\overline{S2:0}$ | 3 | 20 | ns | 1, 4, 6 |
| $T_{CHOF}$ | $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$ ($\overline{RFSH}$), DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16 | 0 | 20 | ns | 1 |
| $T_{CLOF}$ | $\overline{DEN}$, AD15:0 (AD7:0, A15:8) | 0 | 20 | ns | 1 |

## AC SPECIFICATIONS

### AC Characteristics—80C186EC25 (Continued)

| Symbol | Parameter | 25 MHz | | Units | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| **SYNCHRONOUS INPUTS** | | | | | |
| $T_{CHIS}$ | $\overline{TEST}$, NMI, INT4:0, BCLK1:0, T1:0IN, READY, $\overline{CTS1:0}$, P2.6, P2.7 | 10 | | ns | 1, 9 |
| $T_{CHIH}$ | $\overline{TEST}$, NMI, INT4:0, BCLK1:0, T1:0IN, READY, $\overline{CTS1:0}$ | 3 | | ns | 1, 9 |
| $T_{CLIS}$ | AD15:0 (AD7:0), READY | 10 | | ns | 1, 10 |
| $T_{CLIH}$ | READY, AD15:0 (AD7:0) | 3 | | ns | 1, 10 |
| $T_{CLIS}$ | HOLD, PEREQ, $\overline{ERROR}$ | 10 | | ns | 1, 9 |
| $T_{CLIH}$ | HOLD, PEREQ, $\overline{ERROR}$ | 3 | | ns | 1, 9 |

**NOTES:**
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measure at $V_{IH}$ for high time, $V_{IL}$ for low time.
3. Only required to guarantee $I_{CC}$. Maximum limits are bounded by $T_C$, $T_{CH}$ and $T_{CL}$.
4. Specified for a 50 pF load, see Figure 13 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 14 for rise and fall times outside 50 pF.
6. See Figure 14 for rise and fall times.
7. $T_{CHOV1}$ applies to $\overline{BHE}$ ($\overline{RFSH}$), $\overline{LOCK}$ and A19:16 only after a HOLD release.
8. $T_{CHOV2}$ applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper operation.

## AC SPECIFICATIONS

### AC Characteristics—80C186EC-20/80C186EC-13

| Symbol | Parameter | Min | Max | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| **INPUT CLOCK** | | **20 MHz** | | **13 MHz** | | | |
| TF | CLKIN Frequency | 0 | 40 | 0 | 26 | MHz | 1 |
| TC | CLKIN Period | 25 | ∞ | 38.5 | ∞ | ns | 1 |
| TCH | CLKIN High Time | 10 | ∞ | 12 | ∞ | ns | 1, 2 |
| TCL | CLKIN Low Time | 10 | ∞ | 12 | ∞ | ns | 1, 2 |
| TCR | CLKIN Rise Time | 1 | 10 | 1 | 10 | ns | 1, 3 |
| TCF | CLKIN Fall Time | 1 | 10 | 1 | 10 | ns | 1, 3 |
| **OUTPUT CLOCK** | | | | | | | |
| $T_{CD}$ | CLKIN to CLKOUT Delay | 0 | 17 | 0 | 23 | ns | 1, 4 |
| T | CLKOUT Period | | 2 * TC | | 2 * TC | ns | 1 |
| $T_{PH}$ | CLKOUT High Time | (T/2) − 5 | (T/2) + 5 | (T/2) − 5 | (T/2) + 5 | ns | 1 |
| $T_{PL}$ | CLKOUT Low Time | (T/2) − 5 | (T/2) + 5 | (T/2) − 5 | (T/2) + 5 | ns | 1 |
| $T_{PR}$ | CLKOUT Rise Time | 1 | 6 | 1 | 6 | ns | 1, 5 |
| $T_{PF}$ | CLKOUT Fall Time | 1 | 6 | 1 | 6 | ns | 1, 5 |
| **OUTPUT DELAYS** | | | | | | | |
| $T_{CHOV1}$ | ALE, $\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{BHE}$ ($\overline{RFSH}$), $\overline{LOCK}$, A19:16 | 3 | 20 | 3 | 25 | ns | 1, 4, 6, 7 |
| $T_{CHOV2}$ | $\overline{GCS7:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{RD}$, $\overline{WR}$, $\overline{NCS}$, $\overline{WDTOUT}$ | 3 | 23 | 3 | 30 | ns | 1, 4, 6, 8 |
| $T_{CLOV1}$ | $\overline{BHE}$ ($\overline{RFSH}$), $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT | 3 | 20 | 3 | 25 | ns | 1, 4, 6 |
| $T_{CLOV2}$ | $\overline{RD}$, $\overline{WR}$, $\overline{GSC7:0}$, $\overline{LCS}$, $\overline{UCS}$, AD15:0 (AD7:0, A15:8), $\overline{NCS}$, $\overline{INTA}$, $\overline{S2:0}$, A19:16 | 3 | 23 | 3 | 30 | ns | 1, 4, 6 |
| $T_{CHOF}$ | $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$ ($\overline{RFSH}$), DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16 | 0 | 25 | 0 | 30 | ns | 1 |
| $T_{CLOF}$ | $\overline{DEN}$, AD15:0 (AD7:0, A15:8) | 0 | 25 | 0 | 30 | ns | 1 |
| **INPUT REQUIREMENTS** | | | | | | | |
| $T_{CHIS}$ | $\overline{TEST}$, NMI, T1IN, T0IN, READY, $\overline{CTS1:0}$, BCLK1:0, P3.4, P3.5 | 10 | | 10 | | ns | 1, 9 |
| $T_{CHIH}$ | $\overline{TEST}$, NMI, T1IN, T0IN, READY, $\overline{CTS1:0}$, BCLK1:0, P3.4, P3.5 | 3 | | 3 | | ns | 1, 9 |
| $T_{CLIS}$ | AD15:0 (AD7:0), READY | 10 | | 10 | | ns | 1, 10 |
| $T_{CLIH}$ | AD15:0 (AD7:0), READY | 3 | | 3 | | ns | 1, 10 |
| $T_{CLIS}$ | HOLD, $\overline{RESIN}$, PEREQ, $\overline{ERROR}$, DRQ3:0 | 10 | | 10 | | ns | 1, 9 |
| $T_{CLIH}$ | HOLD, $\overline{RESIN}$, REREQ, $\overline{ERROR}$, DRQ3:0 | 3 | | 3 | | ns | 1, 9 |

**NOTES:**
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measure at $V_{IH}$ for high time, $V_{IL}$ for low time.
3. Only required to guarantee $I_{CC}$. Maximum limits are bounded by $T_C$, $T_{CH}$ and $T_{CL}$.
4. Specified for a 50 pF load, see Figure 14 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 15 for rise and fall times outside 50 pF.
6. See Figure 15 for rise and fall times.
7. $T_{CHOV1}$ applies to $\overline{BHE}$ ($\overline{RFSH}$), $\overline{LOCK}$ and A19:16 only after a HOLD release.
8. $T_{CHOV2}$ applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper operation.

## AC Characteristics—80L186EC13

| Symbol | Parameter | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| **INPUT CLOCK** | | **13 MHz** | | | |
| $T_F$ | CLKIN Frequency | 0 | 26 | MHz | 1 |
| $T_C$ | CLKIN Period | 38.5 | ∞ | ns | 1 |
| $T_{CH}$ | CLKIN High Time | 15 | ∞ | ns | 1, 2 |
| $T_{CL}$ | CLKIN Low Time | 15 | ∞ | ns | 1, 2 |
| $T_{CR}$ | CLKIN Rise Time | 1 | 10 | ns | 1, 3 |
| $T_{CF}$ | CLKIN Fall Time | 1 | 10 | ns | 1, 3 |
| **OUTPUT CLOCK** | | | | | |
| $T_{CD}$ | CLKIN to CLKOUT Delay | 0 | 20 | ns | 1, 4 |
| T | CLKOUT Period | | 2 * TC | ns | 1 |
| $T_{PH}$ | CLKOUT High Time | (T/2) − 5 | (T/2) + 5 | ns | 1 |
| $T_{PL}$ | CLKOUT Low Time | (T/2) − 5 | (T/2) + 5 | ns | 1 |
| $T_{PR}$ | CLKOUT Rise Time | 1 | 10 | ns | 1, 5 |
| $T_{PF}$ | CLKOUT Fall Time | 1 | 10 | ns | 1, 5 |
| **OUTPUT DELAYS** | | | | | |
| $T_{CHOV1}$ | $\overline{S2:0}$, DT/$\overline{R}$, $\overline{BHE}$, $\overline{LOCK}$ | 3 | 28 | ns | 1, 4, 6, 7 |
| $T_{CHOV2}$ | $\overline{LCS}$, $\overline{UCS}$, $\overline{DEN}$, A19:16, $\overline{RD}$, $\overline{WR}$, $\overline{NCS}$, $\overline{WDTOUT}$, ALE | 3 | 32 | ns | 1, 4, 6, 8 |
| $T_{CHOV3}$ | $\overline{GCS7:0}$ | 3 | 34 | ns | 1, 4, 6 |
| $T_{CLOV1}$ | $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT | 3 | 28 | ns | 1, 4, 6 |
| $T_{CLOV2}$ | $\overline{RD}$, $\overline{WR}$, AD15:0 (AD7:0, A15:8), $\overline{BHE}$ ($\overline{RFSH}$), $\overline{NCS}$, $\overline{INTA}$, $\overline{DEN}$ | 3 | 32 | ns | 1, 4, 6 |
| $T_{CLOV3}$ | $\overline{GSC7:0}$, $\overline{LCS}$, $\overline{UCS}$ | 3 | 34 | ns | 1, 4, 6 |
| $T_{CLOV4}$ | $\overline{S2:0}$, A19:16 | 3 | 37 | ns | 1, 4, 6 |
| $T_{CHOF}$ | $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$ ($\overline{RFSH}$), DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16 | 0 | 30 | ns | 1 |
| $T_{CLOF}$ | $\overline{DEN}$, AD15:0 (AD7:0, A15:8) | 0 | 35 | ns | 1 |
| **INPUT REQUIREMENTS** | | | | | |
| $T_{CHIS}$ | $\overline{TEST}$, NMI, T1IN, T0IN, READY, $\overline{CTS1:0}$, BCLK1:0, P3.4, P3.5 | 20 | | ns | 1, 9 |
| $T_{CHIH}$ | $\overline{TEST}$, NMI, T1IN, T0IN, READY, $\overline{CTS1:0}$, BCLK1:0, P3.4, P3.5 | 3 | | ns | 1, 9 |
| $T_{CLIS}$ | AD15:0 (AD7:0), READY | 20 | | ns | 1, 10 |
| $T_{CLIH}$ | AD15:0 (AD7:0), READY | 3 | | ns | 1, 10 |
| $T_{CLIS}$ | HOLD, $\overline{RESIN}$, PEREQ, $\overline{ERROR}$, DRQ3:0 | 20 | | ns | 1, 9 |
| $T_{CLIH}$ | HOLD, $\overline{RESIN}$, REREQ, $\overline{ERROR}$, DRQ3:0 | 3 | | ns | 1, 9 |

**NOTES:**
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measure at $V_{IH}$ for high time, $V_{IL}$ for low time.
3. Only required to guarantee $I_{CC}$. Maximum limits are bounded by $T_C$, $T_{CH}$ and $T_{CL}$.
4. Specified for a 50 pF load, see Figure 14 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 15 for rise and fall times outside 50 pF.

## AC Characteristics—80L186EC13 (Continued)

**NOTES:**
6. See Figure 15 for rise and fall times.
7. $T_{CHOV1}$ applies to $\overline{BHE}$ ($\overline{RFSH}$), $\overline{LOCK}$ and A19:16 only after a HOLD release.
8. $T_{CHOV2}$ applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper operation.

## AC Characteristics—80L186EC16 (Operating Temperature 0°C to 70°C)

| Symbol | Parameter | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| **INPUT CLOCK** | | **16 MHz** | | | |
| $T_F$ | CLKIN Frequency | 0 | 32 | MHz | 1 |
| $T_C$ | CLKIN Period | 31.25 | ∞ | ns | 1 |
| $T_{CH}$ | CLKIN High Time | 13 | ∞ | ns | 1, 2 |
| $T_{CL}$ | CLKIN Low Time | 13 | ∞ | ns | 1, 2 |
| $T_{CR}$ | CLKIN Rise Time | 1 | 10 | ns | 1, 3 |
| $T_{CF}$ | CLKIN Fall Time | 1 | 10 | ns | 1, 3 |
| **OUTPUT CLOCK** | | | | | |
| $T_{CD}$ | CLKIN to CLKOUT Delay | 0 | 20 | ns | 1, 4 |
| T | CLKOUT Period | | 2 * TC | ns | 1 |
| $T_{PH}$ | CLKOUT High Time | (T/2) − 5 | (T/2) + 5 | ns | 1 |
| $T_{PL}$ | CLKOUT Low Time | (T/2) − 5 | (T/2) + 5 | ns | 1 |
| $T_{PR}$ | CLKOUT Rise Time | 1 | 9 | ns | 1, 5 |
| $T_{PF}$ | CLKOUT Fall Time | 1 | 9 | ns | 1, 5 |
| **OUTPUT DELAYS** | | | | | |
| $T_{CHOV1}$ | $\overline{S2:0}$, DT/$\overline{R}$, $\overline{BHE}$, $\overline{LOCK}$ | 3 | 25 | ns | 1, 4, 6, 7 |
| $T_{CHOV2}$ | $\overline{LCS}$, $\overline{UCS}$, $\overline{DEN}$, A19:16, $\overline{RD}$, $\overline{WR}$, $\overline{NCS}$, $\overline{WDTOUT}$, $\overline{ALE}$ | 3 | 30 | ns | 1, 4, 6, 8 |
| $T_{CHOV3}$ | $\overline{GCS7:0}$ | 3 | 32 | ns | 1, 4, 6 |
| $T_{CLOV1}$ | $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT | 3 | 25 | ns | 1, 4, 6 |
| $T_{CLOV2}$ | $\overline{RD}$, $\overline{WR}$, AD15:0 (AD7:0, A15:8), $\overline{BHE}$ ($\overline{RFSH}$), $\overline{NCS}$, $\overline{INTA}$, $\overline{DEN}$ | 3 | 30 | ns | 1, 4, 6 |
| $T_{CLOV3}$ | $\overline{GSC7:0}$, $\overline{LCS}$, $\overline{UCS}$ | 3 | 32 | ns | 1, 4, 6 |
| $T_{CLOV4}$ | $\overline{S2:0}$, A19:16 | 3 | 34 | ns | 1, 4, 6 |
| $T_{CHOF}$ | $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$ ($\overline{RFSH}$), DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16 | 0 | 28 | ns | 1 |
| $T_{CLOF}$ | $\overline{DEN}$, AD15:0 (AD7:0, A15:8) | 0 | 32 | ns | 1 |
| **INPUT REQUIREMENTS** | | | | | |
| $T_{CHIS}$ | $\overline{TEST}$, NMI, T1IN, T0IN, READY, $\overline{CTS1:0}$, BCLK1:0, P3.4, P3.5 | 15 | | ns | 1, 9 |
| $T_{CHIH}$ | $\overline{TEST}$, NMI, T1IN, T0IN, READY, $\overline{CTS1:0}$, BCLK1:0, P3.4, P3.5 | 3 | | ns | 1, 9 |
| $T_{CLIS}$ | AD15:0 (AD7:0), READY | 15 | | ns | 1, 10 |
| $T_{CLIH}$ | AD15:0 (AD7:0), READY | 3 | | ns | 1, 10 |
| $T_{CLIS}$ | HOLD, $\overline{RESIN}$, PEREQ, $\overline{ERROR}$, DRQ3:0 | 15 | | ns | 1, 9 |
| $T_{CLIH}$ | HOLD, $\overline{RESIN}$, PEREQ, $\overline{ERROR}$, DRQ3:0 | 3 | | ns | 1, 9 |

## AC Characteristics—80L186EC16 (Continued)

**NOTES:**
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measure at $V_{IH}$ for high time, $V_{IL}$ for low time.
3. Only required to guarantee $I_{CC}$. Maximum limits are bounded by $T_C$, $T_{CH}$ and $T_{CL}$.
4. Specified for a 50 pF load, see Figure 14 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 15 for rise and fall times outside 50 pF.
6. See Figure 15 for rise and fall times.
7. $T_{CHOV1}$ applies to $\overline{BHE}$ ($\overline{RFSH}$), $\overline{LOCK}$ and A19:16 only after a HOLD release.
8. $T_{CHOV2}$ applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper operation.

## Relative Timings (80C186EC-25/20/13, 80L186EC-16/13)

| Symbol | Parameter | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| **RELATIVE TIMINGS** | | | | | |
| $T_{LHLL}$ | ALE Active Pulse Width | T − 15 | | ns | |
| $T_{AVLL}$ | AD Valid Setup before ALE Falls | ½T − 10 | | ns | |
| $T_{PLLL}$ | Chip Select Valid before ALE Falls | ½T − 10 | | ns | 1 |
| $T_{LLAX}$ | AD Hold after ALE Falls | ½T − 10 | | ns | |
| $T_{LLWL}$ | ALE Falling to $\overline{WR}$ Falling | ½T − 15 | | ns | 1 |
| $T_{LLRL}$ | ALE Falling to $\overline{RD}$ Falling | ½T − 15 | | ns | 1 |
| $T_{WHLH}$ | $\overline{WR}$ Rising to Next ALE Rising | ½T − 10 | | ns | 1 |
| $T_{AFRL}$ | AD Float to $\overline{RD}$ Falling | 0 | | ns | |
| $T_{RLRH}$ | $\overline{RD}$ Active Pulse Width | 2T − 5 | | ns | 2 |
| $T_{WLWH}$ | $\overline{WR}$ Active Pulse Width | 2T − 5 | | ns | 2 |
| $T_{RHAX}$ | $\overline{RD}$ Rising to Next Address Active | T − 15 | | ns | |
| $T_{WHDX}$ | Output Data Hold after $\overline{WR}$ Rising | T − 15 | | ns | |
| $T_{WHPH}$ | $\overline{WR}$ Rise to Chip Select Rise | ½T − 10 | | ns | 1 |
| $T_{RHPH}$ | $\overline{RD}$ Rise to Chip Select Rise | ½T − 10 | | ns | 1 |
| $T_{PHPL}$ | Chip Select Inactive to Next Chip Select Active | ½T − 10 | | ns | 1 |
| $T_{OVRH}$ | $\overline{ONCE}$ Active Setup to $\overline{RESIN}$ Rising | T | | ns | |
| $T_{RHOX}$ | $\overline{ONCE}$ Hold after $\overline{RESIN}$ Rise | T | | ns | |
| $T_{IHIL}$ | $\overline{INTA}$ High to Next $\overline{INTA}$ Low during INTA Cycle | 4T − 5 | | ns | 4 |
| $T_{ILIH}$ | $\overline{INTA}$ Active Pulse Width | 2T − 5 | | ns | 2, 4 |
| $T_{CVIL}$ | CAS2:0 Setup before 2nd $\overline{INTA}$ Pulse Low | 8T | | ns | 2, 4 |
| $T_{ILCX}$ | CAS2:0 Hold after 2nd $\overline{INTA}$ Pulse Low | 4T | | ns | 2, 4 |
| $T_{IRES}$ | Interrupt Resolution Time | | 150 | ns | 3 |
| $T_{IRLH}$ | IR Low Time to Reset Edge Detector | 50 | | ns | |
| $T_{IRHIF}$ | IR Hold Time after 1st $\overline{INTA}$ Falling | 25 | | ns | 4, 5 |

## Relative Timings (80C186EC-25/20/13, 80L186EC-16/13)

**NOTES:**
1. Assumes equal loading on both pins.
2. Can be extended using wait states.
3. Interrupt resolution time is the delay between an unmasked interrupt request going active and the interrupt output of the 8259A module going active. This is not directly measureable by the user. For interrupt pin INT7 the delay from an active signal to an active input to the CPU would actually be twice the $T_{IRES}$ value since the signal must pass through two 8259A modules.
4. See INTA Cycle Waveforms for definition.
5. To guarantee interrupt is not spurious.

## Serial Port Mode 0 Timings (80C186EC-25/20/13, 80L186EC-16/13)

| Symbol | Parameter | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| **RELATIVE TIMINGS** | | | | | |
| $T_{XLXL}$ | TXD Clock Period | T (n + 1) | | ns | 1, 2 |
| $T_{XLXH}$ | TXD Clock Low to Clock High (N > 1) | 2T − 35 | 2T + 35 | ns | 1 |
| $T_{XLXH}$ | TXD Clock Low to Clock High (N = 1) | T − 35 | T + 35 | ns | 1 |
| $T_{XHXL}$ | TXD Clock High to Clock Low (N > 1) | (n − 1) T − 35 | (n − 1) T + 35 | ns | 1, 2 |
| $T_{XHXL}$ | TXD Clock High to Clock Low (N = 1) | T − 35 | T + 35 | ns | 1 |
| $T_{QVXH}$ | RXD Output Data Setup to TXD Clock High (N > 1) | (n − 1)T − 35 | | ns | 1, 2 |
| $T_{QVXH}$ | RXD Output Data Setup to TXD Clock High (N = 1) | T − 35 | | ns | 1 |
| $T_{XHQX}$ | RXD Output Data Hold after TXD Clock High (N > 1) | 2T − 35 | | ns | 1 |
| $T_{XHQX}$ | RXD Output Data Hold after TXD Clock High (N = 1) | T − 35 | | ns | 1 |
| $T_{XHQZ}$ | RXD Output Data Float after Last TXD Clock High | | T + 20 | ns | 1 |
| $T_{DVXH}$ | RXD Input Data Setup to TXD Clock High | T + 20 | | ns | 1 |
| $T_{XHDX}$ | RXD Input Data Setup after TXD Clock High | 0 | | ns | 1 |

**NOTES:**
1. See Figure 13 for Waveforms.
2. n is the value in the BxCMP register ignoring the ICLK bit.

## AC TEST CONDITIONS

The AC specifications are tested with the 50 pF load shown in Figure 7. See the Derating Curves section to see how timings vary with load capacitance.

Specifications are measured at the $V_{CC}/2$ crossing point, unless otherwise specified. See AC Timing Waveforms for AC specification definitions, test pins and illustrations.

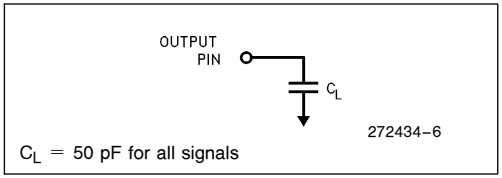



**Figure 7. AC Test Load**

## AC TIMING WAVEFORMS

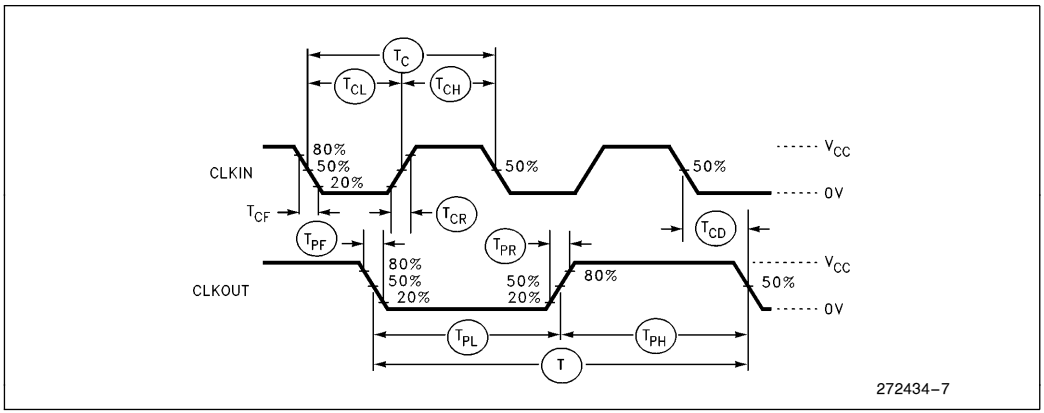



**Figure 8. Input and Output Clock Waveforms**

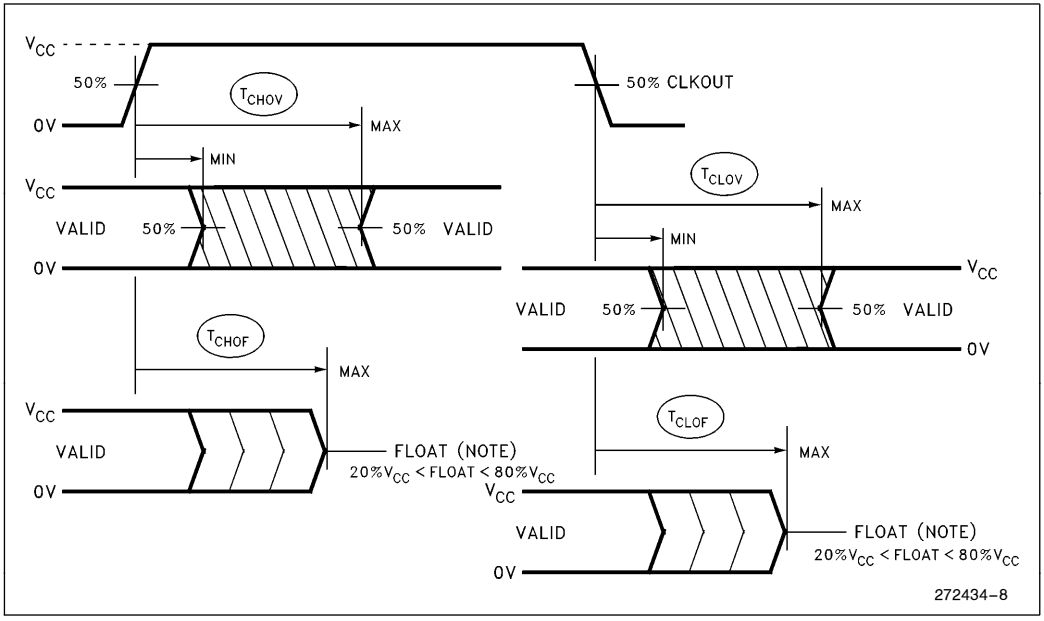



**Figure 9. Output Delay and Float Waveforms**

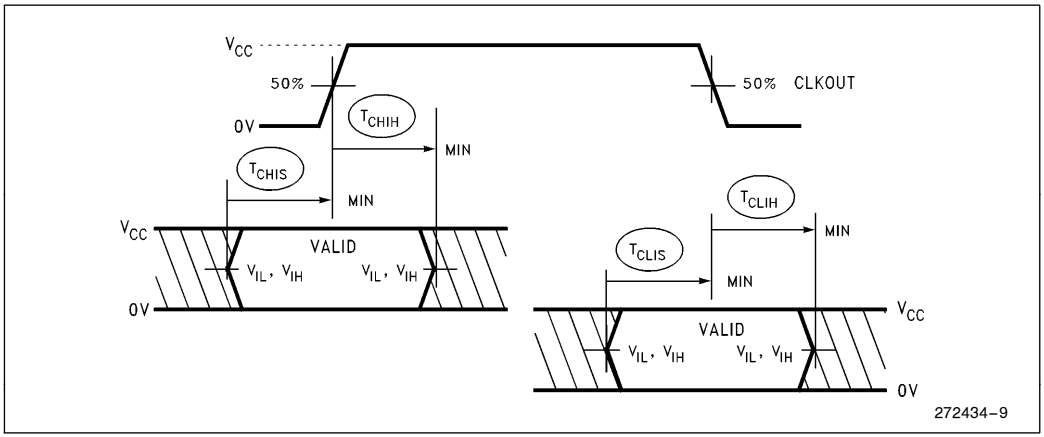



**Figure 10. Input Setup and Hold**

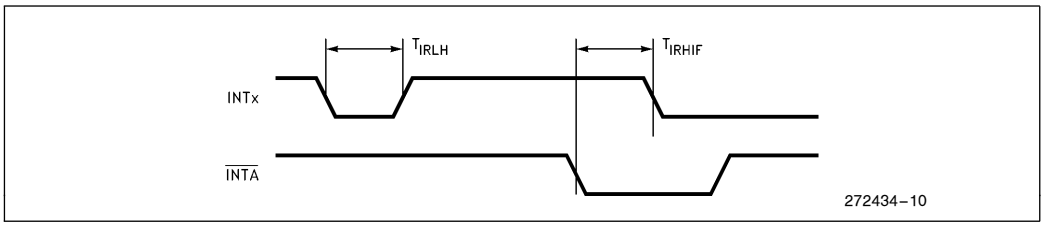



**Figure 11. Relative Interrupt Signal Timings**

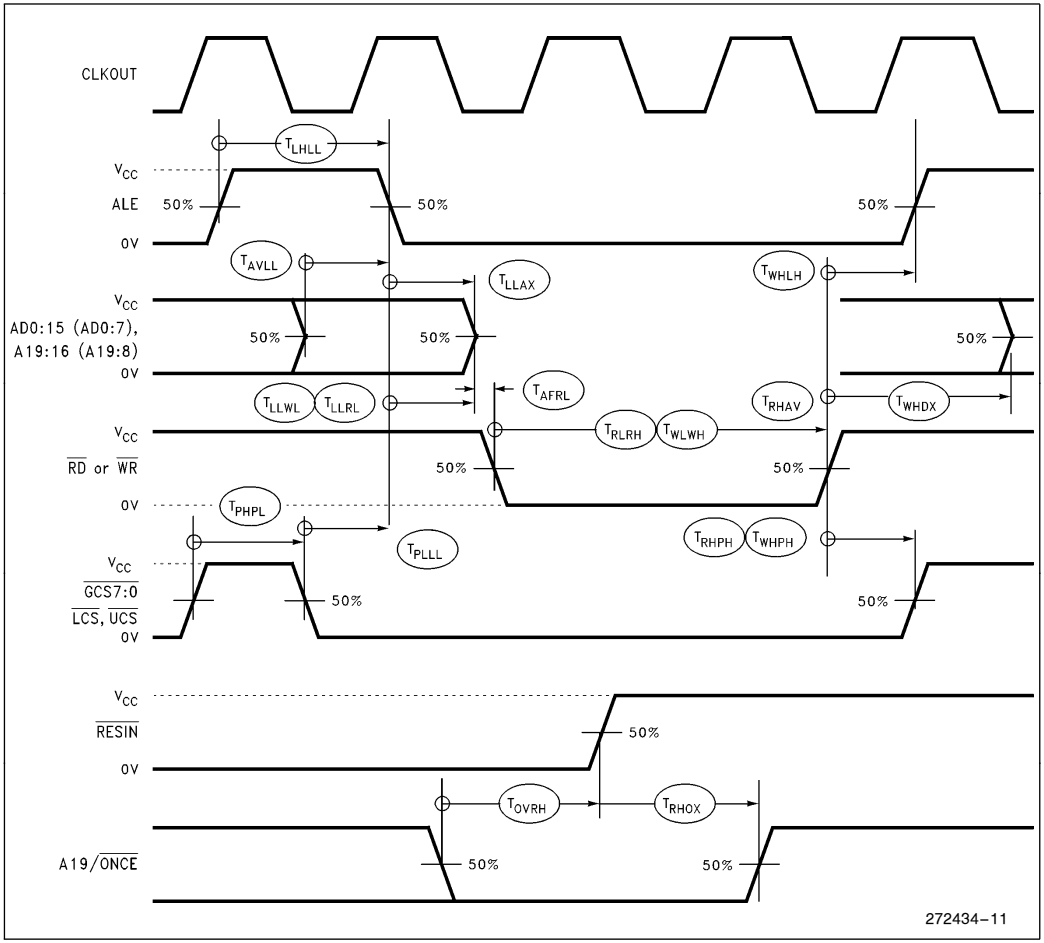



**Figure 12. Relative Signal Waveform**

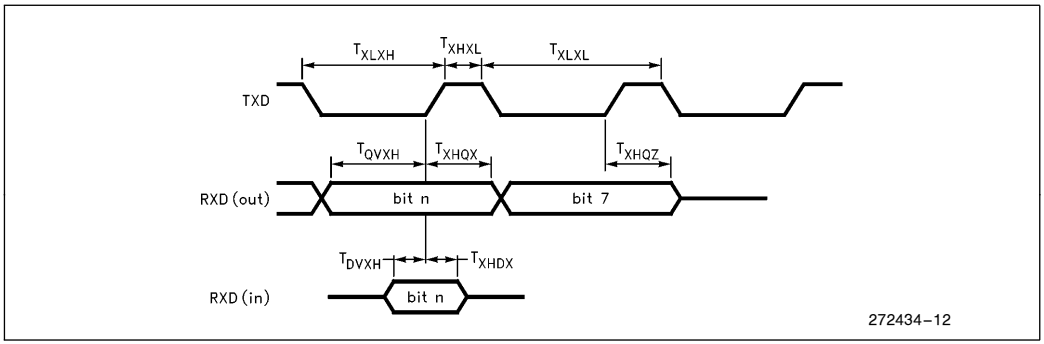



**Figure 13. Serial Port Mode 0 Waveform**

## DERATING CURVES

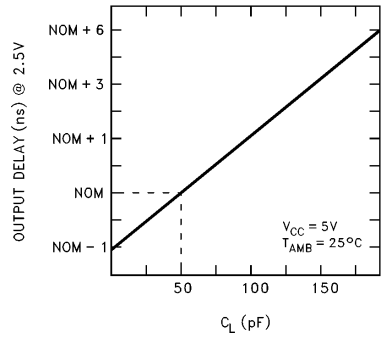



**Figure 14. Typical Output Delay Variations versus Load Capacitance**

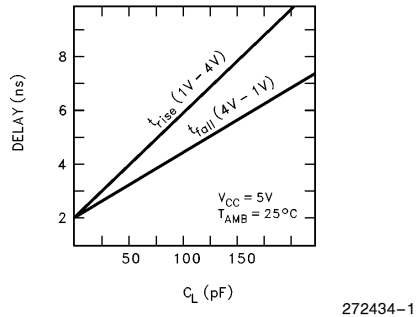



**Figure 15. Typical Rise and Fall Variations versus Load Capacitance**

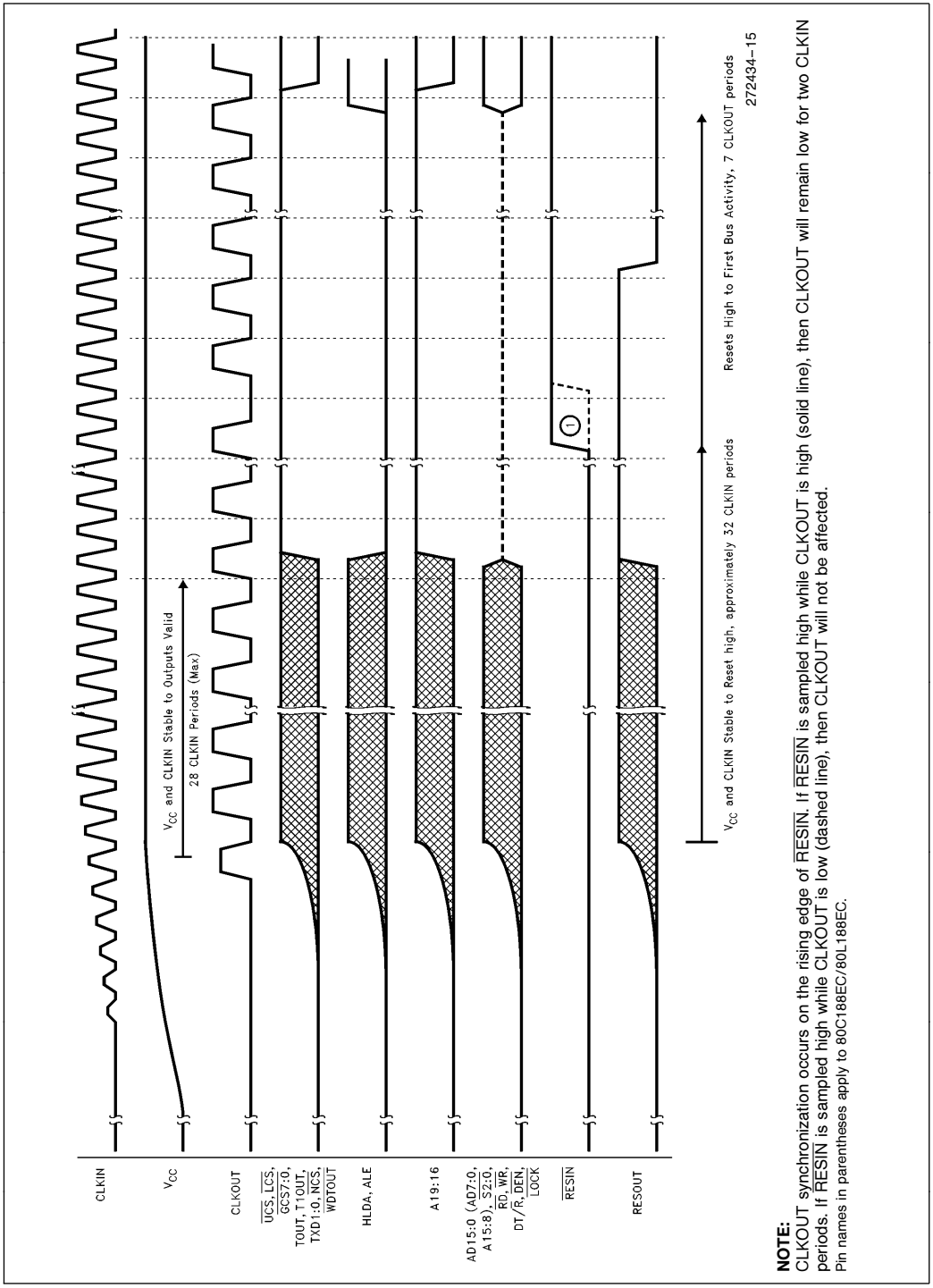
## RESET

The processor will perform a reset operation any time the $\overline{\text{RESIN}}$ pin is active. The $\overline{\text{RESIN}}$ pin is synchronized before it is presented internally, which means that the clock must be operating before a reset can take effect. From a power-on state, $\overline{\text{RESIN}}$ must be held active (low) in order to guarantee correct initialization of the processor. **Failure to provide $\overline{\text{RESIN}}$ while the device is powering up will result in unspecified operation of the device.**

Figure 16 shows the correct reset sequence when first applying power to the processor. An external clock connected to CLKIN must not exceed the $V_{CC}$ threshold being applied to the processor. This is normally not a problem if the clock driver is supplied with the same $V_{CC}$ that supplies the processor. When attaching a crystal to the device, $\overline{\text{RESIN}}$ must remain active until both $V_{CC}$ and CLKOUT are stable (the length of time is application specific and depends on the startup characteristics of the crystal circuit). The $\overline{\text{RESIN}}$ pin is designed to operate correctly using a RC reset circuit, but the designer must ensure that the ramp time for $V_{CC}$ is not so long that $\overline{\text{RESIN}}$ is never sampled at a logic low level when $V_{CC}$ reaches minimum operating conditions.

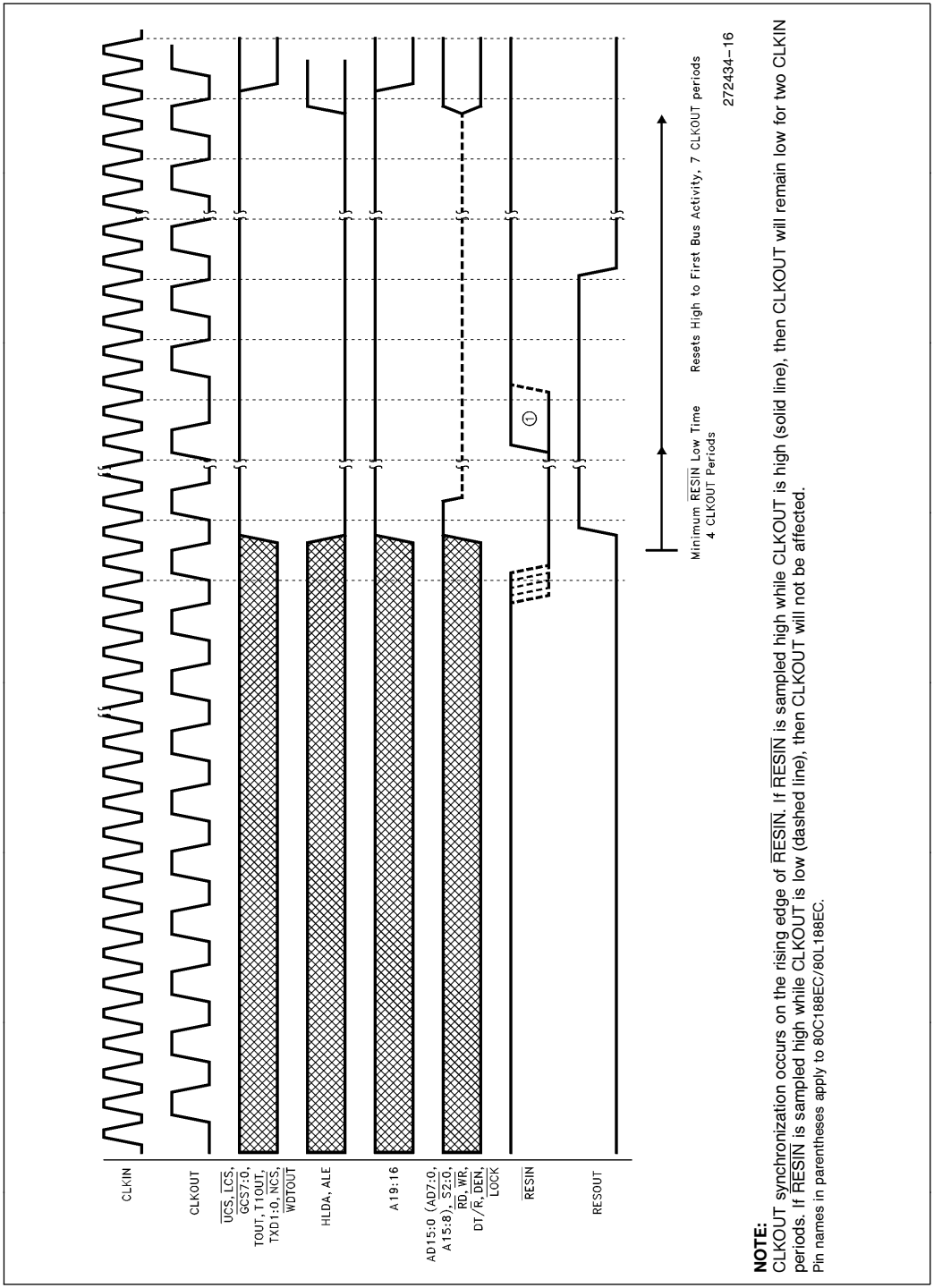
Figure 17 shows the timing sequence when $\overline{\text{RESIN}}$ is applied after $V_{CC}$ is stable and the device has been operating. Note that a reset will terminate all activity and return the processor to a known operating state. Any bus operation that is in progress at the time $\overline{\text{RESIN}}$ is asserted will terminate immediately (note that most control signals will be driven to their inactive state first before floating).

While $\overline{\text{RESIN}}$ is active, bus signals $\overline{\text{LOCK}}$, A19/S16/$\overline{\text{ONCE}}$ and A18:16 are configured as inputs and weakly held high by internal pullup transistors. Only A19/$\overline{\text{ONCE}}$ can be overdriven to a low and is used to enable the ONCE Mode. Forcing $\overline{\text{LOCK}}$ or A18:16 low at any time while $\overline{\text{RESIN}}$ is low is prohibited and will cause unspecified device operation.




**NOTE:**
CLKOUT synchronization occurs on the rising edge of $\overline{RESIN}$. If $\overline{RESIN}$ is sampled high while CLKOUT is high (solid line), then CLKOUT will remain low for two CLKIN periods. If $\overline{RESIN}$ is sampled high while CLKOUT is low (dashed line), then CLKOUT will not be affected.
Pin names in parentheses apply to 80C188EC/80L188EC.

**Figure 16. Cold RESET Waveforms**

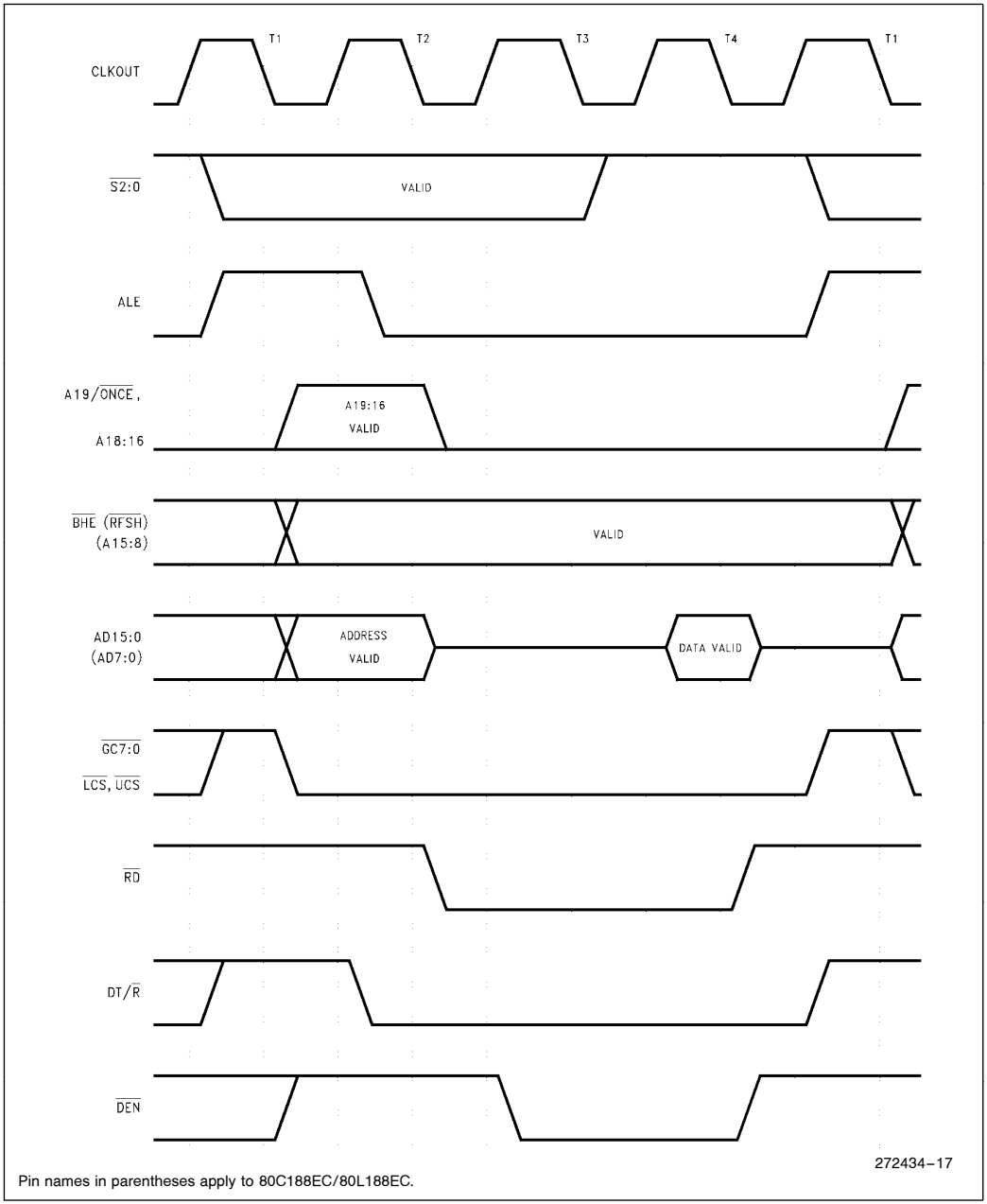



**NOTE:**
CLKOUT synchronization occurs on the rising edge of RESIN. If RESIN is sampled high while CLKOUT is high (solid line), then CLKOUT will remain low for two CLKIN periods. If RESIN is sampled high while CLKOUT is low (dashed line), then CLKOUT will not be affected.
Pin names in parentheses apply to 80C188EC/80L188EC.

**Figure 17. Warm RESET Waveforms**

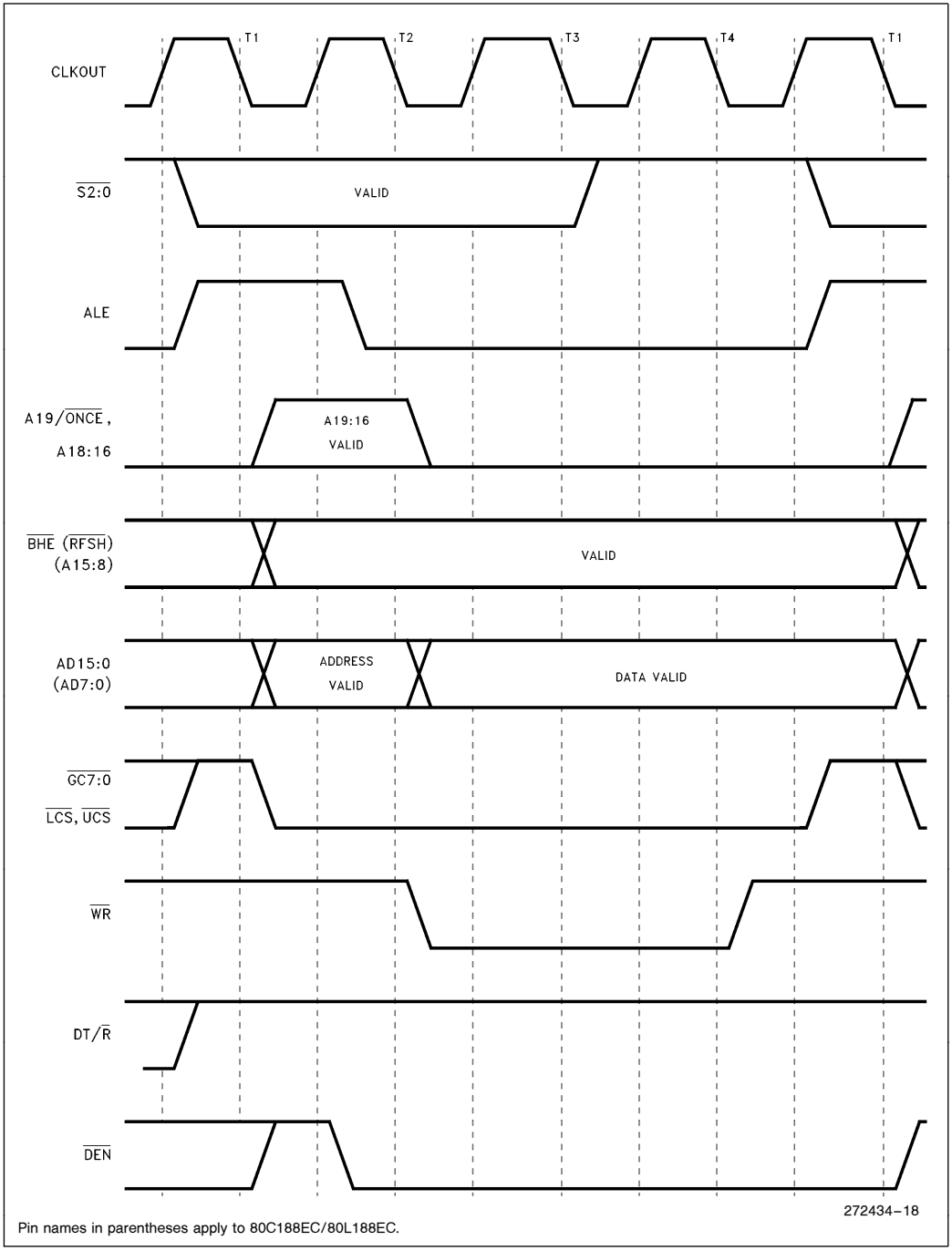
## BUS CYCLE WAVEFORMS

Figures 18 through 24 present the various bus cycles that are generated by the processor. What is shown in the figure is the relationship of the various bus signals to CLKOUT. These figures along with the information present in AC Specifications allow the user to determine all the critical timing analysis needed for a given application.



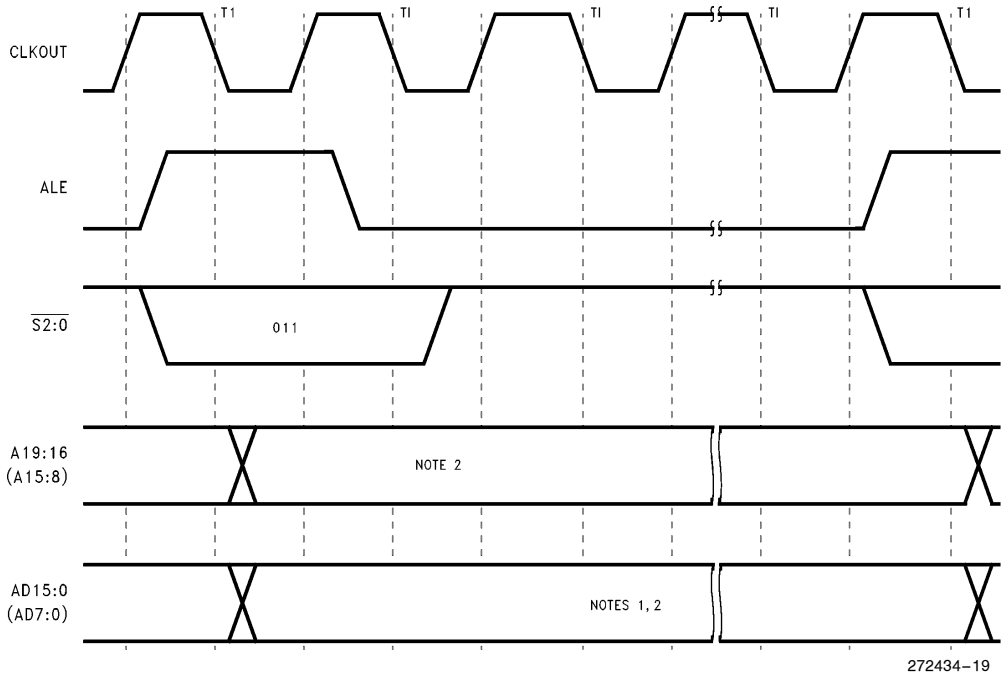

Pin names in parentheses apply to 80C188EC/80L188EC.

**Figure 18. Memory Read, I/O Read, Instruction Fetch and Refresh Waveforms**




Pin names in parentheses apply to 80C188EC/80L188EC.

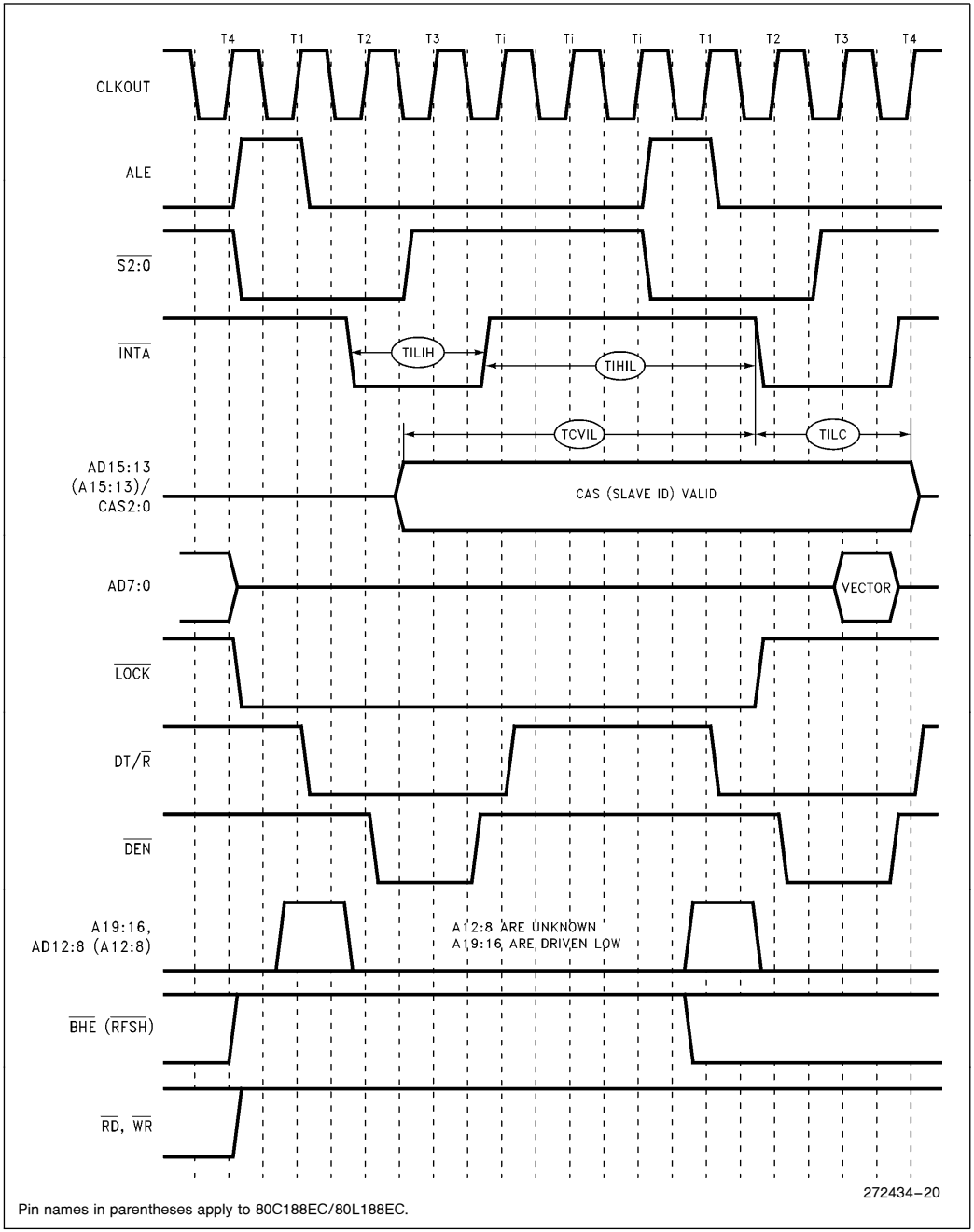
**Figure 19. Memory Write and I/O Write Cycle Waveforms**




**NOTES:**
1. Address information is invalid. If previous bus cycle was a read, then the AD15:0 (AD7:0) lines will float during T1. Otherwise, the AD15:0 (AD7:0) lines will continue to drive during T1 (data is invalid). All other control lines are in their inactive state.
2. All address lines drive zeros while in Powerdown or Idle Mode.

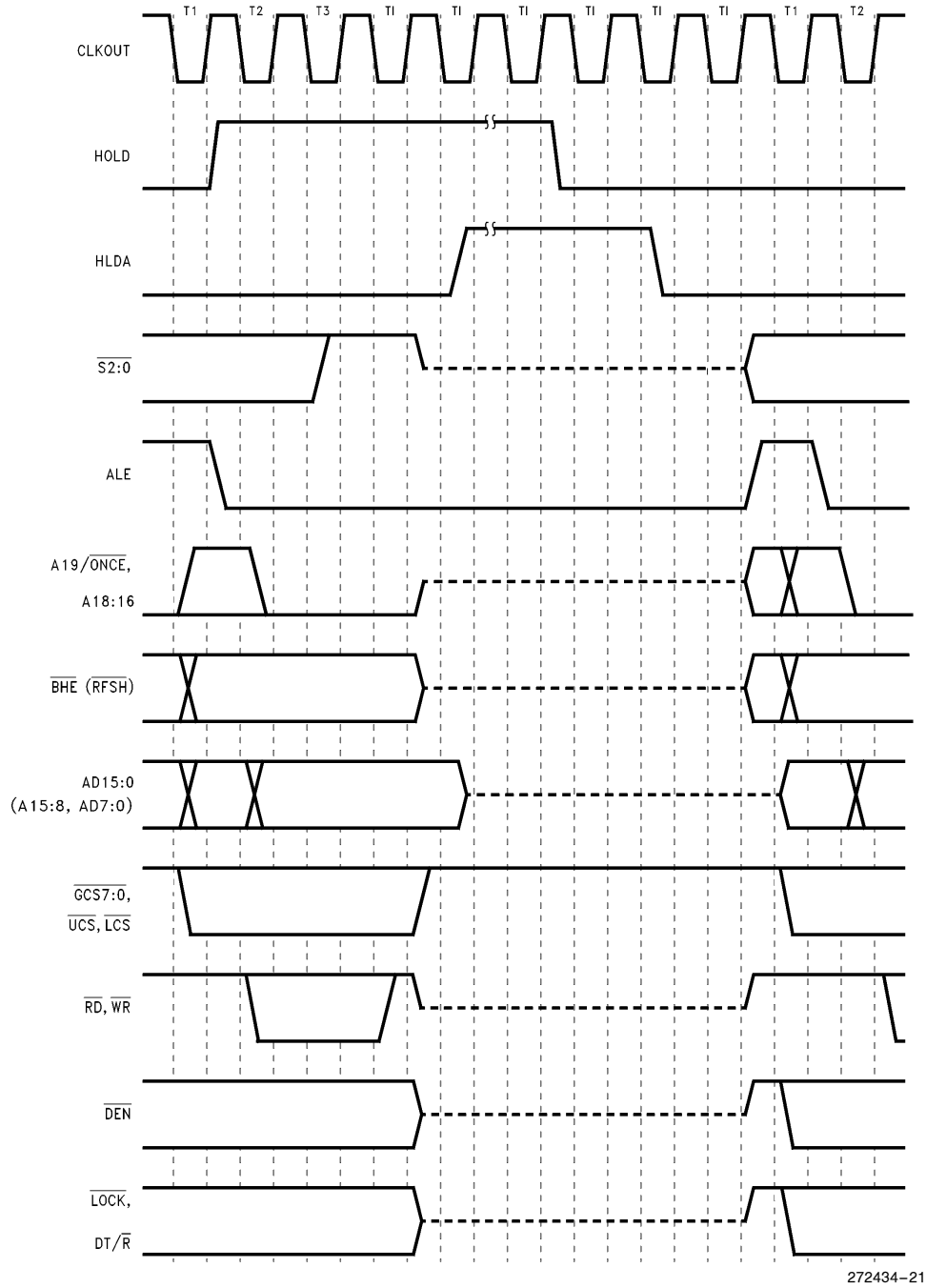
Pin names in parentheses apply to 80C188EC/80L188EC.

**Figure 20. Halt Cycle Waveforms**



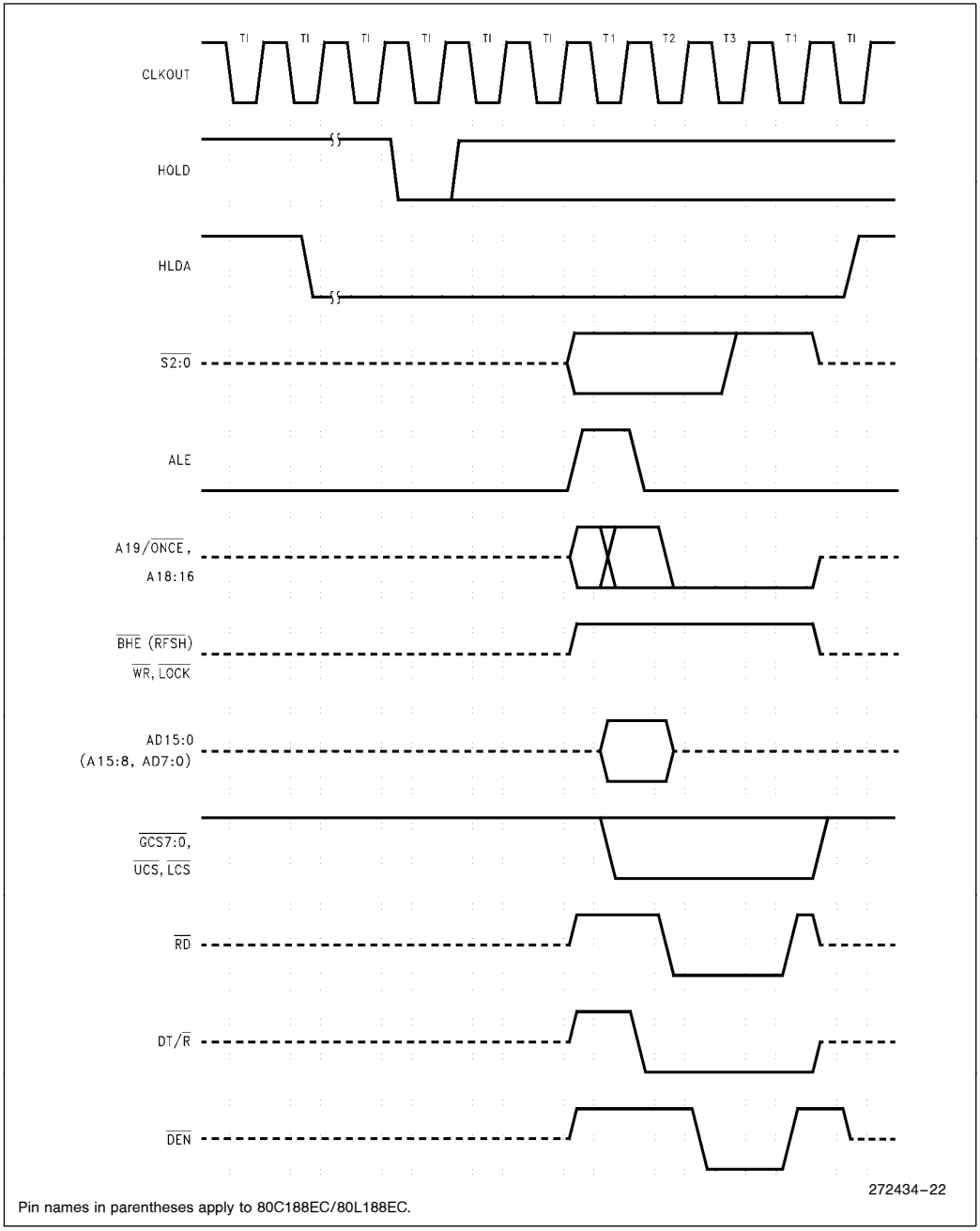

Pin names in parentheses apply to 80C188EC/80L188EC.

**Figure 21. Interrupt Acknowledge Cycle Waveforms**



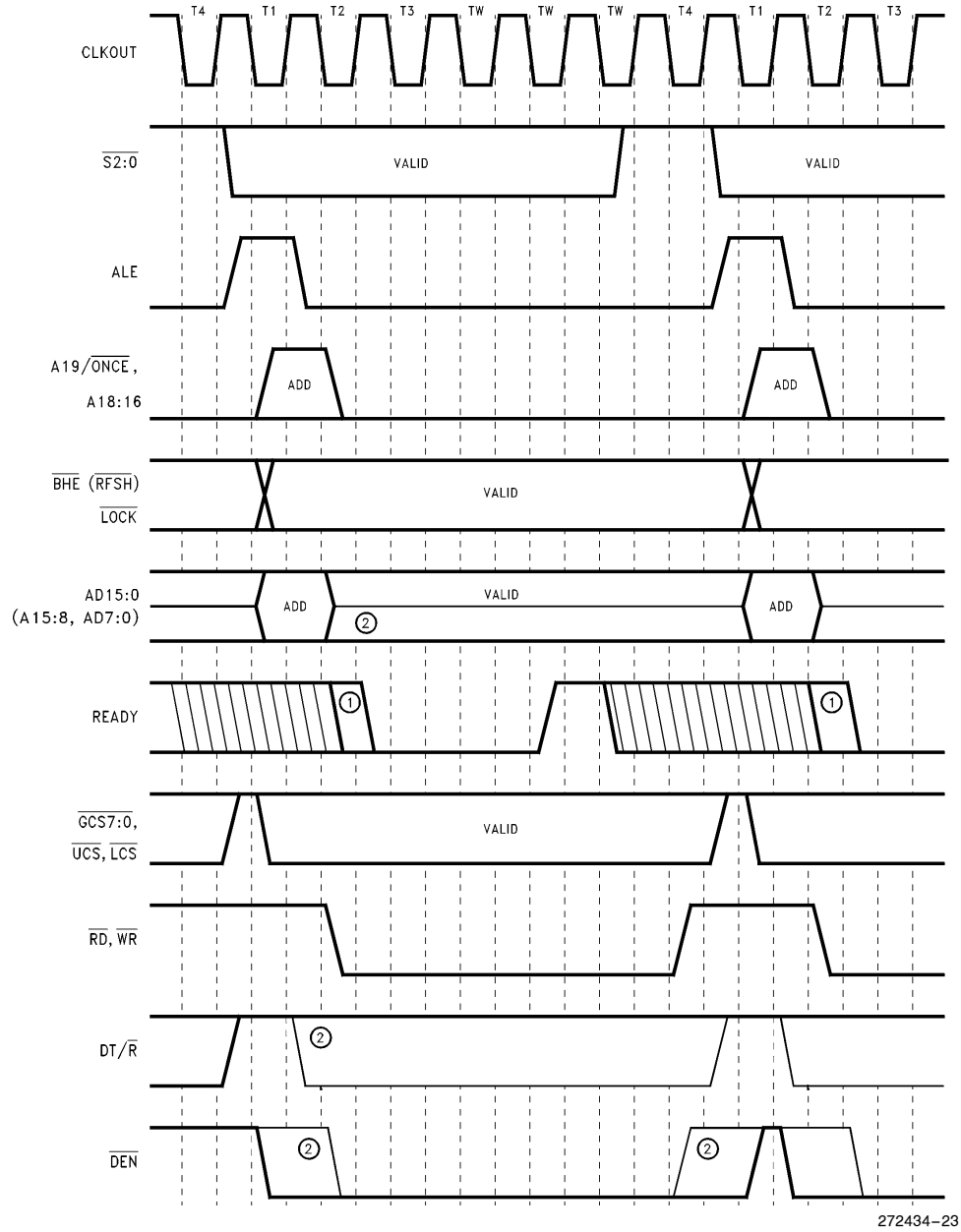

Pin names in parentheses apply to 80C188EC/80L188EC.

**Figure 22. HOLD/HLDA Cycle Waveforms**




Pin names in parentheses apply to 80C188EC/80L188EC.

**Figure 23. Refresh during HLDA Waveforms**




**NOTES:**
1. READY must be low by either edge to cause a wait state.
2. Lighter lines indicate READ cycles, darker lines indicate WRITE cycles.

Pin names in parentheses apply to 80C188EC/80L188EC.

**Figure 24. READY Cycle Waveforms**

## 80C186EC/80C188EC EXECUTION TIMINGS

A determination of program execution timing must consider the bus cycles necessary to prefetch instructions as well as the number of execution unit cycles necessary to execute instructions. The following instruction timings represent the **minimum** execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

- The opcode, along with any data or displacement required for execution of a particular instruction, has been prefetched and resides in the queue at the time it is needed.
- No wait states or bus HOLDs occur.
- All word-data is located on even-address boundaries (80C186EC only).

All jumps and calls include the time required to fetch the opcode of the next instruction at the destination address.

All instructions which involve memory accesses can require one or two additional clocks above the minimum timings shown due to the asynchronous handshake between the bus interface unit (BIU) and execution unit.

With a 16-bit BIU, the 80C186EC has sufficient bus performance to ensure that an adequate number of prefetched bytes will reside in the queue (6 bytes) most of the time. Therefore, actual program execution time will not be substantially greater than that derived from adding the instruction timings shown.

The 80C188EC 8-bit BIU is limited in its performance relative to the execution unit. A sufficient number of prefetched bytes may not reside in the prefetch queue (4 bytes) much of the time. Therefore, actual program execution time will be substantially greater than that derived from adding the instruction timings shown.

## INSTRUCTION SET SUMMARY

| Function | Format | | | | 80C186EC Clock Cycles | 80C188EC Clock Cycles | Comments |
|---|---|---|---|---|---|---|---|
| **DATA TRANSFER** | | | | | | | |
| **MOV = Move:** | | | | | | | |
| Register to Register/Memory | 1000100w | mod reg r/m | | | 2/12 | 2/12* | |
| Register/memory to register | 1000101w | mod reg r/m | | | 2/9 | 2/9* | |
| Immediate to register/memory | 1100011w | mod 000 r/m | data | data if w=1 | 12/13 | 12/13 | 8/16-bit |
| Immediate to register | 1011w reg | data | data if w=1 | | 3/4 | 3/4 | 8/16-bit |
| Memory to accumulator | 1010000w | addr-low | addr-high | | 8 | 8* | |
| Accumulator to memory | 1010001w | addr-low | addr-high | | 9 | 9* | |
| Register/memory to segment register | 10001110 | mod 0 reg r/m | | | 2/9 | 2/13 | |
| Segment register to register/memory | 10001100 | mod 0 reg r/m | | | 2/11 | 2/15 | |
| **PUSH = Push:** | | | | | | | |
| Memory | 11111111 | mod 110 r/m | | | 16 | 20 | |
| Register | 01010 reg | | | | 10 | 14 | |
| Segment register | 000reg110 | | | | 9 | 13 | |
| Immediate | 011010s0 | data | data if s=0 | | 10 | 14 | |
| **PUSHA = Push All** | 01100000 | | | | 36 | 68 | |
| **POP = Pop:** | | | | | | | |
| Memory | 10001111 | mod 000 r/m | | | 20 | 24 | |
| Register | 01011 reg | | | | 10 | 14 | |
| Segment register | 000reg111 | (reg≠01) | | | 8 | 12 | |
| POPA = Pop All | 01100001 | | | | 51 | 83 | |
| **XCHG = Exchange:** | | | | | | | |
| Register/memory with register | 1000011w | mod reg r/m | | | 4/17 | 4/17* | |
| Register with accumulator | 10010 reg | | | | 3 | 3 | |
| **IN = Input from:** | | | | | | | |
| Fixed port | 1110010w | port | | | 10 | 10* | |
| Variable port | 1110110w | | | | 8 | 8* | |
| **OUT = Output to:** | | | | | | | |
| Fixed port | 1110011w | port | | | 9 | 9* | |
| Variable port | 1110111w | | | | 7 | 7* | |
| **XLAT** = Translate byte to AL | 11010111 | | | | 11 | 15 | |
| **LEA** = Load EA to register | 10001101 | mod reg r/m | | | 6 | 6 | |
| **LDS** = Load pointer to DS | 11000101 | mod reg r/m | (mod≠11) | | 18 | 26 | |
| **LES** = Load pointer to ES | 11000100 | mod reg r/m | (mod≠11) | | 18 | 26 | |
| **LAHF** = Load AH with flags | 10011111 | | | | 2 | 2 | |
| **SAHF** = Store AH into flags | 10011110 | | | | 3 | 3 | |
| **PUSHF** = Push flags | 10011100 | | | | 9 | 13 | |
| **POPF** = Pop flags | 10011101 | | | | 8 | 12 | |

Shaded areas indicate instructions not available in 8086/8088 microsystems.

**NOTE:**
*Clock cycles shown for byte transfers, for word operations, add 4 clock cycles for all memory transfers.

## INSTRUCTION SET SUMMARY (Continued)

| Function | Format | | | | 80C186EC Clock Cycles | 80C188EC Clock Cycles | Comments |
|---|---|---|---|---|---|---|---|
| **DATA TRANSFER** (Continued) | | | | | | | |
| **SEGMENT = Segment Override:** | | | | | | | |
| **CS** | 00101110 | | | | 2 | 2 | |
| **SS** | 00110110 | | | | 2 | 2 | |
| **DS** | 00111110 | | | | 2 | 2 | |
| **ES** | 00100110 | | | | 2 | 2 | |
| **ARITHMETIC** | | | | | | | |
| **ADD = Add:** | | | | | | | |
| Reg/memory with register to either | 000000dw | mod reg r/m | | | 3/10 | 3/10* | |
| Immediate to register/memory | 100000sw | mod 000 r/m | data | data if s w=01 | 4/16 | 4/16* | |
| Immediate to accumulator | 0000010w | data | data if w=1 | | 3/4 | 3/4 | 8/16-bit |
| **ADC = Add with carry:** | | | | | | | |
| Reg/memory with register to either | 000100dw | mod reg r/m | | | 3/10 | 3/10* | |
| Immediate to register/memory | 100000sw | mod 010 r/m | data | data if s w=01 | 4/16 | 4/16* | |
| Immediate to accumulator | 0001010w | data | data if w=1 | | 3/4 | 3/4 | 8/16-bit |
| **INC = Increment:** | | | | | | | |
| Register/memory | 1111111w | mod 000 r/m | | | 3/15 | 3/15* | |
| Register | 01000 reg | | | | 3 | 3 | |
| **SUB = Subtract:** | | | | | | | |
| Reg/memory and register to either | 001010dw | mod reg r/m | | | 3/10 | 3/10* | |
| Immediate from register/memory | 100000sw | mod 101 r/m | data | data if s w=01 | 4/16 | 4/16* | |
| Immediate from accumulator | 0010110w | data | data if w=1 | | 3/4 | 3/4* | 8/16-bit |
| **SBB = Subtract with borrow:** | | | | | | | |
| Reg/memory and register to either | 000110dw | mod reg r/m | | | 3/10 | 3/10* | |
| Immediate from register/memory | 100000sw | mod 011 r/m | data | data if s w=01 | 4/16 | 4/16* | |
| Immediate from accumulator | 0001110w | data | data if w=1 | | 3/4 | 3/4* | 8/16-bit |
| **DEC = Decrement** | | | | | | | |
| Register/memory | 1111111w | mod 001 r/m | | | 3/15 | 3/15* | |
| Register | 01001 reg | | | | 3 | 3 | |
| **CMP = Compare:** | | | | | | | |
| Register/memory with register | 0011101w | mod reg r/m | | | 3/10 | 3/10* | |
| Register with register/memory | 0011100w | mod reg r/m | | | 3/10 | 3/10* | |
| Immediate with register/memory | 100000sw | mod 111 r/m | data | data if s w=01 | 3/10 | 3/10* | |
| Immediate with accumulator | 0011110w | data | data if w=1 | | 3/4 | 3/4 | 8/16-bit |
| **NEG** = Change sign register/memory | 1111011w | mod 011 r/m | | | 3/10 | 3/10* | |
| **AAA** = ASCII adjust for add | 00110111 | | | | 8 | 8 | |
| **DAA** = Decimal adjust for add | 00100111 | | | | 4 | 4 | |
| **AAS** = ASCII adjust for subtract | 00111111 | | | | 7 | 7 | |
| **DAS** = Decimal adjust for subtract | 00101111 | | | | 4 | 4 | |
| **MUL** = Multiply (unsigned): | 1111011w | mod 100 r/m | | | | | |
| Register-Byte | | | | | 26–28 | 26–28 | |
| Register-Word | | | | | 35–37 | 35–37 | |
| Memory-Byte | | | | | 32–34 | 32–34 | |
| Memory-Word | | | | | 41–43 | 41–43* | |

Shaded areas indicate instructions not available in 8086/8088 microsystems.

**NOTE:**

*Clock cycles shown for byte transfers, for word operations, add 4 clock cycles for all memory transfers.

## INSTRUCTION SET SUMMARY (Continued)

| Function | Format | | | | 80C186EC Clock Cycles | 80C188EC Clock Cycles | Comments |
|---|---|---|---|---|---|---|---|
| **ARITHMETIC** (Continued) | | | | | | | |
| **IMUL** = Integer multiply (signed): | 1 1 1 1 0 1 1 w | mod 1 0 1 r/m | | | | | |
| Register-Byte | | | | | 25–28 | 25–28 | |
| Register-Word | | | | | 34–37 | 34–37 | |
| Memory-Byte | | | | | 31–34 | 32–34 | |
| Memory-Word | | | | | 40–43 | 40–43* | |
| **IMUL** = Integer Immediate multiply (signed) | 0 1 1 0 1 0 s 1 | mod reg r/m | data | data if s=0 | 22–25/ 29–32 | 22–25/ 29–32 | |
| **DIV** = Divide (unsigned): | 1 1 1 1 0 1 1 w | mod 1 1 0 r/m | | | | | |
| Register-Byte | | | | | 29 | 29 | |
| Register-Word | | | | | 38 | 38 | |
| Memory-Byte | | | | | 35 | 35 | |
| Memory-Word | | | | | 44 | 44* | |
| **IDIV** = Integer divide (signed): | 1 1 1 1 0 1 1 w | mod 1 1 1 r/m | | | | | |
| Register-Byte | | | | | 44–52 | 44–52 | |
| Register-Word | | | | | 53–61 | 53–61 | |
| Memory-Byte | | | | | 50–58 | 50–58 | |
| Memory-Word | | | | | 59–67 | 59–67* | |
| **AAM** = ASCII adjust for multiply | 1 1 0 1 0 1 0 0 | 0 0 0 0 1 0 1 0 | | | 19 | 19 | |
| **AAD** = ASCII adjust for divide | 1 1 0 1 0 1 0 1 | 0 0 0 0 1 0 1 0 | | | 15 | 15 | |
| **CBW** = Convert byte to word | 1 0 0 1 1 0 0 0 | | | | 2 | 2 | |
| **CWD** = Convert word to double word | 1 0 0 1 1 0 0 1 | | | | 4 | 4 | |
| **LOGIC** | | | | | | | |
| **Shift/Rotate Instructions:** | | | | | | | |
| Register/Memory by 1 | 1 1 0 1 0 0 0 w | mod TTT r/m | | | 2/15 | 2/15 | |
| Register/Memory by CL | 1 1 0 1 0 0 1 w | mod TTT r/m | | | 5+n/17+n | 5+n/17+n | |
| Register/Memory by Count | 1 1 0 0 0 0 0 w | mod TTT r/m | count | | 5+n/17+n | 5+n/17+n | |
| | **TTT Instruction**<br>0 0 0 ROL<br>0 0 1 ROR<br>0 1 0 RCL<br>0 1 1 RCR<br>1 0 0 SHL/SAL<br>1 0 1 SHR<br>1 1 1 SAR | | | | | | |
| **AND** = **And:** | | | | | | | |
| Reg/memory and register to either | 0 0 1 0 0 0 d w | mod reg r/m | | | 3/10 | 3/10* | |
| Immediate to register/memory | 1 0 0 0 0 0 0 w | mod 1 0 0 r/m | data | data if w=1 | 4/16 | 4/16* | |
| Immediate to accumulator | 0 0 1 0 0 1 0 w | data | data if w=1 | | 3/4 | 3/4* | 8/16-bit |
| **TEST** = **And function to flags, no result:** | | | | | | | |
| Register/memory and register | 1 0 0 0 0 1 0 w | mod reg r/m | | | 3/10 | 3/10 | |
| Immediate data and register/memory | 1 1 1 1 0 1 1 w | mod 0 0 0 r/m | data | data if w=1 | 4/10 | 4/10* | |
| Immediate data and accumulator | 1 0 1 0 1 0 0 w | data | data if w=1 | | 3/4 | 3/4 | 8/16-bit |
| **OR** = **Or:** | | | | | | | |
| Reg/memory and register to either | 0 0 0 0 1 0 d w | mod reg r/m | | | 3/10 | 3/10* | |
| Immediate to register/memory | 1 0 0 0 0 0 0 w | mod 0 0 1 r/m | data | data if w=1 | 4/16 | 4/16* | |
| Immediate to accumulator | 0 0 0 0 1 1 0 w | data | data if w=1 | | 3/4 | 3/4* | 8/16-bit |

Shaded areas indicate instructions not available in 8086/8088 microsystems.

**NOTE:**
*Clock cycles shown for byte transfers, for word operations, add 4 clock cycles for all memory transfers.

## INSTRUCTION SET SUMMARY (Continued)

| Function | Format | 80C186EC Clock Cycles | 80C188EC Clock Cycles | Comments |
|---|---|---|---|---|
| **LOGIC** (Continued) | | | | |
| **XOR** = **Exclusive or:** | | | | |
| Reg/memory and register to either | 0 0 1 1 0 0 d w \| mod reg r/m | 3/10 | 3/10* | |
| Immediate to register/memory | 1 0 0 0 0 0 0 w \| mod 1 1 0 r/m \| data \| data if w=1 | 4/16 | 4/16* | |
| Immediate to accumulator | 0 0 1 1 0 1 0 w \| data \| data if w=1 | 3/4 | 3/4 | 8/16-bit |
| **NOT** = Invert register/memory | 1 1 1 1 0 1 1 w \| mod 0 1 0 r/m | 3/10 | 3/10* | |
| **STRING MANIPULATION** | | | | |
| **MOVS** = Move byte/word | 1 0 1 0 0 1 0 w | 14 | 14* | |
| **CMPS** = Compare byte/word | 1 0 1 0 0 1 1 w | 22 | 22* | |
| **SCAS** = Scan byte/word | 1 0 1 0 1 1 1 w | 15 | 15* | |
| **LODS** = Load byte/wd to AL/AX | 1 0 1 0 1 1 0 w | 12 | 12* | |
| **STOS** = Store byte/wd from AL/AX | 1 0 1 0 1 0 1 w | 10 | 10* | |
| **INS** = Input byte/wd from DX port | 0 1 1 0 1 1 0 w | 14 | 14 | |
| **OUTS** = Output byte/wd to DX port | 0 1 1 0 1 1 1 w | 14 | 14 | |
| Repeated by count in CX (REP/REPE/REPZ/REPNE/REPNZ) | | | | |
| **MOVS** = Move string | 1 1 1 1 0 0 1 0 \| 1 0 1 0 0 1 0 w | 8+8n | 8+8n* | |
| **CMPS** = Compare string | 1 1 1 1 0 0 1 z \| 1 0 1 0 0 1 1 w | 5+22n | 5+22n* | |
| **SCAS** = Scan string | 1 1 1 1 0 0 1 z \| 1 0 1 0 1 1 1 w | 5+15n | 5+15n* | |
| **LODS** = Load string | 1 1 1 1 0 0 1 0 \| 1 0 1 0 1 1 0 w | 6+11n | 6+11n* | |
| **STOS** = Store string | 1 1 1 1 0 0 1 0 \| 1 0 1 0 1 0 1 w | 6+9n | 6+9n* | |
| **INS** = Input string | 1 1 1 1 0 0 1 0 \| 0 1 1 0 1 1 0 w | 8+8n | 8+8n* | |
| **OUTS** = Output string | 1 1 1 1 0 0 1 0 \| 0 1 1 0 1 1 1 w | 8+8n | 8+8n* | |
| **CONTROL TRANSFER** | | | | |
| **CALL** = **Call:** | | | | |
| Direct within segment | 1 1 1 0 1 0 0 0 \| disp-low \| disp-high | 15 | 19 | |
| Register/memory indirect within segment | 1 1 1 1 1 1 1 1 \| mod 0 1 0 r/m | 13/19 | 17/27 | |
| Direct intersegment | 1 0 0 1 1 0 1 0 \| segment offset<br>segment selector | 23 | 31 | |
| Indirect intersegment | 1 1 1 1 1 1 1 1 \| mod 0 1 1 r/m (mod ≠ 11) | 38 | 54 | |
| **JMP** = **Unconditional jump:** | | | | |
| Short/long | 1 1 1 0 1 0 1 1 \| disp-low | 14 | 14 | |
| Direct within segment | 1 1 1 0 1 0 0 1 \| disp-low \| disp-high | 14 | 14 | |
| Register/memory indirect within segment | 1 1 1 1 1 1 1 1 \| mod 1 0 0 r/m | 11/17 | 11/21 | |
| Direct intersegment | 1 1 1 0 1 0 1 0 \| segment offset<br>segment selector | 14 | 14 | |
| Indirect intersegment | 1 1 1 1 1 1 1 1 \| mod 1 0 1 r/m (mod ≠ 11) | 26 | 34 | |

Shaded areas indicate instructions not available in 8086/8088 microsystems.

**NOTE:**
*Clock cycles shown for byte transfers, for word operations, add 4 clock cycles for all memory transfers.

## INSTRUCTION SET SUMMARY (Continued)

| Function | Format | | | | 80C186EC Clock Cycles | 80C188EC Clock Cycles | Comments |
|---|---|---|---|---|---|---|---|
| **CONTROL TRANSFER** (Continued) | | | | | | | |
| **RET** = **Return from CALL:** | | | | | | | |
| Within segment | 11000011 | | | | 16 | 20 | |
| Within seg adding immed to SP | 11000010 | data-low | data-high | | 18 | 22 | |
| Intersegment | 11001011 | | | | 22 | 30 | |
| Intersegment adding immediate to SP | 11001010 | data-low | data-high | | 25 | 33 | |
| **JE/JZ** = Jump on equal/zero | 01110100 | disp | | | 4/13 | 4/13 | JMP not taken/JMP taken |
| **JL/JNGE** = Jump on less/not greater or equal | 01111100 | disp | | | 4/13 | 4/13 | |
| **JLE/JNG** = Jump on less or equal/not greater | 01111110 | disp | | | 4/13 | 4/13 | |
| **JB/JNAE** = Jump on below/not above or equal | 01110010 | disp | | | 4/13 | 4/13 | |
| **JBE/JNA** = Jump on below or equal/not above | 01110110 | disp | | | 4/13 | 4/13 | |
| **JP/JPE** = Jump on parity/parity even | 01111010 | disp | | | 4/13 | 4/13 | |
| **JO** = Jump on overflow | 01110000 | disp | | | 4/13 | 4/13 | |
| **JS** = Jump on sign | 01111000 | disp | | | 4/13 | 4/13 | |
| **JNE/JNZ** = Jump on not equal/not zero | 01110101 | disp | | | 4/13 | 4/13 | |
| **JNL/JGE** = Jump on not less/greater or equal | 01111101 | disp | | | 4/13 | 4/13 | |
| **JNLE/JG** = Jump on not less or equal/greater | 01111111 | disp | | | 4/13 | 4/13 | |
| **JNB/JAE** = Jump on not below/above or equal | 01110011 | disp | | | 4/13 | 4/13 | |
| **JNBE/JA** = Jump on not below or equal/above | 01110111 | disp | | | 4/13 | 4/13 | |
| **JNP/JPO** = Jump on not par/par odd | 01111011 | disp | | | 4/13 | 4/13 | |
| **JNO** = Jump on not overflow | 01110001 | disp | | | 4/13 | 4/13 | |
| **JNS** = Jump on not sign | 01111001 | disp | | | 4/13 | 4/13 | |
| **JCXZ** = Jump on CX zero | 11100011 | disp | | | 5/15 | 5/15 | |
| **LOOP** = Loop CX times | 11100010 | disp | | | 6/16 | 6/16 | LOOP not taken/LOOP taken |
| **LOOPZ/LOOPE** = Loop while zero/equal | 11100001 | disp | | | 6/16 | 6/16 | |
| **LOOPNZ/LOOPNE** = Loop while not zero/equal | 11100000 | disp | | | 6/16 | 6/16 | |
| **ENTER** = Enter Procedure | 11001000 | data-low | data-high | L | | | |
| L = 0 | | | | | 15 | 19 | |
| L = 1 | | | | | 25 | 29 | |
| L > 1 | | | | | 22+16(n−1) | 26+20(n−1) | |
| **LEAVE** = Leave Procedure | 11001001 | | | | 8 | 8 | |
| **INT** = **Interrupt:** | | | | | | | |
| Type specified | 11001101 | type | | | 47 | 47 | |
| Type 3 | 11001100 | | | | 45 | 45 | if INT. taken/ if INT. not taken |
| **INTO** = Interrupt on overflow | 11001110 | | | | 48/4 | 48/4 | |
| **IRET** = Interrupt return | 11001111 | | | | 28 | 28 | |
| **BOUND** = Detect value out of range | 01100010 | mod reg r/m | | | 33–35 | 33–35 | |

Shaded areas indicate instructions not available in 8086/8088 microsystems.

**NOTE:**
*Clock cycles shown for byte transfers, for word operations, add 4 clock cycles for all memory transfers.

## INSTRUCTION SET SUMMARY (Continued)

| Function | Format | 80C186EC Clock Cycles | 80C188EC Clock Cycles | Comments |
|---|---|---|---|---|
| **PROCESSOR CONTROL** | | | | |
| **CLC** = Clear carry | 11111000 | 2 | 2 | |
| **CMC** = Complement carry | 11110101 | 2 | 2 | |
| **STC** = Set carry | 11111001 | 2 | 2 | |
| **CLD** = Clear direction | 11111100 | 2 | 2 | |
| **STD** = Set direction | 11111101 | 2 | 2 | |
| **CLI** = Clear interrupt | 11111010 | 2 | 2 | |
| **STI** = Set interrupt | 11111011 | 2 | 2 | |
| **HLT** = Halt | 11110100 | 2 | 2 | |
| **WAIT** = Wait | 10011011 | 6 | 6 | if $\overline{TEST}$ = 0 |
| **LOCK** = Bus lock prefix | 11110000 | 2 | 2 | |
| **NOP** = No Operation | 10010000 | 3 | 3 | |
| | (TTT LLL are opcode to processor extension) | | | |

Shaded areas indicate instructions not available in 8086/8088 microsystems.

**NOTE:**
*Clock cycles shown for byte transfers, for word operations, add 4 clock cycles for all memory transfers.

The Effective Address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

EA calculation time is 4 clock cycles for all modes, and is included in the execution times given whenever appropriate.

**Segment Override Prefix**

| 0 | 0 | 1 | reg | 1 | 1 | 0 |
|---|---|---|---|---|---|---|

reg is assigned according to the following:

| reg | Segment Register |
|---|---|
| 00 | ES |
| 01 | CS |
| 10 | SS |
| 11 | DS |

REG is assigned according to the following table:

| 16-Bit (w = 1) | 8-Bit (w = 0) |
|---|---|
| 000 AX | 000 AL |
| 001 CX | 001 CL |
| 010 DX | 010 DL |
| 011 BX | 011 BL |
| 100 SP | 100 AH |
| 101 BP | 101 CH |
| 110 SI | 110 DH |
| 111 DI | 111 BH |

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

## ERRATA

An 80C186EC/80L186EC with a STEPID value of 0002H has no known errata. A device with a STEPID of 0002H can be visually identified by noting the **presence** of an ''A'' or ''B'' alpha character next to the FPO number or the absence of any alpha character. The FPO number location is shown in Figures 4, 5 and 6.

## REVISION HISTORY

This data sheet replaces the following data sheets:

| | |
|---|---|
| 272072-003 | 80C186EC |
| 272076-003 | 80C188EC |
| 272332-001 | 80L186EC |
| 272333-001 | 80L188EC |
| 272373-001 | SB80C188EC/SB80L188EC |
| 272372-001 | SB80C186EC/SB80L186EC |

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