



PSMN8R5-100ES

N-channel 100 V 8.5 mΩ standard level MOSFET in I2PAK

11 October 2012

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in a I2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources

1.3 Applications

- AC-to-DC power supply equipment
- Motor control
- Server power supplies
- Synchronous rectification

1.4 Quick reference data

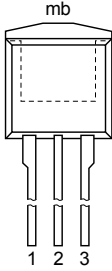
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	-	100	V
I _D	drain current	T _j = 25 °C; V _{GS} = 10 V; Fig. 1	[1]	-	-	100	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 2		-	-	263	W
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 13 ; Fig. 12		-	6.4	8.5	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	V _{GS} = 10 V; I _D = 25 A; V _{DS} = 50 V;		-	33	-	nC
Q _{G(tot)}	total gate charge	Fig. 14 ; Fig. 15		-	111	-	nC
Avalanche Ruggedness							
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 100 A; V _{sup} ≤ 100 V; R _{GS} = 50 Ω; unclamped; Fig. 3		-	-	219	mJ

[1] Continuous current limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 I2PAK (SOT226)	
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN8R5-100ES	I2PAK	plastic single-ended package (I2PAK); TO-262	SOT226

4. Marking

Table 4. Marking codes

Type number	Marking code
PSMN8R5-100ES	PSMN8R5-100ES

5. Limiting values

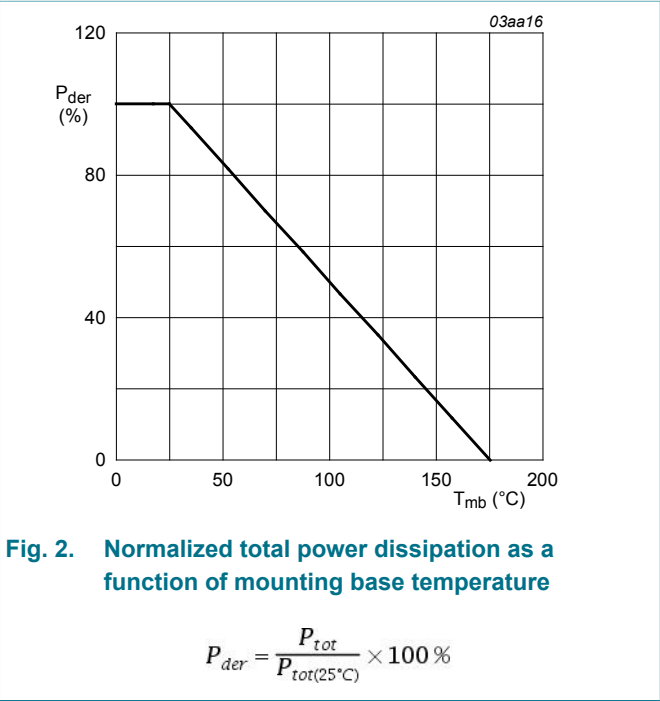
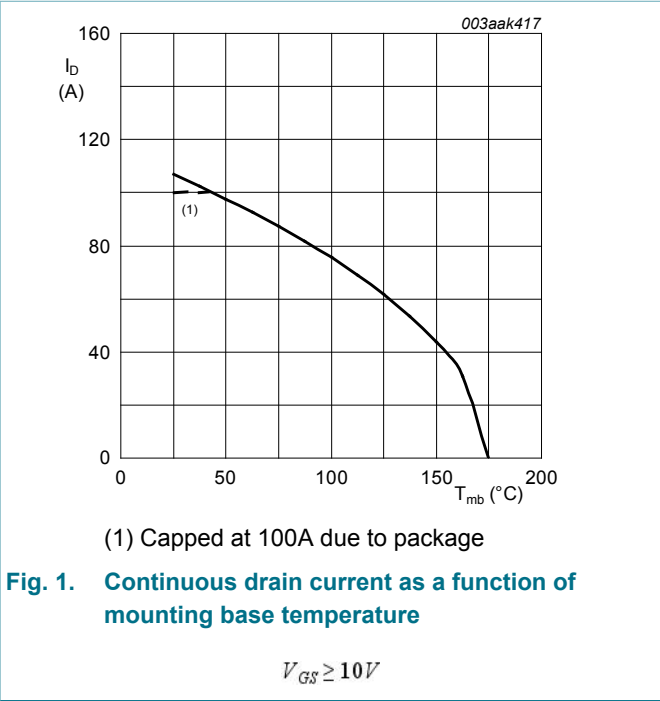
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$		-	100	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$		-	100	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_j = 25\text{ °C}$; Fig. 1	[1]	-	100	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 1		-	75	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 4		-	429	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 2		-	263	W
T_{stg}	storage temperature			-55	175	°C

Symbol	Parameter	Conditions		Min	Max	Unit
T _j	junction temperature			-55	175	°C
T _{sld(M)}	peak soldering temperature			-	260	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C	[1]	-	100	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	429	A
Avalanche Ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 100 A; V _{sup} ≤ 100 V; R _{GS} = 50 Ω; unclamped; Fig. 3		-	219	mJ

[1] Continuous current limited by package.



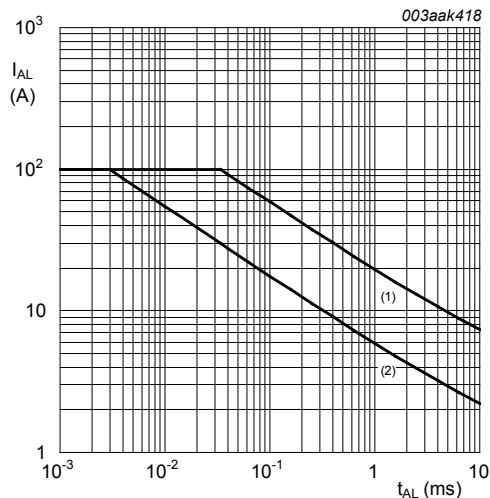


Fig. 3. Avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j(jnt)} = 25^{\circ}\text{C}$; (2) $T_{j(jnt)} = 130^{\circ}\text{C}$

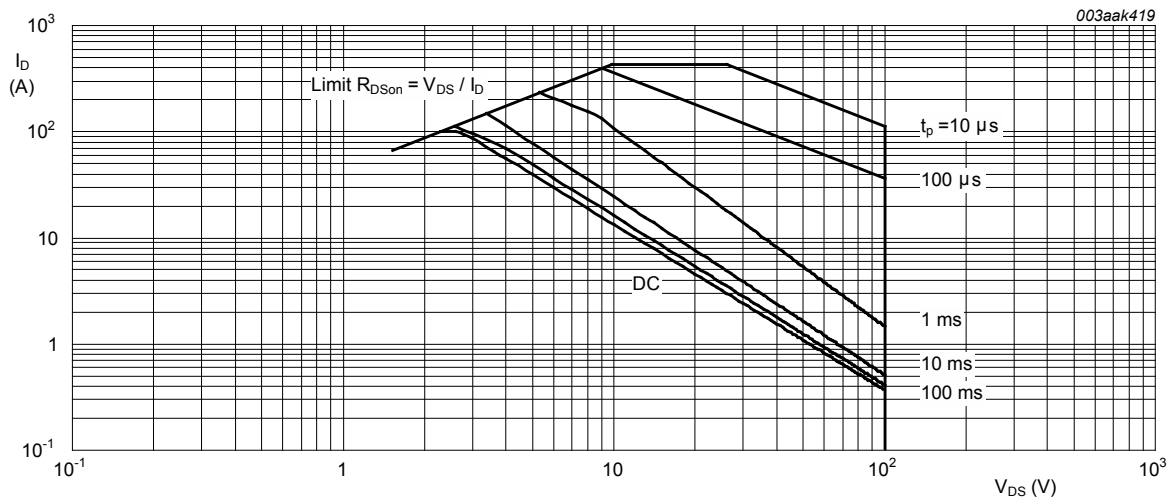


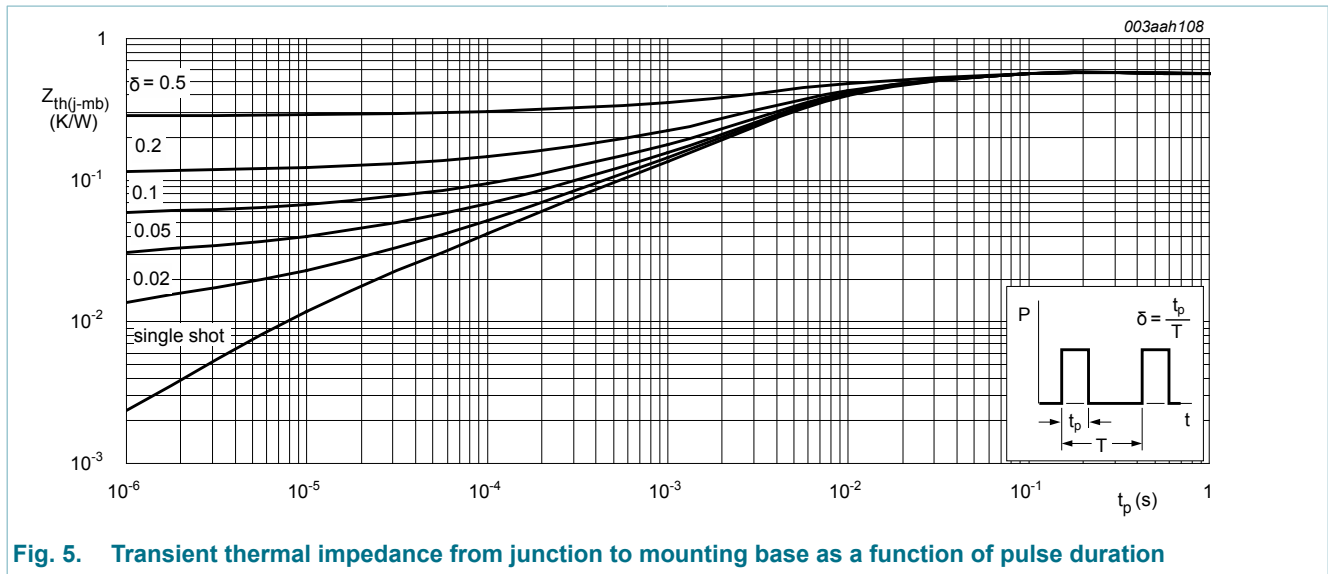
Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}\text{C}$; I_{DM} is a single pulse

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.49	0.57	K/W



7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_J = 25 ^\circ C$	100	-	-	V
		$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_J = -55 ^\circ C$	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA$; $V_{DS} = V_{GS}$; $T_J = 25 ^\circ C$; Fig. 10 ; Fig. 11	2.4	3	4	V
V_{GSth}	gate-source threshold voltage	$I_D = 1 mA$; $V_{DS} = V_{GS}$; $T_J = 175 ^\circ C$; Fig. 10	1	-	-	V
		$I_D = 1 mA$; $V_{DS} = V_{GS}$; $T_J = -55 ^\circ C$; Fig. 10	-	-	4.5	V
I_{DSS}	drain leakage current	$V_{DS} = 100 V$; $V_{GS} = 0 V$; $T_J = 25 ^\circ C$	-	0.02	1	μA
		$V_{DS} = 100 V$; $V_{GS} = 0 V$; $T_J = 100 ^\circ C$	-	-	20	μA
I_{GSS}	gate leakage current	$V_{GS} = -20 V$; $V_{DS} = 0 V$; $T_J = 25 ^\circ C$	-	2	100	nA
		$V_{GS} = 20 V$; $V_{DS} = 0 V$; $T_J = 25 ^\circ C$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 V$; $I_D = 25 A$; $T_J = 175 ^\circ C$; Fig. 12	-	-	22.6	mΩ
		$V_{GS} = 10 V$; $I_D = 25 A$; $T_J = 100 ^\circ C$; Fig. 12	-	-	14.9	mΩ
		$V_{GS} = 10 V$; $I_D = 25 A$; $T_J = 25 ^\circ C$; Fig. 13 ; Fig. 12	-	6.4	8.5	mΩ
R_G	gate resistance	$f = 1 MHz$	-	0.71	-	Ω

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 50 V; V _{GS} = 10 V; Fig. 14 ; Fig. 15		-	111	-	nC
Q _{GS}	gate-source charge			-	24	-	nC
Q _{GS(th)}	pre-threshold gate-source charge			-	16	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge			-	8	-	nC
Q _{GD}	gate-drain charge			-	33	-	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 15 A; V _{DS} = 50 V; Fig. 14 ; Fig. 15		-	4.4	-	V
C _{iss}	input capacitance	V _{DS} = 50 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 16 ; Fig. 17		-	5512	-	pF
C _{oss}	output capacitance	V _{DS} = 50 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 16		-	380	-	pF
C _{rss}	reverse transfer capacitance	V _{DS} = 50 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 16 ; Fig. 17		-	256	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 50 V; R _L = 2 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω		-	20	-	ns
t _r	rise time			-	35	-	ns
t _{d(off)}	turn-off delay time			-	87	-	ns
t _f	fall time			-	43	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 18		-	0.82	1.2	V
t _{rr}	reverse recovery time	I _S = 25 A; di _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 50 V		-	53	-	ns
Q _r	recovered charge			-	124	-	nC

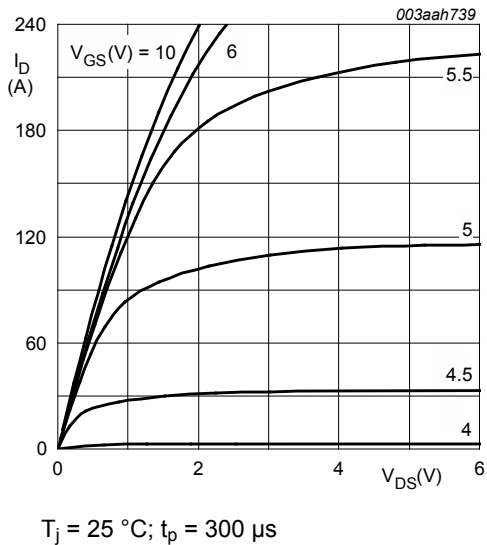


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

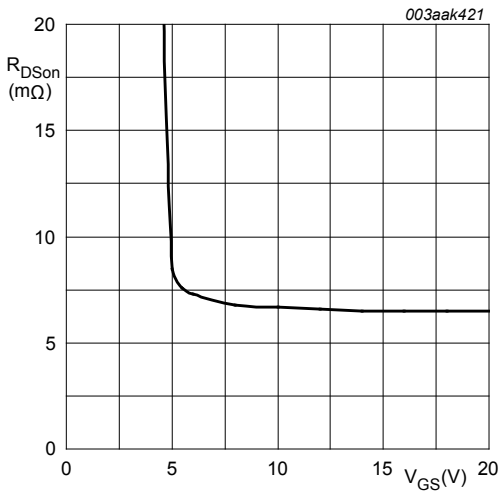


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25^\circ\text{C}; I_D = 25\text{ A}$

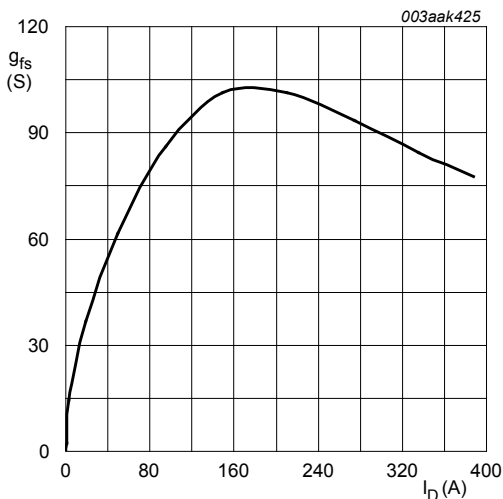


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25^\circ\text{C}; V_{DS} = 10\text{ V}$

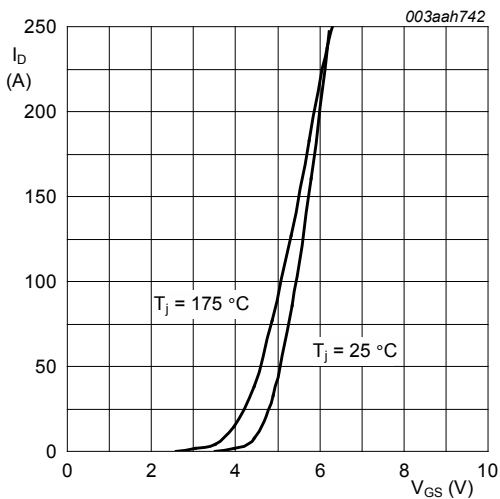


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10\text{ V}$

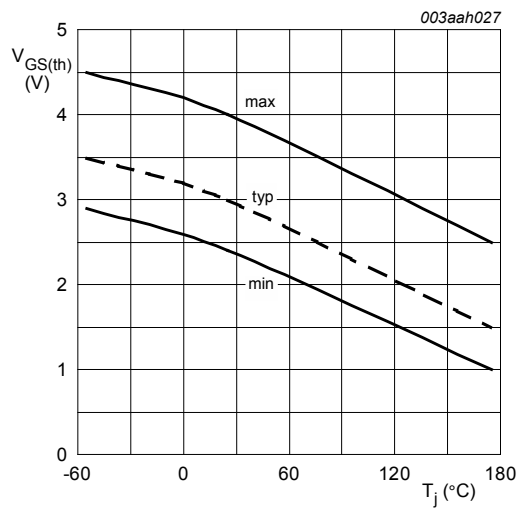


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$

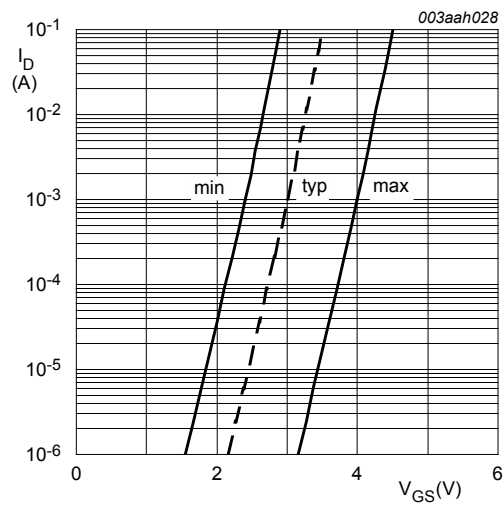


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25^\circ\text{C}; V_{DS} = 5\text{ V}$$

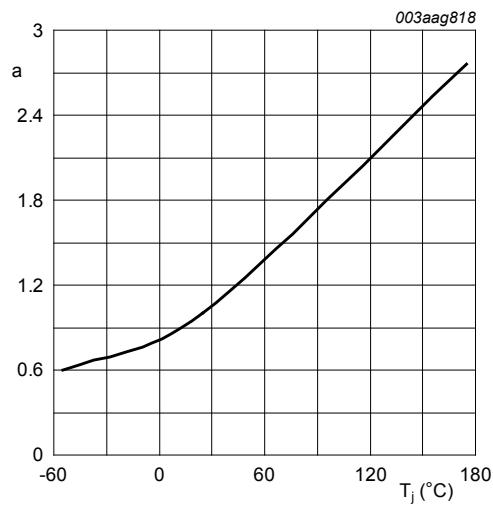


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

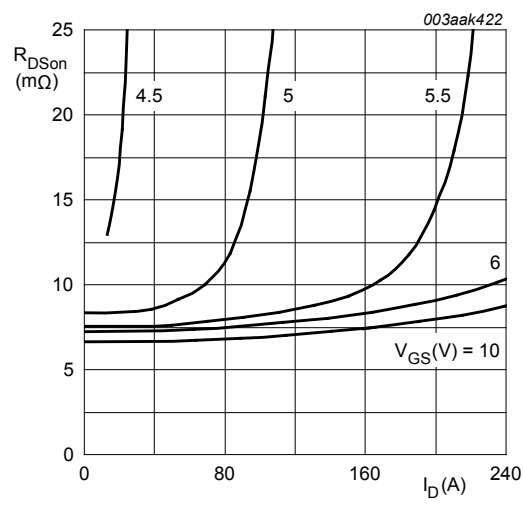


Fig. 13. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^\circ\text{C}$$

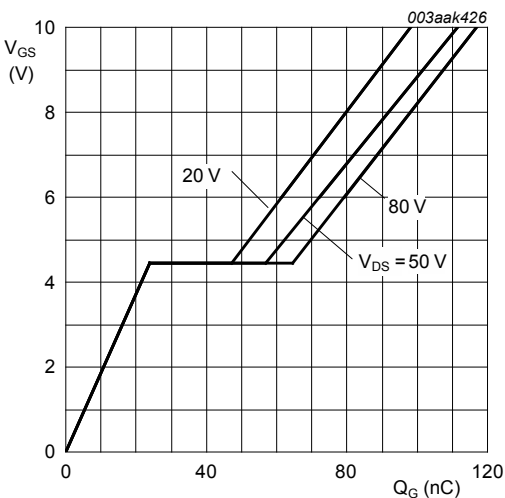


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^\circ\text{C}; I_D = 25\text{ A}$

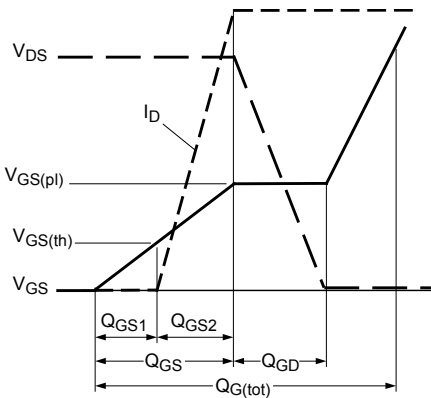


Fig. 15. Gate charge waveform definitions

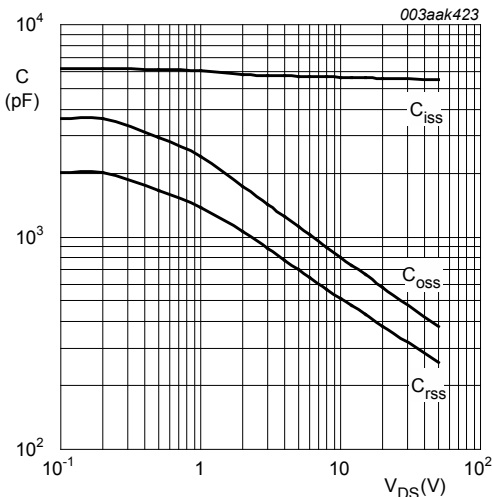


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

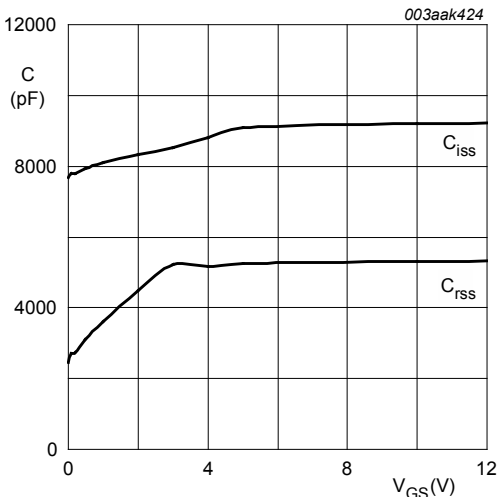


Fig. 17. Input and reverse transfer capacitances as a function of gate-source voltage, typical values

$f = 1\text{ MHz}; V_{DS} = 0\text{ V}$

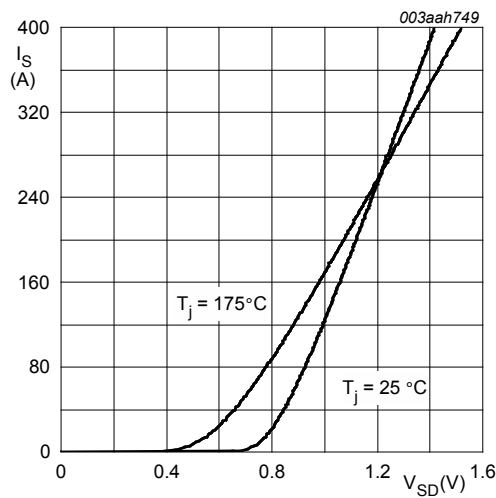


Fig. 18. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$V_{GS} = 0V$

8. Package outline

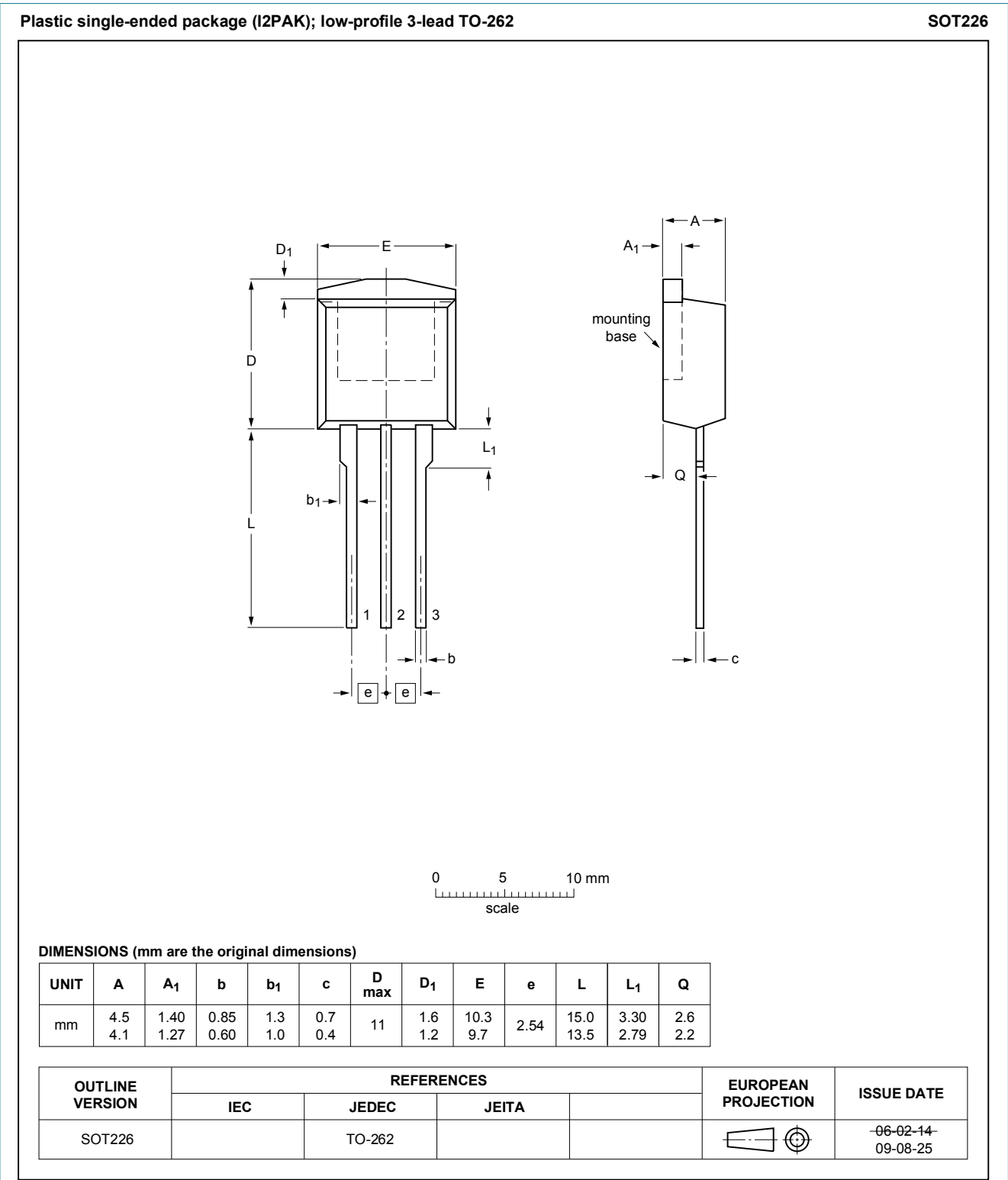


Fig. 19. Package outline I2PAK (SOT226)

9. Legal information

9.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Date of release: 11 October 2012

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