
ML610Q101/ML610Q102

8-bit Microcontroller

GENERAL DESCRIPTION

This LSI is a high-performance 8-bit CMOS microcontroller into which rich peripheral circuits, such as timers, PWM, UART, voltage level supervisor (VLS) function, and 10-bit successive approximation type A/D converter, are incorporated around 8-bit CPU nX-U8/100.

The CPU nX-U8/100 is capable of efficient instruction execution in 1-instruction 1-clock mode by pipe line architecture parallel processing.

The on-chip debug function that is installed enables program debugging and programming.

FEATURES

- CPU
 - 8-bit RISC CPU (CPU name: nX-U8/100)
 - Instruction system: 16-bit instructions
 - Instruction set:
 - Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
 - On-Chip debug function
 - Minimum instruction execution time
 - 30.5 μ s (@32.768kHz system clock)
 - 0.122 μ s (@8.192MHz system clock)
- Internal memory
 - ML610Q101 : Internal 4Kbyte Flash ROM (2K \times 16 bits) (including unusable 32 byte test data area)
 - ML610Q102 : Internal 6Kbyte Flash ROM (3K \times 16 bits) (including unusable 32 byte test data area)
 - Internal 256byte data RAM (256 \times 8 bits)
- Interrupt controller
 - 1 non-maskable interrupt source (Internal source: 1)
 - 21 maskable interrupt sources (Internal sources: 16, External sources: 5)
- Time base counter (TBC)
 - Low-speed time base counter \times 1 channel
 - High-speed time base counter \times 1 channel
- Watchdog timer (WDT)
 - Non-maskable interrupt and reset
 - Free running
 - Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s)
- Timer
 - 8 bits \times 6 channels (16-bit configuration available)
 - Support Continuous timer mode/one shot timer mode
 - Timer start/stop function by software or external trigger input

- PWM
 - Resolution 16 bits × 1 channel
 - Support Continuous timer mode/one shot timer mode
 - PWM start/stop function by software or external trigger input
- UART
 - Half-duplex
 - TXD/RXD × 1 channels
 - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
 - Positive logic/negative logic selectable
 - Built-in baud rate generator
- Successive approximation type A/D converter (SA-ADC)
 - 10-bit A/D converter
 - Input × 6 channels
- Analog Comparator
 - Operating voltage: $V_{DD} = 2.7V$ to $5.5V$
 - Input voltage by common mode: $V_{DD} = 0.1V$ to $V_{DD} - 1.5V$
 - Hysteresis (Comparator0 only): 20mV(Typ.)
 - Allows selection of interrupt disabled mode,falling-edge interrupt mode,rising-edge interrupt mode, or both-edge interrupt mode.
- General-purpose ports (GPIO)
 - Input/output port × 11 channels (including secondary functions)
- Reset
 - Reset by the RESET_N pin
 - Reset by power-on detection
 - Reset by the watchdog timer (WDT) overflow
 - Reset by voltage level supervisor(VLS)
- Voltage level supervisor(VLS)
 - Judgment accuracy: $\pm 3.0\%$ (Typ.)
 - It can be used for low level detection reset.
- Clock
 - Low-speed clock:
 - Built-in RC oscillation (32.768 kHz)
 - High-speed clock:
 - Built-in PLL oscillation (16.384 MHz), external clock
 - The clock of the CPU is 8.192MHz(Max)
 - Selection of high-speed clock mode by software:
 - Built-in PLL oscillation, external clock
- Power management
 - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
 - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
 - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
 - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.

- Shipment
 - 16-pin plastic SSOP
 - ML610Q101-xxxMB (Blank product: ML610Q101-NNNMB)
 - ML610Q102-xxxMB (Blank product: ML610Q102-NNNMB)
- Guaranteed operating range
 - Operating temperature: -40°C to 85°C
 - Operating voltage: $V_{\text{DD}} = 2.7\text{V}$ to 5.5V

BLOCK DIAGRAM
ML610Q101 Block Diagram

Figure 1 show the block diagram of the ML610Q101.

"*" indicates secondary function, tertiary function or quaternary function of each port.

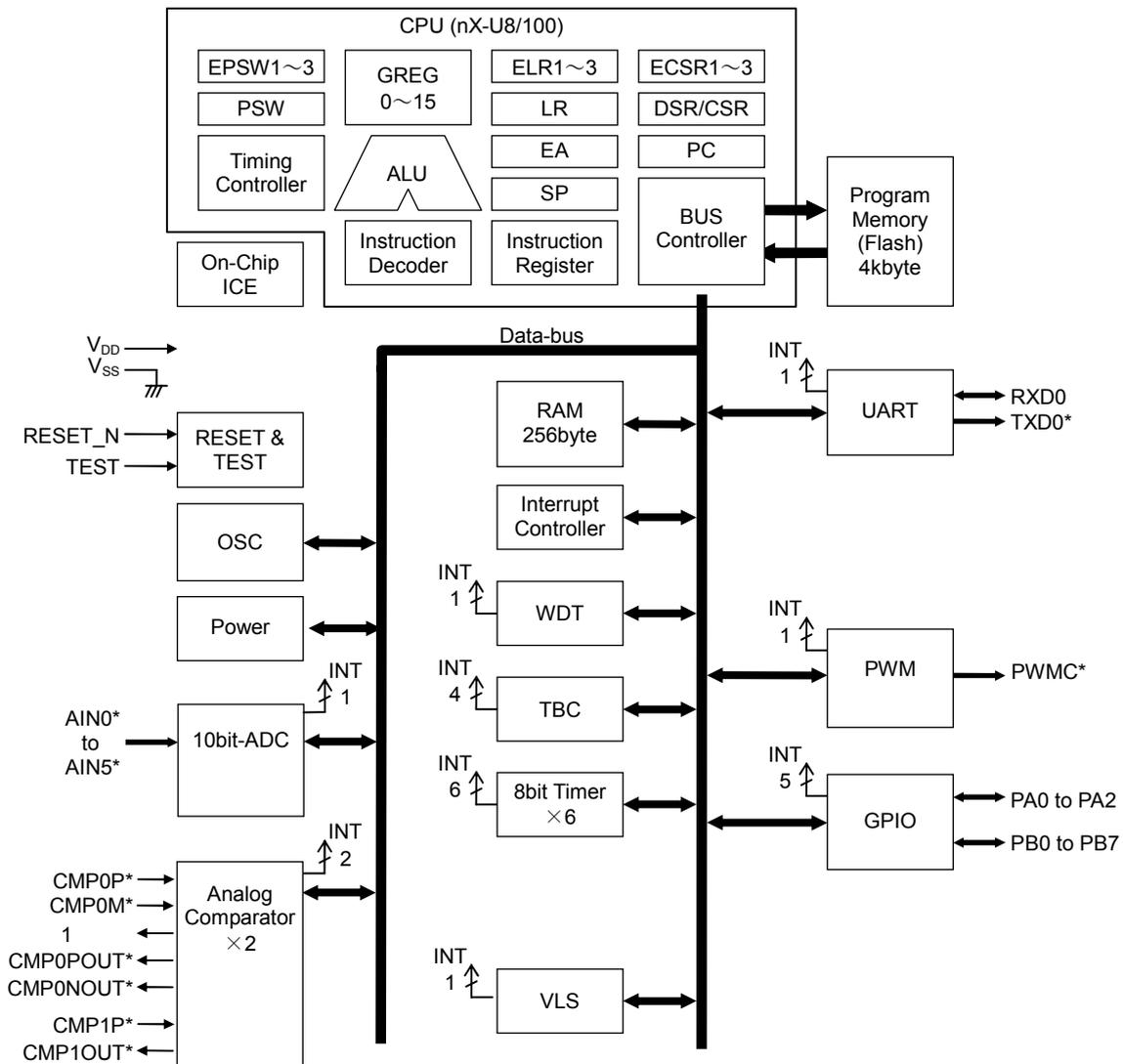


Figure 1 ML610Q101 Block Diagram

ML610Q102 Block Diagram

Figure 2 show the block diagram of the ML610Q102.

"*" indicates secondary function, tertiary function or quaternary function of each port.

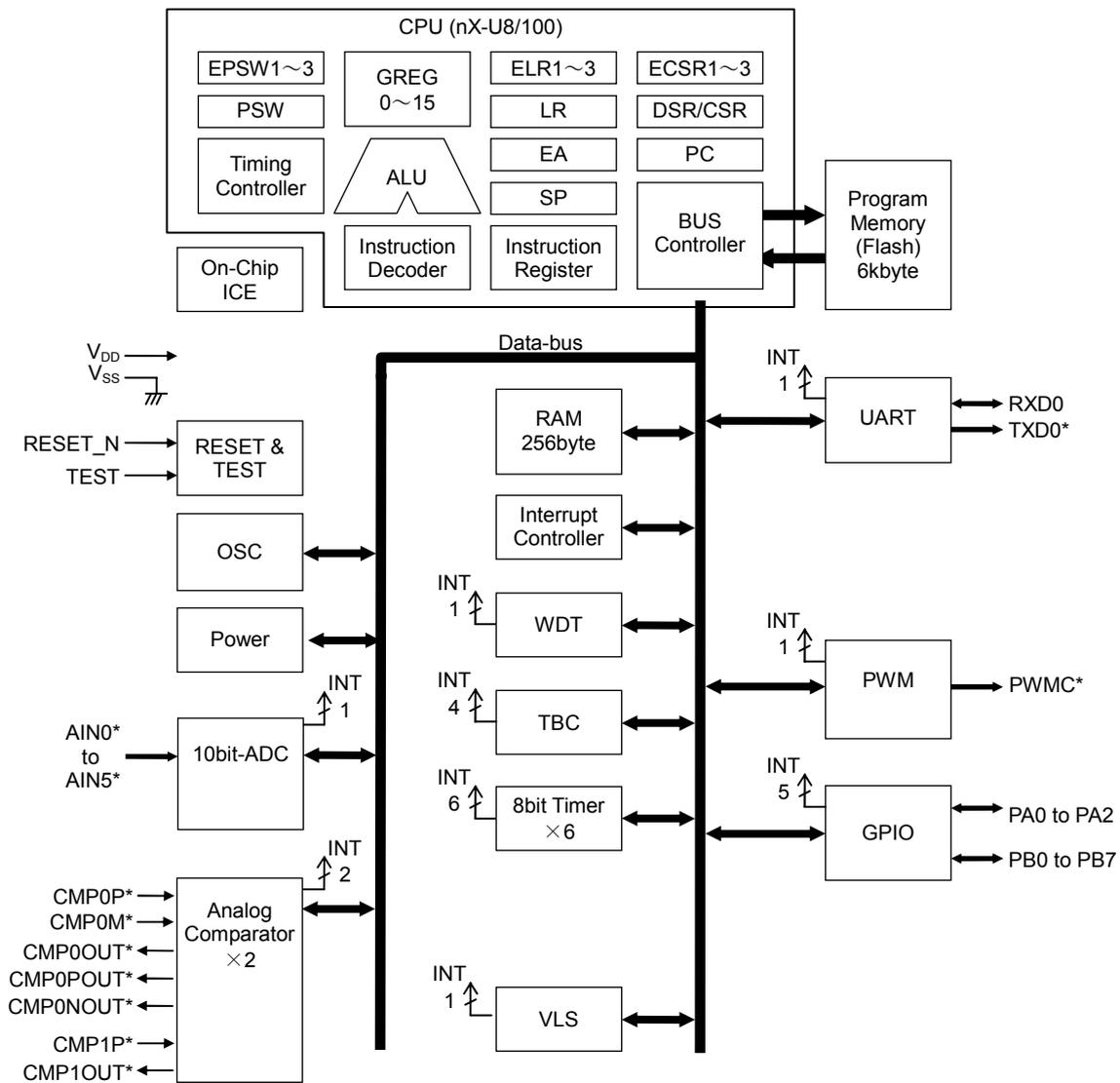


Figure 2 ML610Q102 Block Diagram

PIN CONFIGURATION

ML610Q101/ML610Q102 SSOP16 Pin Layout

Figure 3 show the SSOP16 pin layout of the ML610Q101/ML610Q102.

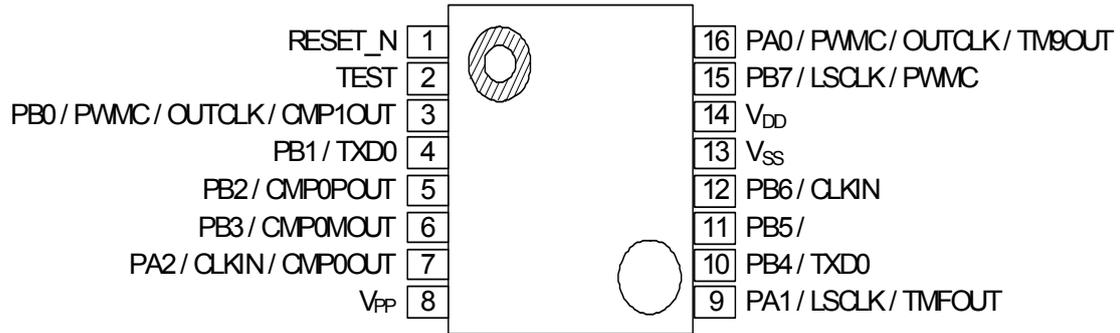


Figure 3 ML610Q101/ML610Q102 SSOP16 Pin Configuration

LIST OF PINS

| PIN No. | Primary function | | | Secondary function | | | Tertiary function | | | Quaternary function | | |
|---------|---------------------------------|-----|--|--------------------|-----|------------------------|-------------------|-----|-------------------------|---------------------|-----|-------------------|
| | Pin name | I/O | Function | Pin name | I/O | Function | Pin name | I/O | Function | Pin name | I/O | Function |
| 1 | RESET_N | I | Reset input pin | — | — | — | — | — | — | — | — | — |
| 2 | TEST | I/O | Input/output pin for testing | — | — | — | — | — | — | — | — | — |
| 3 | PB0/ EXI4/ AIN2/ RXD0 | I/O | Input/output port, External interrupt 4, ADC input 2, UART receive | PWMC | O | PWMC output | OUTCLK | O | High-speed clock output | CMP1OUT | O | CMP1 output |
| 4 | PB1/ EXI5/ AIN3 | I/O | Input/output port, External interrupt 5, ADC input 3 | — | — | — | TXD0 | O | UART data output | — | — | — |
| 5 | PB2 | I/O | Input/output port, | — | — | — | — | — | — | CMP0P OUT | O | CMP0_N output |
| 6 | PB3 | I/O | Input/output port | — | — | — | — | — | — | CMP0N OUT | O | CMP0_N output |
| 7 | PA2/EXI2 | I/O | Input/output port, External interrupt | — | — | — | CLKIN | I | clock input | CMP0O UT | O | CMP0 output |
| 8 | V _{PP} | — | Power supply pin for Flash ROM | — | — | — | — | — | — | — | — | — |
| 9 | PA1/ EXI1/ AIN1/ CMP1P | I/O | Input port, External interrupt 1, ADC input 1, Comparator1 non-inverting input | — | — | — | LSCLK | O | Low speed clock output | TMF OUT | O | timer F output |
| 10 | PB4/ CMP0P | I/O | Input/output port, Comparator0 non-inverting input | — | — | — | TXD0 | O | UART data output | — | — | — |
| 11 | PB5/ RXD0/ CMP0M | I/O | Input/output port, UART data receive, Comparator1 inverting input | — | — | — | — | — | — | — | — | — |
| 12 | PB6/ AIN4 | I/O | Input/output port, ADC input 4 | CLKIN | I | clock input | — | — | — | — | — | — |
| 13 | V _{SS} | — | Negative power supply pin | — | — | — | — | — | — | — | — | — |
| 14 | V _{DD} | — | Positive power supply pin | — | — | — | — | — | — | — | — | — |
| 15 | PB7/ AIN5 | I/O | Input/output port, ADC input 5 | LSCLK | O | Low-speed clock output | — | — | — | PWMC | O | PWMC output |
| 16 | PA0/ EXI0/ AIN0 | I/O | Input port, External interrupt 0, ADC input 0 | PWMC | O | PWMC output | OUTCLK | O | High-speed clock output | TM9OU T | O | timer 9 output |

PIN DESCRIPTION

| Pin name | I/O | Description | Primary/ Secondary/ Tertiary/ Quaternary | Logic |
|--|-----|---|---|-----------------------|
| System | | | | |
| RESET_N | I | Reset input pin. When this pin is set to a "L" level, system reset mode is set and the internal section is initialized. When this pin is set to a "H" level subsequently, program execution starts. A pull-up resistor is internally connected. | — | Negative |
| CLKIN | I | High-speed clock output pin. This pin is used as the tertiary function of the PA2 or the secondary function of PB6 pin. | Secondary/ Tertiary | — |
| LSCLK | O | Low-speed clock output pin. This pin is used as the tertiary function of the PA1 or the secondary function of the PB7 pin. | Secondary/ Tertiary | — |
| OUTCLK | O | High-speed clock output pin. This pin is used as the tertiary function of the PA0 or PB0 pin. | Tertiary | — |
| General-purpose input/output port | | | | |
| PA0 to PA2 PB0 to PB7 | I/O | General-purpose input/output port. Since these pins have secondary functions and tertiary functions and quaternary functions, the pins cannot be used as a port when the secondary functions and tertiary functions and quaternary functions are used. | Primary | Positive |
| UART | | | | |
| TXD0 | O | UART0 data output pin. This pin is used as the tertiary function of the PB1 or PB4 pin. | Tertiary | Positive |
| RXD0 | I | UART0 data input pin. This pin is used as the primary function of the PB0 or PB5 or the quaternary function of the PB7 pin. | Primary | Positive |
| PWM | | | | |
| PWMC | O | PWMC output pin. This pin is used as the secondary function of the PB0 or PA0 or the quaternary function of the PB7 pin. | Secondary Quaternary | Positive |
| External interrupt | | | | |
| EXI0 to 2 | I | External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the PA0 – PA2 pins. | Primary | Positive/ negative |
| EXI4,5 | I | External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the PB0, PB1 pins. | Primary | Positive/ negative |
| Timer | | | | |
| TnTG | I | External clock input pin used for both Timer E and Timer F. These pins are used as the primary function of the PA0-PA2, PB0-PB7 pins. | Primary | — |
| TM9OUT | O | Timer 9 output pin. This pin is used as the quaternary function of the PA0 pin. | Quaternary | Positive |
| TMFOUT | O | Timer F output pin. This pin is used as the quaternary function of the PA1 pin. | Quaternary | Positive |

| Pin name | I/O | Description | Primary/ Secondary/ Tertiary/ Quaternary | Logic |
|---|-----|--|---|----------|
| Successive approximation type A/D converter | | | | |
| AIN0 | I | Channel 0 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PA0 pin. | Primary | — |
| AIN1 | I | Channel 1 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PA1 pin. | Primary | — |
| AIN2 | I | Channel 2 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PB0 pin. | Primary | — |
| AIN3 | I | Channel 3 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PB1 pin. | Primary | — |
| AIN4 | I | Channel 4 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PB6 pin. | Primary | — |
| AIN5 | I | Channel 5 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PB7 pin. | Primary | — |
| Comparator | | | | |
| CMP0P | I | Non-inverting input for comparator0. This pin is used as the primary function of the PB4 pin. | Primary | — |
| CMP0M | I | Inverting input for comparator0. This pin is used as the primary function of the PB5 pin. | Primary | — |
| CMP0OUT | O | Output for comparator0. This pin is used as the quaternary function of the PA2 pin. | Quaternary | — |
| CMP0OUT | O | Output for comparator0. This pin is used as the quaternary function of the PB2 pin. | Quaternary | — |
| CMP0OUT | O | Output for comparator0. This pin is used as the quaternary function of the PB3 pin. | Quaternary | — |
| CMP1P | I | Non-inverting input for comparator1. This pin is used as the primary function of the PA1 pin. | Primary | — |
| CMP1OUT | O | Output for comparator1. This pin is used as the quaternary function of the PB0 pin. | Quaternary | — |
| For testing | | | | |
| TEST | I/O | Input/output pin for testing. A pull-down resistor is internally connected. | — | Positive |
| Power supply | | | | |
| V _{SS} | — | Negative power supply pin. | — | — |
| V _{DD} | — | Positive power supply pin. | — | — |
| V _{PP} | — | Power supply pin for Flash ROM | — | — |

ML610Q101/ML610Q102 TERMINATION OF UNUSED PINS

Table 3 shows methods of terminating the unused pins for ML610Q101/ML610Q102.

Table 3 Termination of Unused Pins

| Pin | Recommended pin termination |
|-----------------|-----------------------------|
| RESET_N | Open |
| TEST | Open |
| PA0 to PA2 | Open |
| PB0 to PB7 | Open |
| V _{PP} | Open |

Note:

It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

| Parameter | Symbol | Condition | Rating | Unit |
|------------------------|-------------------|-----------|------------------------------|------|
| Power supply voltage 1 | V _{DD} | Ta = 25°C | -0.3 to +7.0 | V |
| Power supply voltage 2 | V _{PP} | Ta = 25°C | -0.3 to +9.5 | V |
| Input voltage | V _{IN} | Ta = 25°C | -0.3 to V _{DD} +0.3 | V |
| Output voltage | V _{OUT} | Ta = 25°C | -0.3 to V _{DD} +0.3 | V |
| Output current 1 | I _{OUT1} | Ta = 25°C | -12 to +11 | mA |
| Power dissipation | PD | Ta = 25°C | 0.5 | mW |
| Storage temperature | T _{STG} | — | -55 to +150 | °C |

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

| Parameter | Symbol | Condition | Range | Unit |
|---------------------------|-----------------|--------------------------------|-------------|------|
| Operating temperature | T _{OP} | — | -40 to +85 | °C |
| Operating voltage | V _{DD} | — | 2.7 to 5.5 | V |
| Operating frequency (CPU) | f _{OP} | V _{DD} = 2.7V to 5.5V | 30k to 8.4M | Hz |

OPERATING CONDITIONS OF FLASH MEMORY

(V_{SS}=0V)

| Parameter | Symbol | Condition | Rating | | | Unit |
|------------------------------|-----------------|----------------|--------|------|------|--------|
| | | | Min. | Typ. | Max. | |
| Operating temperature | T _{OP} | At write/erase | 0 | — | +40 | °C |
| Operating voltage | V _{DD} | At write/erase | 4.5 | — | 5.5 | V |
| | V _{PP} | At write/erase | 7.7 | — | 8.3 | |
| Rewrite counts | C _{EP} | — | — | — | 80 | cycles |
| Data retention* ¹ | Y _{DR} | — | 10 | — | — | years |

*¹ : However, please keep active time of the flash memory from exceeding ten years.

V_{pp} pin has internal pull-down resistor.

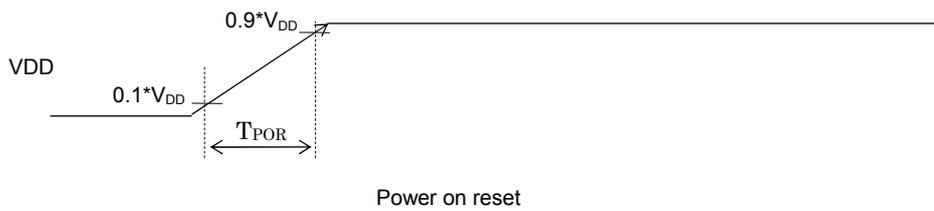
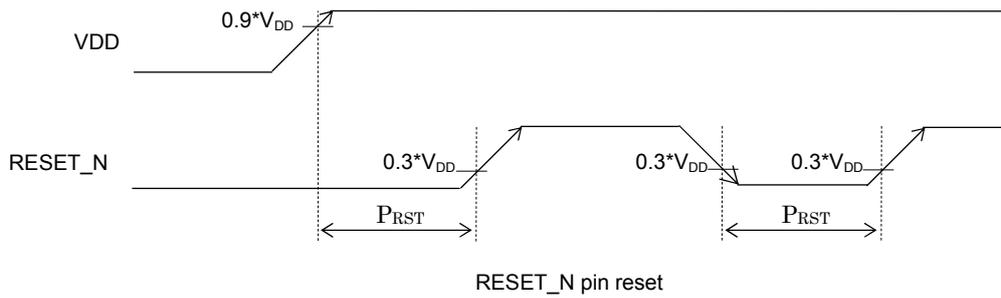
DC CHARACTERISTICS (1/4)

($V_{DD}=2.7$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $+85^{\circ}C$, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit | Measuring circuit |
|---|------------|-------------------------------|------------|--------|------------|---------|-------------------|
| | | | Min. | Typ. | Max. | | |
| Low-speed RC oscillation frequency | f_{RCL} | $T_a = 25^{\circ}C$ | 31 | 32.768 | 34 | kHz | 1 |
| PLL oscillation frequency* ¹ | f_{PLL} | $T_a = 25^{\circ}C$ | Typ. -1% | 16.384 | Typ. +1% | MHz | |
| | | $T_a = -10$ to $+85^{\circ}C$ | Typ. -2% | 16.384 | Typ. +2% | | |
| | | $T_a = -40$ to $+85^{\circ}C$ | Typ. -2.5% | 16.384 | Typ. +2.5% | | |
| Reset pulse width | T_{RST} | — | 100 | — | — | μs | |
| Reset noise elimination pulse width | T_{NRST} | — | — | — | 0.4 | | |
| Power-on reset activation power rise time | T_{POR} | — | — | — | 10 | ms | |

*¹ : 1024 clock average. CPU clk is $f_{PLL} / 2$ max.

RESET



DC CHARACTERISTICS (2/4)

(V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | | Rating | | | Unit | Measuring circuit |
|--|--------------------|--|-----------------|-------------------|-------|-------------------------|------|-------------------|
| | | | | Min. | Typ. | Max. | | |
| VLS Judgment voltage | V _{VLS0F} | Ta=25°C, V _{DD} =fall | | Typ. -3.0 % | 2.85 | Typ. +3.0 % | V | 1 |
| | | V _{DD} =fall | | Typ. -5.0 % | 2.85 | Typ. +5.0 % | | |
| | V _{VLS0R} | Ta=25°C, V _{DD} =rise | | Typ. -3.0 % | 2.92 | Typ. +3.0 % | | |
| | | V _{DD} =rise | | Typ. -5.0 % | 2.92 | Typ. +5.0 % | | |
| | V _{VLS1} | Ta=25°C | VLS0=0 | Typ. -3.0 % | 3.295 | Typ. +3.0 % | | |
| | | | VLS0=1 | | 3.625 | | | |
| | | — | VLS0=0 | Typ. -5.0 % | 3.295 | Typ. +5.0 % | | |
| | | | VLS0=1 | | 3.625 | | | |
| Comparator0 In-phase input voltage range | V _{CMR} | — | | 0.1 | — | V _{DD} -1.5 | V | |
| Comparator0 hysteresis | V _{HYSF} | Ta=25°C, V _{DD} = 5.0V | | 10 | 20 | 30 | mV | 4 |
| | | V _{DD} = 5.0V | | 5 | 20 | 35 | | |
| Comparator0 Input offset voltage | V _{CMOF} | Ta=25°C, V _{DD} = 5.0V | | — | — | 7 | | |
| Comparator Reference-voltage error* ³ | V _{CMREF} | Ta=25°C | | -25 | — | 25 | | |
| | | — | | -50 | — | 50 | | |
| Supply current 1 | IDD1 | CPU: In STOP state. Low-speed/high-speed oscillation: stopped. | Ta=-40 to +85°C | — | 1 | 30 | μA | 1 |
| Supply current 2 | IDD2 | CPU: In 32.768kHz operating state.* ¹ High-speed oscillation: Stopped. | Ta=-40 to +85°C | — | 3.7 | 6 | mA | |

*¹: LTBC and WDT are operating, and significant bits of BLKCON0 to BLKCON4 registers are all "1".*²: When the CPU operating rate is 100%. Minimum instruction execution time: Approx 0.122 μs (at 8.192MHz system clock)*³: Comparator input offset voltage is included.

DC CHARACTERISTICS (3/4)

(V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit | Measuring circuit |
|---|--------|--|-------------------------|------|------|------|-------------------|
| | | | Min. | Typ. | Max. | | |
| Output voltage | VOH | IOH1 = -3.0mA, V _{DD} = 4.5V *1 | V _{DD} -0.7 | — | — | V | 2 |
| | VOL | IOL1 = +8.5mA, V _{DD} = 4.5V *1 | — | — | 0.6 | | |
| Output leakage | IOOH | VOH = V _{DD} (in high-impedance state) | — | — | +1 | μA | 3 |
| | IOOL | VOL = V _{SS} (in high-impedance state) | -1 | — | — | | |
| Input current 1 (RESET_N) | IIH1 | VIH1 = V _{DD} | — | — | 1 | μA | 4 |
| | IIL1 | VIL1 = V _{SS} , V _{DD} = 5.0V | -650 | -500 | -350 | | |
| Input current 1 (TEST) | IIH1 | VIH1 = V _{DD} = 5.0V | 20 | 115 | 200 | | |
| | IIL1 | VIL1 = V _{SS} | -1 | — | — | | |
| Input current 2 (PA0-PA2) (PB0-PB7) | IIH2 | VIH2 = V _{DD} = 5.0V (when pulled-down) | 20 | 115 | 200 | | |
| | IIL2 | VIL2 = V _{SS} , V _{DD} =5.0V (when pulled-up) | -200 | -100 | -20 | | |

*1 : When the one terminal output state.

DC CHARACTERISTICS (4/4)

(V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

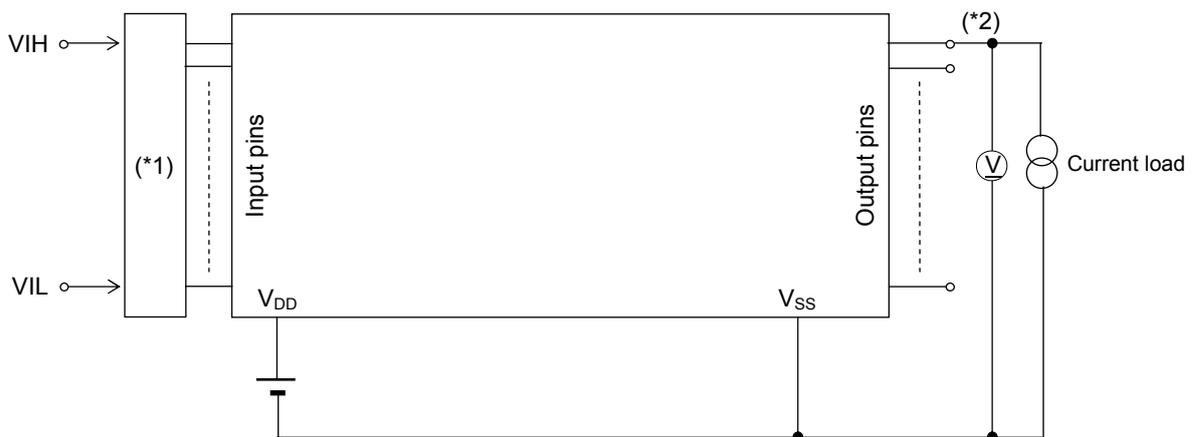
| Parameter | Symbol | Condition | Rating | | | Unit | Measuring circuit |
|---|--------|------------------------|-------------------------|------|-------------------------|------|-------------------|
| | | | Min. | Typ. | Max. | | |
| Input voltage 1 (RESET_N) (TEST) (PA0 to PA2) (PB0, to PB7) | VIH1 | — | 0.7 ×V _{DD} | — | V _{DD} | V | 2 |
| | VIL1 | — | 0 | — | 0.3 ×V _{DD} | | |
| Input pin capacitance (PA0 to PA2) (PB0 to PB7) | CIN | f = 10kHz Ta = 25°C | — | — | 20 | pF | — |

MEASURING CIRCUITS

MEASURING CIRCUIT 1



MEASURING CIRCUIT 2



- *1: Input logic circuit to determine the specified measuring conditions.
- *2: Measured at the specified output pins.

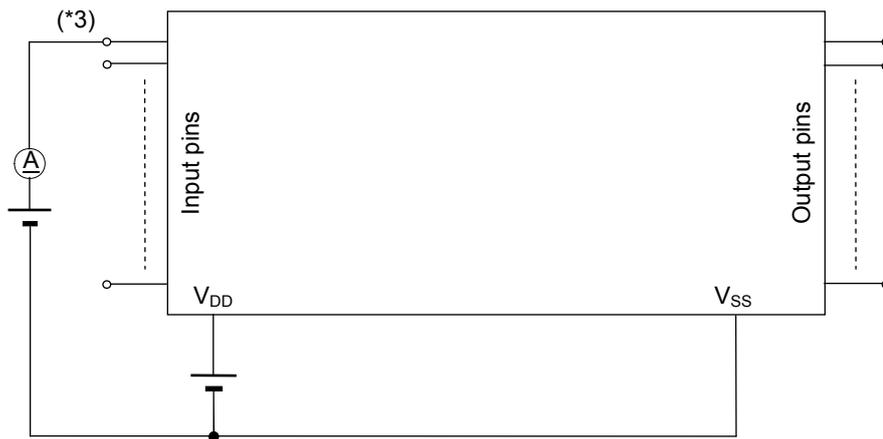
MEASURING CIRCUIT 3



*1: Input logic circuit to determine the specified measuring conditions.

*2: Measured at the specified output pins.

MEASURING CIRCUIT 4

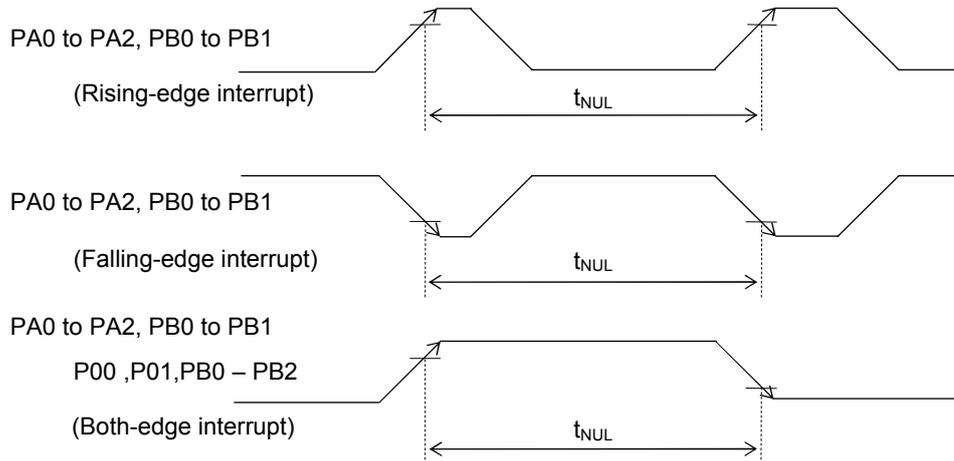


*3: Measured at the specified output pins.

AC CHARACTERISTICS (External Interrupt)

(V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit |
|-----------------------------------|------------------|--|-----------------|------|-----------------|------|
| | | | Min. | Typ. | Max. | |
| External interrupt disable period | T _{NUL} | Interrupt: Enabled (MIE = 1), CPU: NOP operation System clock: 32.768kHz | 2.5 x sysclk | — | 3.5 x sysclk | μs |

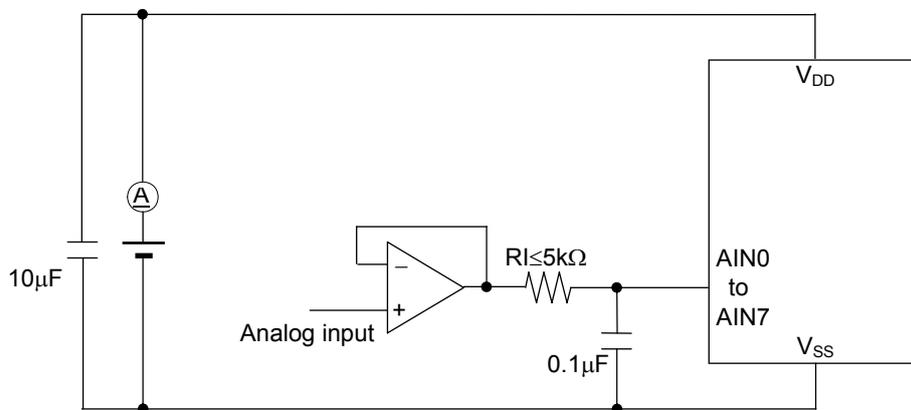


Electrical Characteristics of Successive Approximation Type A/D Converter

($V_{DD}=2.7$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $+85^{\circ}C$, unless otherwise specified)

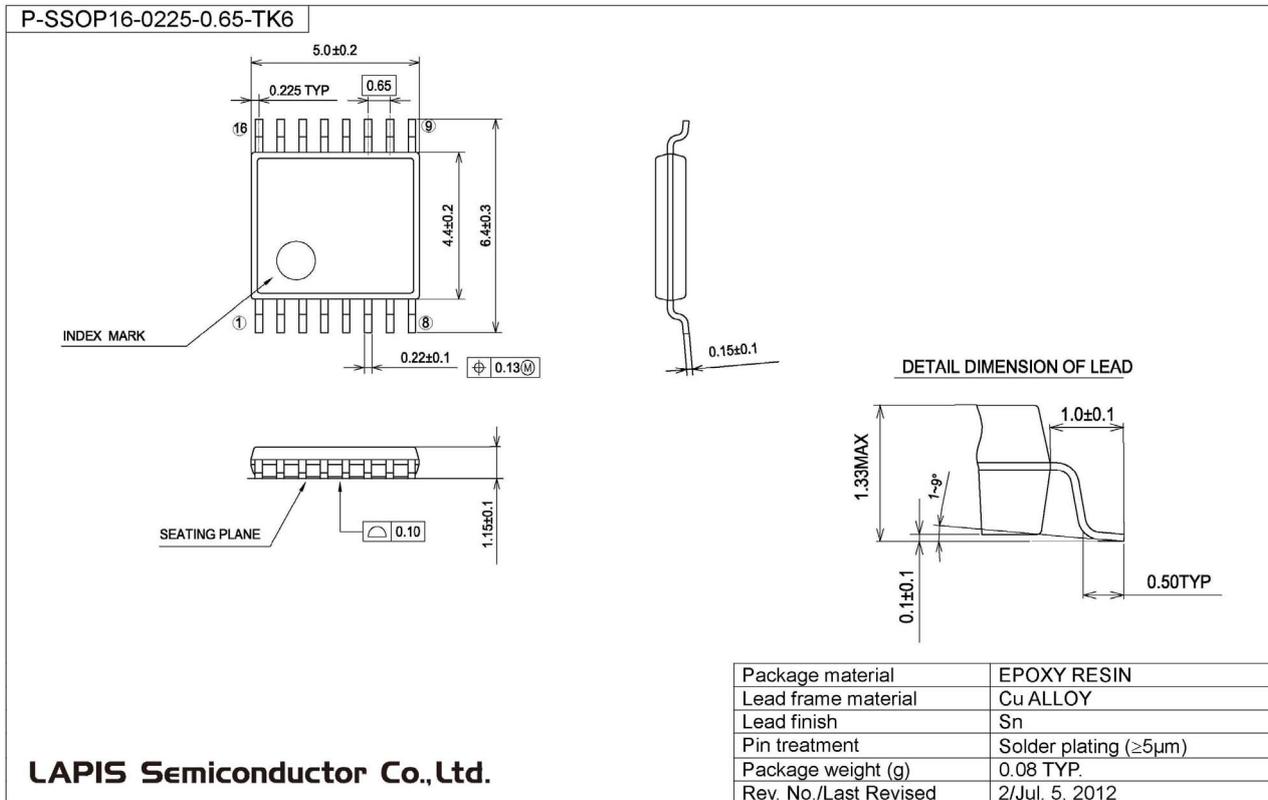
| Parameter | Symbol | Condition | Rating | | | Unit |
|----------------------------------|------------|--------------------------------------|--------|------|------|-----------|
| | | | Min. | Typ. | Max. | |
| Resolution | n | — | — | — | 10 | bit |
| Integral non-linearity error | INL | $R_I \leq 5k\Omega$, HSCLK=8.192MHz | -4 | — | +4 | LSB |
| Differential non-linearity error | DNL | $R_I \leq 5k\Omega$, HSCLK=8.192MHz | -3 | — | +3 | |
| Zero-scale error | V_{OFF} | $R_I \leq 5k\Omega$, HSCLK=8.192MHz | -4 | — | +4 | |
| Full-scale error | FSE | $R_I \leq 5k\Omega$, HSCLK=8.192MHz | -4 | — | +4 | |
| Conversion time | t_{CONV} | — | — | 102 | — | ϕ/CH |

ϕ : $f_{PLL}/4$



PACKAGE DIMENSIONS

(Unit: mm)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

| Document No. | Date | Page | | Description |
|---------------|-------------|------------------|-----------------|-----------------|
| | | Previous Edition | Current Edition | |
| FEDL610Q101-1 | Jan,23,2013 | - | - | Final edition 1 |

NOTES

No copying or reproduction of this document, in part or in whole, is permitted without the consent of LAPIS Semiconductor Co., Ltd.

The content specified herein is subject to change for improvement without notice.

The content specified herein is for the purpose of introducing LAPIS Semiconductor's products (hereinafter "Products"). If you wish to use any such Product, please be sure to refer to the specifications, which can be obtained from LAPIS Semiconductor upon request.

Examples of application circuits, circuit constants and any other information contained herein illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

Great care was taken in ensuring the accuracy of the information specified in this document. However, should you incur any damage arising from any inaccuracy or misprint of such information, LAPIS Semiconductor shall bear no responsibility for such damage.

The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. LAPIS Semiconductor does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by LAPIS Semiconductor and other parties. LAPIS Semiconductor shall bear no responsibility whatsoever for any dispute arising from the use of such technical information.

The Products specified in this document are intended to be used with general-use electronic equipment or devices (such as audio visual equipment, office-automation equipment, communication devices, electronic appliances and amusement devices).

The Products specified in this document are not designed to be radiation tolerant.

While LAPIS Semiconductor always makes efforts to enhance the quality and reliability of its Products, a Product may fail or malfunction for a variety of reasons.

Please be sure to implement in your equipment using the Products safety measures to guard against the possibility of physical injury, fire or any other damage caused in the event of the failure of any Product, such as derating, redundancy, fire control and fail-safe designs. LAPIS Semiconductor shall bear no responsibility whatsoever for your use of any Product outside of the prescribed scope or not in accordance with the instruction manual.

The Products are not designed or manufactured to be used with any equipment, device or system which requires an extremely high level of reliability the failure or malfunction of which may result in a direct threat to human life or create a risk of human injury (such as a medical instrument, transportation equipment, aerospace machinery, nuclear-reactor controller, fuel-controller or other safety device). LAPIS Semiconductor shall bear no responsibility in any way for use of any of the Products for the above special purposes. If a Product is intended to be used for any such special purpose, please contact a ROHM sales representative before purchasing.

If you intend to export or ship overseas any Product or technology specified herein that may be controlled under the Foreign Exchange and the Foreign Trade Law, you will be required to obtain a license or permit under the Law.

Copyright 2013 LAPIS Semiconductor Co., Ltd.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[ROHM Semiconductor:](#)

[ML610Q101-NNNMBZ0ATL](#) [ML610Q102-NNNMBZ0ATL](#) [ML610Q101-NNNGDZ0ANL](#) [ML610Q102-NNNGDZ0ANL](#)
[ML610Q102 reference board](#)

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

moschip.ru_4

moschip.ru_6

moschip.ru_9