# **BUK9875-100A**

# N-channel TrenchMOS logic level FET

19 March 2014

**Product data sheet** 

## 1. General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

#### 2. Features and benefits

- Low conduction losses due to low on-state resistance
- Q101 compliant
- Suitable for logic level gate drive sources

## 3. Applications

- 12 V, 24 V and 42 V loads
- Automotive and general purpose power switching
- Motors, lamps and solenoids

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 150 °C	-	-	100	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 5 V; T <sub>sp</sub> = 25 °C; <u>Fig. 2</u> ; <u>Fig. 3</u>	-	-	7	Α
P <sub>tot</sub>	total power dissipation	T <sub>sp</sub> = 25 °C; <u>Fig. 1</u>	-	-	8	W
Static charact	eristics					
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS}$ = 4.5 V; $I_{D}$ = 8 A; $T_{j}$ = 25 °C	-	-	84	mΩ
		$V_{GS}$ = 10 V; $I_D$ = 8 A; $T_j$ = 25 °C	-	62	72	mΩ
		$V_{GS} = 5 \text{ V}; I_D = 8 \text{ A}; T_j = 25 ^{\circ}\text{C}; Fig. 12;$ Fig. 13	-	64	75	mΩ
Avalanche rug	ggedness					
E <sub>DS(AL)S</sub>	non-repetitive drain- source avalanche energy	$I_D$ = 7 A; $V_{sup} \le 100$ V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 5 V; $T_{j(init)}$ = 25 °C; unclamped	-	-	49	mJ



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## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	4	D I
2	D	drain		
3	S	source		G UNA
4	D	drain	⊟1 ⊟2 ⊟3 SC-73 (SOT223)	mbb076 S

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9875-100A	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223
BUK9875-100A/CU	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

# 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9875-100A	987510A
BUK9875-100A/CU	987510

# 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 150 °C	-	100	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	100	V
V <sub>GS</sub>	gate-source voltage		-10	10	V
P <sub>tot</sub>	total power dissipation	T <sub>sp</sub> = 25 °C; <u>Fig. 1</u>	-	8	W
I <sub>D</sub>	drain current	T <sub>sp</sub> = 25 °C; V <sub>GS</sub> = 5 V; <u>Fig. 2</u> ; <u>Fig. 3</u>	-	7	Α
		T <sub>sp</sub> = 100 °C; V <sub>GS</sub> = 5 V; <u>Fig. 2</u>	-	4	Α
I <sub>DM</sub>	peak drain current	$T_{sp}$ = 25 °C; pulsed; $t_p \le 10$ μs; Fig. 3	-	28	Α

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Symbol	Parameter	Conditions	Min	Max	Unit
T <sub>stg</sub>	storage temperature		-55	150	°C
T <sub>j</sub>	junction temperature		-55	150	°C
$V_{GSM}$	peak gate-source voltage	pulsed; $t_p \le 50 \mu s$	-15	15	V
Source-drain	n diode				-
I <sub>S</sub>	source current	$T_{sp} = 25 ^{\circ}C$	-	7	Α
I <sub>SM</sub>	peak source current	pulsed; $t_p \le 10 \ \mu s$ ; $T_{sp} = 25 \ ^{\circ}C$	-	28	Α
Avalanche re	uggedness				
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$I_D$ = 7 A; $V_{sup} \le 100$ V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 5 V; $T_{j(init)}$ = 25 °C; unclamped	-	49	mJ

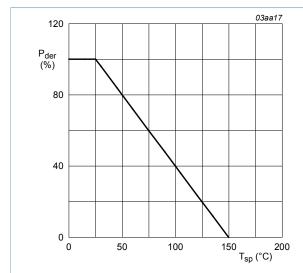


Fig. 1. Normalized total power dissipation as a function of solder point temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100 \,\%$$

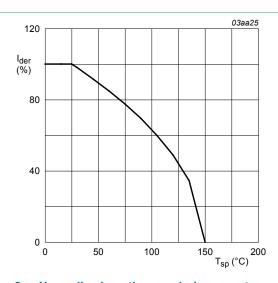


Fig. 2. Normalized continuous drain current as a function of solder point temperature

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$

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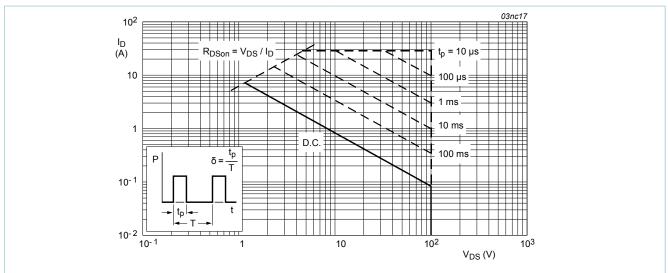


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$$T_{amb} = 25^{\circ}C; I_{DM}$$
 is single pulse

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-sp)</sub>	thermal resistance from junction to solder point		-	-	15	K/W
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	Fig. 4	-	120	-	K/W

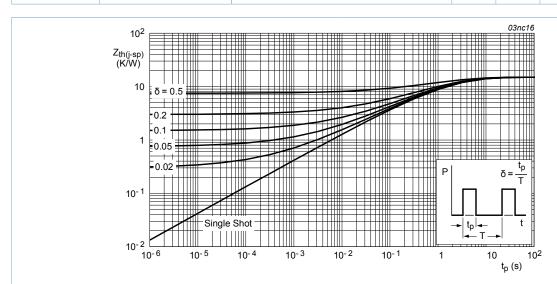


Fig. 4. Transient thermal impedance from junction to solder point as a function of pulse duration

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## 10. Characteristics

Table 7 Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics		'			
V <sub>(BR)DSS</sub>	drain-source	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	100	-	-	V
breakdown vo	breakdown voltage	I <sub>D</sub> = 0.25 mA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = -55 °C	89	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C};$ Fig. 11	1	1.5	2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C};$ Fig. 11	-	-	2.3	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ °C};$ Fig. 11	0.6	-	-	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 100 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	0.05	10	μΑ
		V <sub>DS</sub> = 100 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 150 °C	-	-	500	μΑ
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 10 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
		V <sub>GS</sub> = -10 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 8 A; T <sub>j</sub> = 150 °C; Fig. 12; Fig. 13	-	-	162	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 8 A; T <sub>j</sub> = 25 °C	-	-	84	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 8 A; T <sub>j</sub> = 25 °C	-	62	72	mΩ
		V <sub>GS</sub> = 5 V; I <sub>D</sub> = 8 A; T <sub>j</sub> = 25 °C; <u>Fig. 12</u> ; <u>Fig. 13</u>	-	64	75	mΩ
Dynamic ch	naracteristics		'			
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz;	-	1270	1690	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; <u>Fig. 14</u>	-	140	167	pF
C <sub>rss</sub>	reverse transfer capacitance		-	90	124	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \Omega; V_{GS} = 5 \text{ V};$	-	13	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 10 \Omega; T_j = 25 °C$	-	120	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	58	-	ns
t <sub>f</sub>	fall time		-	57	-	ns
Source-drai	in diode		'	1		-1
V <sub>SD</sub>	source-drain voltage	$I_S = 5 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}; Fig. 15$	-	0.85	1.2	V
					+	
t <sub>rr</sub>	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s};$ $V_{GS} = -10 \text{ V}; V_{DS} = 30 \text{ V}; T_i = 25 ^{\circ}\text{C}$	-	63	-	ns

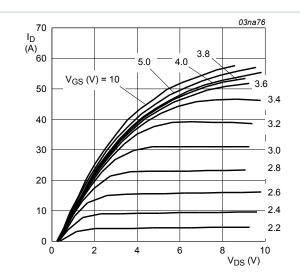


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values



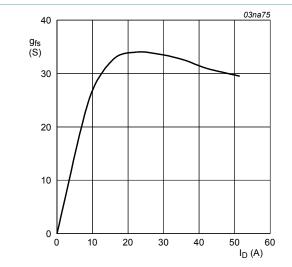


Fig. 7. Forward transconductance as a function of drain current; typical values

$$T_j=25^{\circ}C; V_{DS}=25V$$

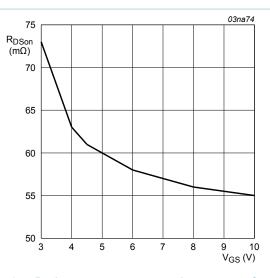
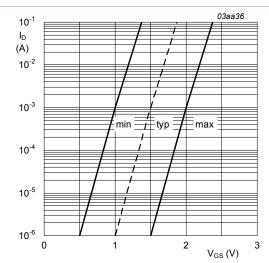


Fig. 6. Drain-source on-state resistance as a function of gate-source; typical values

$$T_j=25^{\circ}C; I_D=8A$$



 $T_i$  = 25 °C;  $V_{DS}$  = 5 V

Fig. 8. Sub-threshold drain current as a function of gate-source voltage

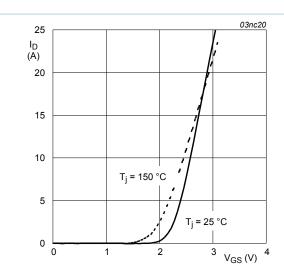


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values



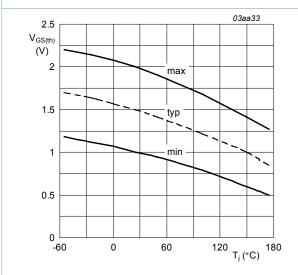


Fig. 11. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1 mA; V_{DS} = V_{GS}$$

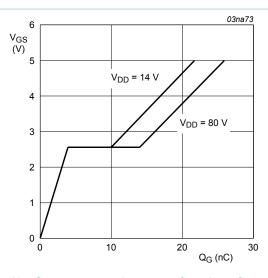


Fig. 10. Gate-source voltage as a function of turn-on gate charge; typical values

$$T_j = 25^{\circ}C; I_D = 20A$$

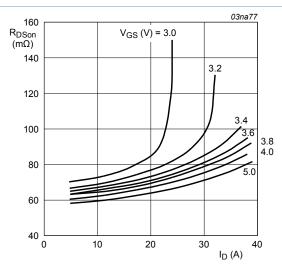


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^{\circ}C$$

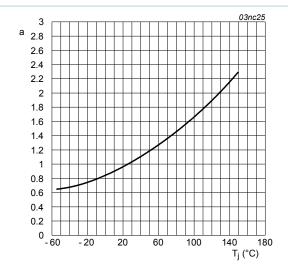


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

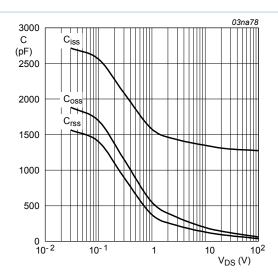


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0V; f = 1MHz$$

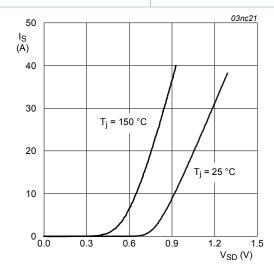
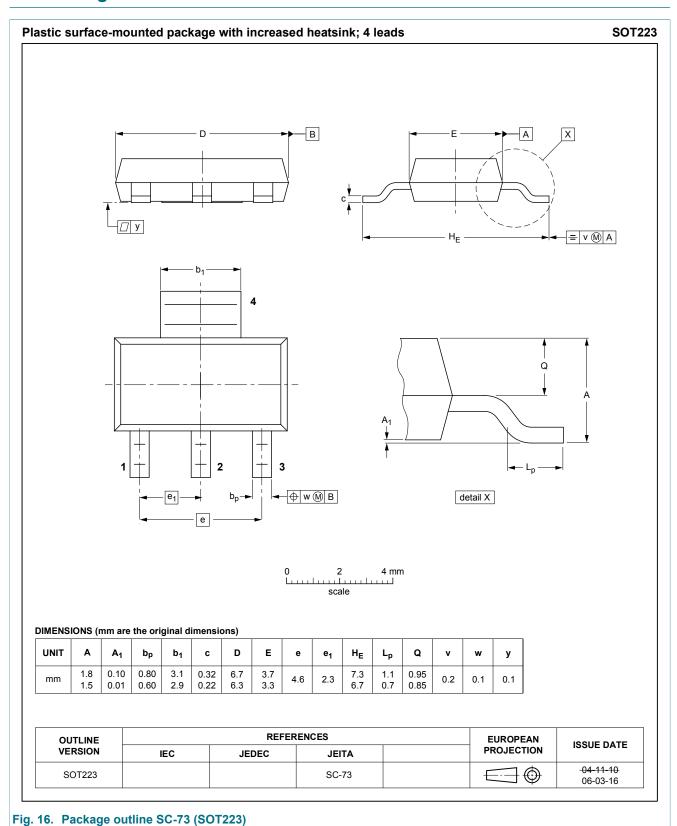


Fig. 15. Reverse diode current as a function of reverse diode voltage;typical value

$$V_{GS} = 0V$$

## 11. Package outline



#### N-channel TrenchMOS logic level FET

## 12. Legal information

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