

CMOS Digital Integrated Circuit Silicon Monolithic

TC358768AXBG/TC358778XBG

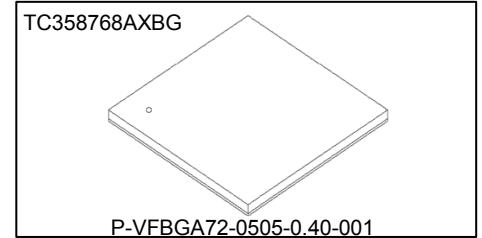
Mobile Peripheral Devices

Overview

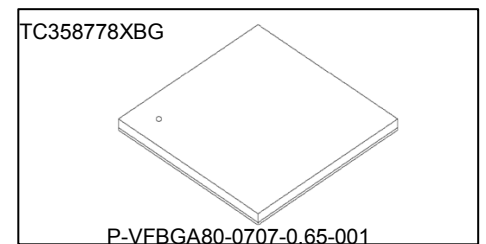
Parallel Port to MIPI® DSI (TC358768AXBG/TC358778XBG) is a bridge device that converts RGB to DSI. All internal registers can be access through I²C or SPI.

Features

- DSI-TX Interface
 - ✧ MIPI® DSI compliant (Version 1.02.00– June 28, 2010)
 - Support DSI Video Mode data transfer
 - DCS Command for panel register access
 - ✧ Supports up to 1 Gbps per data lane
 - ✧ Supports 1, 2, 3 or 4 data lanes
 - ✧ Supports video data formats
 - RGB888/666/565
- RGB Interface
 - ✧ Supports data formats
 - 24-bit data bus
 - RGB888/666/565 data formats
 - ✧ Up to 166 MHz input clock
 - ✧ Support VSYNC/HSYNC polarity option (default LOW)
 - ✧ Support DE polarity option (default High)
- I²C/SPI Slave Interface (Option to select either I²C or SPI interface)
 - ✧ I²C Interface (when CS=L)
 - Support for normal (100KHz), fast mode (400 kHz) and Special mode (1 MHz)
 - Configure all TC358768AXBG/TC358778XBG internal registers
 - Writing to DCS registers will trigger DCS Command transmits over DSI
 - ✧ SPI interface (when CS=H)
 - SPI interface support for up to 25 MHz operation.
 - Configure all TC358768AXBG/TC358778XBG internal registers
 - Writing to DCS registers will trigger DCS Command transmits over DSI
- GPIO signals
 - ✧ 2 GPIO signals
 - Two GPIO signals can be configured as SPI signals (SPI_SS and SPI_MISO)
 - Or One GPIO signal can be configured as Interrupt output signal, INT.
- System
 - ✧ Clock and power management support to achieve low power states.
- Power supply inputs
 - ✧ Core and MIPI® D-PHY: 1.2V
 - ✧ I/O: 1.8V – 3.3V
- Typical Power Consumption
 - ✧ WXGA @60fps: Pixel Clk: 74.25 MHz, DSIClk: 312 MHz → 66.7 mW
 - ✧ 1080P @60fps: Pixel Clk: 148.5 MHz, DSIClk: 471 MHz → 91.4 mW
 - ✧ Power Down Condition is achieved by turning off clock sources: PClk and RefClk.



Weight: 32.0 mg (Typ.)



Weight: 66.1 mg (Typ.)

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1. MIPI DSI, "mipi_DSI_specification_v01-02-00, June 28, 2010"
2. MIPI DCS "DRAFT mipi_DCS_specification_v01-02-00_r0-02, December 2008"
3. MIPI D-PHY, "mipi_D-PHY_specification_v01-00-00, May 14, 2009"
4. I²C bus specification, version 2.1, January 2000, Philips Semiconductor

1. Overview

The Parallel Port to MIPI® DSI (TC358768AXBG/TC358778XBG) is a bridge device that converts RGB to DSI. All internal registers can be access through I²C or SPI.

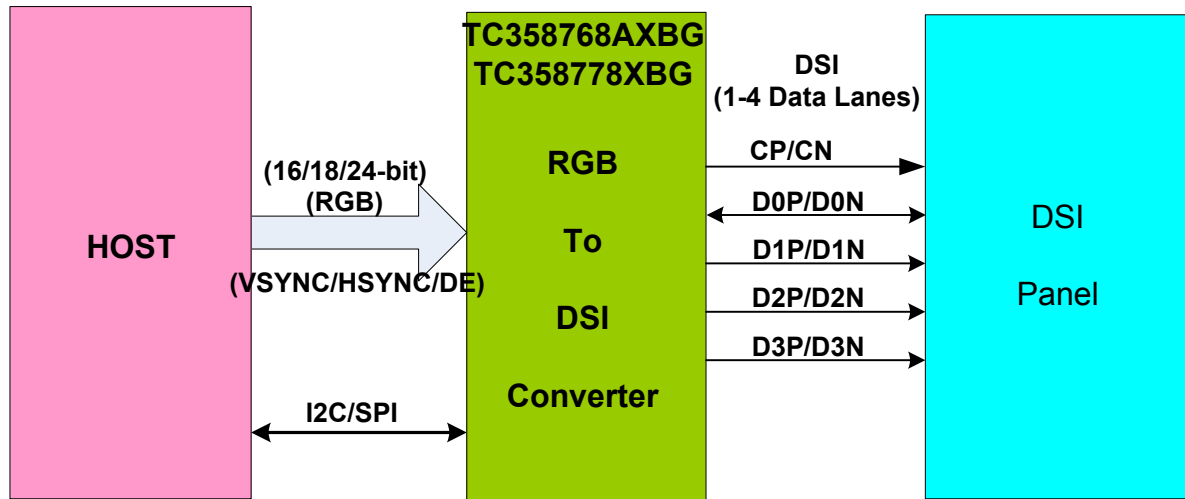


Figure 1.1 System Overview with TC358768AXBG/TC358778XBG in RGB to DSI-TX

2. Features

Below are the main features supported by TC358768AXBG/TC358778XBG.

- DSI-TX Interface
 - ✧ MIPI® DSI compliant (Version 1.02.00– June 28, 2010)
 - Support DSI Video Mode data transfer
 - DCS Command for panel register access
 - ✧ Supports up to 1 Gbps per data lane
 - ✧ Supports 1, 2, 3 or 4 data lanes
 - ✧ Supports video data formats
 - RGB888/666/565
- RGB Interface
 - ✧ Supports data formats
 - 24-bit data bus
 - RGB888/666/565 data formats
 - ✧ Up to 166 MHz input clock
 - ✧ Support VSYNC/HSYNC polarity option (default LOW)
 - ✧ Support DE polarity option (default High)
- I²C/SPI Slave Interface (Option to select either I²C or SPI interface)
 - ✧ I²C Interface (when CS=L)
 - Support for normal (100 kHz), fast mode (400 kHz) and Special mode (1 MHz)
 - Configure all TC358768AXBG/TC358778XBG internal registers
 - Writing to DCS registers will trigger DCS Command transmits over DSI
 - ✧ SPI interface (when CS =H)
 - SPI interface support for up to 25 MHz operation.
 - Configure all TC358768AXBG/TC358778XBG internal registers
 - Writing to DCS registers will trigger DCS Command transmits over DSI
- GPIO signals
 - ✧ 2 GPIO signals
 - Two GPIO signals can be configured as SPI signals (SPI_SS and SPI_MISO)
 - Or One GPIO signal can be configured as Interrupt output signal, INT.
- System
 - ✧ Clock and power management support to achieve low power states.
- Power supply inputs
 - ✧ Core and MIPI® D-PHY: 1.2 V
 - ✧ I/O: 1.8 V to 3.3 V

- Typical Power Consumption

- ✧ WXGA @60fps: Pixel Clk: 74.25 MHz, DSIClk: 312 MHz → 66.7 mW
- ✧ 1080P @60fps: Pixel Clk: 148.5 MHz, DSIClk: 471 MHz → 91.4 mW

	VDDC	VDDIO	VDDMIPI	Total Power	
	1.2 V	3.3 V	1.2 V		
1080P Video	42.8 mA	0.4 mA	32.3 mA	91.44	mW
	51.36 mW	1.32 mW	38.76 mW		
WXGA Video	34.71 mA	0.167 mA	20.36 mA	66.64	mW
	41.652 mW	0.551 mW	24.432 mW		
Power Down w/o PCLK, RefClk	0.074 mA	0.025 mA	0.004 mA	176.1	μW
	0.089 mW	0.0825 mW	0.0048 mW		

- ✧ Power Down Condition is achieved by turning off clock sources: PClk and RefClk.

3. External Pins

3.1. TC358768AXBG pinout description

TC358768AXBG resides in BGA72 pin packages. The following table gives the signals of TC358768AXBG and their function.

Table 3.1 TC358768AXBG Functional Signal List

Group	Pin Name	I/O	Type	Function	Note
System: Reset & Clock (4)	RESX	I	Sch	System reset input, active low	
	REFCLK	I	N	Reference clock input (6MHz - 40MHz)	
	MSEL	I	N	Mode Select 1'b0: Test mode 1'b1: Normal mode	
	CS	I	N	Configuration Select - When CS=L, enable I ² C interface - When CS=H, enable SPI interface	
MIPI-DSI (10)	MIPI_CP		PHY	MIPI-DSI clock positive	
	MIPI_CN		PHY	MIPI-DSI clock negative	
	MIPI_D0P		PHY	MIPI-DSI Data 0 positive	
	MIPI_D0N		PHY	MIPI-DSI Data 0 negative	
	MIPI_D1P		PHY	MIPI-DSI Data 1 positive	
	MIPI_D1N		PHY	MIPI-DSI Data 1 negative	
	MIPI_D2P		PHY	MIPI-DSI Data 2 positive	
	MIPI_D2N		PHY	MIPI-DSI Data 2 negative	
	MIPI_D3P		PHY	MIPI-DSI Data 3 positive	
	MIPI_D3N		PHY	MIPI-DSI Data 3 negative	
I2C (2)	I2C_SCL	OD	Sch	I ² C serial clock or SPI_SCLK	4 mA
	I2C_SDA	OD	Sch	I ² C serial data or SPI_MOSI	4 mA
Parallel Port IF (28)	PD[23:0]	I	N	Parallel Port Input Data Note: PD[23:16] can be configure to be GPIO[10:3]	
	VSYNC	I	N	Parallel port VSYNC signal	
	HSYNC	I	N	Parallel port HSYNC signal	
	DE	I	N	Parallel Port DE signal	
	PCLK	I	N	Parallel Port Clock signal	
GPIO (2)	GPIO[2:1]	I/O	N	GPIO[2:1] signals - (GPIO[1] option to become SPI_SS or INT signal) - (GPIO[2] option to become SPI_MISO signal)	4 mA
POWER (9)	VDDC (1.2 V)	NA		VDD for Internal Core (3)	
	VDDIO (1.8 V-3.3 V)	NA		VDDIO is for IO power supply (4)	
	VDD_MIPI (1.2 V)	NA		VDD for the MIPI (2)	
GROUND (17)	VSS	NA		Ground	

3.2. TC358768AXBG BGA72 Pin Count Summary

Table 3.2 TC358768AXBG BGA 72 Pin Count Summary

Group Name	Pin Count	Notes
SYSTEM	4	
MIPI-DSI	10	
I2C IF	2	
GPIO	2	
Parallel Port IF	28	
POWER	9	IO, MIPI and Core Power
GROUND	17	
TOTAL	72	

3.3. TC358778XBG pinout description

TC358778XBG resides in BGA80 pin packages. The following table gives the signals of TC358778XBG and their function.

Table 3.3 TC358778XBG Functional Signal List

Group	Pin Name	I/O	Type	Function	Note
System: Reset & Clock (4)	RESX	I	Sch	System reset input, active low	
	REFCLK	I	N	Reference clock input (6MHz - 40MHz)	
	MSEL	I	N	Mode Select 1'b0: Test mode 1'b1: Normal mode	
	CS	I	N	Configuration Select - When CS=L, enable I ² C interface - When CS=H, enable SPI interface	
MIPI-DSI (10)	MIPI_CP		PHY	MIPI-DSI clock positive	
	MIPI_CN		PHY	MIPI-DSI clock negative	
	MIPI_D0P		PHY	MIPI-DSI Data 0 positive	
	MIPI_D0N		PHY	MIPI-DSI Data 0 negative	
	MIPI_D1P		PHY	MIPI-DSI Data 1 positive	
	MIPI_D1N		PHY	MIPI-DSI Data 1 negative	
	MIPI_D2P		PHY	MIPI-DSI Data 2positive	
	MIPI_D2N		PHY	MIPI-DSI Data 2negative	
	MIPI_D3P		PHY	MIPI-DSI Data 3positive	
	MIPI_D3N		PHY	MIPI-DSI Data 3 negative	
I2C IF (2)	I2C_SCL	OD	Sch	I ² C serial clock or SPI_SCLK	4 mA
	I2C_SDA	OD	Sch	I ² C serial data or SPI_MOSI	4 mA
Parallel Port IF (28)	PD[23:0]	I	N	Parallel Port Input Data Note: PD[23:16] can be configure to be GPIO[10:3]	
	VSYNC	I	N	Parallel port VSYNC signal	
	HSYNC	I	N	Parallel port HSYNC signal	
	DE	I	N	Parallel Port DE signal	
	PCLK	I	N	Parallel Port Clock signal	
GPIO (2)	GPIO[2:1]	I/O	N	GPIO[2:1] signals - (GPIO[1] option to become SPI_SSor INT signal) - (GPIO[2] option to become SPI_MISO signal)	4 mA
POWER (9)	VDDC (1.2V)	NA		VDD for Internal Core (3)	
	VDDIO (1.8V - 3.3V)	NA		VDDIO is for IO power supply (4)	
	VDD_MIPI (1.2V)	NA		VDD for the MIPI (2)	
GROUND (25)	VSS	NA		Ground	

3.4. TC358778XBG BGA80 Pin Count Summary

Table 3.4 TC358778XBG BGA 80 Pin Count Summary

Group Name	Pin Count	Notes
SYSTEM	4	
MIPI-DSI	10	
I2C IF	2	
GPIO	2	
Parallel Port IF	28	
POWER	9	IO, MIPI and Core Power
GROUND	25	
TOTAL	80	

3.5. TC358768AXBG Pin Layout

A1 VSS	A2 PD17	A3 PD19	A4 PD21	A5 PD23	A6 GPIO2	A7 I2C_SCL	A8 MSEL	A9 VSS
B1 VDDC	B2 PD16	B3 PD18	B4 PD20	B5 PD22	B6 GPIO1	B7 I2C_SDA	B8 RESX	B9 VDDIO
C1 PD15	C2 PD14	C3 VSS	C4 VSS	C5 VSS	C6 VSS	C7 VDD_MIPI	C8 MIPI_D3P	C9 MIPI_D3N
D1 PD13	D2 PD12	D3 VSS				D7 VSS	D8 MIPI_D2P	D9 MIPI_D2N
E1 VSS	E2 VSS	E3 VDDC				E7 VDD_MIPI	E8 MIPI_CP	E9 MIPI_CN
F1 VSS	F2 VSS	F3 VSS				F7 VSS	F8 MIPI_D1P	F9 MIPI_D1N
G1 PD11	G2 PD10	G3 VDDIO	G4 VSS	G5 VSS	G6 VDDIO	G7 VDDIO	G8 MIPI_D0P	G9 MIPI_D0N
H1 VDDC	H2 PD8	H3 PD6	H4 PD4	H5 PD2	H6 PD0	H7 PCLK	H8 DE	H9 CS
J1 VSS	J2 PD9	J3 PD7	J4 PD5	J5 PD3	J6 PD1	J7 REFCLK	J8 VSYNC	J9 HSYNC

Figure 3.1 TC358768AXBG 72-Pin Layout (Top View)

3.6. TC358778XBG Pin Layout

A1 VSS	A2 PD17	A3 PD19	A4 PD21	A5 PD23	A6 GPIO2	A7 VDDC	A8 I2C_SCL	A9 MSEL	A10 VSS
B1 VDDC	B2 PD16	B3 PD18	B4 PD20	B5 PD22	B6 GPIO1	B7 VSS	B8 I2C_SDA	B9 RESX	B10 VDDIO
C1 PD15	C2 PD14	C3	C4	C5	C6	C7	C8	C9 MIPI_D3P	C10 MIPI_D3N
D1 PD13	D2 PD12	D3	D4 VSS	D5 VSS	D6 VSS	D7 VSS	D8	D9 MIPI_D2P	D10 MIPI_D2N
E1 PD11	E2 PD10	E3	E4 VSS	E5 VSS	E6 VSS	E7 VSS	E8	E9 VSS	E10 VDD_MIPI
F1 PD9	F2 PD8	F3	F4 VSS	F5 VSS	F6 VSS	F7 VSS	F8	F9 MIPI_CP	F10 MIPI_CN
G1 PD7	G2 PD6	G3	G4 VSS	G5 VSS	G6 VSS	G7 VSS	G8	G9 MIPI_D1P	G10 MIPI_D1N
H1 VDDIO	H2 VSS	H3	H4	H5	H6	H7	H8	H9 VSS	H10 VDD_MIPI
J1 PD4	J2 PD2	J3 PD0	J4 VSS	J5 VSS	J6 PCLK	J7 DE	J8 CS	J9 MIPI_D0P	J10 MIPI_D0N
K1 PD5	K2 PD3	K3 PD1	K4 VDDC	K5 VDDIO	K6 REFCLK	K7 VSYNC	K8 HSYNC	K9 VDDIO	K10 VSS

Figure 3.2 TC358778XBG 80-Pin Layout (Top View)

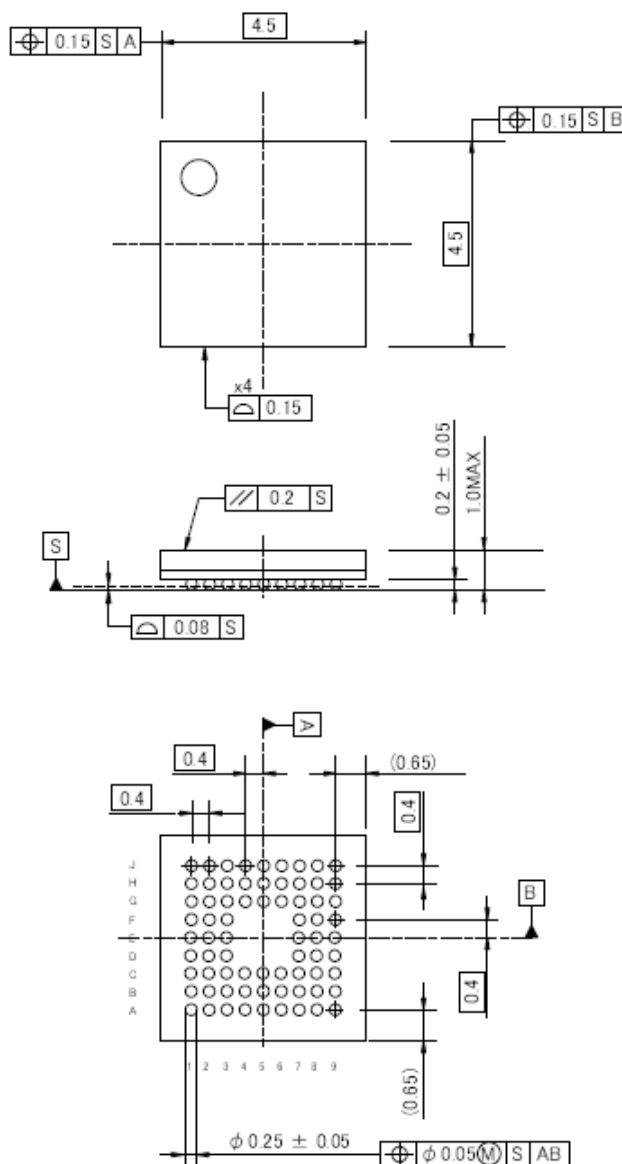
4. Package

4.1. TC358768AXBG Package

The packages for TC358768AXBG is described in the figure below.

P-VFBGA72-0505-0.40-001

"Unit:mm"



Weight: 32.0 mg (Typ.)

Figure 4.1 TC358768AXBG P-VFBGA72-0505-0.40-001 package

Table 4.1 TC358768AXBG P-VFBGA72-0505-0.40-001 Mechanical Dimension

Dimension	Min	Typ.	Max
Solder ball pitch	-	0.4 mm	-
Solder ball height	0.15 mm	0.2 mm	0.25 mm
Package dimension	-	4.5 × 4.5 mm ²	-
Package height	-	-	1.0 mm

4.2. TC358778XBG Package

The package for TC358778XBG is described in the figure below.

P-VFBGA80-0707-0.65-001

"Unit:mm"

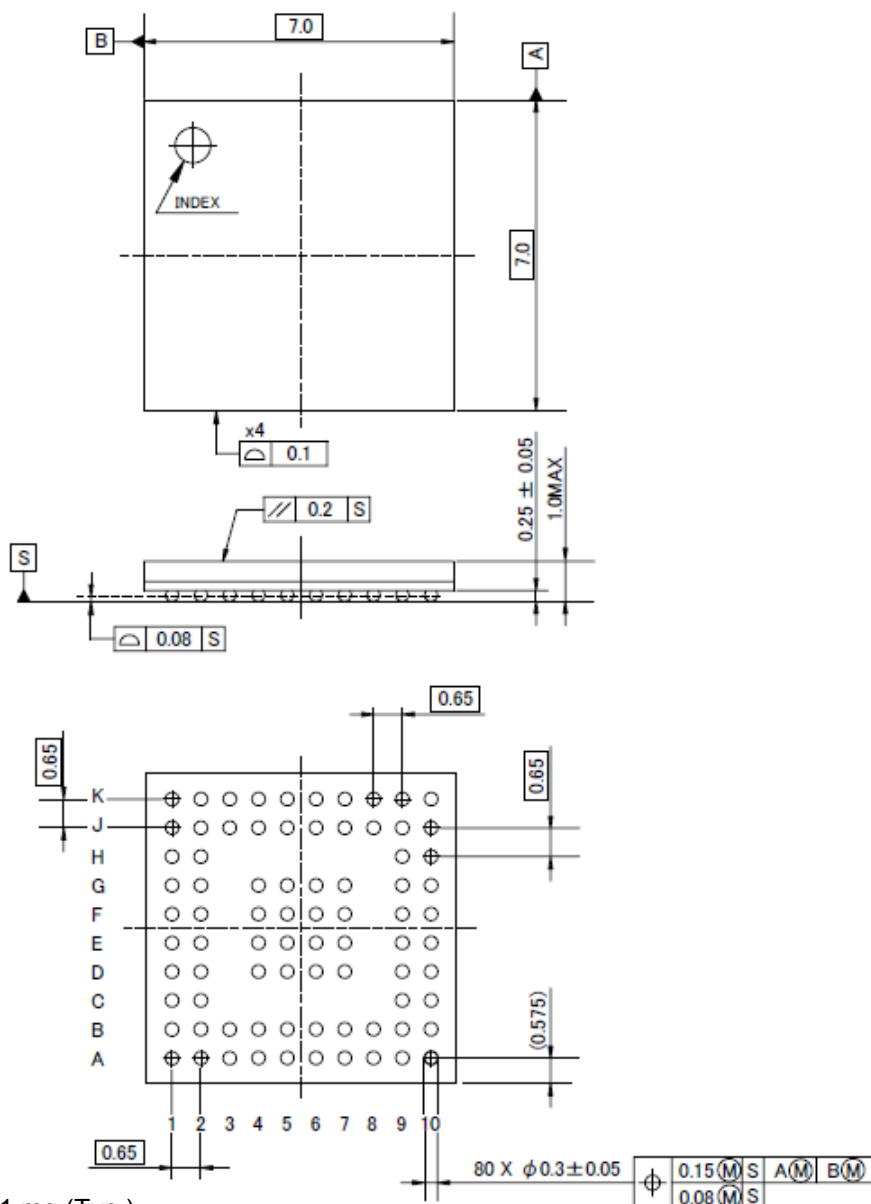


Figure 4.2 TC358778XB P-VFBGA80-0707-0.65-001 package

Table 4.2 P-VFBGA80-0707-0.65-001 Mechanical Dimension

Dimension	Min	Typ.	Max
Solder ball pitch	-	0.65 mm	-
Solder ball height	0.20 mm	0.25 mm	0.30 mm
Package dimension	-	7.0 × 7.0 mm ²	-
Package height	-	-	1.0 mm

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

VSS= 0V reference

Parameter	Symbol	Rating	Unit
Supply voltage (1.8V - Digital IO)	VDDIO	-0.3 to +3.9	V
Supply voltage (1.2V - Digital Core)	VDDC	-0.3 to +1.8	V
Supply voltage (1.2V - MIPI PHY)	VDD_MIPI	-0.3 to +1.8	V
Input voltage (DSI IO)	V _{IN_DSI}	-0.3 to VDD_MIPI+0.3	V
Output voltage (DSI IO)	V _{OUT_DSI}	-0.3 to VDD_MIPI+0.3	V
Input voltage (Digital IO)	V _{IN_IO}	-0.3 to VDDIO+0.3	V
Output voltage (Digital IO)	V _{OUT_IO}	-0.3 to VDDIO+0.3	V
Junction temperature	T _j	125	°C
Storage temperature	T _{stg}	-40 to +125	°C

5.2. Operating Condition

VSS= 0 V reference

Parameter	Symbol	Min	Typ.	Max	Unit
Supply voltage (1.8V - Digital IO)	VDDIO	1.65	1.8	1.95	V
Supply voltage (3.3V - Digital IO)	VDDIO	3.0	3.3	3.6	V
Supply voltage (1.2V - Digital Core)	VDDC	1.1	1.2	1.3	V
Supply voltage (1.2V - MIPI PHY)	VDD_MIPI	1.1	1.2	1.3	V
Operating temperature (ambient temperature with voltage applied)	T _a	-30	+25	+85	°C
Supply Noise Voltage	V _{SN}	-	-	100	mV _{pp}

5.3. DC Electrical Specification

Parameter	Symbol	Min	Typ.	Max	Unit
Input voltage, High level input ^{Note1}	V_{IH}	0.7 VDDIO	-	VDDIO	V
Input voltage, Low level input ^{Note1}	V_{IL}	0	-	0.3 VDDIO	V
Input voltage High level CMOS Schmitt Trigger ^{Note1,2}	V_{IHS}	0.7 VDDIO	-	VDDIO	V
Input voltage Low level CMOS Schmitt Trigger ^{Note1,2}	V_{ILS}	0	-	0.3 VDDIO	V
Output voltage High level (Condition: $I_{OH} = -0.4$ mA) ^{Note1, Note2}	V_{OH}	0.8 VDDIO	-	VDDIO	V
Output voltage Low level (Condition: $I_{OL} = 2$ mA) ^{Note1, Note2}	V_{OL}	0	-	0.2 VDDIO	V
Input leak current, High level (Normal IO or Pull-up IO) (Condition: $V_{IN} = +VDDIO$, VDDIO = 3.6 V)	I_{ILH1} ^{Note3}	-10	-	10	μA
Input leak current, High level (Pull-down IO) (Condition: $V_{IN} = +VDDIO$, VDDIO = 3.6 V)	I_{ILH2} ^{Note3}	-	-	100	μA
Input leak current, Low level (Normal IO or Pull-down IO) (Condition: $V_{IN} = 0$ V, VDDIO = 3.6 V)	I_{ILL1} ^{Note4}	-10	-	10	μA
Input leak current, Low level (Pull-up IO) (Condition: $V_{IN} = 0$ V, VDDIO = 3.6 V)	I_{ILL2} ^{Note4}	-	-	200	μA

Note 1: Each power source is operating within recommended operation condition.

Note 2: Current output value is specified to each IO buffer individually. Output voltage changes with output current value.

Note 3: Normal pin or Pull-up IO pin applied VDDIO supply voltage to V_{in} (input voltage)

Note 4: Normal pin or Pull-down IO pin applied VSSIO (0V) to V_{in} (input voltage)

6. Revision History

Table 6.1 Revision History

Revision	Date	Description
1.11	2014-05-28	Newly released

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