**ULTRA-LOW CURRENT CONSUMPTION
NORMALLY-OFF FAINT SIGNAL DETECTION IC**

Rev.1.3_02

The S-5470 Series, developed by CMOS technology, is a normally-off faint signal detection IC with an ultra-low current consumption.

This IC has a function to detect certain current level of 0.7 nA typ., which makes it possible to detect faint signals for a variety of electric generating devices or sensor devices. It also has a function to detect the difference of current level, and thus detects difference between strengths of two signals input at the same time.

Due to its ultra-low current consumption and low-voltage operation, the S-5470 Series is suitable for battery-operated small mobile device applications.

## ■ Features

- Ultra-low current consumption:    $I_{DD} \leq 0.1$ nA typ.
- Faint current detection:    $I_{DET} = 0.7$ nA typ.
- Wide operation voltage range:    $V_{DD} = 0.9$ V to 5.5 V
- Detection of faint signal:    Detects faint signals of approximately 0.7 nW (1.0 V, 0.7 nA typ.)
- Detection of signal strength difference:    Detects difference between strengths of two signals input at the same time
- Lead-free (Sn 100%), halogen-free

## ■ Applications

- Detects output signals of electric generating devices or sensor devices with high internal resistance
- Advanced sensing using two electric generating devices or sensor devices
- Miniaturization and low power consumption for various sensors of portable and wireless devices
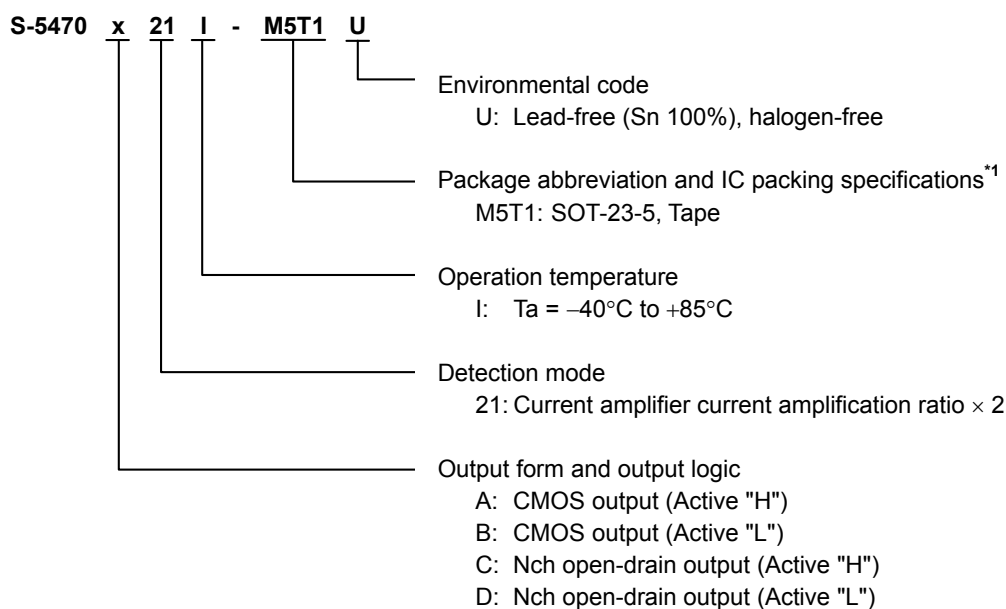
## ■ Package

- SOT-23-5

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## ■ Block Diagrams

### 1. CMOS output product



***1.** Parasitic diode

**Figure 1**

### 2. Nch open-drain output product



***1.** Parasitic diode

**Figure 2**

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# ■ Product Name Structure

Users can select the output form and output logic for the S-5470 Series. Refer to "**1.    Product name**" regarding the contents of the product name, "**2.    Package**" regarding the package drawings, "**3.    Product name list**" regarding details of the product name.

## 1.    Product name

S-5470   **x**   **21**   **I**   -   **M5T1**   **U**

Environmental code
    U:  Lead-free (Sn 100%), halogen-free

Package abbreviation and IC packing specifications[1]
    M5T1: SOT-23-5, Tape

Operation temperature
    I:    Ta = −40°C to +85°C

Detection mode
    21: Current amplifier current amplification ratio × 2

Output form and output logic
    A:  CMOS output (Active "H")
    B:  CMOS output (Active "L")
    C:  Nch open-drain output (Active "H")
    D:  Nch open-drain output (Active "L")

**  *1.**    Refer to the tape drawing.

## 2.    Package

**Table 1    Package Drawing Codes**

| Package  Name | Dimension | Tape | Reel |
|---|---|---|---|
| SOT-23-5 | MP005-A-P-SD | MP005-A-C-SD | MP005-A-R-SD |

## 3.    Product name list

**Table 2**

| Product Name | Output Form | Output Logic | Detection Mode |
|---|---|---|---|
| S-5470A21I-M5T1U | CMOS output | Active  "H" | Current amplifier current amplification ratio × 2 |
| S-5470B21I-M5T1U | CMOS output | Active  "L" | Current amplifier current amplification ratio × 2 |
| S-5470C21I-M5T1U | Nch open-drain output | Active  "H" | Current amplifier current amplification ratio × 2 |
| S-5470D21I-M5T1U | Nch open-drain output | Active  "L" | Current amplifier current amplification ratio × 2 |

**Remark**    Please contact our sales office for products other than the above.
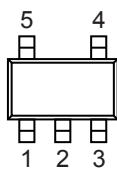
# ■ Pin Configuration

### 1. SOT-23-5

Top view



**Figure 3**

**Table 3**

| Pin No. | Symbol | Description |
|---------|--------|-------------|
| 1 | VDD | Power supply pin |
| 2 | VSS | GND pin |
| 3 | INM | Reference current input pin |
| 4 | INP | Detection current input pin |
| 5 | OUT | Output pin |

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■ **Absolute Maximum Ratings**

**Table 4**

(Ta = +25°C unless otherwise specified)

| Item | | Symbol | Absolute Maximum Rating | Unit |
|---|---|---|---|---|
| Power supply voltage | | $V_{DD}$ | $V_{SS} - 0.3$ to $V_{SS} + 7.0$ | V |
| Input voltage | | $V_{INP}, V_{INM}$ | $V_{SS} - 0.3$ to $V_{SS} + 7.0$ | V |
| Output voltage | CMOS output product | $V_{OUT}$ | $V_{SS} - 0.3$ to $V_{DD} + 0.3$ | V |
| | Nch open-drain output product | | $V_{SS} - 0.3$ to $V_{SS} + 7.0$ | V |
| Output pin current | | $I_{SOURCE}$ | 20 | mA |
| | | $I_{SINK}$ | 20 | mA |
| Power dissipation | | $P_D$ | 600[*1] | mW |
| Operation ambient temperature | | $T_{opr}$ | −40 to +85 | °C |
| Storage temperature | | $T_{stg}$ | −55 to +125 | °C |

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Name: JEDEC STANDARD51-7

**Caution**   **The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**
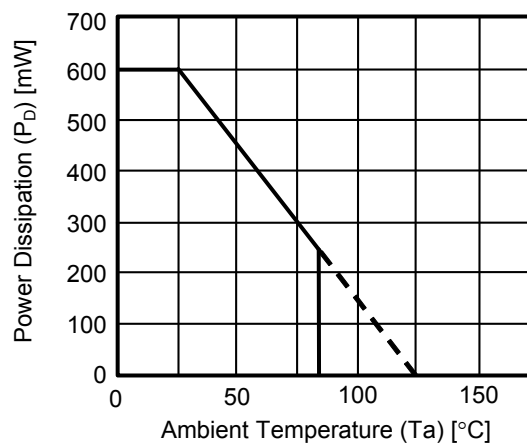


**Figure 4   Power Dissipation of Package (When Mounted on Board)**

## ■ Electrical Characteristics

**Table 5**

(Ta = +25°C, $V_{DD}$ = 3.0 V unless otherwise specified)

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | Ta = −40°C to +85°C | | 0.9 | − | 5.5 | V | − |
| Current consumption | $I_{DD}$ | $V_{INP}$ = $V_{SS}$, $V_{INM}$ = $V_{SS}$ | | − | 0.01 | 10 | nA | 1 |
| | | $V_{INP}$ = 1.0 V, $V_{INM}$ = $V_{SS}$ | | − | 0.02 | 10 | nA | 1 |
| Detection current | $I_{DET}$ | − | | 0.52 | 0.7 | 0.88 | nA | 2 |
| Release current | $I_{REL}$ | − | | $I_{DET} \times$ 0.7 | $I_{DET} \times$ 0.8 | $I_{DET} \times$ 0.9 | nA | 2 |
| Detection current temperature coefficient | $I_{tc}$ | Ta = −40°C to +85°C | | − | ±0.5 | − | %/°C | − |
| Input current | $I_{INP}$ | $V_{INP}$ = 1.0 V | | 20 | − | − | μA | 3 |
| | $I_{INM}$ | $V_{INM}$ = 1.0 V | | 10 | − | − | μA | 3 |
| Current amplifier current amplification ratio × 2 | $G_{INM}$ | − | | 1.8 | 2.0 | 2.2 | Times | 4 |
| Source current | $I_{SOURCE}$ | CMOS output product $V_{OUT}$ = $V_{DD}$ − 0.3 V | $V_{DD}$ = 0.9 V | 0.01 | 0.4 | − | mA | 5 |
| | | | $V_{DD}$ = 3.0 V | 3.5 | 4.8 | − | mA | 5 |
| Sink current | $I_{SINK}$ | $V_{OUT}$ = 0.3 V | $V_{DD}$ = 0.9 V | 0.5 | 1.7 | − | mA | 6 |
| | | | $V_{DD}$ = 3.0 V | 7.0 | 9.2 | − | mA | 6 |
| Output response time | $t_{OD}$ | − | | − | − | 15 | ms | − |

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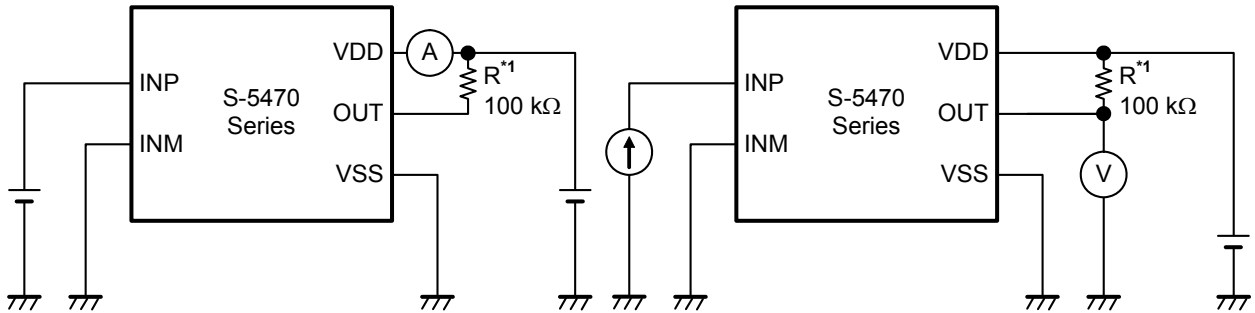
# ■ Test Circuits

**\*1.** Resistor (R) is unnecessary for the CMOS output product.  **\*1.** Resistor (R) is unnecessary for the CMOS output product.

**Figure 5   Test Circuit 1**                                **Figure 6   Test Circuit 2**
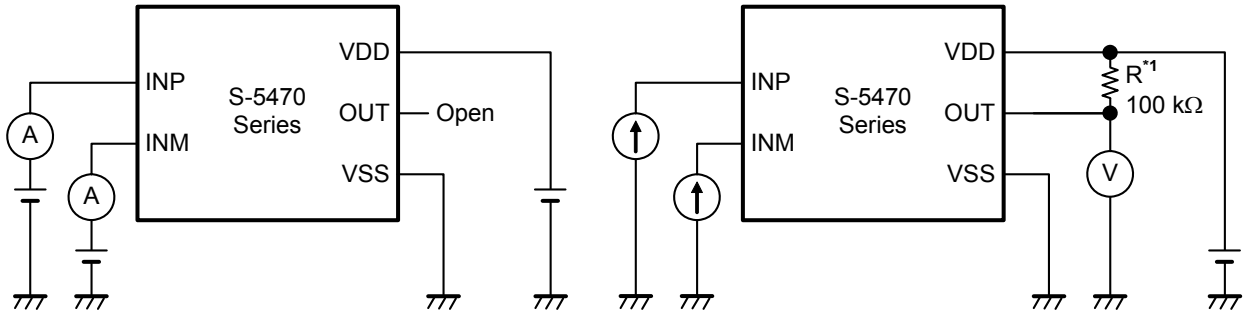
**\*1.** Resistor (R) is unnecessary for the CMOS output product.

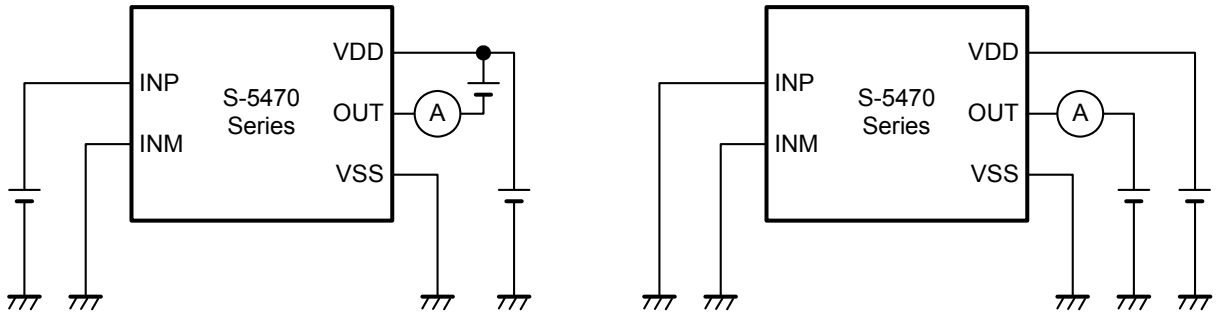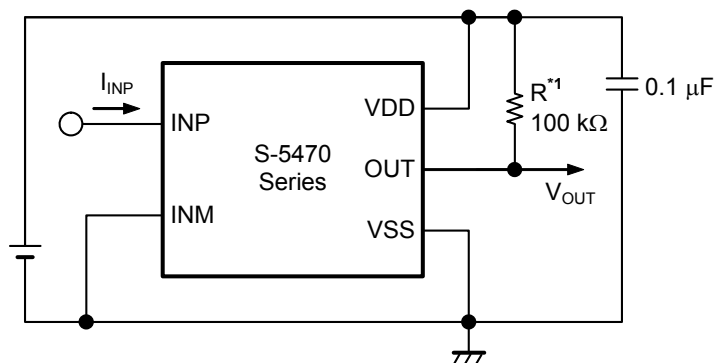**Figure 7   Test Circuit 3**                                **Figure 8   Test Circuit 4**

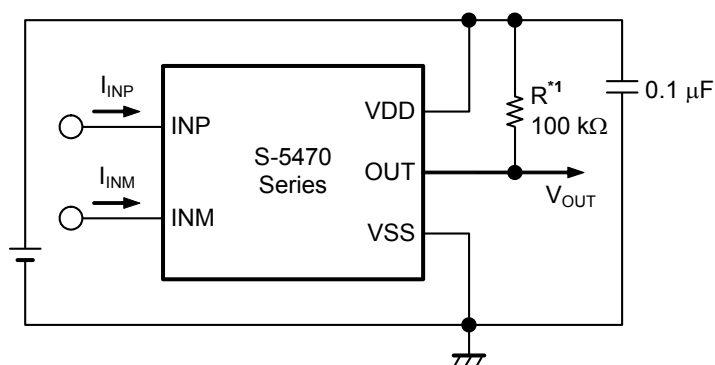**Figure 9   Test Circuit 5**                                **Figure 10   Test Circuit 6**

# ■ Standard Circuits

**1.  Certain current level detector**



*1.  Resistor (R) is unnecessary for the CMOS output product.

**Figure 11**

**2.  Current level difference detector**



*1.  Resistor (R) is unnecessary for the CMOS output product.

**Figure 12**

**Caution   The above connection diagram and constant will not guarantee successful operation. Perform
thorough evaluation using the actual application to set the constant.**

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# ■ Operation

The S-5470 Series detects either certain current level or the difference of current level.
The operation of the S-5470 Series is described below, using CMOS output and active "H" products as examples.

### 1. Basic operation when detecting certain current level (INM pin = $V_{SS}$)

The S-5470 Series operates as follows when the INM pin is connected to VSS pin.

(1) If $I_{INP}$ is lower than $I_{DET}$, an "L" level signal is output from the OUT pin.
(2) If $I_{INP}$ increases and becomes equal to or higher than $I_{DET}$, an "H" level signal is output from the OUT pin (point A in **Figure 14**). Even if $I_{INP}$ decreases and falls below $I_{DET}$, as long as $I_{INP}$ is higher than $I_{REL}$, an "H" level signal is output from the OUT pin.
(3) If $I_{INP}$ then decreases further and becomes equal to or lower than $I_{REL}$, an "L" level signal is output from the OUT pin (point B in **Figure 14**).

**Remark**   $I_{INP}$: Current input to the INP pin
  $I_{DET}$: Detection current (refer to "**4. 1   Detection current ($I_{DET}$)**")
  $I_{REL}$: Release current (refer to "**4. 2   Release current ($I_{REL}$)**")

**Caution 1.   There are internal diodes at the INP pin and the INM pin. Therefore, in order to input a current to the INP pin and the INM pin, an input voltage of at least the forward voltage of these diodes is required.**
  **2.   Feed-through current ($I_{PEAK}$ = 100 nA) flows around the time when the OUT pin voltage switches, as shown in Figure 14. Therefore, if the input current is fixed around this time, the current consumption will increase.**
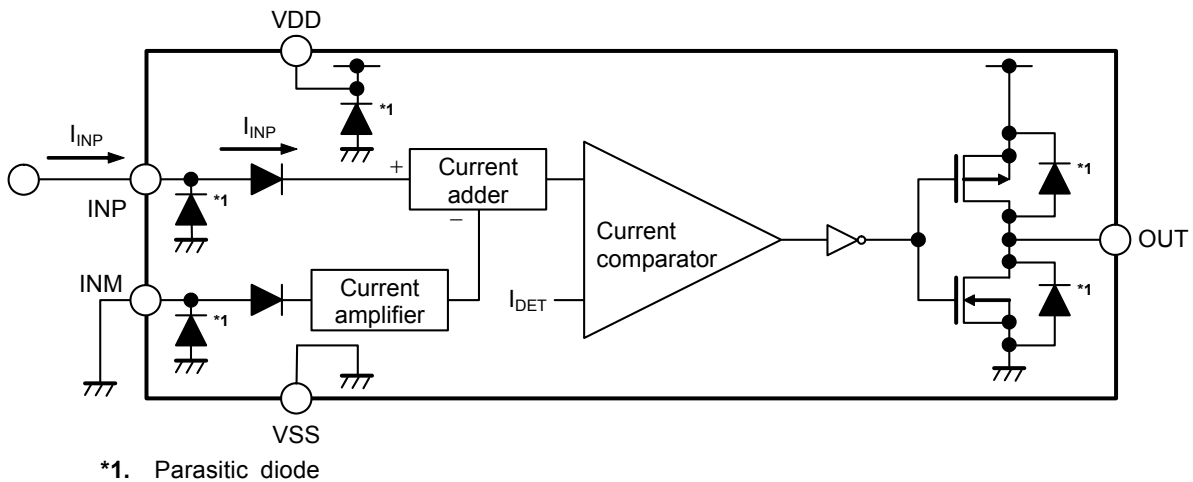


**\*1.**   Parasitic diode
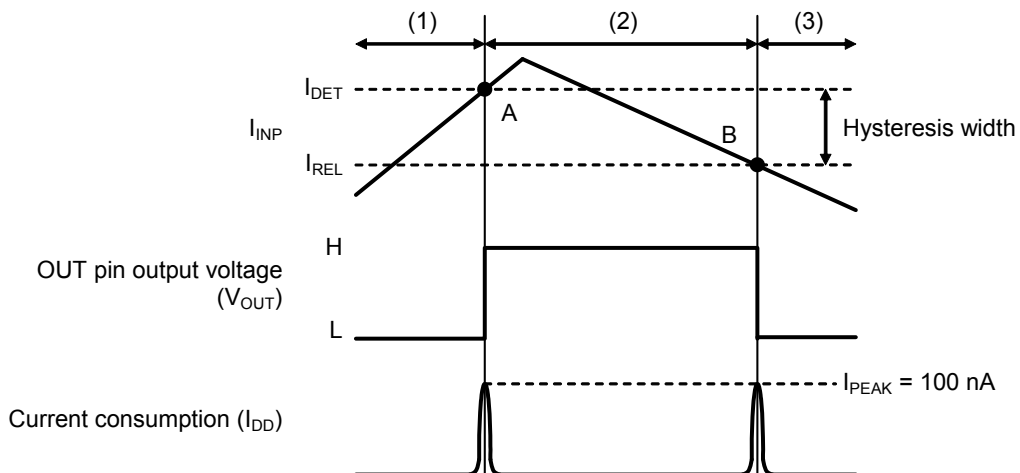**Figure 13   Diagram of the Operation when Detecting Certain Current Level**



**Figure 14   Operation when Detecting Certain Current Level**
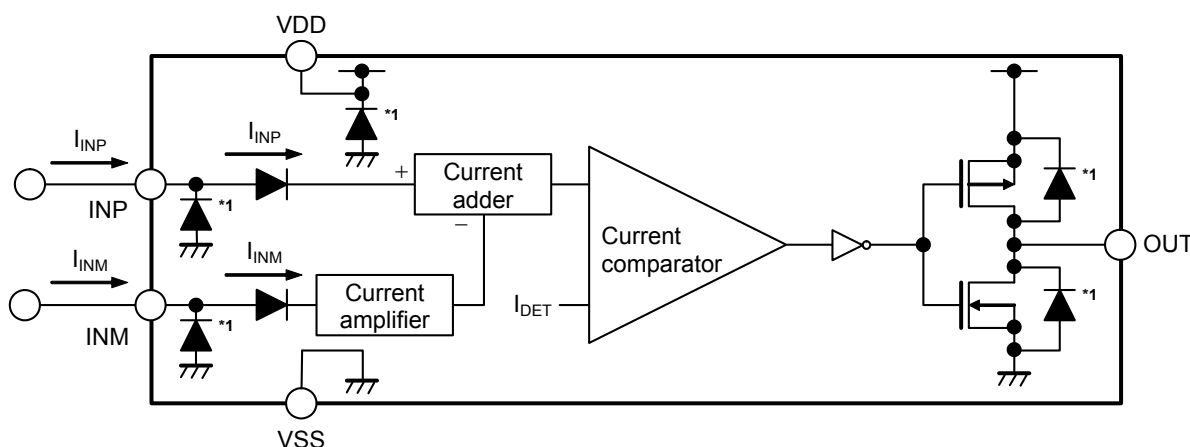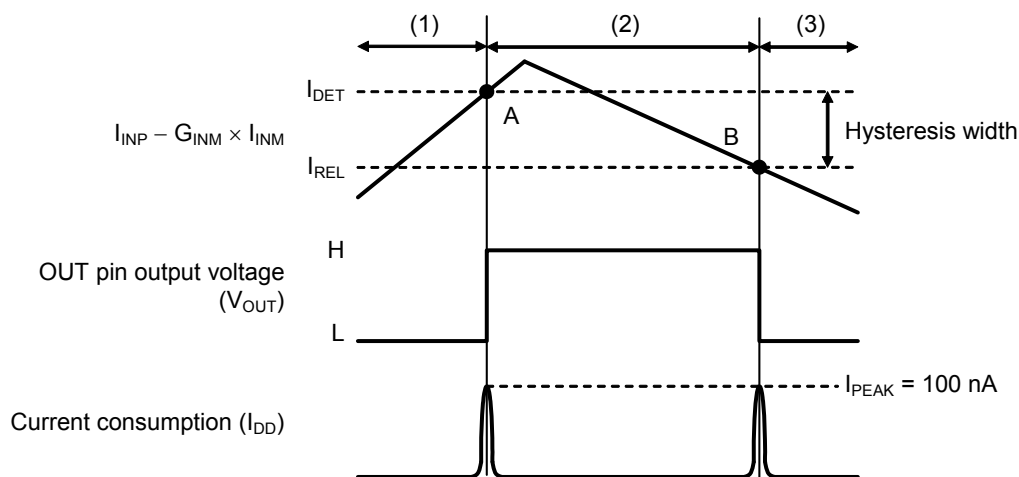
2. **Basic operation when detecting the difference of current level**
   **(Current amplifier current amplification ratio $\times$ $G_{INM}$)**

The S-5470 Series operates as follows when current ($I_{INM}$) is applied to the INM pin.

(1) If $I_{INP}$ is lower than $I_{DET} + G_{INM} \times I_{INM}$, an "L" level signal is output from the OUT pin.

(2) If $I_{INP}$ increases and becomes equal to or higher than $I_{DET} + G_{INM} \times I_{INM}$, an "H" level signal is output from the OUT pin (point A in **Figure 16**). Even if $I_{INP}$ decreases and falls below $I_{DET} + G_{INM} \times I_{INM}$, as long as $I_{INP}$ is higher than $I_{REL} + G_{INM} \times I_{INM}$, an "H" level signal is output from the OUT pin.

(3) If $I_{INP}$ then decreases further and becomes equal to or lower than $I_{REL} + G_{INM} \times I_{INM}$, an "L" level signal is output from the OUT pin (point B in **Figure 16**).

**Remark** $I_{INP}$: Current input to the INP pin
$I_{INM}$: Current input to the INM pin
$I_{DET}$: Detection current (refer to "**4. 1 Detection current ($I_{DET}$)**")
$I_{REL}$: Release current (refer to "**4. 2 Release current ($I_{REL}$)**")

**Caution 1.** **There are internal diodes at the INP pin and the INM pin. Therefore, in order to input a current to the INP pin and the INM pin, an input voltage of at least the forward voltage of these diodes is required.**

**2.** **Feed-through current ($I_{PEAK}$ = 100 nA) flows around the time when the OUT pin voltage switches, as shown in Figure 16. Therefore, if the input current is fixed around this time, the current consumption will increase.**



**\*1.** Parasitic diode

**Figure 15   Diagram of the Operation when Detecting the Difference of Current Level**



**Figure 16   Operation when Detecting the Difference of Current Level**

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3.   **Temperature characteristics of detection current**

The shaded area in **Figure 17** shows the temperature characteristics of the detection voltage in the operation temperature range.
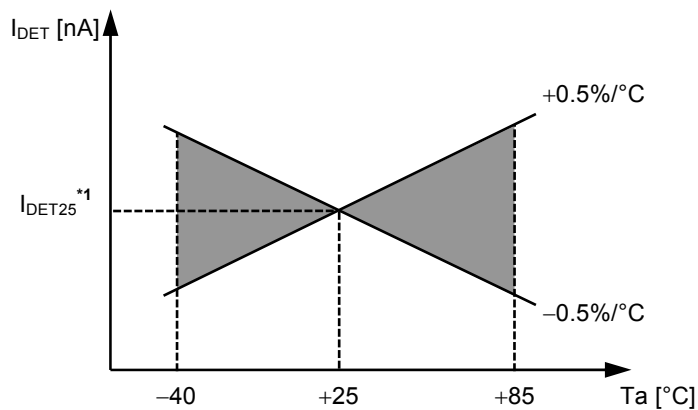


**\*1.**   $I_{DET25}$: Detection current value at Ta = +25°C

**Figure 17   Temperature Characteristics of Detection Current**

## 4. Explanation of terms

### 4. 1 Detection current ($I_{DET}$)

The detection current ($I_{DET}$) is the current at which the output switches to "H".
The detection current varies slightly even among products with the same specification. The variation in detection current from the minimum detection current ($I_{DET}$ min.) to the maximum detection current ($I_{DET}$ max.) is called the detection current range (refer to **Figure 18**).
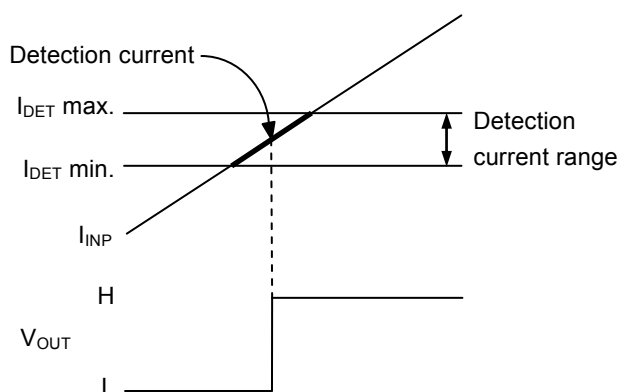


**Figure 18   Detection Current**

### 4. 2 Release current ($I_{REL}$)

The release current ($I_{REL}$) is the current at which the output switches to "L".
The release current varies slightly even among products with the same specification. The variation in release current from the minimum release current ($I_{REL}$ min.) to the maximum release current ($I_{REL}$ max.) is called the release current range (refer to **Figure 19**).
The range is calculated from the actual detection current ($I_{DET}$) of a product and is in the range of $I_{DET} \times 0.7 \le I_{REL} \le I_{DET} \times 0.9$.
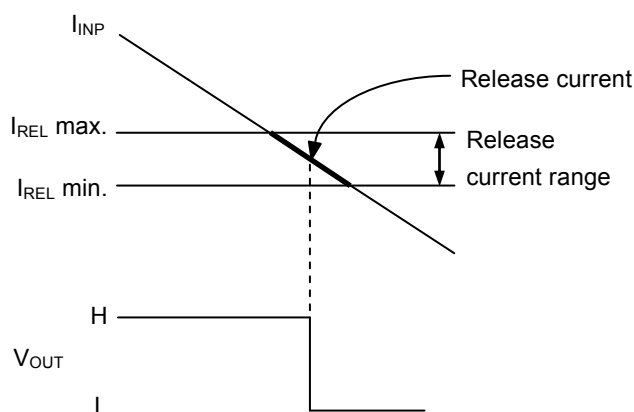


**Figure 19   Release Current**

### 4. 3 Hysteresis width

The hysteresis width is the current difference between the detection current and the release current (current at point B − current at point A in "**Figure 14   Operation when Detecting Certain Current Level**" and "**Figure 16 Operation when Detecting the Difference of Current Level**").
The hysteresis width between the detection current and the release current prevents malfunction caused by noise in the input current.

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# ■ Application Circuits

### 1. Certain photocurrent level detector

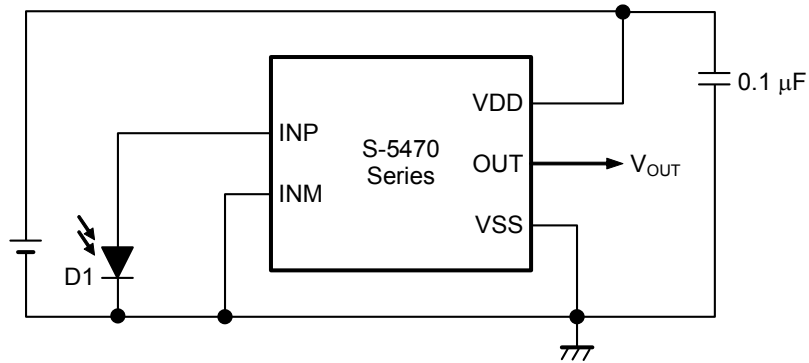If PD or LED exceeds a certain value, the output signal inverts.

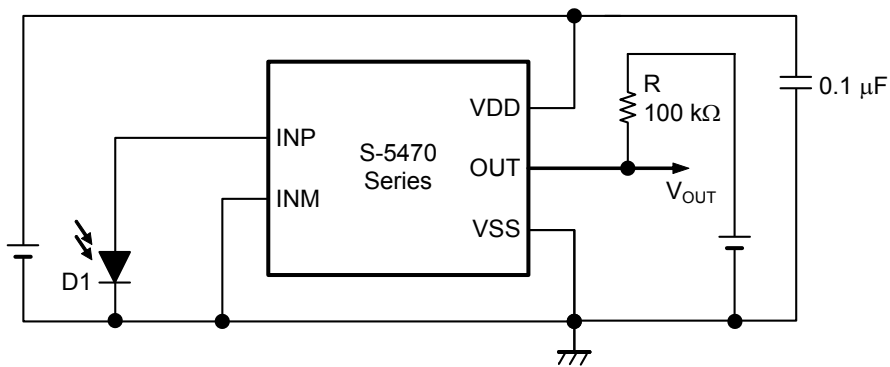**Figure 20   Example Certain Photocurrent Level Detector (CMOS Output Product)**

**Figure 21   Example Certain Photocurrent Level Detector (Nch Open-drain Output Product)**

**Caution   The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.**

## 2. Photocurrent level difference detector

If the difference in the photocurrent generated by the two PDs or the two LEDs exceeds a certain value, the output signal inverts.
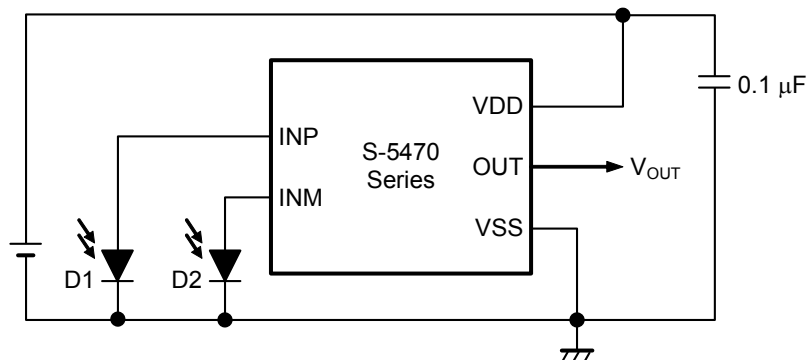
**Figure 22  Example Photocurrent Level Difference Detector (CMOS Output Product)**
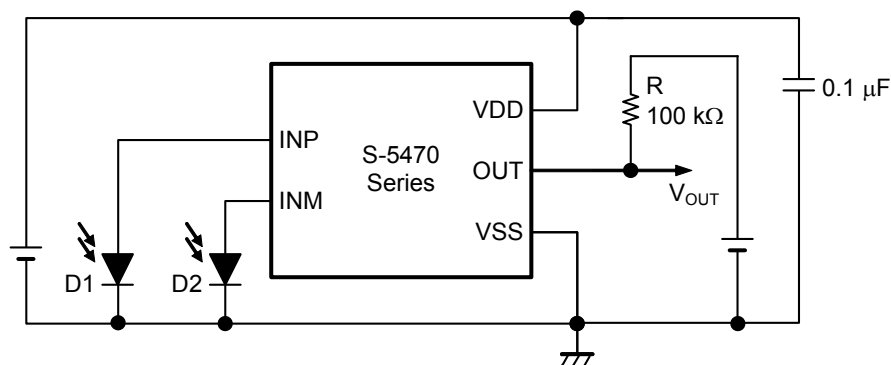
**Figure 23  Example Photocurrent Level Difference Detector (Nch Open-drain Output Product)**

**Caution   The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.**

### 3.  Selection of PD or LED

Use PD or LED whose generation voltage is 1.0 V or more under usable light quantity.
Moreover, as for the test circuit shown in **Figure 24**, select PD or LED that satisfies the conditions below with detection or measurement of the quantity of light incidence in usage environment.

- Certain photocurrent level detector
  $I_{DET} \leq I$
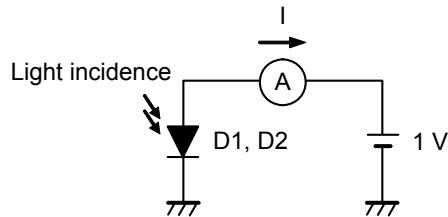- Photocurrent level difference detector
  $1\ nA \leq I \leq 20\ \mu A$



**Figure 24**

Caution  1.   Select PD or LED after thorough evaluation with actual application. ABLIC Inc. shall not take responsibility for operation and characteristics of PD or LED.

2.   As for the circuit of detecting photocurrent difference, shown in Figure 22 and Figure 23, use the two PDs or the two LEDs that have the same characteristics in generation voltage and in generation current, respectively.

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# ■ Precautions

- Use the S-5470 Series with the output current of 20 mA or less.

- The S-5470 Series may malfunction if the power supply voltage changes suddenly.

- As for the detecting circuit of the photocurrent difference (Refer to "**Figure 22, Figure 23   Example Photocurrent Level Difference Detector**"), use the S-5470 Series when input current of INP pin is 20 $\mu$A or less and input current of INM pin is 10 $\mu$A or less. In case of input current excess, note that the S-5470 Series might malfunction.

- The output in the S-5470 Series is unstable in lower voltage than the minimum operation voltage. At the time of power-on, use the S-5470 Series after output stabilization.

- Set a capacitor of 0.1 $\mu$F or more between the VDD pin and VSS pin for stabilization.

- Since INP pin and INM pin is easy to be affected by disturbance noise, perform countermeasures such as mounting external parts to ICs as close as possible.

- If power impedance is high, the S-5470 Series may malfunction due to voltage drop caused by feed-through current. Set wire patterns carefully for lower power impedance.

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.
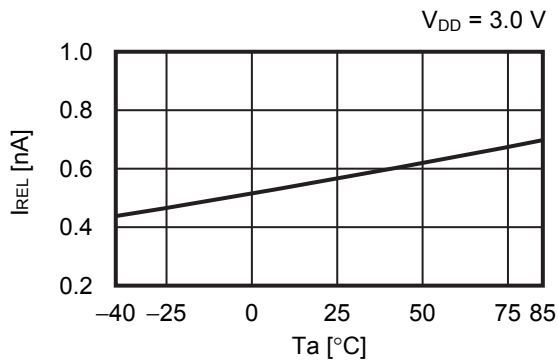
# ■ Characteristics (Typical Data)
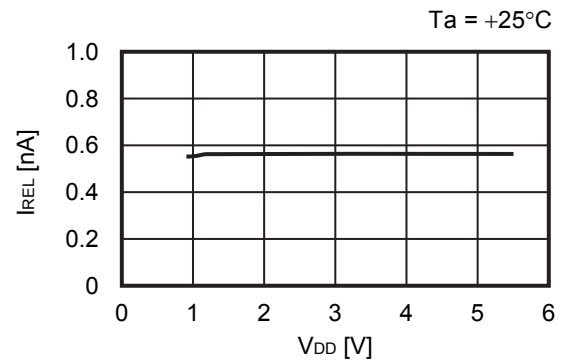
**1.  Detection current vs. Temperature**

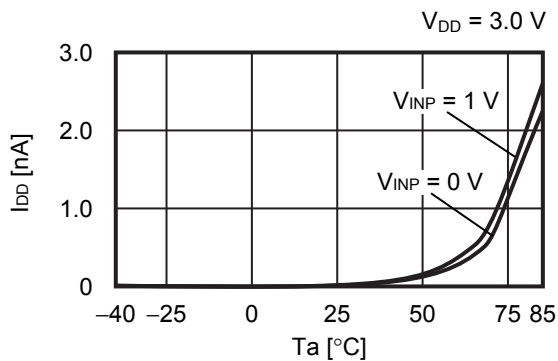$V_{DD}$ = 3.0 V
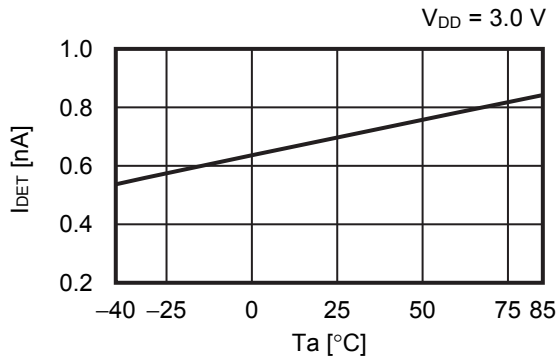


**2.  Detection current vs. Power supply voltage**
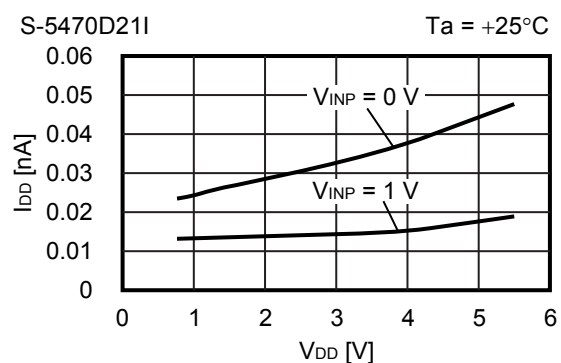
Ta = +25°C
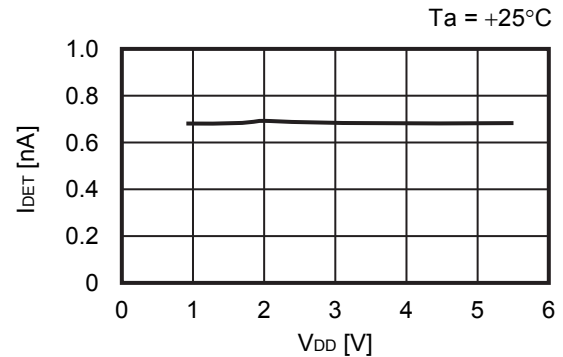


**3.  Release current vs. Temperature**

$V_{DD}$ = 3.0 V



**4.  Release current vs. Power supply voltage**
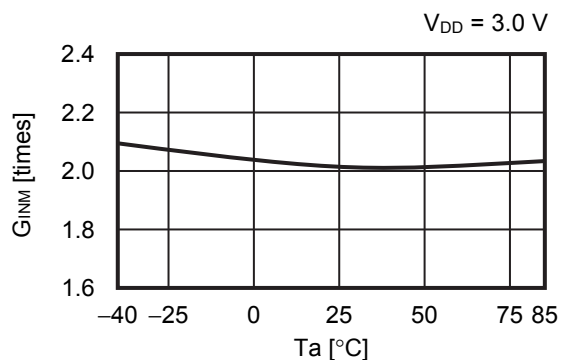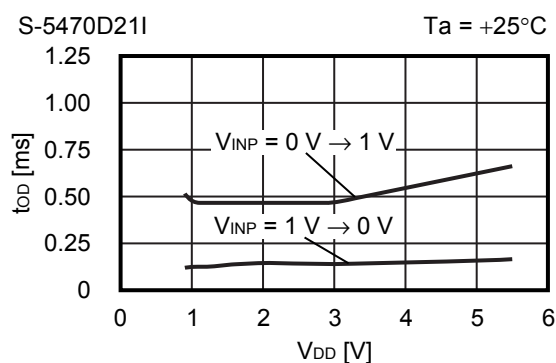
Ta = +25°C



**5.  Current consumption vs. Temperature**

$V_{DD}$ = 3.0 V

## 6. Current consumption vs. Power supply

S-5470A21I                    Ta = +25°C



S-5470B21I                    Ta = +25°C



S-5470C21I                    Ta = +25°C



S-5470D21I                    Ta = +25°C
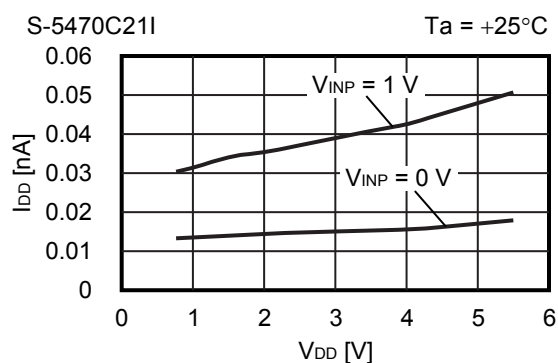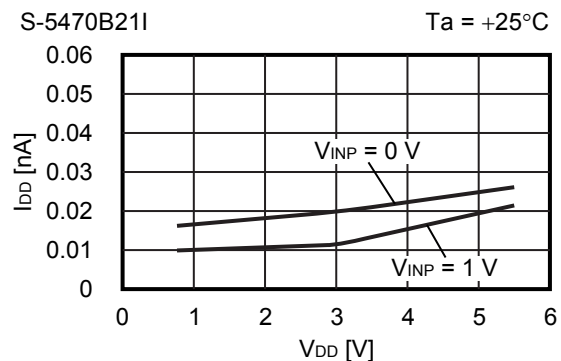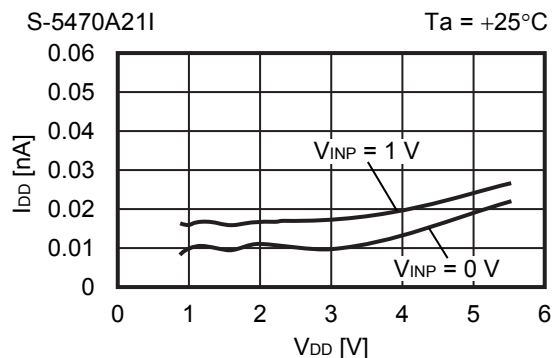


## 7. Current amplifier current amplication ratio vs. Temperature

$V_{DD}$ = 3.0 V

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## 8. Output response time vs. Power supply voltage

S-5470A21I                          Ta = +25°C

$V_{INP} = 1 \, V \rightarrow 0 \, V$

$V_{INP} = 0 \, V \rightarrow 1 \, V$

$t_{OD}$ [ms]

$V_{DD}$ [V]

S-5470B21I                          Ta = +25°C

$V_{INP} = 0 \, V \rightarrow 1 \, V$

$V_{INP} = 1 \, V \rightarrow 0 \, V$

$t_{OD}$ [ms]

$V_{DD}$ [V]

S-5470C21I                          Ta = +25°C

$V_{INP} = 1 \, V \rightarrow 0 \, V$

$V_{INP} = 0 \, V \rightarrow 1 \, V$

$t_{OD}$ [ms]

$V_{DD}$ [V]

S-5470D21I                          Ta = +25°C

$V_{INP} = 0 \, V \rightarrow 1 \, V$

$V_{INP} = 1 \, V \rightarrow 0 \, V$

$t_{OD}$ [ms]

$V_{DD}$ [V]
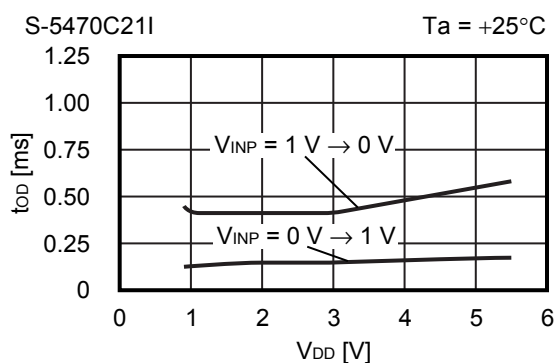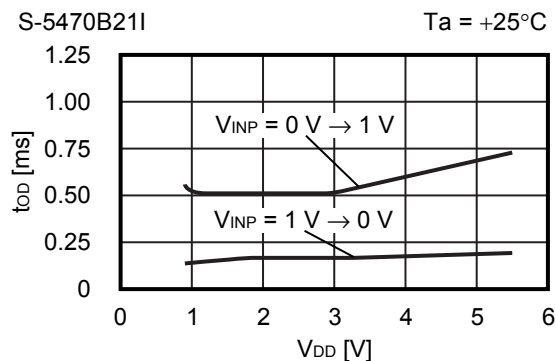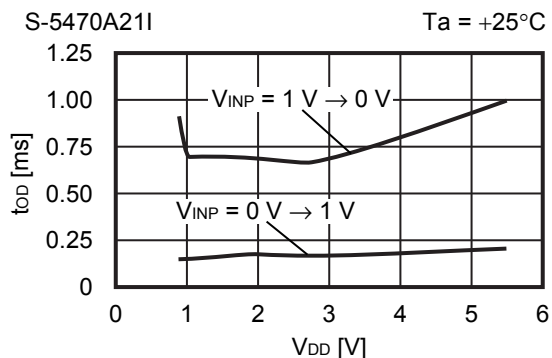
## 9. Source current vs. Power supply voltage

Ta = +25°C

Ta = −40°C

Ta = +85°C

$I_{SOURCE}$ [mA]

$V_{DD}$ [V]
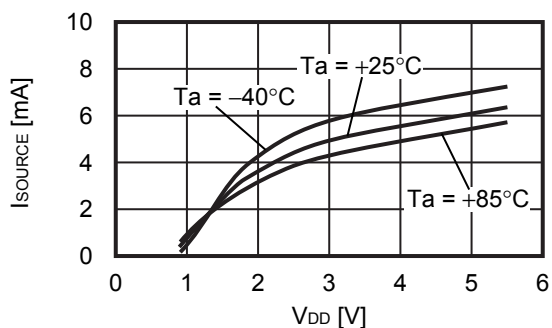
## 10. Sink current vs. Power supply voltage

Ta = −40°C      Ta = +25°C

Ta = +85°C

$I_{SINK}$ [mA]

$V_{DD}$ [V]

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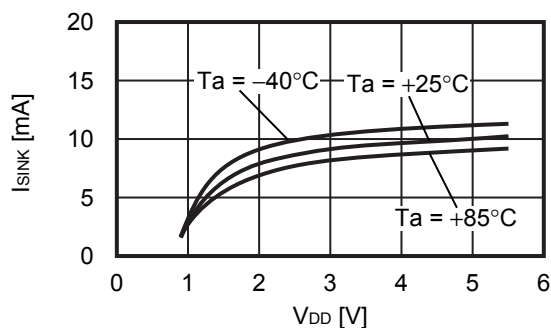
## ■ Marking Specification
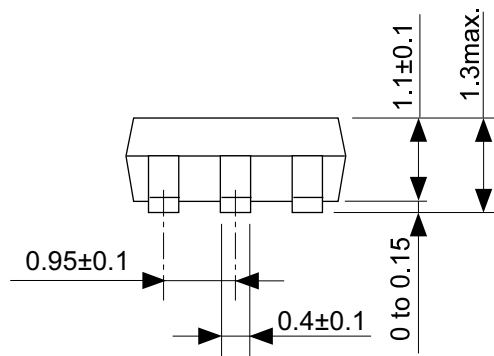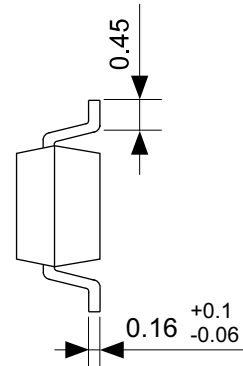
### 1. SOT-23-5

Top view
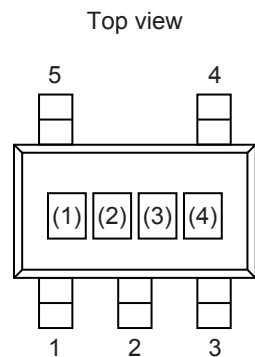


(1) to (3):     Product code (Refer to **Product name vs. Product code**)
(4):            Lot number

**Product name vs. Product code**

| Product Name | Product Code | | |
|---|---|---|---|
| | (1) | (2) | (3) |
| S-5470A21I-M5T1U | Y | H | A |
| S-5470B21I-M5T1U | Y | H | I |
| S-5470C21I-M5T1U | Y | H | Q |
| S-5470D21I-M5T1U | Y | H | Y |

2.9±0.2

1.9±0.2

5 4

1.6

2.8 +0.2 -0.3

1 2 3

0.45

0.16 +0.1 -0.06

1.1±0.1

1.3max.

0.95±0.1

0.4±0.1

0 to 0.15
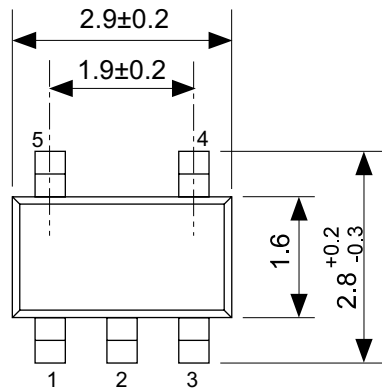
No. MP005-A-P-SD-1.3

| TITLE | SOT235-A-PKG Dimensions |
|---|---|
| No. | MP005-A-P-SD-1.3 |
| ANGLE | ⊕ ⊏ |
| UNIT | mm |
| | |

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ø1.5 +0.1 -0

2.0±0.05

4.0±0.1(10 pitches:40.0±0.2)

1.75±0.1

0.25±0.1

3.5±0.05

8.0±0.2

3.25±0.15

ø1.0 +0.2 -0

4.0±0.1

1.4±0.2

3.2±0.2

3 2 1

4 5
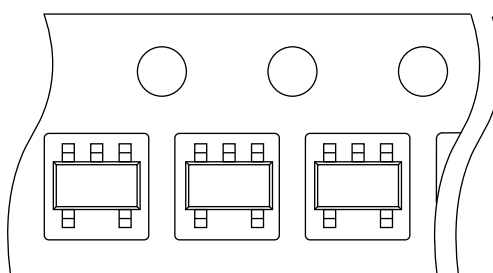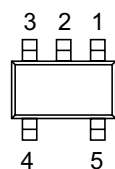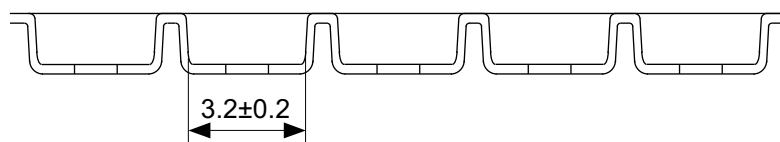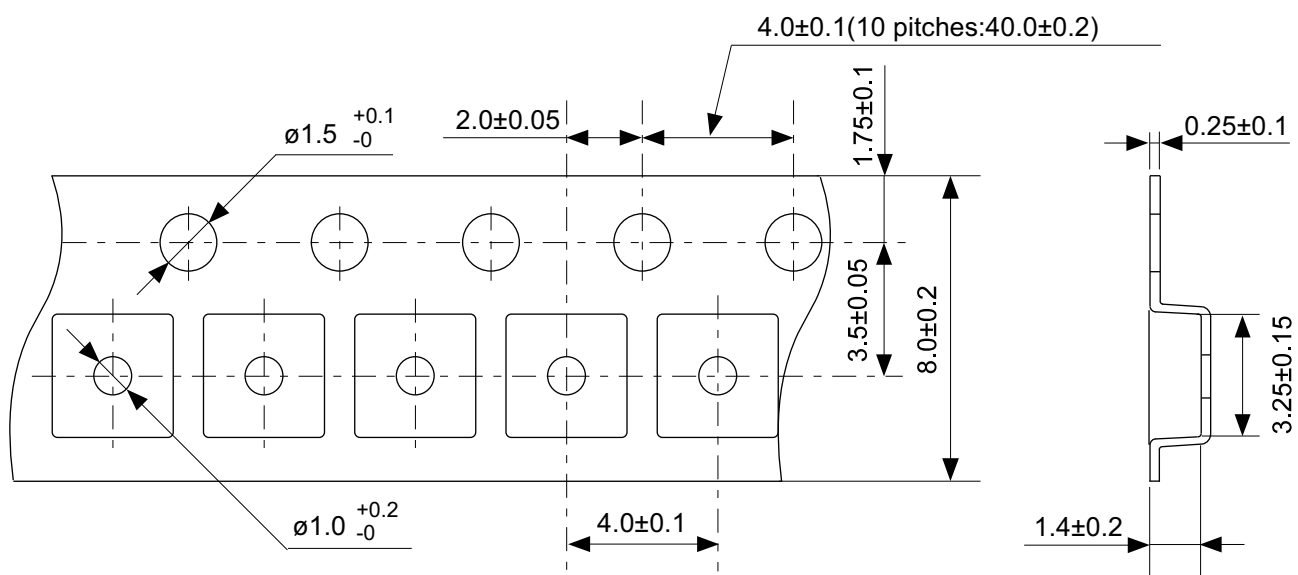
Feed direction

No. MP005-A-C-SD-2.1

| TITLE | SOT235-A-Carrier Tape |
|---|---|
| No. | MP005-A-C-SD-2.1 |
| ANGLE | |
| UNIT | mm |
| | |

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12.5max.

$\phi 60^{+1}_{-0}$

$\phi 180^{+0}_{-3}$

9.0±0.3
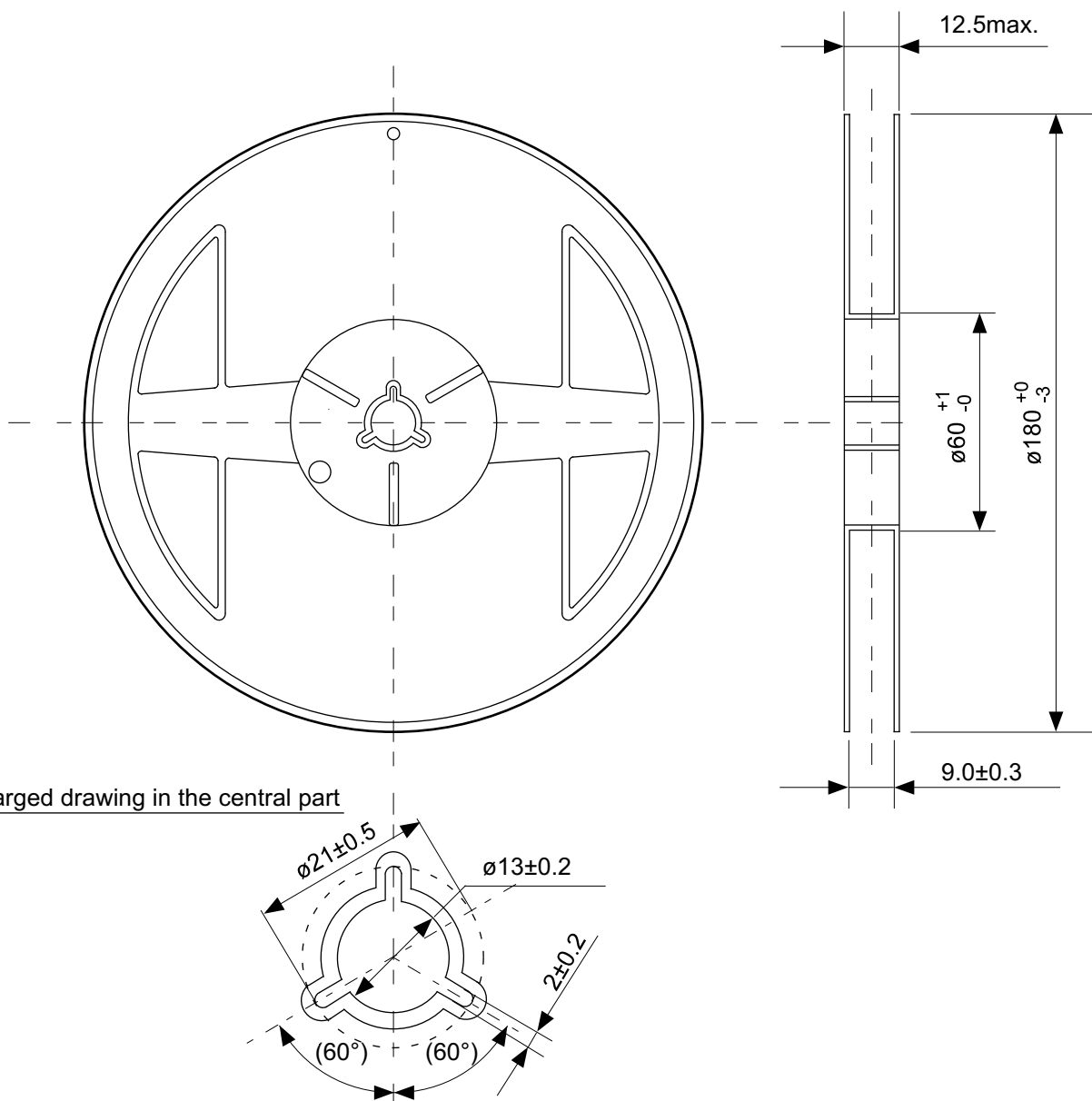
Enlarged drawing in the central part

$\phi 21\pm0.5$

$\phi 13\pm0.2$

2±0.2

(60°)　(60°)

No. MP005-A-R-SD-1.1

| TITLE | SOT235-A-Reel | | |
|---|---|---|---|
| No. | MP005-A-R-SD-1.1 | | |
| ANGLE | | QTY. | 3,000 |
| UNIT | mm | | |
| | | | |
| ABLIC Inc. | | | |

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2.4-2019.07

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