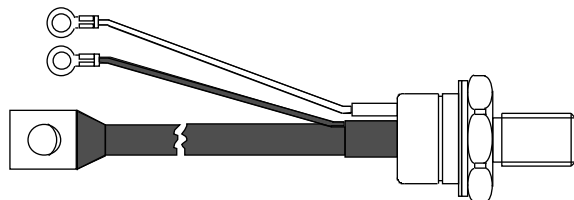


Phase Control Thyristors (Stud Version), 80 A



TO-209AC (TO-94)

FEATURES

- Hermetic glass-metal seal
- International standard case TO-209AC (TO-94)
- Compliant to RoHS directive 2002/95/EC
- Designed and qualified for industrial level



RoHS
COMPLIANT

TYPICAL APPLICATIONS

- DC motor controls
- Controlled DC power supplies
- AC controllers

PRODUCT SUMMARY

$I_{T(AV)}$	80 A
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MAJOR RATINGS AND CHARACTERISTICS

PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		80	A
	T_C	85	°C
$I_{T(RMS)}$		125	A
I_{TSM}	50 Hz	1900	
	60 Hz	1990	
I^2t	50 Hz	18	kA ² s
	60 Hz	16	
V_{DRM}/V_{RRM}		400 to 1200	V
t_q	Typical	110	µs
T_J		- 40 to 125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS

TYPE NUMBER	VOLTAGE CODE	V_{DRM}/V_{RRM} , MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V_{RSM} , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	I_{DRM}/I_{RRM} MAXIMUM AT $T_J = 125\text{ °C}$ mA
80RIA 81RIA	40	400	500	15
	80	800	900	
	120	1200	1300	

80RIA...PbF, 81RIA...PbF, 82RIA...PbF Series



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ABSOLUTE MAXIMUM RATINGS						
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average on-state current at case temperature	I _{T(AV)}	180° conduction, half sine wave			80	A
					85	°C
Maximum RMS on-state current	I _{T(RMS)}	DC at 75 °C case temperature			125	A
Maximum peak, one-cycle non-repetitive surge current	I _{TSM}	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial T _J = T _J maximum	1900	
		t = 8.3 ms			1990	
		t = 10 ms	100 % V _{RRM} reapplied		1600	
		t = 8.3 ms			1675	
Maximum I ² t for fusing	I ² t	t = 10 ms	No voltage		18	
		t = 8.3 ms			16	
		t = 10 ms	100 % V _{RRM} reapplied	12.7		
		t = 8.3 ms		11.7		
Maximum I ² √t for fusing	I ² √t	t = 0.1 ms to 10 ms, no voltage reapplied			180.5	kA ² /s
Low level value of threshold voltage	V _{T(TO)1}	(16.7 % × π × I _{T(AV)}) < I < π × I _{T(AV)} , T _J = T _J maximum			0.99	V
High level value of threshold voltage	V _{T(TO)2}	(I > π × I _{T(AV)}), T _J = T _J maximum			1.13	
Low level value of on-state slope resistance	r _{t1}	(16.7 % × π × I _{T(AV)}) < I < π × I _{T(AV)} , T _J = T _J maximum			2.29	mΩ
High level value of on-state slope resistance	r _{t2}	(I > π × I _{T(AV)}), T _J = T _J maximum			1.84	
Maximum on-state voltage	V _{TM}	I _{pk} = 250 A, T _J = 25 °C, t _p = 10 ms sine pulse			1.60	V
Maximum holding current	I _H	T _J = 25 °C, anode supply 12 V resistive load			200	mA
Typical latching current	I _L				400	

SWITCHING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum non-repetitive rate of rise of turned-on current	di/dt	$T_J = 125 \text{ °C}$, $V_d = \text{Rated } V_{DRM}$, $I_{TM} = 2 \times di/dt$ snubber $0.2 \mu\text{F}$, 15Ω , gate pulse: 20 V , 65Ω , $t_p = 6 \mu\text{s}$, $t_r = 0.5 \mu\text{s}$ Per JEDEC standard RS-397, 5.2.2.6.	300	A/ μs
Typical delay time	t_d	Gate pulse: 10 V , 15Ω source, $t_p = 6 \mu\text{s}$, $t_r = 0.1 \mu\text{s}$, $V_d = \text{Rated } V_{DRM}$, $I_{TM} = 50 \text{ A}$, $T_J = 25 \text{ °C}$	1	μs
Typical turn-off time	t_q	$I_{TM} = 50 \text{ A}$, $T_J = T_J \text{ maximum}$, $di/dt = -5 \text{ A}/\mu\text{s}$, $V_R = 50 \text{ V}$, $dV/dt = 20 \text{ V}/\mu\text{s}$, gate bias: 0 V 25Ω , $t_p = 500 \mu\text{s}$	110	

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = 125 \text{ °C}$ exponential to 67 % rated V_{DRM}	500	V/ μs
Maximum peak reverse and off-state leakage current	I_{RRM} , I_{DRM}	$T_J = 125 \text{ °C}$ rated V_{DRM}/V_{RRM} applied	15	mA



80RIA...PbF, 81RIA...PbF, 82RIA...PbF Series

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TRIGGERING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum peak gate power	P _{GM}	T _J = T _J maximum, t _p ≤ 5 ms		12	W
Maximum average gate power	P _{G(AV)}	T _J = T _J maximum, f = 50 Hz, d% = 50		3	
Maximum peak positive gate current	I _{GM}	T _J = T _J maximum, t _p ≤ 5 ms		3	A
Maximum peak positive gate voltage	+ V _{GM}			20	V
Maximum peak negative gate voltage	- V _{GM}			10	
Maximum DC gate current required to trigger	I _{GT}	T _J = - 40 °C	Maximum required gate trigger/ current/voltage are the lowest value which will trigger all units 6 V anode to cathode applied	270	mA
		T _J = 25 °C		120	
		T _J = 125 °C		60	
Maximum DC gate voltage required to trigger	V _{GT}	T _J = - 40 °C		3.5	V
		T _J = 25 °C		2.5	
		T _J = 125 °C		1.5	
DC gate current not to trigger	I _{GD}	T _J = T _J maximum	Maximum gate current/voltage not to trigger is the maximum value which will not trigger any unit with rated V _{DRM} anode to cathode applied	6	mA
DC gate voltage not to trigger	V _{GD}			0.25	V

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum operating junction temperature range	T _J		- 40 to 125	°C
Maximum storage temperature range	T _{Stg}		- 40 to 150	
Maximum thermal resistance, junction to case	R _{thJC}	DC operation	0.30	K/W
Maximum thermal resistance, case to heatsink	R _{thCS}	Mounting surface, smooth, flat and greased	0.1	
Mounting torque, ± 10 %		Non-lubricated threads	15.5 (137)	N · m (lbf · in)
		Lubricated threads	14 (120)	
Approximate weight			130	g
Case style		See dimensions - link at the end of datasheet	TO-209AC (TO-94)	

80RIA...PbF, 81RIA...PbF, 82RIA...PbF Series

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ΔR_{thJC} CONDUCTION				
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION	RECTANGULAR CONDUCTION	TEST CONDITIONS	UNITS
180°	0.042	0.030	$T_J = T_J \text{ maximum}$	K/W
120°	0.050	0.052		
90°	0.064	0.070		
60°	0.095	0.100		
30°	0.164	0.165		

Note

- The table above shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

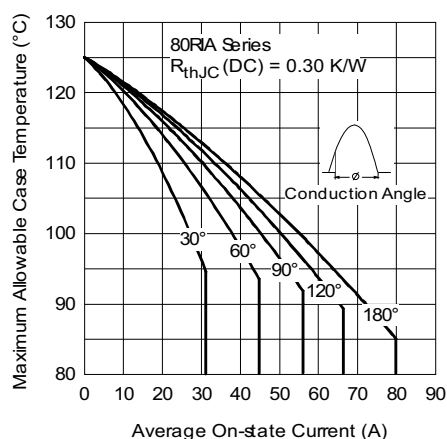


Fig. 1 - Current Ratings Characteristics

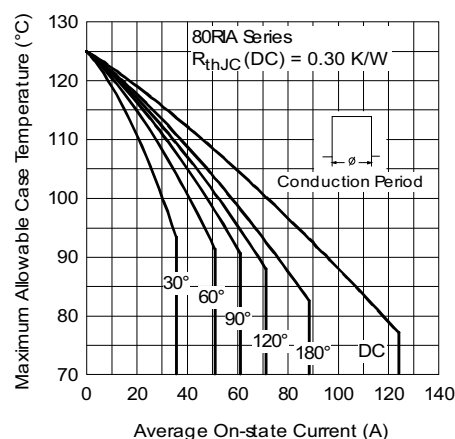


Fig. 2 - Current Ratings Characteristics

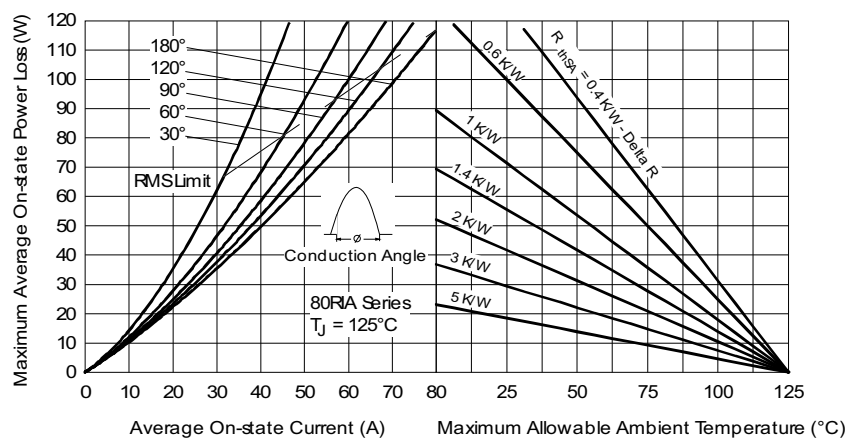


Fig. 3 - On-State Power Loss Characteristics



80RIA...PbF, 81RIA...PbF, 82RIA...PbF Series

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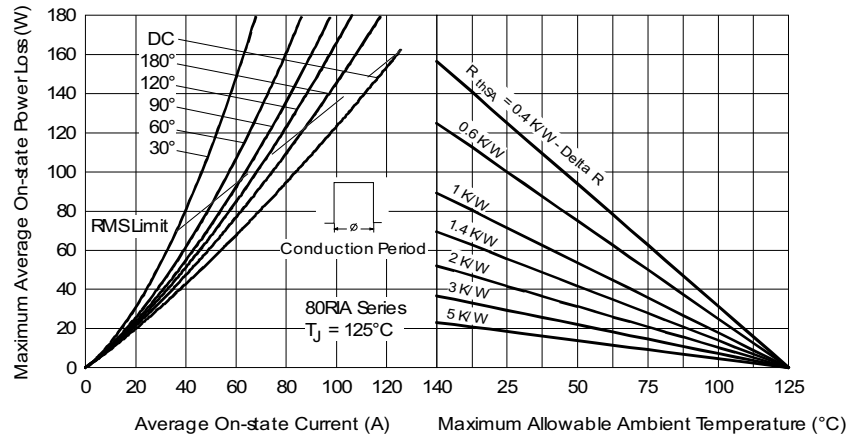


Fig. 4 - On-State Power Loss Characteristics

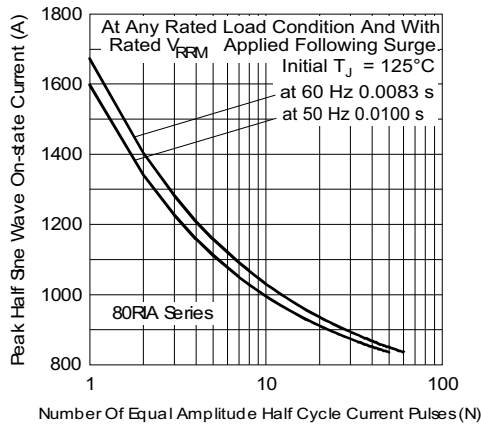


Fig. 5 - Maximum Non-Repetitive Surge Current

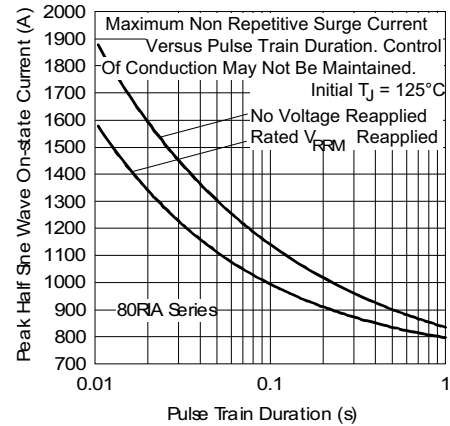


Fig. 6 - Maximum Non-Repetitive Surge Current

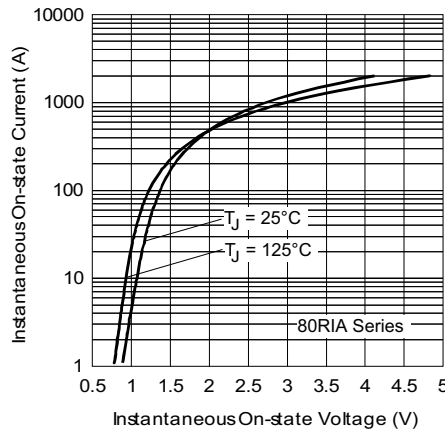


Fig. 7 - On-State Voltage Drop Characteristics

80RIA...PbF, 81RIA...PbF, 82RIA...PbF Series



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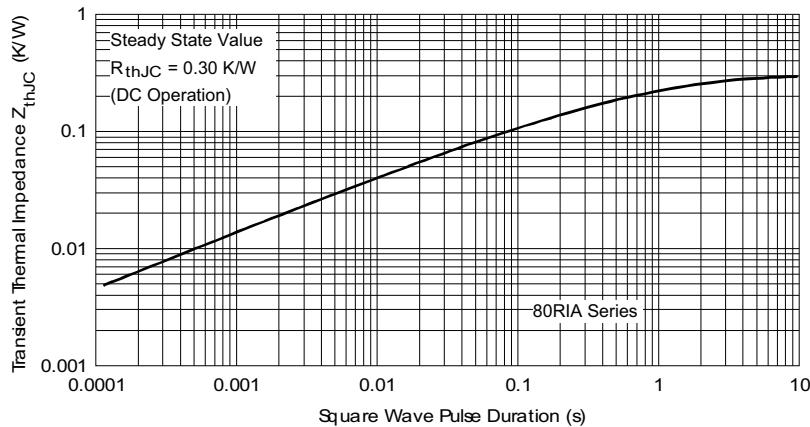


Fig. 8 - Thermal Impedance Z_{thJC} Characteristics

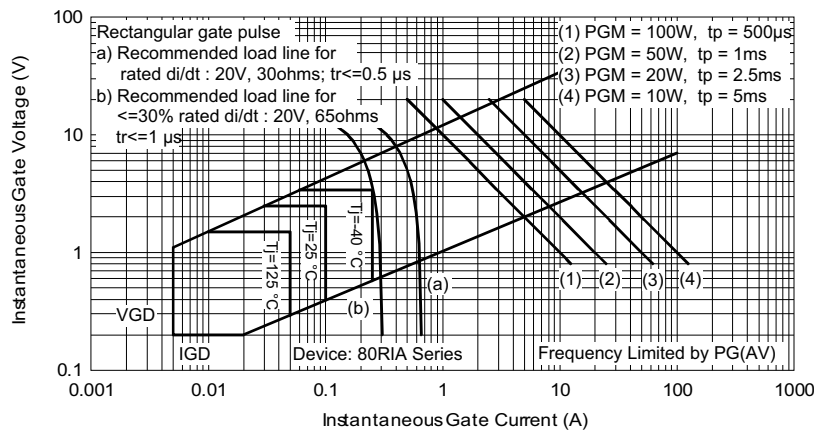


Fig. 9 - Gate Characteristics

ORDERING INFORMATION TABLE

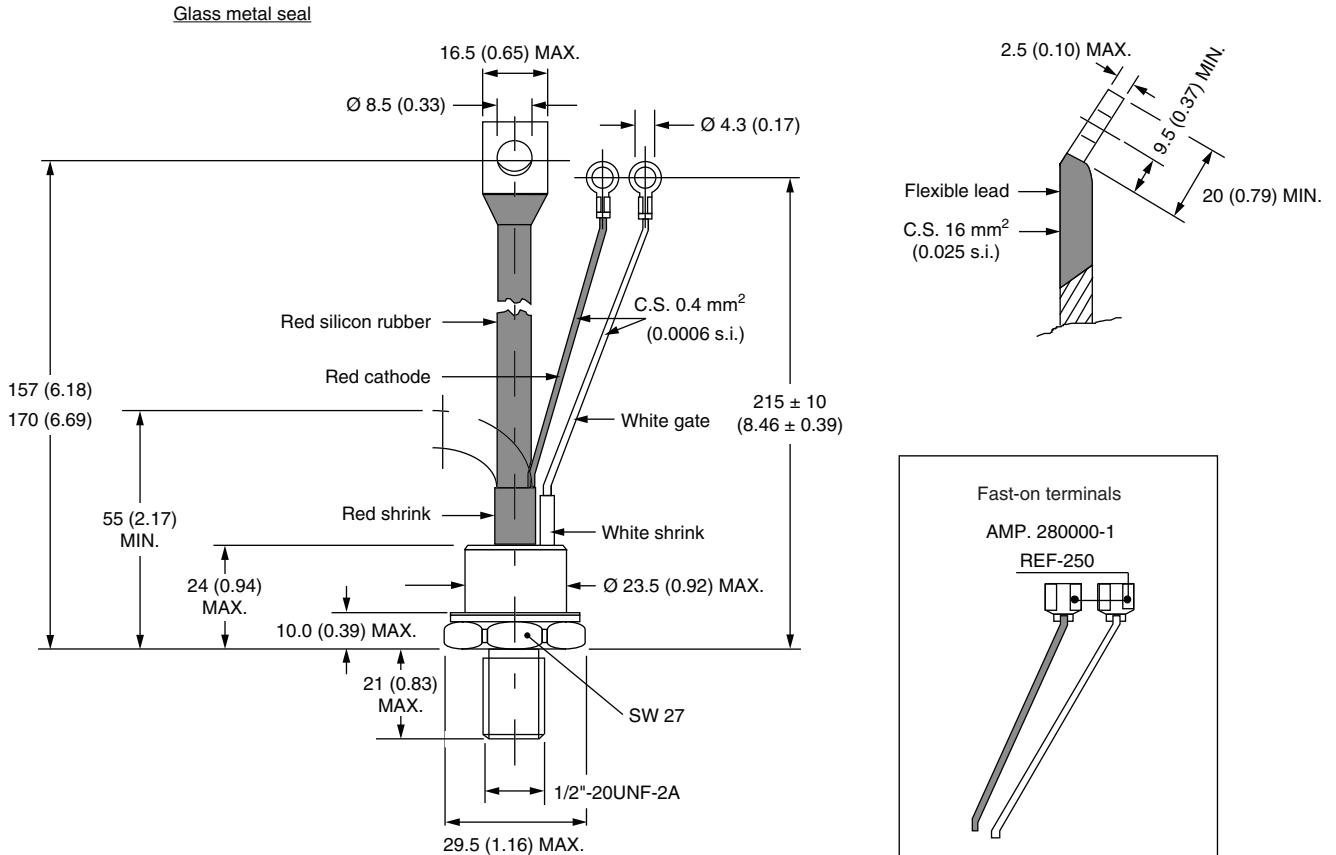
Device code	8	0	RIA	120	M	PbF
	①	②	③	④	⑤	⑥
①	-	$I_{TAV} \times 10 \text{ A}$				
②	-	• 0 = Eyelet terminals (gate and auxiliary cathode leads) • 1 = Fast-on terminals (gate and auxiliary cathode leads) • 2 = Flag terminals (gate and auxiliary cathode terminals)				
③	-	RIA = Essential part number				
④	-	Voltage code $\times 100 = V_{RRM}$ (see Voltage Ratings table)				
⑤	-	• None = Stud base 1/2"-20UNF- 2 A threads • M = Stud base metric threads M12 x 1.75 E 6				
⑥	-	Lead (Pb)-free				

LINKS TO RELATED DOCUMENTS

Dimensions	www.vishay.com/doc?95362
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TO-209AC (TO-94) for 80RIA Series

DIMENSIONS in millimeters (inches)





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