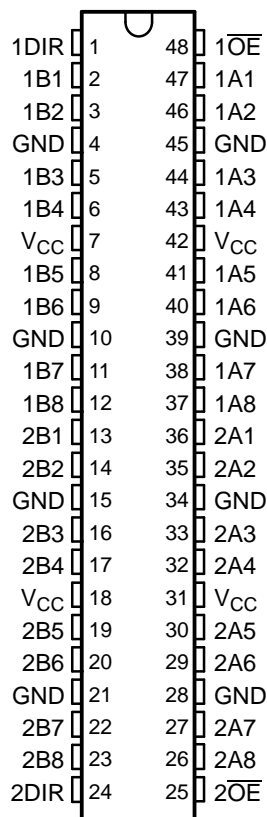


## FEATURES

- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- Typical  $V_{OLP}$  (Output Ground Bounce) <1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs ( $-32\text{-mA } I_{OH}$ ,  $64\text{-mA } I_{OL}$ )
- Latch-Up Performance Exceeds 500 mA Per JESD 70
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )
- Package Options Includes Plastic Thin Very Small-Outline (DGV), Shrink Small-Outline (DL), and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic (WD) Flat Package Using 25-mil Center-to-Center Spacings

SN54ABT16245A . . . WD PACKAGE  
SN74ABT16245A . . . DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



## DESCRIPTION

The 'ABT16245A devices are 16-bit noninverting 3-state transceivers designed for synchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated.

When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16245A is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT16245A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54ABT16245A, SN74ABT16245A

## 16-BIT BUS TRANSCEIVERS

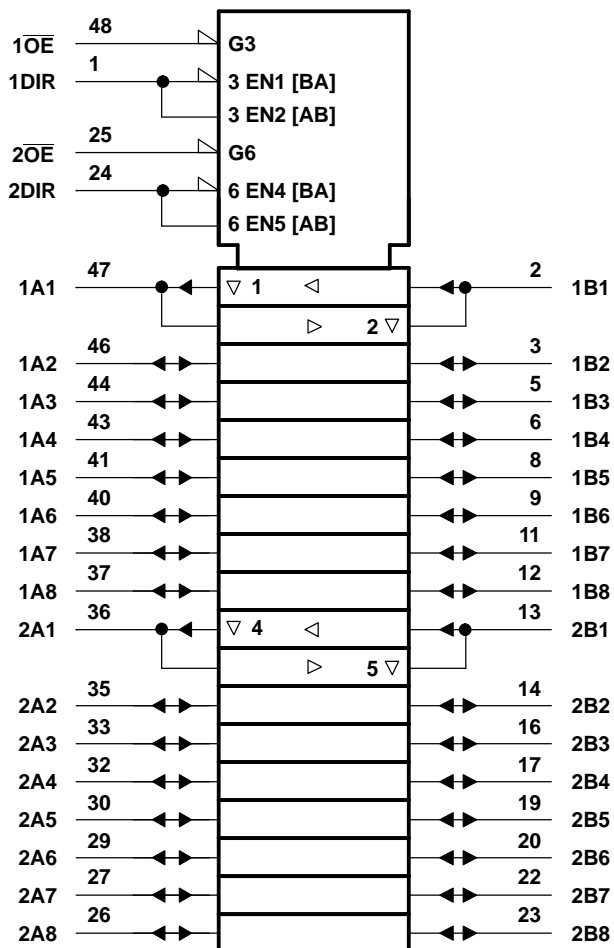
### WITH 3-STATE OUTPUTS

SCBS300G—MARCH 1994—REVISED JANUARY 2006

**FUNCTION TABLE**  
**(EACH 8-BIT SECTION)**

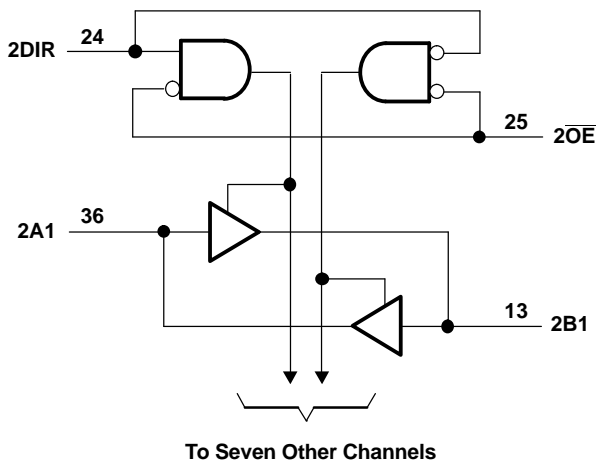
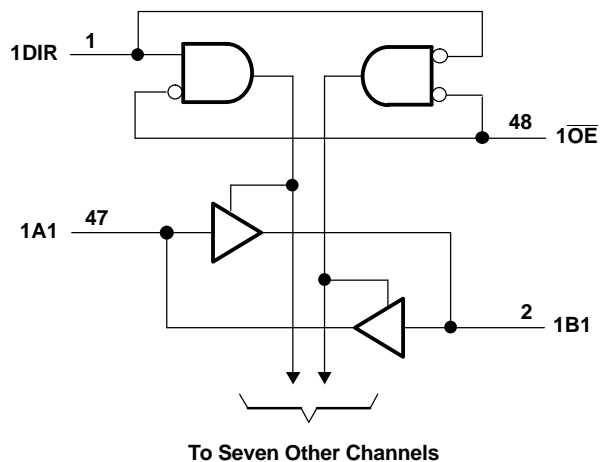
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

**LOGIC SYMBOL <sup>(1)</sup>**



(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### LOGIC DIAGRAM (POSITIVE LOGIC)



### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		−0.5	7	V
V <sub>I</sub>	Input voltage range (except I/O ports) <sup>(2)</sup>		−0.5	7	V
V <sub>O</sub>	Voltage range applied to any output in the high or power-off state		−0.5	5.5	V
I <sub>O</sub>	Current into any output in the low state	SN54ABT16245A	96		mA
		SN74ABT16245A	128		
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	−18		mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	−50		mA
θ <sub>JA</sub>	Package thermal impedance <sup>(3)</sup>	DGG package	89		°C/W
		DGV package	93		
		DL package	94		
T <sub>stg</sub>	Storage temperature range		−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51.

# SN54ABT16245A, SN74ABT16245A

## 16-BIT BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

SCBS300G—MARCH 1994—REVISED JANUARY 2006

#### Recommended Operating Conditions<sup>(1)</sup>

			SN54ABT16245A		SN74ABT16245A		UNIT
			MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2		V
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current			–24		–32	mA
I <sub>OL</sub>	Low-level output current			48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate		200		200		μs/V
T <sub>A</sub>	Operating free-air temperature		–55	125	–40	85	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54ABT16245A		SN74ABT16245A		UNIT
			MIN	TYP <sup>(1)</sup>	MAX	MIN	MAX	MIN	MAX	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2		-1.2		-1.2	V
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA	2.5			2.5		2.5		V
		V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA	3			3		3		
		V <sub>CC</sub> = 4.5 V	2			2				
			2 <sup>(2)</sup>					2		
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V			0.55		0.55			V
					0.55 <sup>(2)</sup>				0.55	
V <sub>hys</sub>				100						mV
I <sub>I</sub>	Control inputs	V <sub>CC</sub> = 0 to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND			±1		±1		±1	μA
	A or B port	V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND			±20 <sup>(2)</sup>		±100		±20	
I <sub>OZPU</sub>		V <sub>CC</sub> = 0 to 2.1 V, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE}$ = X			±50 <sup>(3)</sup>		±50 <sup>(3)</sup>		±50	μA
I <sub>OZPD</sub>		V <sub>CC</sub> = 2.1 V to 0, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE}$ = X			±50 <sup>(3)</sup>		±50 <sup>(3)</sup>		±50	μA
I <sub>OZH</sub> <sup>(4)</sup>		V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 2.7 V, $\overline{OE}$ ≥ 2 V			10 <sup>(5)</sup>		10		10 <sup>(5)</sup>	μA
I <sub>OZL</sub> <sup>(4)</sup>		V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 0.5 V, OE ≥ 2 V			-10 <sup>(5)</sup>		-10		-10 <sup>(5)</sup>	μA
I <sub>off</sub>		V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 5.5 V			±100				±100	μA
I <sub>CEX</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V			50		50		50	μA
I <sub>O</sub> <sup>(6)</sup>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V	-50	-100	-180	-50	-180	-50	-180	mA
I <sub>CC</sub>	A or B port	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND			2		2		2	mA
					32		32		32	
					2		2		2	
ΔI <sub>CC</sub> <sup>(7)</sup>	Data inputs	V <sub>CC</sub> = 5.5 V, One inputs at 3.4 V, Other inputs at V <sub>CC</sub> or GND			2		1.5		2	mA
					0.05		1		0.05	
	Control inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND			1.5		1.5		1.5	
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 2.5 V or 0.5 V		3						pF
C <sub>o</sub>	A or B port	V <sub>O</sub> = 2.5 V or 0.5 V		6						pF

(1) All typical values are at V<sub>CC</sub> = 5 V.

(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

(3) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(4) The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

(5) This limit may vary among suppliers.

(6) Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

(7) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V<sub>CC</sub> or GND.

# SN54ABT16245A, SN74ABT16245A

## 16-BIT BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

SCBS300G—MARCH 1994—REVISED JANUARY 2006

### Switching Characteristics

over recommended operating ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF  
(unless otherwise noted) (see [Figure 1](#) )

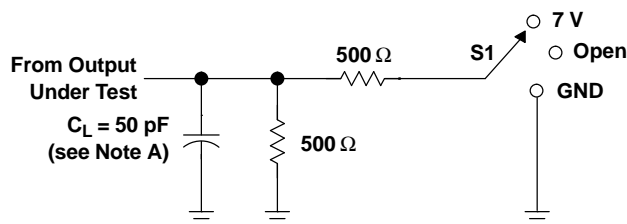
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT16245A					UNIT
			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t <sub>PLH</sub>	A or B	B or A	0.5	2.2	3.4	0.5	4	ns
t <sub>PHL</sub>			0.5	2.3	3.8	0.5	4.6	
t <sub>PZH</sub>	OE	B or A	0.8	3.6	5.2	0.8	5.5	ns
t <sub>PZL</sub>			0.9	3.7	6.1	0.1	7.3	
t <sub>PHZ</sub>	OE	B or A	1.3	4.4	5.8	1.3	6.3	ns
t <sub>PLZ</sub>			1.4	3.3	4.7	1.4	5.5	

### Switching Characteristics

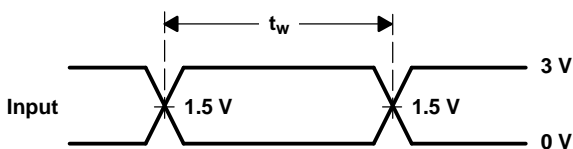
over recommended operating ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF  
(unless otherwise noted) (see [Figure 1](#) )

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT16245A					UNIT
			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t <sub>PLH</sub>	A or B	B or A	1	2.2	3.4	1	3.9	ns
t <sub>PHL</sub>			1	2.3	3.7	1	4.2	
t <sub>PZH</sub>	OE	B or A	1	3.6	5.2	1	6.3	ns
t <sub>PZL</sub>			1	3.7	5.4	1	6.4	
t <sub>PHZ</sub>	OE	B or A	2	4.4	5.8	2	6.3	ns
t <sub>PLZ</sub>			1.5	3.3	4.7	1.5	5.2	

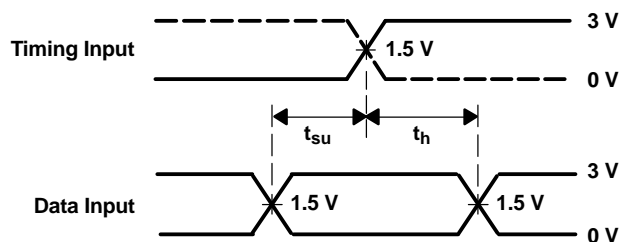
## PARAMETER MEASUREMENT INFORMATION



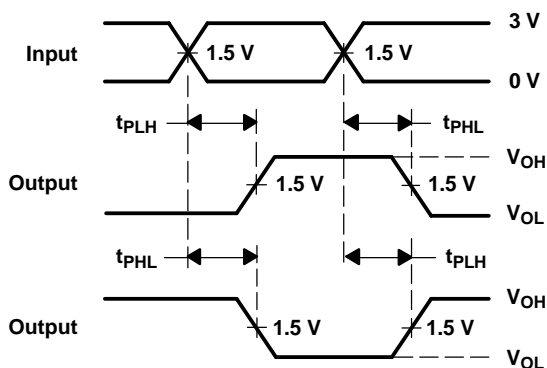
LOAD CIRCUIT



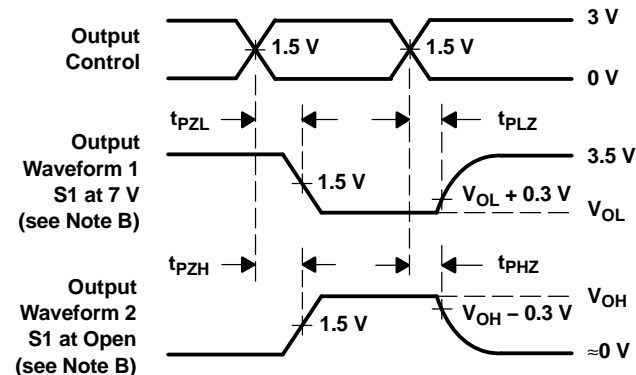
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
5962-9317501MXA	ACTIVE	CFP	WD	48	1	TBD	Call TI	Call TI	
74ABT16245ADGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74ABT16245ADGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74ABT16245ADGVRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT16245ADGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT16245ADGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT16245ADL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT16245ADLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT16245ADLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT16245ADLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ54ABT16245AWD	ACTIVE	CFP	WD	48	1	TBD	A42	N / A for Pkg Type	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.



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**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF SN54ABT16245A, SN74ABT16245A :**

- Catalog: [SN74ABT16245A](#)
- Enhanced Product: [SN74ABT16245A-EP](#), [SN74ABT16245A-EP](#)
- Military: [SN54ABT16245A](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT16245ADGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74ABT16245ADGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74ABT16245ADLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

## TAPE AND REEL BOX DIMENSIONS

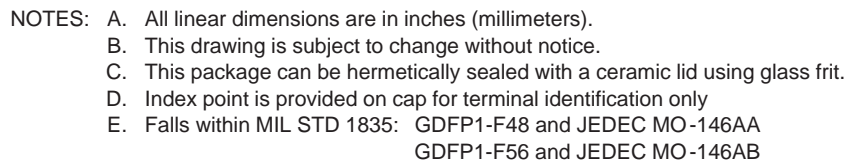


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT16245ADGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74ABT16245ADGVR	TVSOP	DGV	48	2000	367.0	367.0	38.0
SN74ABT16245ADLR	SSOP	DL	48	1000	367.0	367.0	55.0

## CERAMIC DUAL FLATPACK

48 LEADS SHOWN



## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DL (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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