

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ C7

600V CoolMOS™ C7 Power Transistor
IPA60R060C7

Data Sheet

Rev. 2.0
Final

1 Description

CoolMOS™ C7 is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies.

600V CoolMOS™ C7 series combines the experience of the leading SJ MOSFET supplier with high class innovation.

The 600V C7 is the first technology ever with $R_{DS(on)} \cdot A$ below $10\text{m}\Omega \cdot \text{mm}^2$.

Features

- Suitable for hard and soft switching (PFC and high performance LLC)
- Increased MOSFET dv/dt ruggedness to 120V/ns
- Increased efficiency due to best in class FOM $R_{DS(on)} \cdot E_{oss}$ and $R_{DS(on)} \cdot Q_g$
- Best in class $R_{DS(on)}$ /package
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)

Benefits

- Increased economies of scale by use in PFC and PWM topologies in the application
- Higher dv/dt limit enables faster switching leading to higher efficiency
- Enabling higher system efficiency by lower switching losses
- Increased power density solutions due to smaller packages
- Suitable for applications such as server, telecom and solar
- Higher switching frequencies possible without loss in efficiency due to low E_{oss} and Q_g

Applications

PFC stages and PWM stages (TTF, LLC) for high power/performance SMPS e.g. Computing, Server, Telecom, UPS and Solar.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

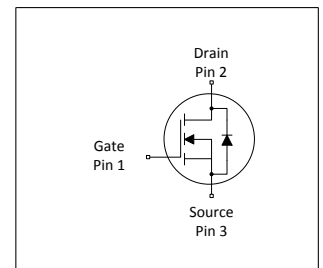


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	60	mΩ
$Q_{g,typ}$	68	nC
$I_{D,pulse}$	135	A
$I_{D,continuous} @ T_j < 150^\circ\text{C}$	54	A
$E_{oss}@400\text{V}$	8.1	μJ
Body diode di/dt	420	A/μs

Type / Ordering Code	Package	Marking	Related Links
IPA60R060C7	PG-TO 220 FullPAK	60C7060	see Appendix A

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2 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	16 10	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	135	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	159	mJ	$I_D=6.4\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.80	mJ	$I_D=6.4\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche current, single pulse	I_{AS}	-	-	6.4	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f>1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	34	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-55	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	50	Ncm	M2.5 screws
Continuous diode forward current	I_S	-	-	16	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	135	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	20	V/ns	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq 9.9\text{A}$, $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di/dt	-	-	420	A/ μs	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq 9.9\text{A}$, $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage	V_{ISO}	-	-	2500	V	V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{min}$

¹⁾ Limited by $T_{j,max}$.

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch

3 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	3.69	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	°C/W	lead
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	-	-	°C/W	n.a.
Soldering temperature, wavesoldering only allowed at leads	T_{sld}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

4 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	$V_{GS}=0\text{V}$, $I_D=1\text{mA}$
Gate threshold voltage	$V_{(GS)th}$	3	3.5	4	V	$V_{DS}=V_{GS}$, $I_D=0.8\text{mA}$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=600$, $V_{GS}=0\text{V}$, $T_j=25^\circ\text{C}$ $V_{DS}=600$, $V_{GS}=0\text{V}$, $T_j=150^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20\text{V}$, $V_{DS}=0\text{V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.052 0.115	0.060 -	Ω	$V_{GS}=10\text{V}$, $I_D=15.9\text{A}$, $T_j=25^\circ\text{C}$ $V_{GS}=10\text{V}$, $I_D=15.9\text{A}$, $T_j=150^\circ\text{C}$
Gate resistance	R_G	-	0.8	-	Ω	$f=1\text{MHz}$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	2850	-	pF	$V_{GS}=0\text{V}$, $V_{DS}=400\text{V}$, $f=250\text{kHz}$
Output capacitance	C_{oss}	-	54	-	pF	$V_{GS}=0\text{V}$, $V_{DS}=400\text{V}$, $f=250\text{kHz}$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	101	-	pF	$V_{GS}=0\text{V}$, $V_{DS}=0\dots400\text{V}$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	1050	-	pF	$I_D=\text{constant}$, $V_{GS}=0\text{V}$, $V_{DS}=0\dots400\text{V}$
Turn-on delay time	$t_{d(on)}$	-	15.5	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=15.9\text{A}$, $R_G=3.3\Omega$; see table 9
Rise time	t_r	-	11	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=15.9\text{A}$, $R_G=3.3\Omega$; see table 9
Turn-off delay time	$t_{d(off)}$	-	79	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=15.9\text{A}$, $R_G=3.3\Omega$; see table 9
Fall time	t_f	-	4	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=15.9\text{A}$, $R_G=3.3\Omega$; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	14	-	nC	$V_{DD}=400\text{V}$, $I_D=15.9\text{A}$, $V_{GS}=0$ to 10V
Gate to drain charge	Q_{gd}	-	23	-	nC	$V_{DD}=400\text{V}$, $I_D=15.9\text{A}$, $V_{GS}=0$ to 10V
Gate charge total	Q_g	-	68	-	nC	$V_{DD}=400\text{V}$, $I_D=15.9\text{A}$, $V_{GS}=0$ to 10V
Gate plateau voltage	V_{plateau}	-	5.0	-	V	$V_{DD}=400\text{V}$, $I_D=15.9\text{A}$, $V_{GS}=0$ to 10V

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0V$, $I_F=15.9A$, $T_J=25^{\circ}C$
Reverse recovery time	t_{rr}	-	390	-	ns	$V_R=400V$, $I_F=15.9A$, $di_F/dt=100A/\mu s$; see table 8
Reverse recovery charge	Q_{rr}	-	6	-	μC	$V_R=400V$, $I_F=15.9A$, $di_F/dt=100A/\mu s$; see table 8
Peak reverse recovery current	I_{rrm}	-	32	-	A	$V_R=400V$, $I_F=15.9A$, $di_F/dt=100A/\mu s$; see table 8

5 Electrical characteristics diagrams

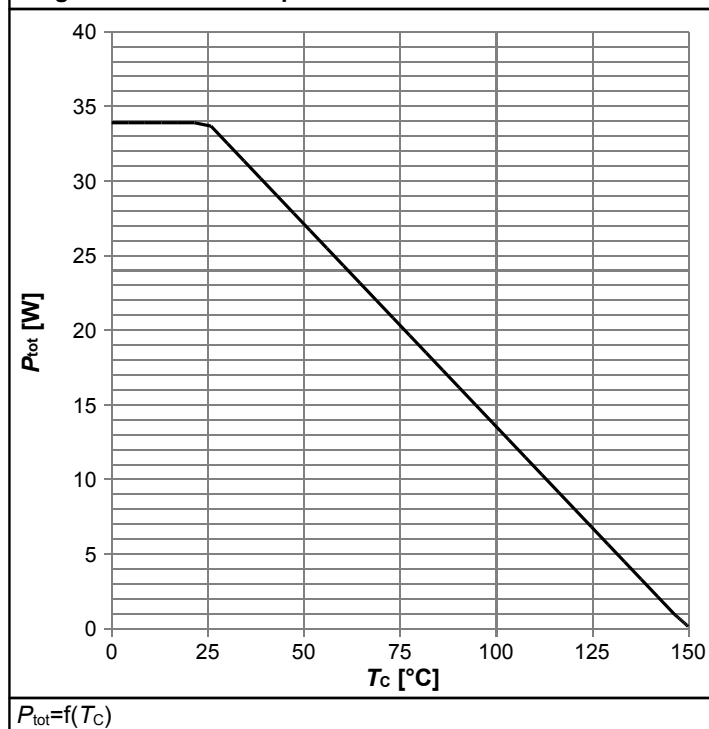
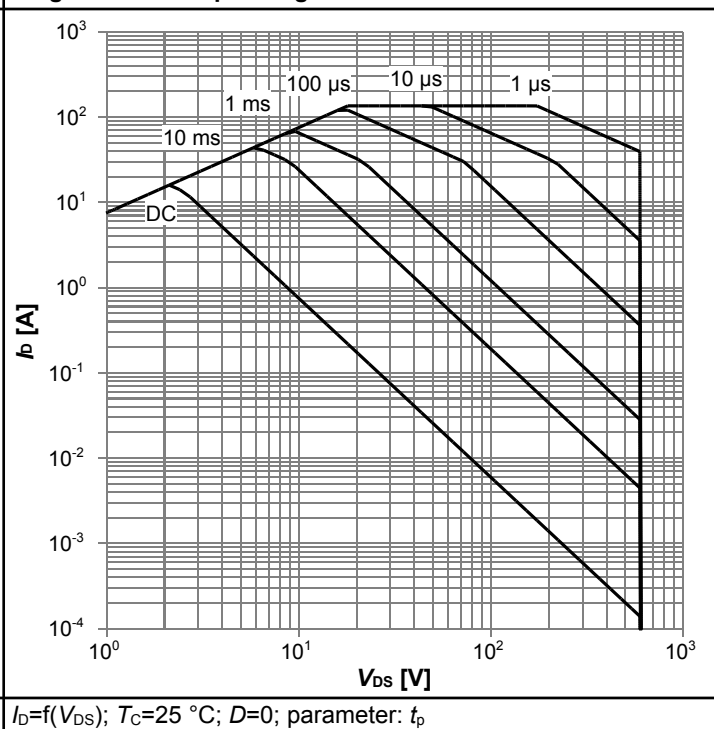
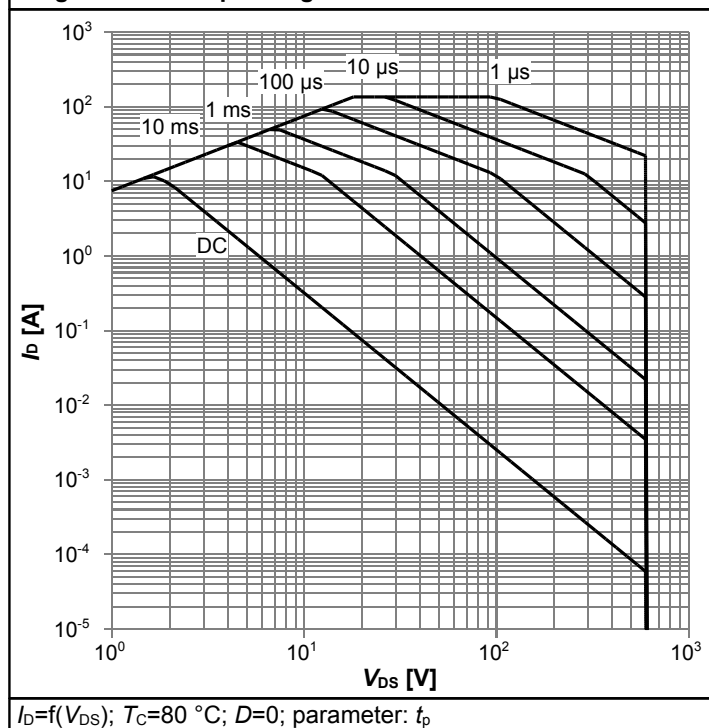
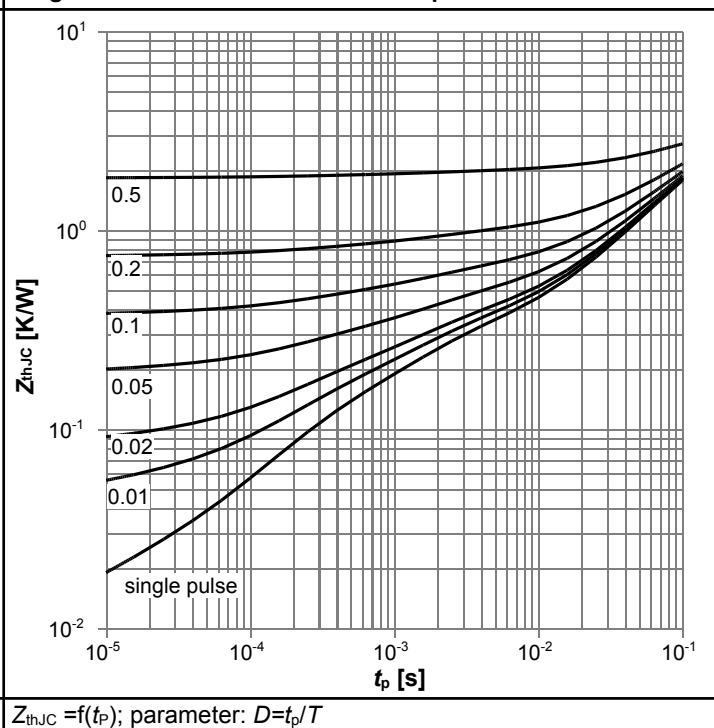
Diagram 1: Power dissipation

Diagram 2: Safe operating area

Diagram 3: Safe operating area

Diagram 4: Max. transient thermal impedance


Diagram 5: Typ. output characteristics


 $I_D = f(V_{DS}); T_J = 25^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 6: Typ. output characteristics


 $I_D = f(V_{DS}); T_J = 125^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 7: Typ. drain-source on-state resistance

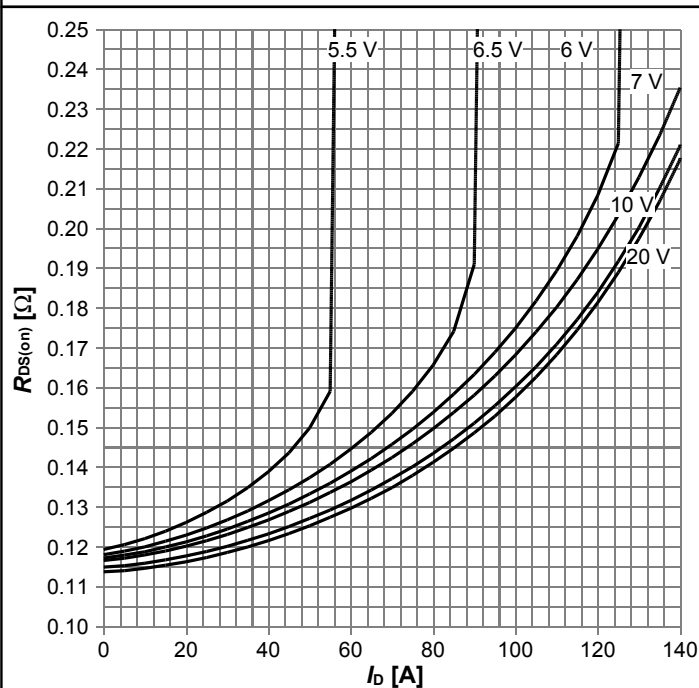

 $R_{DS(on)} = f(I_D); T_J = 125^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 8: Drain-source on-state resistance

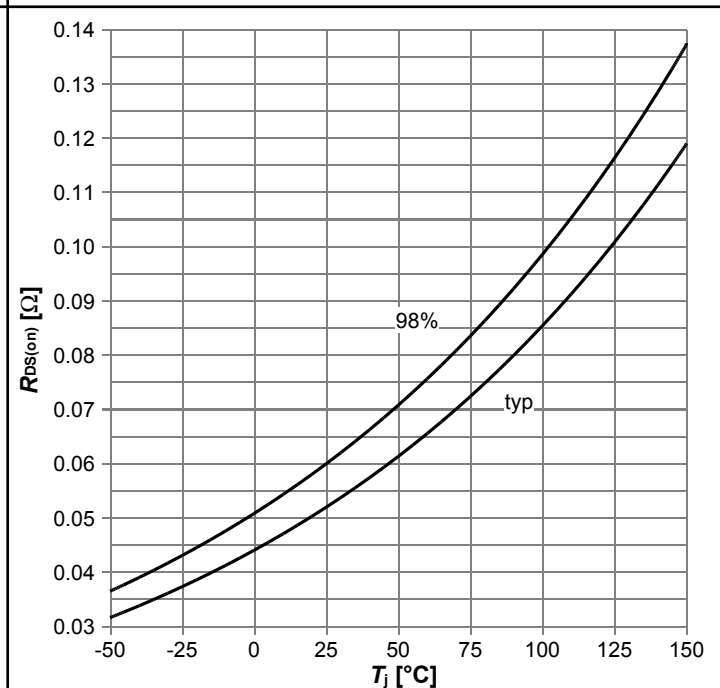

 $R_{DS(on)} = f(T_J); I_D = 15.9\text{ A}; V_{GS} = 10\text{ V}$

Diagram 9: Typ. transfer characteristics

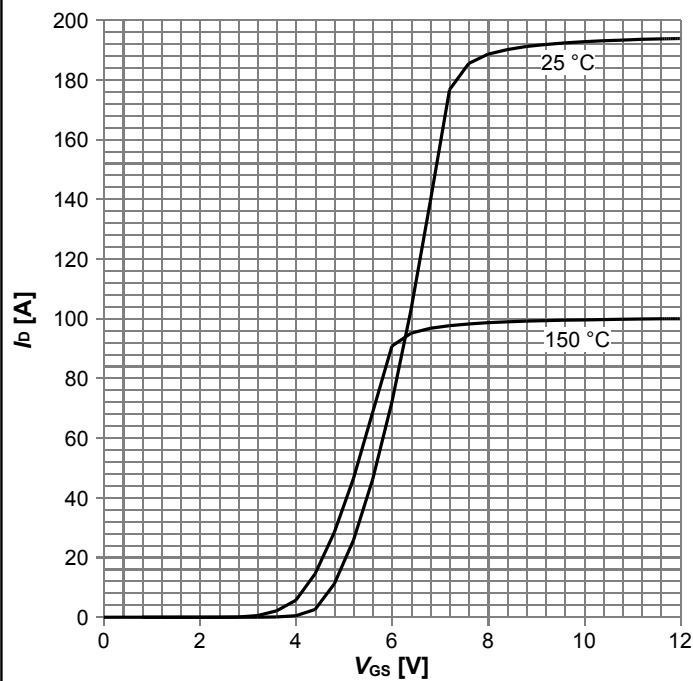

 $I_D = f(V_{GS}); V_{DS} = 20V; \text{parameter: } T_j$

Diagram 10: Typ. gate charge

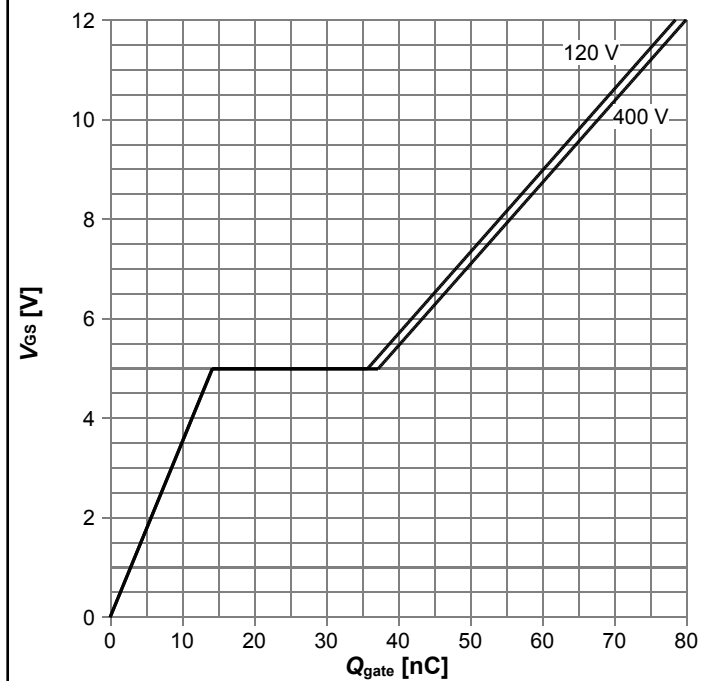

 $V_{GS} = f(Q_{gate}); I_D = 15.9 \text{ A pulsed}; \text{parameter: } V_{DD}$

Diagram 11: Forward characteristics of reverse diode

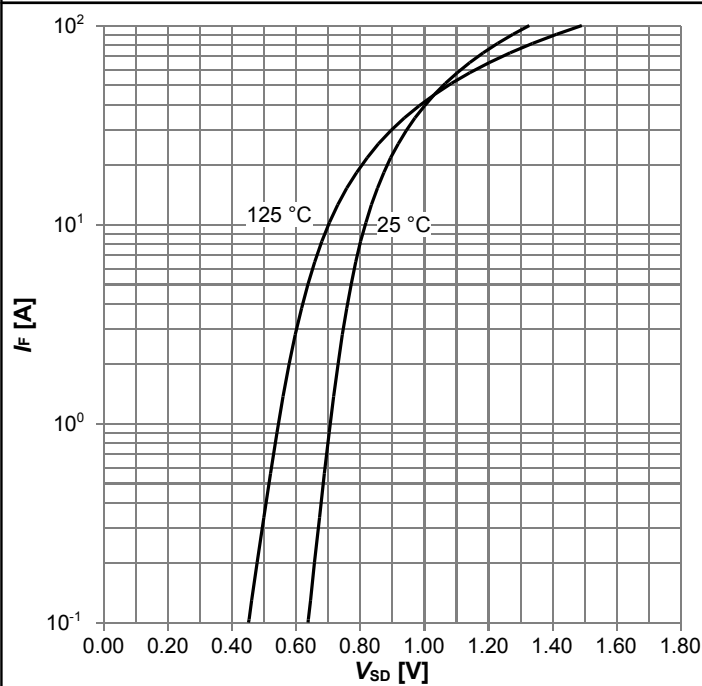

 $I_F = f(V_{SD}); \text{parameter: } T_j$

Diagram 12: Avalanche energy

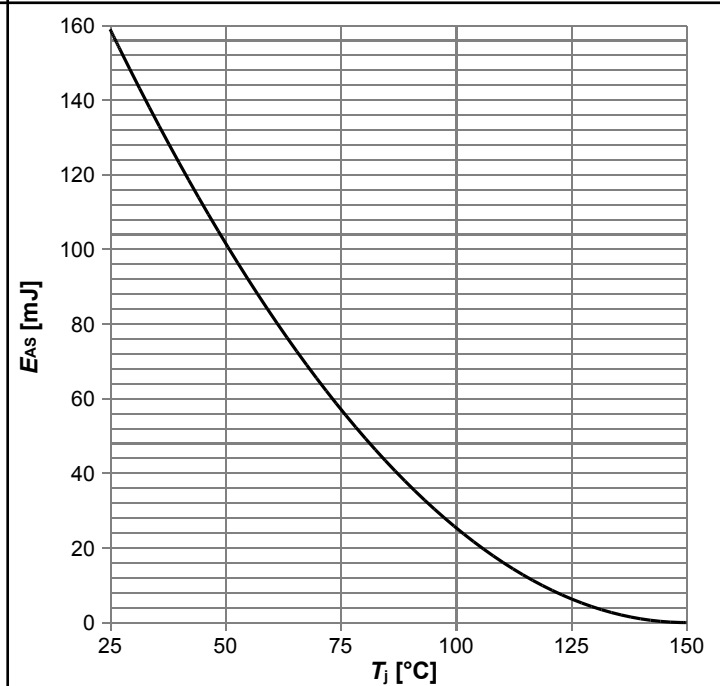

 $E_{AS} = f(T_j); I_D = 6.4 \text{ A}; V_{DD} = 50 \text{ V}$

Diagram 13: Drain-source breakdown voltage



$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$

Diagram 14: Typ. capacitances



$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 250 \text{ kHz}$$

Diagram 15: Typ. Coss stored energy



$$E_{oss} = f(V_{DS})$$

6 Test Circuits

Table 8 Diode characteristics

Figure 1 consists of two parts. The left part is a schematic diagram of a test circuit for diode characteristics. It shows two diodes connected in series. The first diode is connected to a voltage source V_{DS} through a resistor R_{g1} . The second diode is connected to a current source I_F through a resistor R_{g2} . The circuit is powered by a battery. The right part is a graph of the diode recovery waveform. The vertical axis is labeled V, I and the horizontal axis is labeled t . The graph shows the voltage V_{DS} and current I_F over time. The current I_F is initially at a constant value I_F and then decreases linearly with a slope dI_F/dt . The voltage V_{DS} is initially at a constant value V_{DS} and then increases linearly with a slope dV_{DS}/dt . The recovery time t_{rr} is defined as the time from the start of the current decrease to the point where the current reaches $10\% I_{rm}$. The graph also shows the forward charge Q_F and reverse charge Q_S areas under the current curve.

Table 9 Switching times

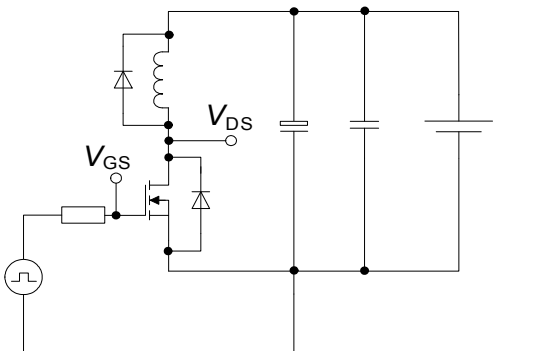
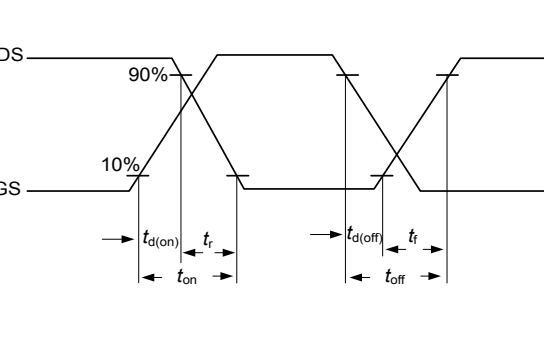
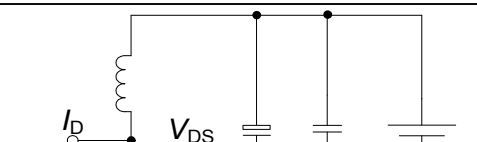
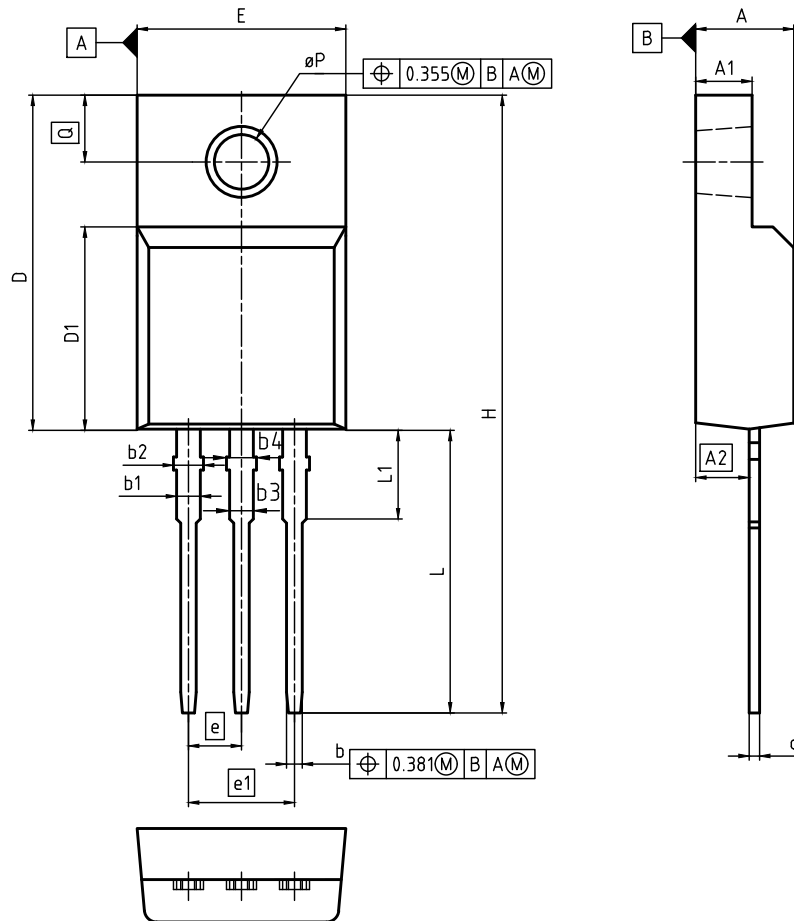
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 **Unclamped inductive load**

Unclamped inductive load test circuit	Unclamped inductive waveform
	

7 Package Outlines



DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.50	4.90	0.177	0.193
A1	2.34	2.85	0.092	0.112
A2	2.42	2.86	0.095	0.113
b	0.65	0.90	0.026	0.035
b1	0.95	1.38	0.037	0.054
b2	0.95	1.51	0.037	0.059
b3	0.65	1.38	0.026	0.054
b4	0.65	1.51	0.026	0.059
c	0.40	0.63	0.016	0.025
D	15.67	16.15	0.617	0.636
D1	8.97	9.83	0.353	0.387
E	10.00	10.65	0.394	0.419
e	2.54 (BSC)		0.100 (BSC)	
e1	5.08		0.200	
N	3		3	
H	28.70	29.75	1.130	1.171
L	12.78	13.75	0.503	0.541
L1	2.83	3.45	0.111	0.136
øP	2.95	3.38	0.116	0.133
Q	3.15	3.50	0.124	0.138

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Figure 1 Outline PG-TO 220 FullPAK, dimensions in mm/inches

8 Appendix A

Table 11 Related Links

- IFX CoolMOS™ C7 Webpage: www.infineon.com
- IFX CoolMOS™ C7 application note: www.infineon.com
- IFX CoolMOS™ C7 simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPA60R060C7

Revision: 2015-12-01, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2015-12-01	Release of final version

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

moschip.ru_4

moschip.ru_6

moschip.ru_9