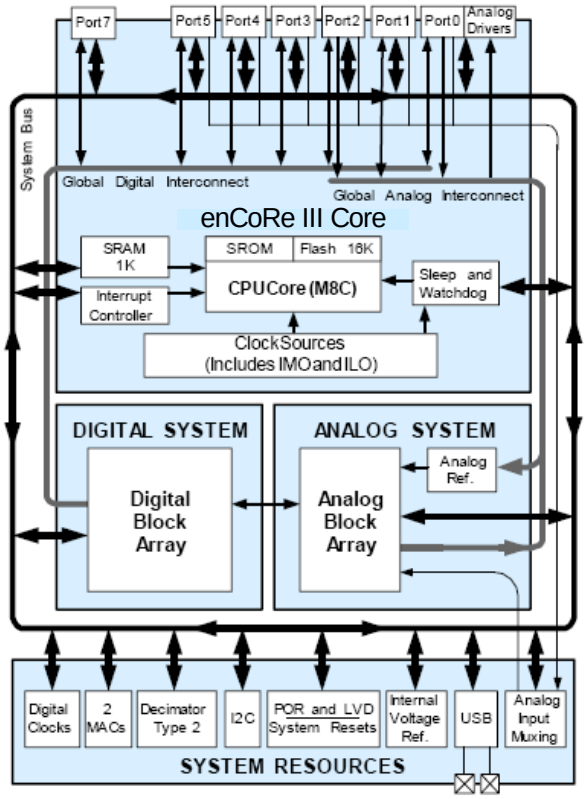
CY7C64215

enCoRe™ III Full Speed USB Controller

Features

- Powerful Harvard Architecture Processor
  - M8C Processor Speeds to 24 MHz
  - Two 8x8 Multiply, 32-Bit Accumulate
  - 3.15 to 5.25V Operating Voltage
  - USB 2.0 USB-IF Certified. TID# 40000110
  - Commercial Operating Temperature Range: 0°C to +70°C
  - Industrial Operating Temperature Range: –40°C to +85°C
- Advanced Peripherals (enCoRe™ III Blocks)
  - 6 Analog enCoRe III Blocks provide:
    - Up to 14-Bit Incremental and Delta Sigma ADCs
  - Programmable Threshold Comparator
  - Four Digital enCoRe III Blocks Provide:
    - 8-Bit and 16-Bit PWMs, Timers, and Counters
    - I^2C Master
    - SPI Master or Slave
    - Full Duplex UART
    - CYFISNP and CYFISPI Modules to Talk to Cypress CYFI Radio
- Complex Peripherals by Combining Blocks
- Full Speed USB (12 Mbps)
  - Four Unidirectional Endpoints
  - One Bidirectional Control Endpoint
  - Dedicated 256 Byte Buffer
  - No External Crystal Required
  - Operational at 3.15V to 3.5V or 4.35V to 5.25V
- Flexible On-Chip Memory
  - 16K Flash Program Storage 50,000 Erase/Write Cycles
  - 1K SRAM Data Storage
  - In-System Serial Programming (ISSP)
  - Partial Flash Updates
  - Flexible Protection Modes
  - EEPROM Emulation in Flash
- Programmable Pin Configurations
  - 25 mA Sink on all GPIO
  - Pull Up, Pull Down, High Z, Strong, or Open Drain Drive Modes on all GPIO
  - Configurable Interrupt on all GPIO
- Precision, Programmable Clocking
  - Internal ±4% 24 and 48 MHz Oscillator with Support for External Clock Oscillator
  - Internal Oscillator for Watchdog and Sleep
  - .25% Accuracy for USB with no External Components
- Additional System Resources
  - I^2C Slave, Master, and Multi-Master to 400 kHz
  - Watchdog and Sleep Timers
  - User-Configurable Low Voltage Detection
  - Integrated Supervisory Circuit
  - On-Chip Precision Voltage Reference
- Complete Development Tools
  - Free Development Software (PSoC Designer™)
  - Full Featured, In-Circuit Emulator and Programmer
  - Full Speed Emulation
  - Complex Breakpoint Structure
  - 128K Bytes Trace Memory

Block Diagram



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Applications

- PC HID devices
  - Mouse (Optomechanical, Optical, Trackball)
  - Keyboards
  - Joysticks
- Gaming
  - Game Pads
  - Console Keyboards
- General Purpose
  - Barcode Scanners
  - POS Terminal
  - Consumer Electronics
  - Toys
  - Remote Controls
  - USB to Serial

enCoRe III Functional Overview

The enCoRe III is based on flexible PSoC architecture and is a full featured, full speed (12 Mbps) USB part. Configurable analog, digital, and interconnect circuitry enable a high level of integration in a host of consumer, and communication applications.

This architecture enables the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in both 28-pin SSOP and 56-pin QFN packages.

enCoRe III architecture, as illustrated in the "Block Diagram" on page 1, is comprised of four main areas: enCoRe III Core, Digital System, Analog System, and System Resources including a full speed USB port. Configurable global busing enables all the device resources to combine into a complete custom system. The enCoRe III CY7C64215 can have up to seven I/O ports that connect to the global digital and analog interconnects, providing access to 4 digital blocks and 6 analog blocks.

enCoRe III Core

The enCoRe III Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIO (General Purpose I/O).

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with up to 20 vectors, to simplify programming of real-time embedded events. Program execution is timed and protected using the included Sleep and Watch Dog Timers (WDT).

Memory encompasses 16K of Flash for program storage, 1K of SRAM for data storage, and up to 2K of EEPROM emulated using the Flash. Program Flash uses four protection levels on blocks of 64 bytes, enabling customized software IP protection.

enCoRe III incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator) accurate to 8% over temperature and voltage as well as an option for an external clock oscillator. USB operation requires the OSC LOCK bit of the USB_CR0 register to be set to obtain IMO accuracy to .25%.

The 24 MHz IMO is doubled to 48 MHz for use by the digital system, if needed. The 48 MHz clock is required to clock the USB block and must be enabled for communication. A low power 32 kHz ILO (internal low speed oscillator) is provided for the Sleep Timer and WDT. The clocks, together with programmable clock dividers (System Resource), provide flexibility to integrate almost any timing requirement into enCoRe III. In USB systems, the IMO self-tunes to ±0.25% accuracy for USB communication.

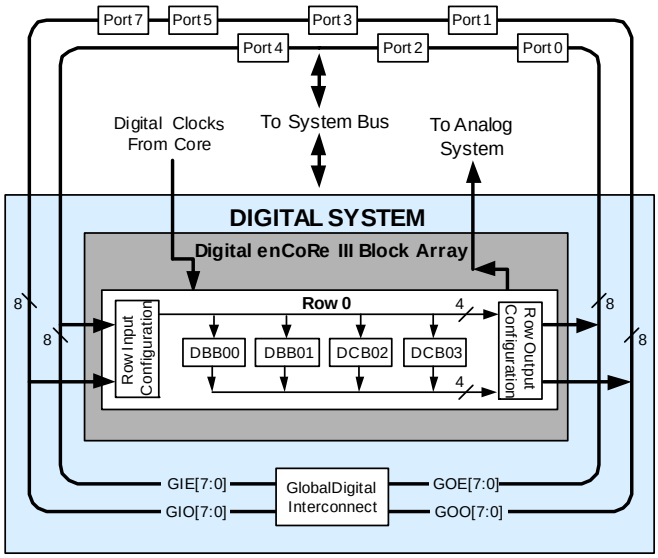
The extended temperature range for the Industrial operating range (–40°C to +85°C) requires the use of an external clock oscillator, which is only available on the 56-pin QFN package.

enCoRe III GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin's drive mode may be selected from eight options, enabling great flexibility in external interfacing. Every pin also has capability to generate a system interrupt on high level, low level, and change from last read.

The Digital System

The Digital System is composed of four digital enCoRe III blocks. Each block is an 8-bit resource that is used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.

Figure 1. Digital System Block Diagram



The following digital configurations can be built from the blocks:

- PWMs, Timers, and Counters (8-bit and 16-bit)
- UART 8-bit with selectable parity
- SPI master and slave
- I^2C Master
- RF Interface: Interface to Cypress CYFI Radio

The digital blocks are connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also enable signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

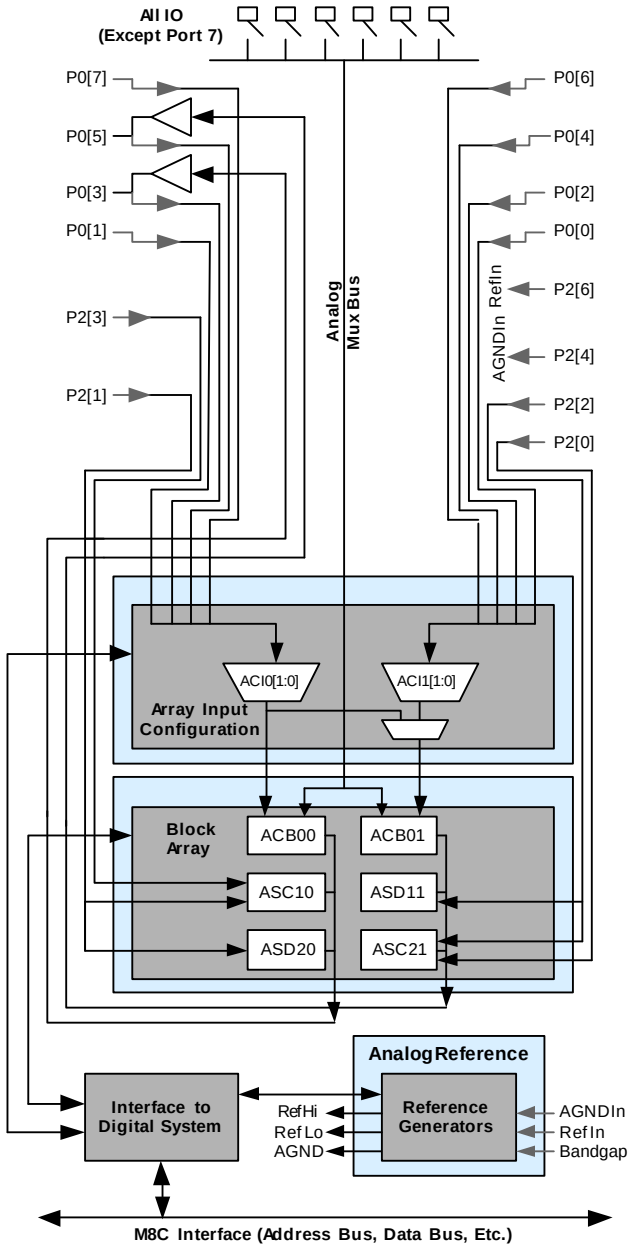
[+] Feedback

The Analog System

The Analog System is composed of six configurable blocks, comprised of an opamp circuit enabling the creation of complex analog signal flows. Analog peripherals are very flexible and are customized to support specific application requirements. enCoRe III analog function supports the Analog-to-digital converters (with 6 to 14-bit resolution, selectable as Incremental, and Delta Sigma) and programmable threshold comparator).

Analog blocks are arranged in two columns of three, with each column comprising one CT (Continuous Time - AC B00 or AC B01) and two SC (Switched Capacitor - ASC10 and ASD20 or ASD11 and ASC21) blocks, as shown in Figure 2.

Figure 2. Analog System Block Diagram



The Analog Multiplexer System

The Analog Mux Bus can connect to every GPIO pin in ports 0–5. Pins which are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with comparators and analog-to-digital converters. It is split into two sections for simultaneous dual-channel processing. An additional 8:1 analog input multiplexer provides a second path to bring Port 0 pins to the analog array.

Additional System Resources

System Resources provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, low voltage detection, and power-on reset. Brief statements describing the merits of each resource follow.

- Full Speed USB (12 Mbps) with five configurable endpoints and 256 bytes of RAM. No external components required except two series resistors. Industrial temperature operating range for USB requires an external clock oscillator.
- Two multiply accumulates (MACs) provide fast 8-bit multipliers with 32-bit accumulate, to assist in both general math and digital filters.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of Delta Sigma ADCs.
- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks are routed to both the digital and analog systems.
- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.

enCoRe III Device Characteristics

enCoRe III devices have four digital blocks and six analog blocks. The following table lists the resources available for specific enCoRe III devices.

Table 1. enCoRe III Device Characteristics

Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY7C64215 28 Pin	up to 22	1	4	22	2	2	6	1K	16K
CY7C64215 56 Pin	up to 50	1	4	48	2	2	6	1K	16K

Getting Started

The quickest path to understanding the enCoRe III silicon is by reading this data sheet and using the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the enCoRe V integrated circuit and presents specific pin, register, and electrical specifications. For in-depth information, along with detailed programming information, reference the *PSoC Programmable System-on-Chip Technical Reference Manual*, which can be found on http://www.cypress.com/psoc.

For up-to-date Ordering, Packaging, and Electrical Specification information, reference the latest enCoRe V device data sheets on the web at http://www.cypress.com/go/usb.

Development Kits

Development Kits are available online from Cypress at www.cypress.com/shop and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark. Under Product Categories, click USB (Universal Serial Bus) to view a current list of available items.

Technical Training Modules

Free technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

Consultants

Certified USB consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to www.cypress.com/cypros.

Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at www.cypress.com/support. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs. They are located here: www.cypress.com/psoc. Select Application Notes under the Documentation tab.

Development Tools

PSoC Designer is a Microsoft® Windows® based, integrated development environment for enCoRe III. The PSoC Designer IDE and application runs on Windows XP or Vista.

PSoC Designer helps the customer to select an operating configuration for the enCoRe III, write application code that uses the enCoRe III, and debug the application. This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and the CYASM macro assembler for the CPUs. PSoC Designer also supports a high-level C language compiler developed specifically for the devices in the family.

PSoC Designer Software Subsystems

Device Editor

The Device Editor subsystem enables the user to select different onboard analog and digital components called user modules using the enCoRe III blocks. Examples of user modules are ADCs, SPIM, UART, and PWMs.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration enables changing configurations at run time.

PSoC Designer sets up power on initialization tables for selected enCoRe III block configurations and creates source code for an application framework. The framework contains software to operate the selected components and, if the project uses more than one operating configuration, contains routines to switch between different sets of enCoRe III block configurations at run time. PSoC Designer can print out a configuration sheet for a given project configuration for use during application programming in conjunction with the Device Data Sheet. Once the framework is generated, the user can add application-specific code to flesh out the framework. It is also possible to change the selected components and regenerate the framework.

Application Editor

In the Application Editor you can edit your C language and Assembly language source code. You can also assemble, compile, link, and build.

Assembler. The macro assembler enables the assembly code to merge seamlessly with C code. The link libraries automatically use absolute addressing or is compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compiler. A C language compiler is available that supports the enCoRe III family of devices. Even if you have never worked in the C language before, the product quickly enables you to create complete C programs for the enCoRe III devices.

The embedded, optimizing C compiler provides all the features of C tailored to the enCoRe III architecture. It comes complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, enabling the designer to test the program in a physical system while providing an internal view of the enCoRe III device. Debugger commands enable the designer to read and program and read and write data memory, read and write I/O registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also enables the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

Hardware Tools

In-Circuit Emulator

A low cost, high functionality ICE Cube is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal which operates with all enCoRe III devices.

Designing with User Modules

The development process for the enCoRe III device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the enCoRe III architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called enCoRe III Blocks, have the ability to implement a wide variety of user-selectable functions. Each block has several registers that determine its function and connectivity to other blocks, multiplexers, buses and to the I/O pins. Iterative development cycles permit you to adapt the hardware and software. This substantially lowers the risk of having to select a different part to meet the final design requirements.

To speed the development process, the PSoC Designer Integrated Development Environment (IDE) provides a library of pre-built, pre-tested hardware peripheral functions, called “User Modules.” User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and mixed signal varieties.

The user module library contains the following digital and analog module designs:

- Analog Blocks
  - Incremental ADC (ADCINC)
  - Delta Sigma ADC (DelSig)
  - Programmable Threshold Comparator (CMPPRG)
- Digital Blocks
  - Counters: 8-bit and 16-bit (Counter8 and Counter 16)
  - PWMs: 8-bit and 16-bit (PWM8 and PWM16)
  - Timers: 8-bit and 16-bit (Timer8 and Timer 16)
  - I^2C Master (I^2CM)
  - SPI Master (SPIM)
  - SPI Slave (SPIS)
  - Full Duplex UART (UART)
  - RF (CYFISNP and CYFISPI)
- System Resources
  - Protocols:
    - USBFS
    - I2C Bootheader (Boothdr I^2C)
    - USB Bootheader (BoothdrUSBFS)
    - USBUART
  - Digital System Resources
    - E2PROM
    - LCD
    - LED
    - 7-segment LED (LED7SEG)
    - Shadow Registers (SHADOWREG)
    - Sleep Timer

Each user module establishes the basic register settings that implement the selected function. It also provides parameters that enable you to tailor its precise configuration to your particular application. For example, a Pulse Width Modulator User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit the designer to establish the pulse width and duty cycle. User modules also provide tested software to cut development time. The user module application programming interface (API) provides high-level functions to control and respond to hardware events at run-time. The API also provides optional interrupt service routines that is adapted as needed.

The API functions are documented in user module data sheets that are viewed directly in the PSoC Designer IDE. These data sheets explain the internal operation of the user module and provide performance specifications. Each data sheet describes the use of each user module parameter and documents the setting of each register controlled by the user module.

The development process starts when you open a new project and bring up the Device Editor/Chip Layout View, a graphical user interface (GUI) for configuring the hardware. You pick the user modules you need for your project and map them onto the PSoC blocks with point-and-click simplicity. Next, you build signal chains by interconnecting user modules to each other and the I/O pins. At this stage, you also configure the clock source connections and enter parameter values directly or by selecting values from drop-down menus. When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Application” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the high-level user module API functions.

The next step is to write your main program, and any sub-routines using PSoC Designer’s Application Editor subsystem. The Application Editor includes a Project Manager that enables you to open the project source code files (including all generated code files) from a hierarchal view. The source code editor provides syntax coloring and advanced edit features for both C and assembly language. File search capabilities include simple string searches and recursive “grep-style” patterns. A single mouse click invokes the Build Manager. It employs a professional-strength “makefile” system to automatically analyze all file dependencies and run the compiler and assembler as necessary. Project level options control optimization strategies used by the compiler and linker. Syntax errors are displayed in a console window. Double clicking the error message takes you directly to the offending line of source code. When all is correct, the linker builds a HEX file image suitable for programming.

The last step in the development process takes place inside the PSoC Designer’s Debugger subsystem. The Debugger downloads the HEX image to the In-Circuit Emulator (ICE CUBE) where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and enables you define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

Document Conventions

Acronyms Used

The following table lists the acronyms that are used in this document.

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CPU	central processing unit
CT	continuous time
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
FSR	full scale range
GPIO	general purpose I/O
GUI	graphical user interface
HBM	human body model
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
PC	program counter
PLL	phase-locked loop
POR	power on reset
PPOR	precision power on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse width modulator
SC	switched capacitor
SRAM	static random access memory
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
I/O	input/output
IPOR	imprecise power on reset

Units of Measure

A units of measure table is located in the Electrical Specifications section. Table 5 on page 13 lists all the abbreviations used to measure the enCoRe III devices.

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (For example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimal.

Pin Information

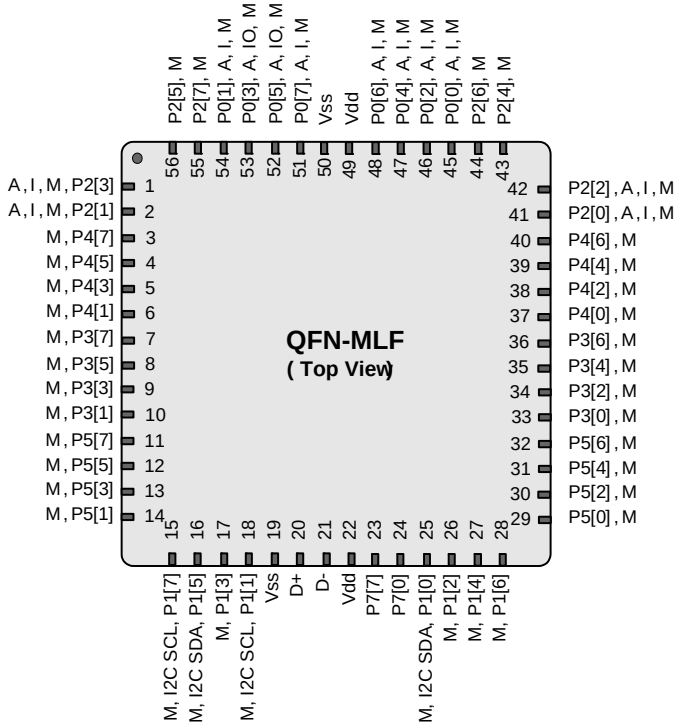
56-Pin Part Pinout

The CY7C64215 enCoRe III device is available in a 56-pin package which is listed and illustrated in the following table. Every port pin (labeled “P”) is capable of Digital I/O. However, Vss and Vdd are not capable of Digital I/O.

Table 2. 56-Pin Part Pinout (QFN-MLF SAWN)[1]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I, M	P2[3]	Direct Switched Capacitor Block Input.
2	I/O	I, M	P2[1]	Direct Switched Capacitor Block Input.
3	I/O	M	P4[7]	
4	I/O	M	P4[5]	
5	I/O	M	P4[3]	
6	I/O	M	P4[1]	
7	I/O	M	P3[7]	
8	I/O	M	P3[5]	
9	I/O	M	P3[3]	
10	I/O	M	P3[1]	
11	I/O	M	P5[7]	
12	I/O	M	P5[5]	
13	I/O	M	P5[3]	
14	I/O	M	P5[1]	
15	I/O	M	P1[7]	I2C Serial Clock (SCL).
16	I/O	M	P1[5]	I2C Serial Data (SDA).
17	I/O	M	P1[3]	
18	I/O	M	P1[1]	I2C Serial Clock (SCL), ISSP-SCLK.
19	Power		Vss	Ground Connection.
20	USB		D+	
21	USB		D-	
22	Power		Vdd	Supply Voltage.
23	I/O		P7[7]	
24	I/O		P7[0]	
25	I/O	M	P1[0]	I2C Serial Data (SDA), ISSP-SDATA.
26	I/O	M	P1[2]	
27	I/O	M	P1[4]	Optional External Clock Input EXTCLK.
28	I/O	M	P1[6]	
29	I/O	M	P5[0]	
30	I/O	M	P5[2]	
31	I/O	M	P5[4]	
32	I/O	M	P5[6]	
33	I/O	M	P3[0]	
34	I/O	M	P3[2]	
35	I/O	M	P3[4]	
36	I/O	M	P3[6]	
37	I/O	M	P4[0]	
38	I/O	M	P4[2]	
39	I/O	M	P4[4]	
40	I/O	M	P4[6]	
41	I/O	I, M	P2[0]	Direct Switched Capacitor Block Input.
42	I/O	I, M	P2[2]	Direct Switched Capacitor Block Input.
43	I/O	M	P2[4]	External Analog Ground (AGND) Input.
44	I/O	M	P2[6]	External Voltage Reference (VREF) Input.
45	I/O	I, M	P0[0]	Analog Column Mux Input.
46	I/O	I, M	P0[2]	Analog Column Mux Input and Column Output.
47	I/O	I, M	P0[4]	Analog Column Mux Input and Column Output.
48	I/O	I, M	P0[6]	Analog Column Mux Input.
49	Power		Vdd	Supply Voltage.
50	Power		Vss	Ground Connection.
51	I/O	I, M	P0[7]	Analog Column Mux Input.
52	I/O	I/O, M	P0[5]	Analog Column Mux Input and Column Output
53	I/O	I/O, M	P0[3]	Analog Column Mux Input and Column Output.
54	I/O	I, M	P0[1]	Analog Column Mux Input.
55	I/O	M	P2[7]	
56	I/O	M	P2[5]	

Figure 3. CY7C64215 56-Pin enCoRe III Device



LEGEND A = Analog, I = Input, O = Output, and M = Analog Mux Input.

Note
1. The center pad on the QFN-MLF package should be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.

[+] Feedback

28-Pin Part Pinout

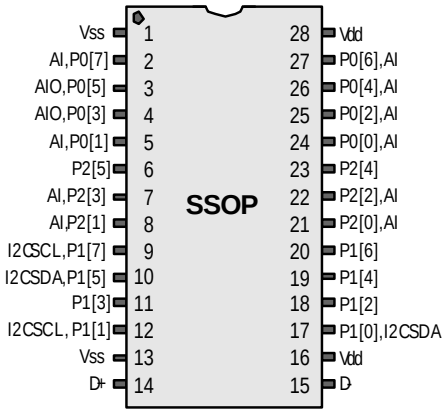
The CY7C64215 enCoRe III device is available in a 28-pin package which is listed and illustrated in the following table. Every port pin (labeled with a “P”) is capable of Digital I/O. However, Vss and Vdd are not capable of Digital I/O.

Table 3. 28-Pin Part Pinout (SSOP)

Pin No.	Type		Name	Description
	Digital	Analog		
1	Power		GND	Ground Connection.
2	I/O	I, M	P0[7]	Analog Column Mux Input.
3	I/O	I/O,M	P0[5]	Analog Column Mux Input and Column Output.
4	I/O	I/O,M	P0[3]	Analog Column Mux Input and Column Output.
5	I/O	I,M	P0[1]	Analog Column Mux Input.
6	I/O	M	P2[5]	
7	I/O	M	P2[3]	Direct Switched Capacitor Block Input.
8	I/O	M	P2[1]	Direct Switched Capacitor Block Input.
9	I/O	M	P1[7]	I2C Serial Clock (SCL).
10	I/O	M	P1[5]	I2C Serial Data (SDA).
11	I/O	M	P1[3]	
12	I/O	M	P1[1]	I2C Serial Clock (SCL), ISSP-SCLK.
13	Power		GND	Ground Connection.
14	USB		D+	
15	USB		D-	
16	Power		Vdd	Supply Voltage.
17	I/O	M	P1[0]	I2C Serial Data (SDA), ISSP-SDATA.
18	I/O	M	P1[2]	
19	I/O	M	P1[4]	
20	I/O	M	P1[6]	
21	I/O	M	P2[0]	Direct Switched Capacitor Block Input.
22	I/O	M	P2[2]	Direct Switched Capacitor Block Input.
23	I/O	M	P2[4]	External Analog Ground (AGND) Input.
24	I/O	M	P0[0]	Analog Column Mux Input.
25	I/O	M	P0[2]	Analog Column Mux Input and Column Output.
26	I/O	M	P0[4]	Analog Column Mux Input and Column Output.
27	I/O	M	P0[6]	Analog Column Mux Input.
28	Power		Vdd	Supply Voltage.

LEGEND A = Analog, I = Input, O = Output, and M = Analog Mux Input.

Figure 4. CY7C64215 28-Pin enCoRe III Device



[+] Feedback

Register Reference

The register conventions specific to this section are listed in the following table.

Table 4. Register Conventions

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The enCoRe III device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set the user is in Bank 1.

Note In the following register mapping tables, blank fields are Reserved and should not be accessed.

[+] Feedback

Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	PMA0_DR	40	RW	ASC10CR0	80	RW		C0	
PRT0IE	01	RW	PMA1_DR	41	RW	ASC10CR1	81	RW		C1	
PRT0GS	02	RW	PMA2_DR	42	RW	ASC10CR2	82	RW		C2	
PRT0DM2	03	RW	PMA3_DR	43	RW	ASC10CR3	83	RW		C3	
PRT1DR	04	RW	PMA4_DR	44	RW	ASD11CR0	84	RW		C4	
PRT1IE	05	RW	PMA5_DR	45	RW	ASD11CR1	85	RW		C5	
PRT1GS	06	RW	PMA6_DR	46	RW	ASD11CR2	86	RW		C6	
PRT1DM2	07	RW	PMA7_DR	47	RW	ASD11CR3	87	RW		C7	
PRT2DR	08	RW	USB_SOF0	48	R		88			C8	
PRT2IE	09	RW	USB_SOF1	49	R		89			C9	
PRT2GS	0A	RW	USB_CR0	4A	RW		8A			CA	
PRT2DM2	0B	RW	USBIO_CR0	4B	#		8B			CB	
PRT3DR	0C	RW	USBIO_CR1	4C	RW		8C			CC	
PRT3IE	0D	RW		4D			8D			CD	
PRT3GS	0E	RW	EP1_CNT1	4E	#		8E			CE	
PRT3DM2	0F	RW	EP1_CNT	4F	RW		8F			CF	
PRT4DR	10	RW	EP2_CNT1	50	#	ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW	EP2_CNT	51	RW	ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW	EP3_CNT1	52	#	ASD20CR2	92	RW		D2	
PRT4DM2	13	RW	EP3_CNT	53	RW	ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW	EP4_CNT1	54	#	ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW	EP4_CNT	55	RW	ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW	EP0_CR	56	#	ASC21CR2	96	RW	I2C_CFG	D6	RW
PRT5DM2	17	RW	EP0_CNT	57	#	ASC21CR3	97	RW	I2C_SCR	D7	#
	18		EP0_DR0	58	RW		98		I2C_DR	D8	RW
	19		EP0_DR1	59	RW		99		I2C_MSCR	D9	#
	1A		EP0_DR2	5A	RW		9A		INT_CLR0	DA	RW
	1B		EP0_DR3	5B	RW		9B		INT_CLR1	DB	RW
PRT7DR	1C	RW	EP0_DR4	5C	RW		9C		INT_CLR2	DC	RW
PRT7IE	1D	RW	EP0_DR5	5D	RW		9D		INT_CLR3	DD	RW
PRT7GS	1E	RW	EP0_DR6	5E	RW		9E		INT_MSK3	DE	RW
PRT7DM2	1F	RW	EP0_DR7	5F	RW		9F		INT_MSK2	DF	RW
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W	AMUXCFG	61	RW		A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCB02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCB02DR2	2A	RW		6A		MUL1_DH	AA	R	MUL0_DH	EA	R
DCB02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCB03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCB03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCB03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCB03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD		DAC_D	FD	RW
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	PMA0_WA	40	RW	ASC10CR0	80	RW	USBIO_CR2	C0	RW
PRT0DM1	01	RW	PMA1_WA	41	RW	ASC10CR1	81	RW	USB_CR1	C1	#
PRT0IC0	02	RW	PMA2_WA	42	RW	ASC10CR2	82	RW			
PRT0IC1	03	RW	PMA3_WA	43	RW	ASC10CR3	83	RW			
PRT1DM0	04	RW	PMA4_WA	44	RW	ASD11CR0	84	RW	EP1_CR0	C4	#
PRT1DM1	05	RW	PMA5_WA	45	RW	ASD11CR1	85	RW	EP2_CR0	C5	#
PRT1IC0	06	RW	PMA6_WA	46	RW	ASD11CR2	86	RW	EP3_CR0	C6	#
PRT1IC1	07	RW	PMA7_WA	47	RW	ASD11CR3	87	RW	EP4_CR0	C7	#
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
PRT3DM0	0C	RW		4C			8C			CC	
PRT3DM1	0D	RW		4D			8D			CD	
PRT3IC0	0E	RW		4E			8E			CE	
PRT3IC1	0F	RW		4F			8F			CF	
PRT4DM0	10	RW	PMA0_RA	50	RW		90		GDI_O_IN	D0	RW
PRT4DM1	11	RW	PMA1_RA	51	RW	ASD20CR1	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW	PMA2_RA	52	RW	ASD20CR2	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW	PMA3_RA	53	RW	ASD20CR3	93	RW	GDI_E_OU	D3	RW
PRT5DM0	14	RW	PMA4_RA	54	RW	ASC21CR0	94	RW		D4	
PRT5DM1	15	RW	PMA5_RA	55	RW	ASC21CR1	95	RW		D5	
PRT5IC0	16	RW	PMA6_RA	56	RW	ASC21CR2	96	RW		D6	
PRT5IC1	17	RW	PMA7_RA	57	RW	ASC21CR3	97	RW		D7	
	18			58			98		MUX_CR0	D8	RW
	19			59			99		MUX_CR1	D9	RW
	1A			5A			9A		MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
PRT7DM0	1C	RW		5C			9C			DC	
PRT7DM1	1D	RW		5D			9D		OSC_GO_EN	DD	RW
PRT7IC0	1E	RW		5E			9E		OSC_CR4	DE	RW
PRT7IC1	1F	RW		5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW	CMP_GO_EN	64	RW		A4		VLT_CMP	E4	R
DBB01IN	25	RW		65	RW		A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68			A8		IMO_TR	E8	W
DCB02IN	29	RW		69			A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC		MUX_CR4	EC	RW
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD		MUX_CR5	ED	RW
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD		DAC_CR	FD	RW
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

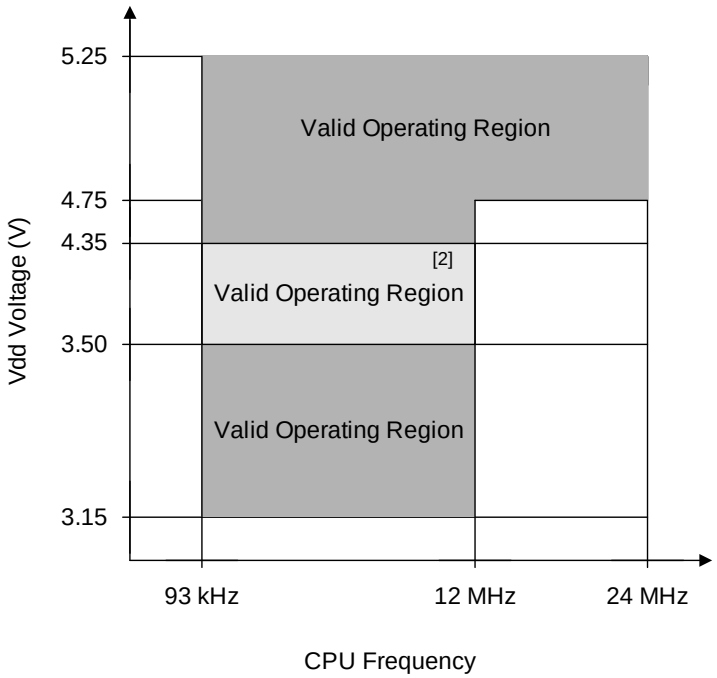
Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY7C64215 enCoRe III. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at http://www.cypress.com/go/usb.

Specifications are valid for –40°C ≤ T_A ≤ 85°C and T_J ≤ 100°C, except where noted. Specifications for devices running at greater than 12 MHz are valid for –40°C ≤ T_A ≤ 70°C and T_J ≤ 82°C.

Figure 5. Voltage versus CPU Frequency



The following table lists the units of measure that are used in this section.

Table 5. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	µW	microwatts
dB	decibels	mA	milliampere
fF	femto farad	ms	millisecond
Hz	hertz	mV	millivolts
KB	1024 bytes	nA	nanoampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolts
kΩ	kilohm	Ω	ohm
MHz	megahertz	pA	picoampere
MΩ	megaohm	pF	picofarad
µA	microampere	pp	peak-to-peak
µF	microfarad	ppm	parts per million
µH	microhenry	ps	picosecond
µs	microsecond	sps	samples per second
µV	microvolts	s	sigma: one standard deviation
µVrms	microvolts root-mean-square	V	volts

Note
2. This is a valid operating region for the CPU, but USB hardware is non-functional in the voltage range from 3.50V – 4.35V.

[+] Feedback

Absolute Maximum Ratings

Table 6. Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{STG}	Storage Temperature	–55	–	+100	°C	Higher storage temperatures reduces data retention time.
T_A	Ambient Temperature with Power Applied	0	–	+70	°C	
Vdd	Supply Voltage on Vdd Relative to Vss	–0.5	–	+6.0	V	
V_{IO}	DC Input Voltage	Vss – 0.5	–	Vdd + 0.5	V	
V_{IO2}	DC Voltage Applied to Tri-state	Vss – 0.5	–	Vdd + 0.5	V	
I_{MIO}	Maximum Current into any Port Pin	–25	–	+50	mA	
I_{MAIO}	Maximum Current into any Port Pin Configured as Analog Driver	–50	–	+50	mA	
ESD	Electro Static Discharge Voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch Up Current	–	–	200	mA	

Operating Temperature

Table 7. Operating Temperature

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{AC}	Commercial Ambient Temperature	0	–	+70	°C	
T_{AI}	Industrial Ambient Temperature	–40	–	+85	°C	USB operation requires the use of an external clock oscillator and the 56-pin QFN package.
T_J	Junction Temperature	–40	–	+100	°C	The temperature rise from ambient to junction is package specific. See “Thermal Impedance” on page 30. The user must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and –40°C ≤ T_A ≤ 85°C, or 3.15V to 3.5V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 8. DC Chip-Level Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
Vdd	Supply Voltage	3.0	–	5.25	V	See DC POR and LVD specifications, Table 16 on page 20. USB hardware is not functional when Vdd is between 3.5V to 4.35V.
I_{DD5}	Supply Current, IMO = 24 MHz (5V)	–	14	27	mA	Conditions are Vdd = 5.0V, T_A = 25°C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off.
I_{DD3}	Supply Current, IMO = 24 MHz (3.3V)	–	8	14	mA	Conditions are Vdd = 3.3V, T_A = 25°C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.367 kHz, analog power = off.
I_{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT.[3]	–	3	6.5	µA	Conditions are with internal slow speed oscillator, Vdd = 3.3V, 0°C ≤ T_A ≤ 55°C, analog power = off.
I_{SBH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT at high temperature.[3]	–	4	25	µA	Conditions are with internal slow speed oscillator, Vdd = 3.3V, 55°C < T_A ≤ 70°C, analog power = off.

DC General Purpose I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and –40°C ≤ T_A ≤ 85°C, or 3.15V to 3.5V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 9. DC GPIO Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
R_{PU}	Pull Up Resistor	4	5.6	8	kΩ	
R_{PD}	Pull down Resistor	4	5.6	8	kΩ	
V_{OH}	High Output Level	Vdd – 1.0	–	–	V	IOH = 10 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined IOH budget.
V_{OL}	Low Output Level	–	–	0.75	V	IOL = 25 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined IOL budget.
I_{OH}	High Level Source Current	10	–	–	mA	
I_{OL}	Low Level Sink Current	25	–	–	mA	
V_{IL}	Input Low Level	–	–	0.8	V	Vdd = 3.15 to 5.25.
V_{IH}	Input High Level	2.1	–		V	Vdd = 3.15 to 5.25.

Note
3. Standby current includes all functions (POR, LVD, WDT, Sleep Time) needed for reliable system operation. This should be compared with devices that have similar functions enabled.

[+] Feedback

Table 9. DC GPIO Specifications (continued)

V_H	Input Hysteresis	–	60	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 µA.
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.

DC Full Speed USB Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges when the IMO is selected as system clock: 4.75V to 5.25V and 0°C ≤ T_A ≤ 70°C, or 3.15V to 3.5V and 0°C ≤ T_A ≤ 70°C, respectively.

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges when an external clock is selected as the system clock: 4.75V to 5.25V and –40°C ≤ T_A ≤ 85°C, or 3.15V to 3.5V and –40°C ≤ T_A ≤ 85°C.

Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 10. DC Full Speed (12 Mbps) USB Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
USB Interface						
V_{DI}	Differential Input Sensitivity	0.2	–	–	V	| (D+) – (D–) |
V_{CM}	Differential Input Common Mode Range	0.8	–	2.5	V	
V_{SE}	Single Ended Receiver Threshold	0.8	–	2.0	V	
C_{IN}	Transceiver Capacitance	–	–	20	pF	
I_{IO}	High Z State Data Line Leakage	–10	–	10	µA	0V < V_{IN} < 3.3V.
R_{EXT}	External USB Series Resistor	23	–	25	Ω	In series with each USB pin.
V_{UOH}	Static Output High, Driven	2.8	–	3.6	V	15 kΩ ± 5% to ground. Internal pull up enabled.
V_{UOHI}	Static Output High, Idle	2.7	–	3.6	V	15 kΩ ± 5% to ground. Internal pull up enabled.
V_{UOL}	Static Output Low	–	–	0.3	V	15 kΩ ± 5% to ground. Internal pull up enabled.
Z_O	USB Driver Output Impedance	28	–	44	Ω	Including R_{EXT} resistor.
V_{CRS}	D+/D– Crossover Voltage	1.3	–	2.0	V	

[+] Feedback

DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and –40°C ≤ T_A ≤ 85°C, or 3.15V to 3.5V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11. 5V DC Analog Output Buffer Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	µV/°C	
V_{CMOB}	Common-Mode Input Voltage Range	0.5	–	Vdd - 1.0	V	
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 0.6 0.6	 – –	 W W	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 32 ohms to Vdd/2) Power = Low Power = High	 0.5xVdd + 1.1 0.5xVdd + 1.1	 – –	 – –	 V V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 32 ohms to Vdd/2) Power = Low Power = High	 – –	 – –	 0.5 x Vdd – 1.3 0.5 x Vdd – 1.3	 V V	
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	 – –	 1.1 2.6	 5.1 8.8	 mA mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	53	64	–	dB	(0.5 x Vdd – 1.3) ≤ V_{OUT} ≤ (Vdd – 2.3).

Table 12. 3.3V DC Analog Output Buffer Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	µV/°C	
V_{CMOB}	Common-Mode Input Voltage Range	0.5	-	Vdd - 1.0	V	
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 1 1	 – –	 W W	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 1K ohms to Vdd/2) Power = Low Power = High	 0.5 x Vdd + 1.0 0.5 x Vdd + 1.0	 – –	 – –	 V V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 1K ohms to Vdd/2) Power = Low Power = High	 – –	 – –	 0.5 x Vdd – 1.0 0.5 x Vdd – 1.0	 V V	
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	 –	 0.8 2.0	 2.0 4.3	 mA mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	34	64	–	dB	(0.5 x Vdd – 1.0) ≤ V_{OUT} ≤ (0.5 x Vdd + 0.9).

[+] Feedback

DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and –40°C ≤ T_A ≤ 85°C, or 3.15V to 3.5V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 13. 5V DC Analog Reference Specifications

Parameter	Description	Min	Typ	Max	Unit
BG	Bandgap Voltage Reference	1.28	1.30	1.32	V
–	AGND = Vdd/2[3]	Vdd/2 – 0.04	Vdd/2 – 0.01	Vdd/2 + 0.007	V
–	AGND = 2 x BandGap[3]	2 x BG – 0.048	2 x BG – 0.030	2 x BG + 0.024	V
–	AGND = P2[4] (P2[4] = Vdd/2)[3]	P2[4] – 0.011	P2[4]	P2[4] + 0.011	V
–	AGND = BandGap[3]	BG – 0.009	BG + 0.008	BG + 0.016	V
–	AGND = 1.6 x BandGap[3]	1.6 x BG – 0.022	1.6 x BG – 0.010	1.6 x BG + 0.018	V
–	AGND Block to Block Variation (AGND = Vdd/2)[3]	–0.034	0.000	0.034	V
–	RefHi = Vdd/2 + BandGap	Vdd/2 + BG – 0.10	Vdd/2 + BG	Vdd/2 + BG + 0.10	V
–	RefHi = 3 x BandGap	3 x BG – 0.06	3 x BG	3 x BG + 0.06	V
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 1.3V)	2 x BG + P2[6] – 0.113	2 x BG + P2[6] – 0.018	2 x BG + P2[6] + 0.077	V
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)	P2[4] + BG – 0.130	P2[4] + BG – 0.016	P2[4] + BG + 0.098	V
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] + P2[6] – 0.133	P2[4] + P2[6] – 0.016	P2[4] + P2[6]+ 0.100	V
–	RefHi = 3.2 x BandGap	3.2 x BG – 0.112	3.2 x BG	3.2 x BG + 0.076	V
–	RefLo = Vdd/2 – BandGap	Vdd/2 – BG – 0.04	Vdd/2 – BG + 0.024	Vdd/2 – BG + 0.04	V
–	RefLo = BandGap	BG – 0.06	BG	BG + 0.06	V
–	RefLo = 2 x BandGap – P2[6] (P2[6] = 1.3V)	2 x BG – P2[6] – 0.084	2 x BG – P2[6] + 0.025	2 x BG – P2[6] + 0.134	V
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2)	P2[4] – BG – 0.056	P2[4] – BG + 0.026	P2[4] – BG + 0.107	V
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] – P2[6] – 0.057	P2[4] – P2[6] + 0.026	P2[4] – P2[6] + 0.110	V

Table 14. 3.3V DC Analog Reference Specifications

Parameter	Description	Min	Typ	Max	Unit
BG	Bandgap Voltage Reference	1.28	1.30	1.32	V
–	AGND = Vdd/2[3]	Vdd/2 – 0.03	Vdd/2 – 0.01	Vdd/2 + 0.005	V
–	AGND = 2 x BandGap[3]	Not Allowed			
–	AGND = P2[4] (P2[4] = Vdd/2)	P2[4] – 0.008	P2[4] + 0.001	P2[4] + 0.009	V
–	AGND = BandGap[3]	BG – 0.009	BG + 0.005	BG + 0.015	V
–	AGND = 1.6 x BandGap[3]	1.6 x BG – 0.027	1.6 x BG – 0.010	1.6 x BG + 0.018	V
–	AGND Column to Column Variation (AGND = Vdd/2)[3]	–0.034	0.000	0.034	V
–	RefHi = Vdd/2 + BandGap	Not Allowed			
–	RefHi = 3 x BandGap	Not Allowed			
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 0.5V)	Not Allowed			
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)	Not Allowed			
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] + P2[6] – 0.075	P2[4] + P2[6] – 0.009	P2[4] + P2[6] + 0.057	V
–	RefHi = 3.2 x BandGap	Not Allowed			
–	RefLo = Vdd/2 – BandGap	Not Allowed			
–	RefLo = BandGap	Not Allowed			
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 0.5V)	Not Allowed			
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2)	Not Allowed			
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] – P2[6] – 0.048	P2[4] – P2[6] + 0.022	P2[4] – P2[6] + 0.092	V

DC Analog enCoRe III Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and –40°C ≤ T_A ≤ 85°C, or 3.15V to 3.5V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 15. DC Analog enCoRe III Block Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
R_{CT}	Resistor Unit Value (Continuous Time)	–	12.2	–	kΩ	
C_{SC}	Capacitor Unit Value (Switched Capacitor)	–	80	–	fF	

Note
3. AGND tolerance includes the offsets of the local buffer in the enCoRe III block. Bandgap voltage is 1.3V ± 0.02V.

[+] Feedback

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and –40°C ≤ T_A ≤ 85°C, or 3.15V to 3.5V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V or 3.3V at 25°C and are for design guidance only.

Note The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the *PSoC Mixed-Signal Array Technical Reference Manual* for more information on the VLT_CR register.

Table 16. DC POR and LVD Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
	Vdd Value for PPOR Trip (positive ramp)					
V_{PPOR0R}	PORLEV[1:0] = 00b		2.91		V	
V_{PPOR1R}	PORLEV[1:0] = 01b	–	4.39	–	V	
V_{PPOR2R}	PORLEV[1:0] = 10b		4.55		V	
	Vdd Value for PPOR Trip (negative ramp)					
V_{PPOR0}	PORLEV[1:0] = 00b		2.82		V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	4.39	–	V	
V_{PPOR2}	PORLEV[1:0] = 10b		4.55		V	
	PPOR Hysteresis					
V_{PH0}	PORLEV[1:0] = 00b	–	92	–	mV	
V_{PH1}	PORLEV[1:0] = 01b	–	0	–	mV	
V_{PH2}	PORLEV[1:0] = 10b	–	0	–	mV	
	Vdd Value for LVD Trip					
V_{LVD0}	VM[2:0] = 000b	2.86	2.92	2.98[4]	V	
V_{LVD1}	VM[2:0] = 001b	2.96	3.02	3.08	V	
V_{LVD2}	VM[2:0] = 010b	3.07	3.13	3.20	V	
V_{LVD3}	VM[2:0] = 011b	3.92	4.00	4.08	V	
V_{LVD4}	VM[2:0] = 100b	4.39	4.48	4.57	V	
V_{LVD5}	VM[2:0] = 101b	4.55	4.64	4.74[5]	V	
V_{LVD6}	VM[2:0] = 110b	4.63	4.73	4.82	V	
V_{LVD7}	VM[2:0] = 111b	4.72	4.81	4.91	V	

Notes
4. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
5. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

[+] Feedback

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and –40°C ≤ T_A ≤ 85°C, or 3.15V to 3.5V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 17. DC Programming Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
I_{DDP}	Supply Current During Programming or Verify	–	15	30	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.1	–	–	V	
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull down resistor.
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	Vss + 0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	Vdd – 1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)	50,000[6]	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash Endurance (total)[7]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

Notes

6. The 50,000 cycle Flash endurance per block will only be guaranteed if the Flash is operating within one voltage range. Voltage ranges are 3.0V to 3.6V and 4.75V to 5.25V.
7. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.

AC Electrical Characteristics

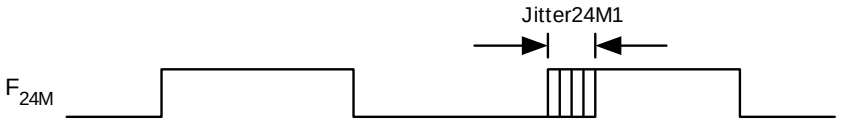
AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and –40°C ≤ T_A ≤ 85°C, or 3.15V to 3.5V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 18. AC Chip-Level Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
$F_{IMO245V}$	Internal Main Oscillator Frequency for 24 MHz (5V)	23.04	24	24.96[7, 8]	MHz	Trimmed for 5V operation using factory trim values.
$F_{IMO243V}$	Internal Main Oscillator Frequency for 24 MHz (3.3V)	22.08	24	25.92[7,9]	MHz	Trimmed for 3.3V operation using factory trim values.
F_{IMOUSB}	Internal Main Oscillator Frequency with USB Frequency Locking Enabled and USB Traffic Present	23.94	24	24.06[8]	MHz	USB operation for system clock source from the IMO is limited to 0°C ≤ T_A ≤ 70°C.
F_{CPU1}	CPU Frequency (5V Nominal)	0.93	24	24.96[7,8]	MHz	
F_{CPU2}	CPU Frequency (3.3V Nominal)	0.93	12	12.96[8, 9]	MHz	
F_{BLK5}	Digital PSoC Block Frequency (5V Nominal)	0	48	49.92[7, 8, 10]	MHz	Refer to the AC Digital Block Specifications.
F_{BLK3}	Digital PSoC Block Frequency (3.3V Nominal)	0	24	25.92[8, 10]	MHz	
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
F_{32K_U}	Internal Low Speed Oscillator Untrimmed Frequency	5	–	–	kHz	
DC_{ILO}	Internal Low Speed Oscillator Duty Cycle	20	50	80	%	
Jitter32k	32 kHz Period Jitter	–	100		ns	
Step24M	24 MHz Trim Step Size	–	50	–	kHz	
Fout48M	48 MHz Output Frequency	46.08	48.0	49.92[7, 9]	MHz	Trimmed. Utilizing factory trim values.
Jitter24M1	24 MHz Period Jitter (IMO) Peak-to-Peak	–	300		ps	
F_{MAX}	Maximum Frequency of Signal on Row Input or Row Output	–	–	12.96	MHz	
SR_{POWER_UP}	Power Supply Slew Rate	–	–	250	V/ms	
$T_{POWERUP}$	Time from End of POR to CPU Executing Code	–	16	100	ms	

Figure 6. 24 MHz Period Jitter (IMO) Timing Diagram



Notes
7. 4.75V < Vdd < 5.25V.
8. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
9. 3.0V < Vdd < 3.6V. See Application Note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on trimming for operation at 3.3V.
10. See the individual user module data sheets for information on maximum frequencies for user modules.

[+] Feedback

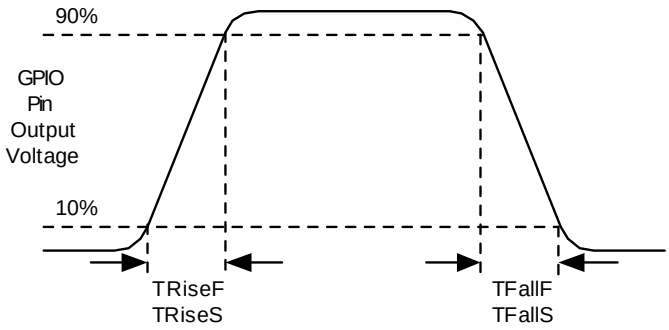
AC General Purpose I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and –40°C ≤ T_A ≤ 85°C, or 3.15V to 3.5V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 19. AC GPIO Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12	MHz	Normal Strong Mode
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	3	–	18	ns	Vdd = 4.5 to 5.25V, 10%–90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	2	–	18	ns	Vdd = 4.5 to 5.25V, 10%–90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	10	27	–	ns	Vdd = 3 to 5.25V, 10%–90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	10	22	–	ns	Vdd = 3 to 5.25V, 10%–90%

Figure 7. GPIO Timing Diagram



AC Full Speed USB Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and –40°C ≤ T_A ≤ 85°C, or 3.15V to 3.5V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 20. AC Full Speed (12 Mbps) USB Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{RFS}	Transition Rise Time	4	–	20	ns	For 50 pF load.
T_{FSS}	Transition Fall Time	4	–	20	ns	For 50 pF load.
T_{RFMFS}	Rise/Fall Time Matching: (T_R/T_F)	90	–	111	%	For 50 pF load.
$T_{DRATEFS}$	Full Speed Data Rate	12 – 0.25%	12	12 + 0.25%	Mbps	

[+] Feedback

AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and –40°C ≤ T_A ≤ 85°C, or 3.15V to 3.5V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 21. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Unit	Notes
Timer	Capture Pulse Width	50[11]	–	–	ns	
	Maximum Frequency, No Capture	–	–	49.92	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, With Capture	–	–	25.92	MHz	
Counter	Enable Pulse Width	50[11]	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	49.92	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, Enable Input	–	–	25.92	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50[11]	–	–	ns	
	Disable Mode	50[12]	–	–	ns	
	Maximum Frequency	–	–	49.92	MHz	4.75V < Vdd < 5.25V.
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	–	–	49.92	MHz	4.75V < Vdd < 5.25V.
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	–	–	24.6	MHz	
SPIM	Maximum Input Clock Frequency	–	–	8.2	MHz	Maximum data rate at 4.1 MHz due to 2 x over clocking.
SPIS	Maximum Input Clock Frequency	–	–	4.1	MHz	
	Width of SS_ Negated Between Transmissions	50[11]	–	–	ns	
Transmitter	Maximum Input Clock Frequency	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.
Receiver	Maximum Input Clock Frequency	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.

AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and –40°C ≤ T_A ≤ 85°C, or 3.15V to 3.5V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 22. AC External Clock Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
F_{OSCEXT}	Frequency for USB Applications	23.94	24	24.06	MHz	USB operation in the extended Industrial temperature range (–40°C ≤ T_A ≤ 85°C) requires that the system clock is sourced from an external clock oscillator.
–	Duty Cycle	47	50	53	%	
–	Powerup to IMO Switch	150	–	–	µs	

Note
11. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

[+] Feedback

AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and –40°C ≤ T_A ≤ 85°C, or 3.15V to 3.5V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 23. 5V AC Analog Output Buffer Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{ROB}	Rising Settling Time to 0.1%, 1V Step, 100 pF Load Power = Low Power = High	 – –	 – –	 2.5 2.5	 µs µs	
T_{SOB}	Falling Settling Time to 0.1%, 1V Step, 100 pF Load Power = Low Power = High	 – –	 – –	 2.2 2.2	 µs µs	
SR_{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100 pF Load Power = Low Power = High	 0.65 0.65	 – –	 – –	 V/µs V/µs	
SR_{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100 pF Load Power = Low Power = High	 0.65 0.65	 – –	 – –	 V/µs V/µs	
BW_{OBSS}	Small Signal Bandwidth, 20mV_{pp}, 3-dB BW, 100 pF Load Power = Low Power = High	 0.8 0.8	 – –	 – –	 MHz MHz	
BW_{OBLS}	Large Signal Bandwidth, 1V_{pp}, 3-dB BW, 100 pF Load Power = Low Power = High	 300 300	 – –	 – –	 kHz kHz	

Table 24. 3.3V AC Analog Output Buffer Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{ROB}	Rising Settling Time to 0.1%, 1V Step, 100 pF Load Power = Low Power = High	 – –	 – –	 3.8 3.8	 µs µs	
T_{SOB}	Falling Settling Time to 0.1%, 1V Step, 100 pF Load Power = Low Power = High	 – –	 – –	 2.6 2.6	 µs µs	
SR_{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100 pF Load Power = Low Power = High	 0.5 0.5	 – –	 – --	 V/µs V/µs	
SR_{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100 pF Load Power = Low Power = High	 0.5 0.5	 – –	 – –	 V/µs V/µs	
BW_{OBSS}	Small Signal Bandwidth, 20mV_{pp}, 3dB BW, 100 pF Load Power = Low Power = High	 0.7 0.7	 – –	 – –	 MHz MHz	
BW_{OBLS}	Large Signal Bandwidth, 1V_{pp}, 3dB BW, 100 pF Load Power = Low Power = High	 200 200	 – –	 – –	 kHz kHz	

[+] Feedback

AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and –40°C ≤ T_A ≤ 85°C, or 3.15V to 3.5V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 25. AC Programming Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
T_{ERASEB}	Flash Erase Time (Block)	–	10	–	ms	
T_{WRITE}	Flash Block Write Time	–	40	–	ms	
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	45	ns	Vdd > 3.6
T_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	–	–	50	ns	3.15 ≤ Vdd ≤ 3.5
$T_{ERASEALL}$	Flash Erase Time (Bulk)	–	40	–	ms	Erase all blocks and protection fields at once.
$T_{PROGRAM_HOT}$	Flash Block Erase + Flash Block Write Time	–	–	100	ms	0°C ≤ T_J ≤ 100°C
$T_{PROGRAM_COLD}$	Flash Block Erase + Flash Block Write Time	–	–	200	ms	-40°C ≤ T_J ≤ 0°C

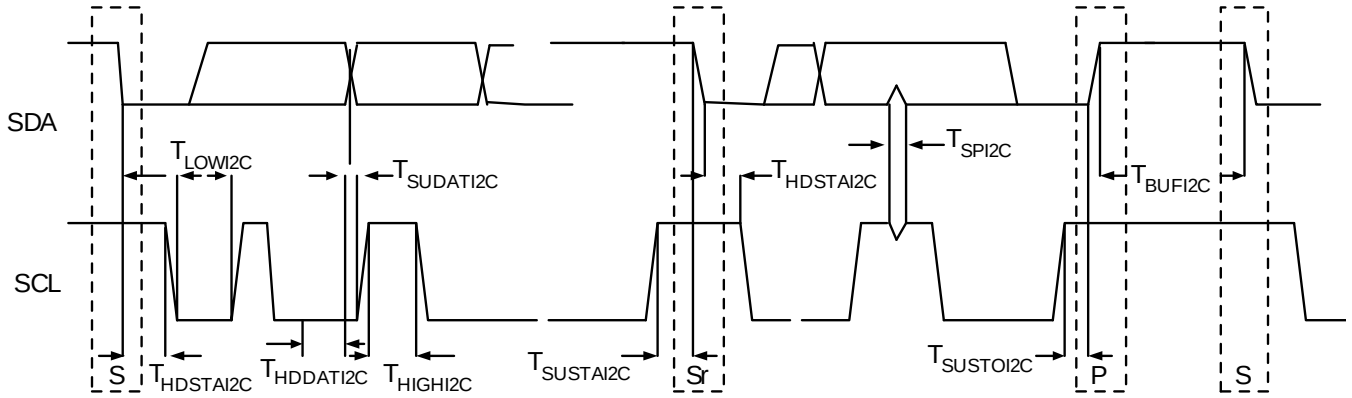
AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and –40°C ≤ T_A ≤ 85°C, or 3.15V to 3.5V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 26. AC Characteristics of the I²C SDA and SCL Pins for Vdd

Parameter	Description	Standard-Mode		Fast-Mode		Unit	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz	
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs	
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs	
$T_{SUSTAI2C}$	Setup Time for a Repeated START Condition	4.7	–	0.6	–	µs	
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs	
$T_{SUDATI2C}$	Data Setup Time	250	–	100[12]	–	ns	
$T_{SUSTOI2C}$	Setup Time for STOP Condition	4.0	–	0.6	–	µs	
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs	
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter.	–	–	0	50	ns	

Figure 8. Definition for Timing for Fast-/Standard-Mode on the I²C Bus



Note

12. A Fast-Mode I²C-bus device can be used in a Standard-Mode I²C-bus system, but the requirement $T_{SUDATI2C} \geq 250$ ns must then be met. This automatically is the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + T_{SUDATI2C} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

[+] Feedback

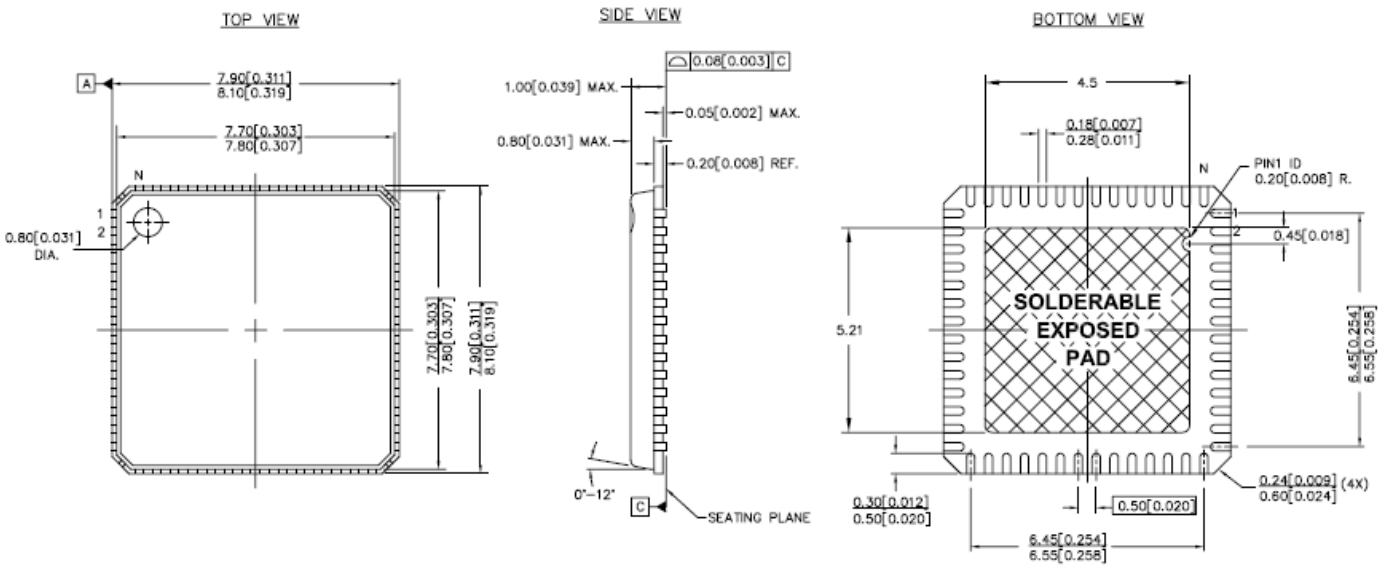
Packaging Information

This section illustrates the package specification for the CY7C64215 enCoRe III, along with the thermal impedance for the package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/design/MR10161.

Package Diagrams

Figure 9. 56-Pin (8x8 mm) QFN-MLF (PUNCH)



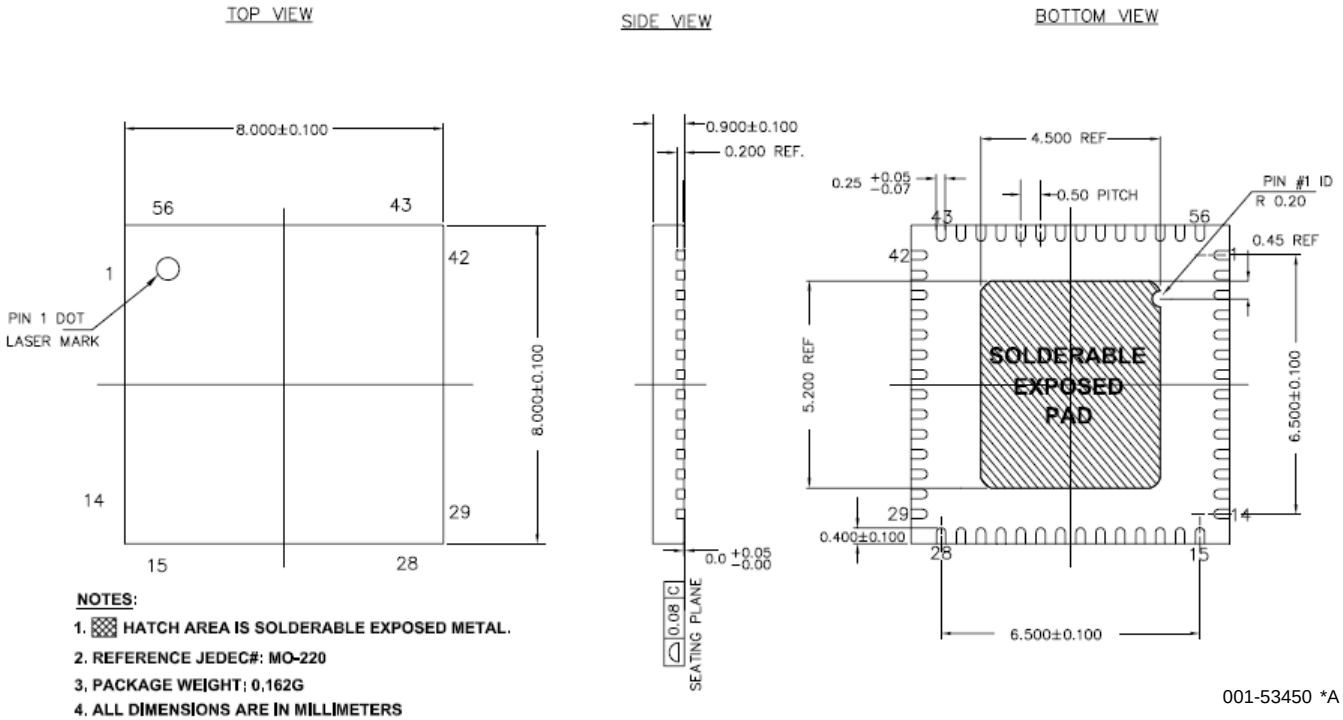
NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.162g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

001-12921 *A

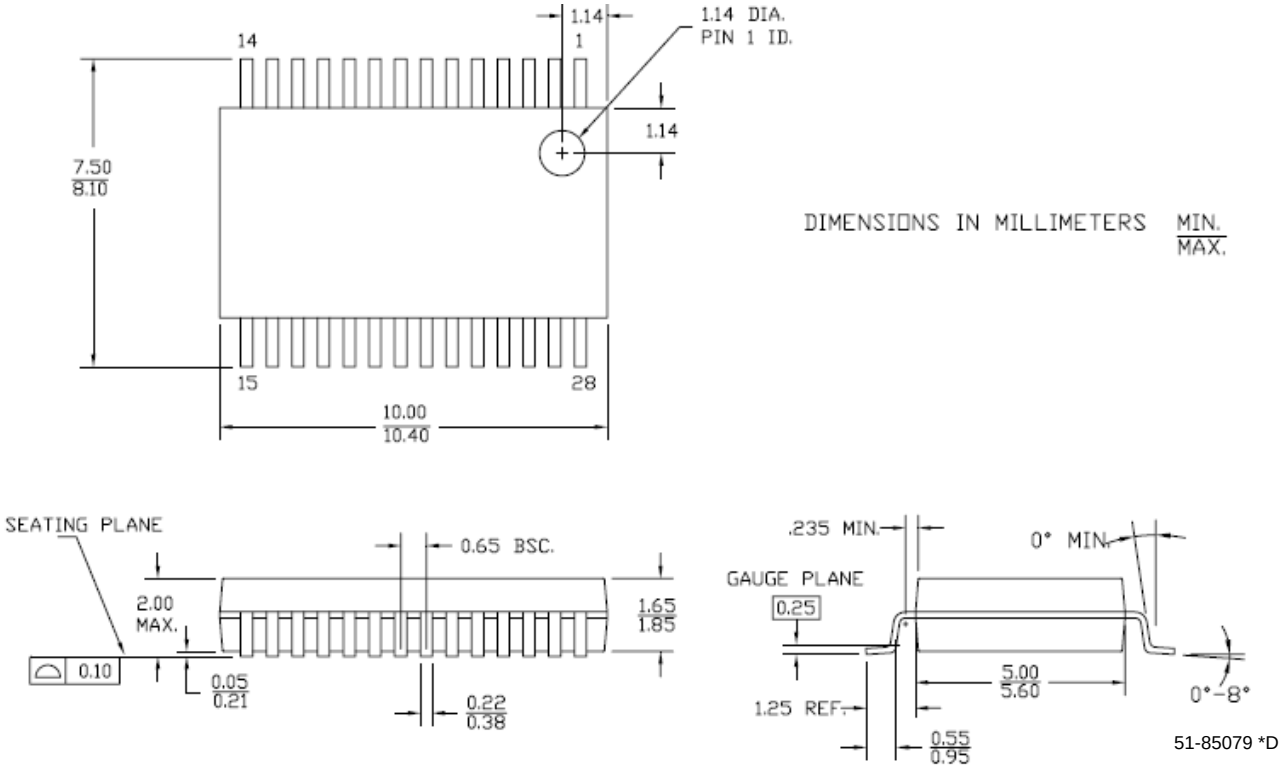
[+] Feedback

Figure 10. 56-Pin QFN (8 X 8 X 0.9 MM) (SAWN)



001-53450 *A

Figure 11. 28-Pin (210-Mil) SSOP



51-85079 *D

[+] Feedback

Thermal Impedance

Table 27. Thermal Impedance for the Package

Package	Typical θ_{JA} [13]
56 Pin QFN[14]	20 ^{o}C/W
28 Pin SSOP	96 ^{o}C/W

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 28. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature[15]	Maximum Peak Temperature
56 Pin QFN	240°C	260°C
28 Pin SSOP	240°C	260°C

Package Handling

Some IC packages require baking before they are soldered onto a PCB to remove moisture that may have been absorbed after leaving the factory. A label on the packaging has details about actual bake temperature and the minimum bake time to remove this moisture. The maximum bake time is the aggregate time that the devices are exposed to the bake temperature. Exceeding this exposure time may degrade device reliability.

Parameter	Description	Min	Typ	Max	Unit
$T_{BAKETEMP}$	Bake Temperature		125	See Package Label	°C
$T_{BAKETIME}$	Bake Time	See Package Label		72	Hours

Notes
13. $T_J = T_A + POWER \times \theta_{JA}$
14. To achieve the thermal impedance specified for the QFN package, the center thermal pad should be soldered to the PCB ground plane.
15. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5°C with Sn-Pb or 245 ± 5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

[+] Feedback

Ordering Information

Package	Ordering Code	Flash Size	SRAM (Bytes)	Temperature Range
56-Pin QFN-MLF (Punch)	CY7C64215-56LFXC	16K	1K	0°C to 70°C
56-Pin QFN-MLF (Punch) (Tape and Reel)	CY7C64215-56LFXCT	16K	1K	0°C to 70°C
28-Pin SSOP	CY7C64215-28PVXC	16K	1K	0°C to 70°C
28-Pin SSOP (Tape and Reel)	CY7C64215-28PVXCT	16K	1K	0°C to 70°C
56-Pin QFN (Sawn) Commercial	CY7C64215-56LTXC	16K	1K	0°C to 70°C
56-Pin QFN (Sawn) Commercial (Tape and Reel)	CY7C64215-56LTXCT	16K	1K	0°C to 70°C
56-Pin QFN (Sawn) Industrial	CY7C64215-56LTXI	16K	1K	–40°C to 85°C
56-Pin QFN (Sawn) Industrial (Tape and Reel)	CY7C64215-56LTXIT	16K	1K	–40°C to 85°C

Document History Page

Description Title: CY7C64215, enCoRe™ III Full Speed USB Controller Document Number: 38-08036				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	131325	See ECN	XGR	New data sheet.
*A	385256	See ECN	BHA	Changed from Advance Information to Preliminary. Added standard data sheet items. Changed Part number from CY7C642xx to CY7C64215.
*B	2547630	08/04/08	AZIEL/PYRS	Operational voltage range for USB specified under "Full Speed USB (12Mbps)". CMP_GO_EN1 register removed as it has no functionality on Radon. Figure "CPU Frequency" adjusted to show invalid operating region for USB with footnote describing reason. DC electrical characteristic, Vdd. Note added describing where USB hardware is non-functional.
*C	2620679	12/12/08	CMCC/PYRS	Added Package Handling information. Deleted note regarding link to amkor.com for MLF package dimensions.
*D	2717887	06/11/2009	DPT	Added 56 -Pin Sawn QFN (8 X 8 mm) package diagram and added CY7C64215-56LTXC part information in the Ordering Information table.
*E	2852393	01/15/2010	BHA/XUT	■ Added Table of Contents. ■ Added external clock oscillator option and Industrial Temperature information to the Features, Pin Information, Electrical Specifications, Operating Temperature, DC Electrical Characteristics, AC Electrical Characteristics, and Ordering Information sections. ■ Updated DC GPIO, AC Chip, and AC Programming Specifications follows: ❒ Replaced TRAMP (time) with SRPOWER_UP (slew rate) specification. ❒ Added IOH, IOL, DCILO, F32K_U, TPOWERUP, TERASEALL, TPROGRAM_HOT, and TPROGRAM_COLD specifications. ❒ Updated Vdd ranges on Figure 5 and Table 8. ❒ Added notes for VM and VDI on Table 10. ❒ Removed TR/TF from Table 20. ■ Update Ordering Information for: CY7C64215-56LFXCT, CY7C64215-28PVXCT, CY7C64215-56LTXIT Tape and Reel. ■ Updated 28-Pin SSOP and 56-Pin QFN PUNCH and SAWN package diagrams. ■ Updated copyright and Sales, Solutions, and Legal Information URLs.

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